

## CMOS Dual Precision Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

**Features:**

- Retriggerable/resettable capability
- Trigger and reset propagation delays independent of  $R_x$ ,  $C_x$
- Triggering from leading or trailing edge
- Q and  $\bar{Q}$  buffered outputs available
- Separate resets
- Replaces CD4538B Type

■ CD14538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor ( $R_x$ ) and an external capacitor ( $C_x$ ) control the timing and accuracy for the circuit. Adjustment of  $R_x$  and  $C_x$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of  $R_x$  and  $C_x$ . Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to  $V_{SS}$ . An unused -TR input should be tied to  $V_{DD}$ . A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to  $V_{DD}$ . However, if an entire section of the CD14538B is not used, its inputs must be tied to either  $V_{DD}$  or  $V_{SS}$ . See Table 1.

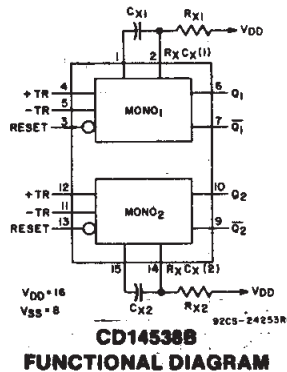
In normal operation the circuit retriggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode,  $\bar{Q}$  is connected to -TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (-TR) is used. The time period (T) for this multivibrator can be calculated by:  $T = R_x C_x$ .

The minimum value of external resistance,  $R_x$ , is 4 k $\Omega$ . The minimum and maximum values of external capacitance,  $C_x$ , are 0 pF and 100  $\mu$ F, respectively.

The CD14538B is interchangeable with type MC14538 and is similar to and pin-compatible with the CD4098B\* and CD4538B. It can replace the CD4538B which type is not recommended for new designs.

The CD14538B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

\*T = 0.5  $R_x C_x$  for  $C_x \geq 1000$  pF    #T =  $R_x C_x$ ;  $C_{x\min} = 5000$  pF



- Wide range of output-pulse widths
- Schmitt-trigger input allows unlimited rise and fall times on +TR and -TR inputs
- 100% tested for maximum quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25 $^{\circ}$ C
- Noise margin (full package-temperature range):
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

**Applications:**

- Pulse delay and timing
- Pulse shaping



TERMINALS 1, 8, 15 ARE  
ELECTRICALLY CONNECTED  
INTERNALLY

92CS-24848R1

**Terminal Assignment**

## CD14538B Types

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	.....	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal)	.....	
INPUT VOLTAGE RANGE, ALL INPUTS	.....	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	.....	$\pm 10mA$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55^\circ C$ to $+100^\circ C$ .....		500mW
For $T_A = +100^\circ C$ to $+125^\circ C$ .....		Derate Linearly at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .....		100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	.....	$-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	.....	$-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79mm$ ) from case for 10s max .....		$+265^\circ C$

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A$ =Full Package-Temperature-Range)	—	3	18	V
Input Pulse Width +TR, -TR, or RESET	$t_{WH}, t_{WL}$	5	140	ns
		10	80	
		15	60	

**TABLE I**  
**CD4538B FUNCTIONAL TERMINAL CONNECTIONS**

FUNCTION	$V_{DD}$ TO TERM. NO.		$V_{SS}$ TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-Retriggerable	3	13			5	11	4-6	12-10

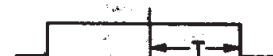
**NOTES:**

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD (T) REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN



RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)



NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)



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# CD14538B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	Min.	+25 Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, I <sub>IN</sub> Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA



Fig. 1 - Logic diagram (1/2 of device shown).

# CD14538B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS, At  $T_A=25^\circ\text{C}$ ; Input  $t_r, t_f=20\text{ ns}$ ,  $C_L=50\text{ pF}$**

CHARACTERISTIC	TEST CONDITIONS $V_{DD}$ (V)	LIMITS			UNITS	
		Min.	Typ.	Max.		
Transition Time $t_{TLH}, t_{THL}$	5	—	100	200	ns	
	10	—	50	100		
	15	—	40	80		
Propagation Delay Time: +TR or -TR to Q or $\bar{Q}$	5	—	300	600		
	10	—	150	300		
	15	—	100	220		
Reset to Q or $\bar{Q}$	5	—	250	500		
	10	—	125	250		
	15	—	95	190		
Minimum Input Pulse Width: +TR, -TR or Reset	5	—	80	140		
	10	—	40	80		
	15	—	30	60		
Output Pulse Width - Q or $\bar{Q}$ : $C_x = 0.002\ \mu\text{F}$ , $R_x = 100\ \text{K}\Omega$	5	198	210	230	μs	
	10	200	212	232		
	15	202	214	234		
$C_x=0.1\ \mu\text{F}$ , $R_x=100\ \text{K}\Omega$	5	9.4	9.97	10.5	ms	
	10	9.4	9.95	10.6		
	15	9.5	10	10.6		
$C_x=10\ \mu\text{F}$ , $R_x=100\ \text{K}\Omega$	5	0.95	1	1.06	s	
	10	0.95	1	1.06		
	15	0.96	1.01	1.07		
Pulse Width Match between circuits in same package: $C_x=0.1\ \mu\text{F}$ , $R_x=100\ \text{K}\Omega$	$100 (T_1 - T_2)$	—	$\pm 1$	—	%	
	$T_1$	5	$\pm 1$	—		
	$T_1$	10	$\pm 1$	—		
Minimum Retrigger Time	$t_r$	5	0	—	ns	
	$t_r$	10	0	—		
	$t_r$	15	0	—		
Input Capacitance	$C_{IN}$	Any Input	—	5	7.5	pF

\*Note: Minimum  $R_x$  value=4 K $\Omega$ , minimum  $C_x$  value=5000 pF.

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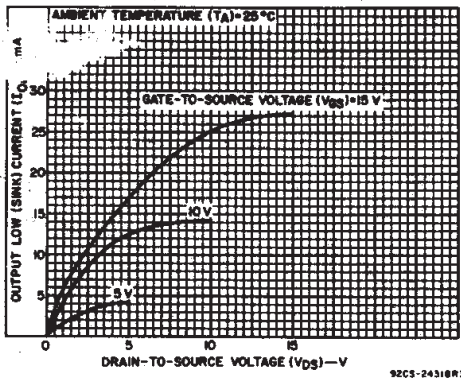


Fig. 2 - Typical output low (sink) current characteristics.

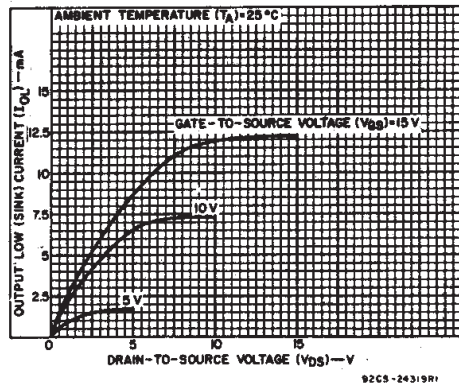


Fig. 3 - Minimum output low (sink) current characteristics.

# CD14538B Types



Fig. 4 - Typical output high (source) current characteristics.



Fig. 5 - Minimum output high (source) current characteristics.



Fig. 6 - Typical propagation delay time as a function of load capacitance (+TR or -TR to Q or  $\bar{Q}$ ).



Fig. 7 - Typical propagation delay time as a function of load capacitance (RESET to Q or  $\bar{Q}$ ).



Fig. 8 - Typical transition time as a function of load capacitance.

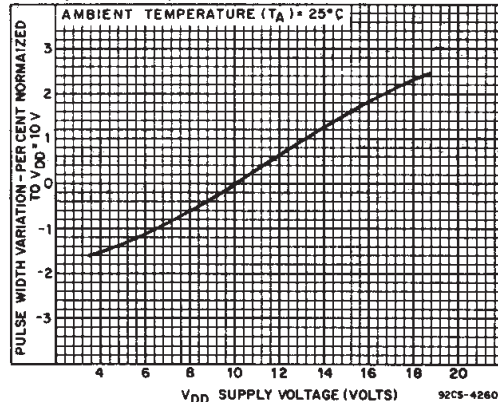


Fig. 9 - Typical pulse-width variation as a function of supply voltage.



Fig. 10 - Typical pulse-width variation as a function of temperature ( $R_x=100\text{ K}\Omega$ ,  $C_x=0.1\text{ }\mu\text{F}$ ).

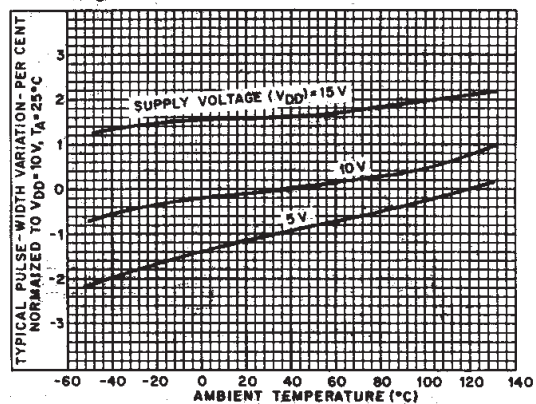


Fig. 11 - Typical pulse-width variation as a function of temperature ( $R_x=100\text{ K}\Omega$ ,  $C_x=2000\text{ pF}$ ).

## CD14538B Types

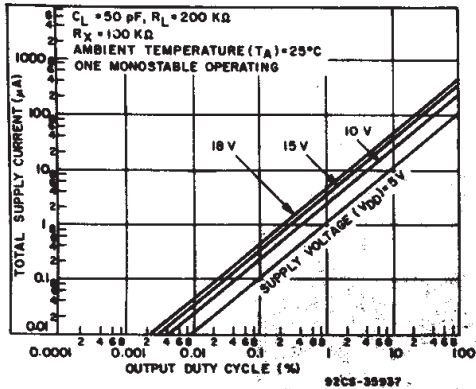


Fig. 12 - Typical total supply current as a function of output duty cycle.

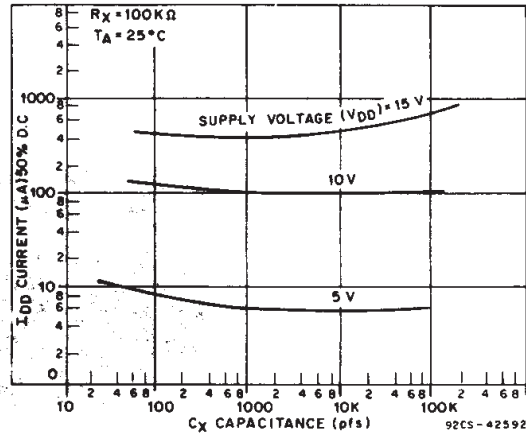
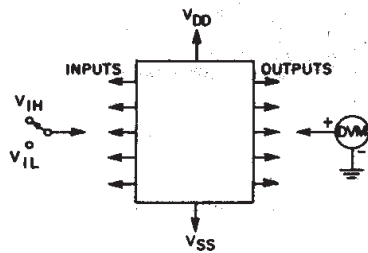


Fig. 13 - Typical total supply current as a function of load capacitance.



92CS-27441R1

Fig. 14 - Input voltage test circuit.

**NOTE:**

1. Test any combination of inputs.
2. When measuring  $V_{IH}$  or  $V_{IL}$  for Schmitt trigger inputs (+TR, -TR), the input must first be brought to  $V_{DD}$  or  $V_{SS}$ , respectively, then reduced to the specified limit.

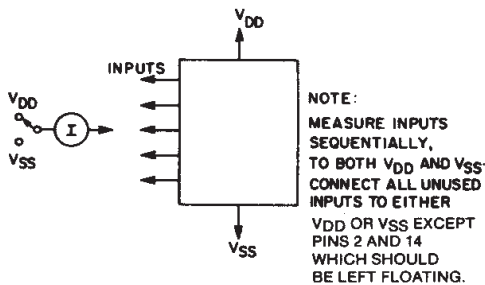
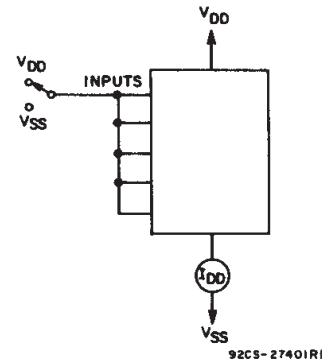


Fig. 15 - Input leakage-current test circuit.

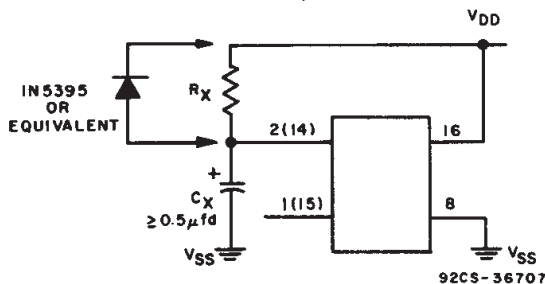


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Fig. 16 - Quiescent device current test circuit.

### Power-Down Mode

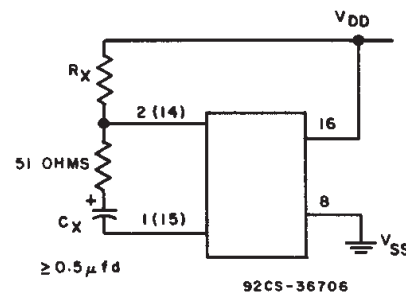
During a rapid power-down condition, as would occur with a power-supply short circuit or with a poorly filtered power supply, the energy stored in  $C_X$  could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when  $C_X$  is  $\geq 0.5$  microfarad, a protection diode with a 1-ampere or higher rating (1N5395 or equivalent) and a separate ground return for  $C_X$  should be provided as shown in Fig. 17.



92CS-36707

Fig. 17 - Rapid power-down protection circuit.

An alternate protection method is shown in Fig. 18, where a 51-ohm current-limiting resistor is inserted in series with  $C_X$ . Note that a small pulse width decrease will occur however, and  $R_X$  must be appropriately increased to obtain the originally desired pulse width.

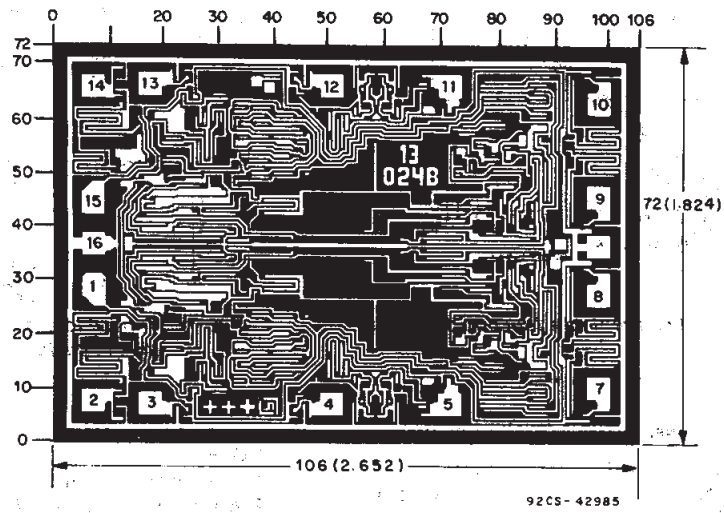


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Fig. 18 - Alternate rapid power-down protection circuit.

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# CD14538B Types



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and pad layout for CD14538BH.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9055701EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9055701EA CD14538BF3A	<a href="#">Samples</a>
CD14538BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD14538BE	<a href="#">Samples</a>
CD14538BF	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD14538BF	<a href="#">Samples</a>
CD14538BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9055701EA CD14538BF3A	<a href="#">Samples</a>
CD14538BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD14538BM	
CD14538BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD14538BM	<a href="#">Samples</a>
CD14538BMT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD14538BM	
CD14538BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD14538B	<a href="#">Samples</a>
CD14538BPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM538B	
CD14538BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM538B	<a href="#">Samples</a>
CD14538BPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM538B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD14538BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD14538BNSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD14538BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD14538BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD14538BNSR	SO	NS	16	2000	356.0	356.0	35.0
CD14538BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD14538BE	N	PDIP	16	25	506	13.97	11230	4.32
CD14538BE	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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