CDx4AC164、CDx4ACT164 8 位串行输入/并行输出移位寄存器

1 特性

- 缓冲输入
- 典型传播延迟
  - V_{CC} = 5V、T_A = 25°C 且 C_L = 50pF 时为 6ns
- 防 SCR 闩锁 CMOS 工艺和电路设计
- 双极 FAST™/AS/S 的速度，同时功耗显著降低
- 平衡传播延迟
- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- ±24mA 输出驱动电流
  - 扇出到 15 个 FAST™ IC
  - 驱动 50Ω 传输线路

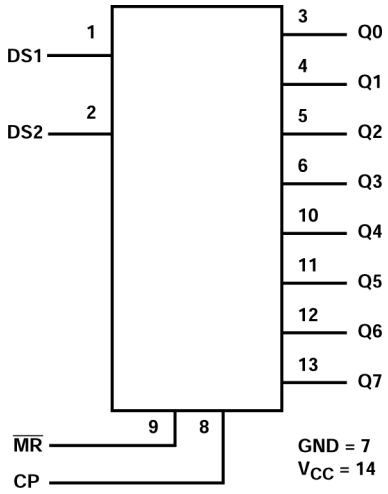
2 说明

’AC164 和 ’ACT164 是采用高级 CMOS 逻辑技术并具有异步复位功能的 8 位串行输入/并行输出移位寄存器。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
CDx4AC(T)164	D（SOIC，14）	8.65mm × 6mm	8.65mm × 3.9mm
	N（PDIP，14）	19.3mm x 9.4mm	19.3mm x 6.35mm

(1) 如需了解更多信息，请参阅第 10 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 x 宽）为标称值，不包括引脚。



功能图

Table of Contents

3 Pin Configuration and Functions

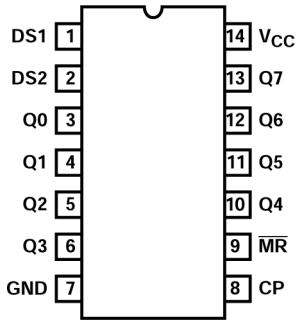


图 3-1. CD54AC164, CD54ACT164 J Package, 14-Pin CERDIP; CD74AC164, CD74ACT164 D or N Package, 14-Pin SOIC or PDIP (Top View)

表 3-1. Pin Functions

NAME	PIN	TYPE	DESCRIPTION
DS1	1	I	Serial input 1
DS2	2	I	Serial input 2
Q0	3	O	Output 0
Q1	4	O	Output 1
Q2	5	O	Output 2
Q3	6	O	Output 3
GND	7	G	Ground
CP	8	I	Clock signal
!MR	9	I	Master reset
Q4	10	O	Output 4
Q5	11	O	Output 5
Q6	12	O	Output 6
Q7	13	O	Output 7
V_{CC}	14	P	Power

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	DC Supply Voltage		-0.5	6	V
I_{IK}	DC Input Diode Current	(V_I < -0.5V or V_I > V_{CC} + 0.5V)		± 20	mA
I_{OK}	DC Output Diode Current	(V_O < -0.5V or V_O > V_{CC} + 0.5V)		±50	mA
I_O	DC Output Source or Sink Current per Output Pin	(V_O > -0.5V or V_O < V_{CC} + 0.5V)		±50	mA
I_{CC} or I_{GND} (2)	DC V_{CC} or Ground Current			±100	mA

(1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
(2) For up to 4 outputs per device, add ±25mA for each additional output.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
T_A	Temperature Range		-55	125	°C
V_{CC} (1)	Supply Voltage Range				
	AC Types		1.5	5.5	V
	ACT Types		4.5	5.5	V
V_I, V_O	DC Input or Output Voltage		0	V_{CC}	V
dt/dv	Input Rise and Fall Slew Rate				
	AC Types	1.5V to 3V		50	ns
	AC Types	3.6V to 5.5V		20	ns
	ACT Types	4.5V to 5.5V		10	ns

(1) Unless otherwise specified, all voltages are referenced to ground.

4.4 Thermal Information

THERMAL METRIC(1)		CDx4AC(T)164		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90	106.6	°C/W

(1) θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

4.5 DC Electrical Specifications

PARAMETER		TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85 °C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
V_{IH}	High Level Input Voltage	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
V_{IL}	Low Level Input Voltage	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
V_{OH}	High Level Output Voltage	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (1) (2)	5.5	-	-	3.85	-	-	-	V
			-50 (1) (2)	5.5	-	-	-	-	3.85	-	V
V_{OL}	Low Level Output Voltage	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (1) (2)	5.5	-	-	-	1.65	-	-	V
			50(1) (2)	5.5	-	-	-	-	-	1.65	V
I_I	Input Leakage Current	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
I_{CC}	Quiescent Supply Current MSI	V_{CC} or GND	0	5.5	-	8	-	80	-	160	μA
ACT TYPES											
V_{IH}	High Level Input Voltage	-	-	4.5 to 5.5	2	-	2	-	2	-	V
V_{IL}	Low Level Input Voltage	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
V_{OH}	High Level Output Voltage	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75(1) (2)	5.5	-	-	3.85	-	-	-	V
			-50 (1) (2)	5.5	-	-	-	-	3.85	-	V
V_{OL}	Low Level Output Voltage	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (1) (2)	5.5	-	-	-	1.65	-	-	V
			50 (1) (2)	5.5	-	-	-	-	-	1.65	V
I_I	Input Leakage Current	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
I_{CC}	Quiescent Supply Current MSI	V_{CC} or GND	0	5.5	-	8	-	80	-	160	μA

PARAMETER		TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85 °C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC}	Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50 Ω transmission-line-drive capability at 85°C, 75 Ω at 125°C.

表 4-1. ACT Input Load Table

INPUT	UNIT LOAD
DS1, DS2	0.5
$\overline{MR}$	0.74
CP	0.71

Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

4.6 Prerequisite for Switching Function

PARAMETER		V_{CC} (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
	AC TYPES						
f_{MAX}	Max. Clock Frequency	1.5	7	-	6	-	MHz
		3.3(1)	62	-	54	-	MHz
		5(2)	86	-	75	-	MHz
t_W	$\overline{MR}$ Pulse Width	1.5	49	-	56	-	ns
		3.3	5.5	-	6.3	-	ns
		5	3.9	-	4.5	-	ns
t_W	CP Pulse Width	1.5	73	-	84	-	ns
		3.3	8.2	-	9.4	-	ns
		5	5.9	-	6.7	-	ns
t_{SU}	Set-up Time	1.5	27	-	31	-	ns
		3.3	3.1	-	3.5	-	ns
		5	2.2	-	2.5	-	ns
t_H	Hold Time	1.5	27	-	31	-	ns
		3.3	3.1	-	3.5	-	ns
		5	2.2	-	2.5	-	ns
t_{REM}	$\overline{MR}$ to CP Removal Time	1.5	1	-	1	-	ns
		3.3	1	-	1	-	ns
		5	1	-	1	-	ns
	ACT TYPES						
f_{MAX}	Max. Clock Frequency	5(2)	80	-	70	-	MHz
t_W	$\overline{MR}$ Pulse Width	5	3.9	-	4.5	-	ns
t_W	CP Pulse Width	5	6.2	-	7.1	-	ns
t_{SU}	Set-up Time	5	2.2	-	2.5	-	ns
t_H	Hold Time	5	2.6	-	3	-	ns
t_{REM}	$\overline{MR}$ to CP Removal Time	5	0	-	0	-	ns

(1) 9. 3.3V Min at 3.6V, Max at 3V.
(2) 10. 5V Min at 5.5V, Max at 4.5V.

4.7 Switching Specifications

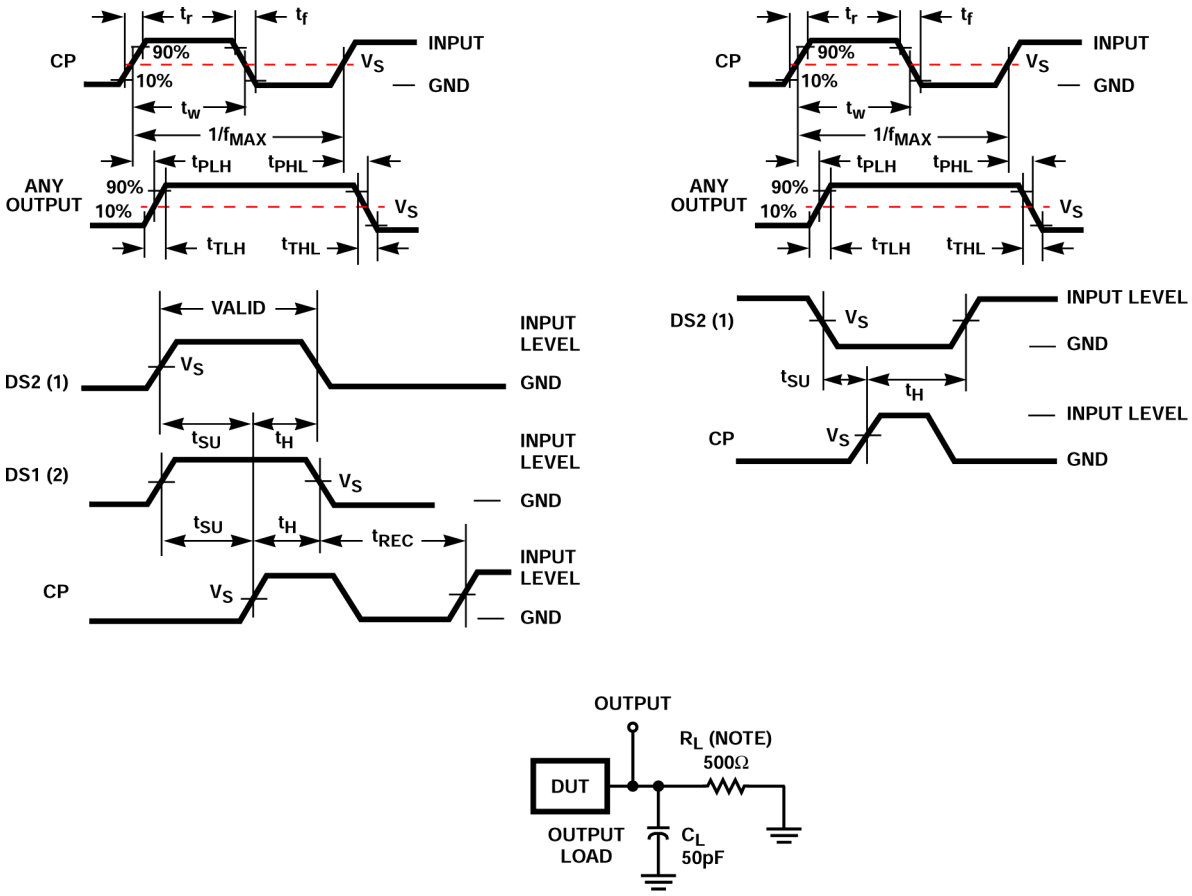
Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER		V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
t_{PLH}, t_{PHL}	Propagation Delay, CP to Qn	1.5	-	-	143	-	-	157	ns
		3.3 (1)	4.5	-	15.9	4.4	-	17.5	ns
		5 (2)	3.2	-	11.4	3.1	-	12.5	ns
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{MR}$ to Qn	1.5	-	-	158	-	-	174	ns
		3.3	5	-	17.7	4.9	-	19.5	ns
		5	3.6	-	12.6	3.5	-	13.9	ns
C_I	Input Capacitance	-	-	-	10	-	-	10	pF
C_{PD} (3)	Power Dissipation Capacitance	-	-	150	-	-	150	-	pF
ACT TYPES									
t_{PLH}, t_{PHL}	Propagation Delay, CP to Qn	5 (2)	3.8	-	13.5	3.7	-	14.9	ns
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{MR}$ to Qn	5	4.1	-	14.4	4	-	15.8	ns
C_I	Input Capacitance	-	-	-	10	-	-	10	pF
C_{PD} (3)	Power Dissipation Capacitance	-	-	150	-	-	150	-	pF

(1) 3.3V Min at 3.6V, Max at 3V.
(2) 5V Min at 5.5V, Max at 4.5V.
(3) C_{PD} is used to determine the dynamic power consumption per device.

5 Parameter Measurement Information

Load Circuit And Voltage Waveforms



For AC Series Only: When VCC = 1.5V, RL = 1kΩ.For AC Series Only: When VCC = 1.5V, RL = 1kΩ.For AC Series Only: When VCC = 1.5V, RL = 1kΩ.

图 5-1. Propagation Delay Times

表 5-1. Propagation Delay Times

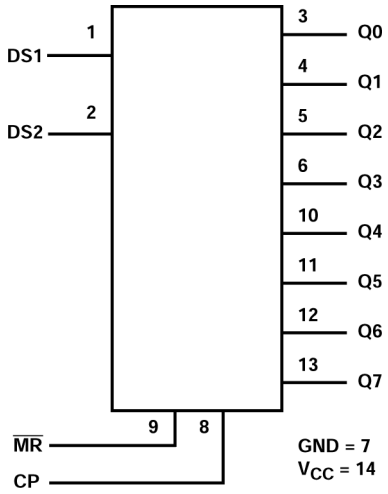
	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

6 Detailed Description

6.1 Overview

The ’AC164 and ’ACT164 are 8-bit serial-in/parallel-out shift registers with asynchronous reset that utilize Advanced CMOS Logic technology. Data is shifted on the positive edge of the clock (CP). A LOW on the Master Reset ($\overline{MR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided; either one can be used as a Data Enable control.

6.2 Functional Block Diagram



6.3 Device Functional Modes

表 6-1. Mode Select - Truth Table

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1	DS2	Q0	Q1 - Q7
RESET (CLEAR)	L	X	X	X	L	L - L
SHIFT	H	↑	l	l	L	q0 - q6
	H	↑	l	h	L	q0 - q6
	H	↑	h	l	L	q0 - q6
	H	↑	h	h	H	q0 - q6

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC164	Click here	Click here	Click here	Click here	Click here
CD74AC164	Click here	Click here	Click here	Click here	Click here
CD54ACT164	Click here	Click here	Click here	Click here	Click here
CD74ACT164	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (November 2023) to Revision C (April 2024)	Page
• Updated R θ JA values: D = 175 to 106.6, all values in °C/W	4

Changes from Revision A (November 1998) to Revision B (November 2023) **Page**

- 添加了*特性*部分、*器件信息*表、*引脚功能*表、*ESD 等级*表、*热性能信息*表、*器件功能模式*、*应用和实施*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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