

CDx4AC257, CDx4ACT257, CD74ACT258 具有三态输出的四路双输入多路复用器

1 特性

- ' AC257、' ACT257..... 同相输出
- CD74ACT258 反相输出
- 缓冲输入
- 典型传播延迟
 - 4.4ns ($V_{CC} = 5V$ 、 $T_A = 25^\circ C$ 且 $C_L = 50pF$ 时)
- ESD 保护超过 2kV (根据 MIL-STD-883 方法 3015)
- 防 SCR 闩锁 CMOS 工艺和电路设计
- 具有双极 FAST™/AS/S 的速度，同时功耗显著降低
- 平衡传播延迟
- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- $\pm 24mA$ 输出驱动电流
 - 扇出到 15 个 FAST™ IC
- 驱动 50 Ω 传输线

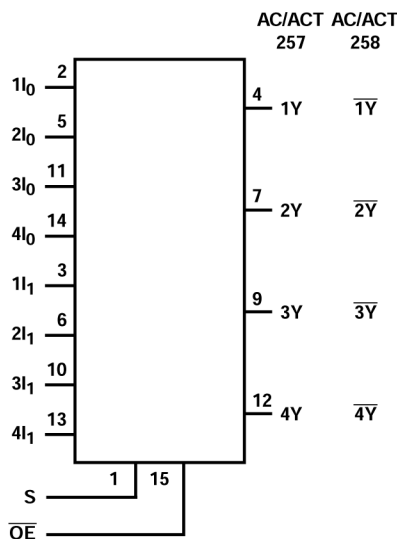
2 说明

' AC257、' ACT257 和 CD74ACT258 是采用高级 CMOS 逻辑技术、具有三态输出的四路双输入多路复用器。

器件信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ | 本体尺寸 ⁽³⁾ |
|-----------------------------------|-------------------|---------------------|---------------------|
| CDx4AC257, CDx4ACT257, CD74ACT258 | D (SOIC , 16) | 9.9mm × 6mm | 9.9mm × 3.9mm |
| | N (PDIP , 16) | 19.3mm × 9.4mm | 19.3mm × 6.35mm |

- (1) 有关更多信息，请参阅节 10。
- (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



功能图

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3 Pin Configuration and Functions

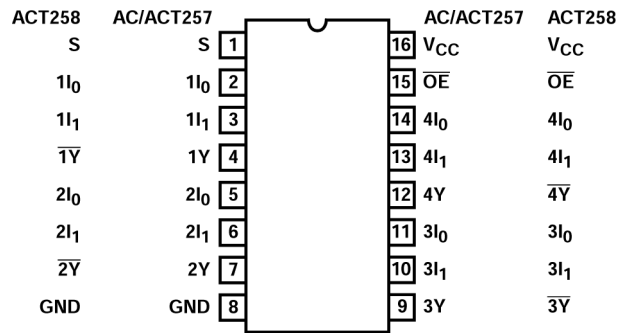


图 3-1. CD54AC257, CD54ACT257 J Package; CD74AC257, CD74ACT257, CD74ACT258 N or D Package; 16-Pin CDIP, PDIP or SOIC (Top View)

表 3-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------|-----|---------------------|-------------------|
| NAME | NO. | | |
| S | 1 | I | Select |
| 1I ₀ | 2 | I | Channel 1 Input 0 |
| 1I ₁ | 3 | I | Channel 1 Input 1 |
| 1Y | 4 | O | Channel 1 Output |
| 2I ₀ | 5 | I | Channel 2 Input 0 |
| 2I ₁ | 6 | I | Channel 2 Input 1 |
| 2Y | 7 | O | Channel 2 Output |
| GND | 8 | G | Ground |
| 3Y | 9 | O | Channel 3 Output |
| 3I ₁ | 10 | I | Channel 3 Input 1 |
| 3I ₀ | 11 | I | Channel 3 Input 0 |
| 4Y | 12 | O | Channel 4 Output |
| 4I ₁ | 13 | I | Channel 4 Input 1 |
| 4I ₀ | 14 | I | Channel 4 Input 0 |
| OE | 15 | I | Output Enable |
| V _{CC} | 16 | P | Positive Supply |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|--|---|-----|---------|
| V _{CC} | Supply voltage | -0.5 | 6 | V |
| I _{IK} | Input diode current | V _I < -0.5V or V _I > V _{CC} + 0.5V | | ±20 mA |
| I _{OK} | Output diode current | V _O < -0.5V or V _O > V _{CC} + 0.5V | | ±50 mA |
| I _O | Output source or sink current per output pin | V _O > -0.5V or V _O < V _{CC} + 0.5V | | ±50 mA |
| I _{CC} or I _{GND} ⁽²⁾ | V _{CC} or ground current | | | ±100 mA |
| T _{stg} | Maximum storage temperature | -65 | 150 | °C |

- (1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
- (2) For up to 4 outputs per device, add ±25mA for each additional output.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------------------------|-------------------------------|-----|-----------------|------|
| T _A | Temperature Range | -55 | 125 | °C |
| V _{CC} ⁽¹⁾ | Supply Voltage Range | | | |
| | AC Types | 1.5 | 5.5 | V |
| | ACT Types | 4.5 | 5.5 | V |
| V _I , V _O | DC Input or Output Voltage | 0 | V _{CC} | V |
| dt/dv | Input Rise and Fall Slew Rate | | | |
| 1.5V to 3V | AC Types | | 50 | ns |
| 3.6V to 5.5V | AC Types | | 20 | ns |
| 4.5V to 5.5V | ACT Types | | 10 | ns |

- (1) Unless otherwise specified, all voltages are referenced to ground.

4.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | D | UNIT |
|-------------------------------|--|---------|------|
| | | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 119.9 | °C/W |

- (1) θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

4.4 Electrical Characteristics

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNIT |
|--------------------------|-----------------|--------------------|---------------------|---------------------|------|------|---------------|------|----------------|------|------|
| | | V _I (V) | I _O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| AC TYPES | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 1.5 | 1.2 | - | 1.2 | - | 1.2 | - | V |
| | | | | 3 | 2.1 | - | 2.1 | - | 2.1 | - | V |
| | | | | 5.5 | 3.85 | - | 3.85 | - | 3.85 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 1.5 | - | 0.3 | - | 0.3 | - | 0.3 | V |
| | | | | 3 | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | | | 5.5 | - | 1.65 | - | 1.65 | - | 1.65 | V |

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNIT |
|---|-------------------|---|-------------------------|---------------------|------|------|---------------|------|----------------|------|------|
| | | V _I (V) | I _O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| High Level Output Voltage | V _{OH} | V _{IH} or V _{IL} | -0.05 | 1.5 | 1.4 | - | 1.4 | - | 1.4 | - | V |
| | | | -0.05 | 3 | 2.9 | - | 2.9 | - | 2.9 | - | V |
| | | | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -4 | 3 | 2.58 | - | 2.48 | - | 2.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 ^{(1), (2)} | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 ^{(1), (2)} | 5.5 | - | - | - | - | 3.85 | - | V |
| Low Level Output Voltage | V _{OL} | V _{IH} or V _{IL} | 0.05 | 1.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 3 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 12 | 3 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 ^{(1), (2)} | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 ^{(1), (2)} | 5.5 | - | - | - | - | 1.65 | V | |
| Input Leakage Current | I _I | V _{CC} or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Three-State Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | μA |
| Quiescent Supply Current MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | μA |
| ACT TYPES | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | V _{OH} | V _{IH} or V _{IL} | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 ^{(1), (2)} | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 ^{(1), (2)} | 5.5 | - | - | - | - | 3.85 | - | V |
| Low Level Output Voltage | V _{OL} | V _{IH} or V _{IL} | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 ^{(1), (2)} | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 ^{(1), (2)} | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | I _I | V _{CC} or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Three-State or Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | μA |
| Quiescent Supply Current MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | μA |
| Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load | Δ I _{CC} | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 2.4 | - | 2.8 | - | 3 | mA |

- (1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- (2) Test verifies a minimum 50 Ω transmission-line-drive capability at 85°C, 75 Ω at 125°C.

表 4-1. ACT Input Load Table

| INPUT | UNIT LOAD |
|-----------------|-----------|
| Data | 0.83 |
| S | 1.27 |
| \overline{OE} | 1.27 |

备注

Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

4.5 Switching Specifications

Input t_r , $t_f = 3ns$, $C_L = 50pF$ (Worst Case)

| PARAMETER | SYMBOL | V_{CC} (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|--|--|--------------------|---------------|-----|------|----------------|-----|------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| AC TYPES | | | | | | | | | |
| Propagation Delay, In to Y AC/ ACT257 | t_{PLH} , t_{PHL} | 1.5 | - | - | 106 | - | - | 117 | ns |
| | | 3.3 ⁽¹⁾ | 3.3 | - | 11.8 | 3.3 | - | 13 | ns |
| | | 5 ⁽²⁾ | 2.4 | - | 8.5 | 2.3 | - | 9.3 | ns |
| Propagation Delay, S to Y AC/ ACT257 | t_{PLH} , t_{PHL} | 1.5 | - | - | 153 | - | - | 168 | ns |
| | | 3.3 | 4.8 | - | 17.1 | 4.7 | - | 18.8 | ns |
| | | 5 | 3.5 | - | 12.2 | 3.4 | - | 13.4 | ns |
| Propagation Delay, \overline{OE} to Y AC/ ACT257 | t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH} | 1.5 | - | - | 167 | - | - | 184 | ns |
| | | 3.3 | 5.3 | - | 18.7 | 5.2 | - | 20.6 | ns |
| | | 5 | 3.8 | - | 13.4 | 3.7 | - | 14.7 | ns |
| Propagation Delay, In to \overline{Y} ' AC/ CD74ACT258 | t_{PLH} , t_{PHL} | 1.5 | - | - | 91 | - | - | 100 | ns |
| | | 3.3 | 2.9 | - | 10.2 | 2.8 | - | 11.2 | ns |
| | | 5 | 2.1 | - | 7.3 | 2 | - | 8 | ns |
| Propagation Delay, S to \overline{Y} ' AC/ CD74ACT258 | t_{PLH} , t_{PHL} | 1.5 | - | - | 153 | - | - | 168 | ns |
| | | 3.3 | 4.8 | - | 17.1 | 4.7 | - | 18.8 | ns |
| | | 5 | 3.5 | - | 12.2 | 3.4 | - | 13.4 | ns |
| Propagation Delay, \overline{OE} to \overline{Y} ' AC/ CD74ACT258 | t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH} | 1.5 | - | - | 167 | - | - | 184 | ns |
| | | 3.3 | 5.3 | - | 18.7 | 5.2 | - | 20.6 | ns |
| | | 5 | 3.8 | - | 13.4 | 3.7 | - | 14.7 | ns |
| Three-State Output Capacitance | C_O | - | - | - | 15 | - | - | 15 | pF |
| Input Capacitance | C_I | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C_{PD} ⁽³⁾ | - | - | 130 | - | - | 130 | - | pF |
| ACT TYPES | | | | | | | | | |
| Propagation Delay, In to Y AC/ ACT257 | t_{PLH} , t_{PHL} | 5 ⁽²⁾ | 2.8 | - | 9.7 | 2.7 | - | 10.7 | ns |
| Propagation Delay, S to Y AC/ ACT257 | t_{PLH} , t_{PHL} | 5 | 4 | - | 14 | 3.9 | - | 15.4 | ns |
| Propagation Delay, \overline{OE} to Y AC/ ACT257 | t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH} | 5 | 4.1 | - | 14.6 | 4 | - | 16.1 | ns |
| Propagation Delay, In to \overline{Y} ' AC/ CD74ACT258 | t_{PLH} , t_{PHL} | 5 | 2.4 | - | 8.5 | 2.3 | - | 9.3 | ns |
| Propagation Delay, S to \overline{Y} ' AC/ CD74ACT258 | t_{PLH} , t_{PHL} | 5 | 4 | - | 14 | 3.9 | - | 15.4 | ns |

Input t_r , $t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case)

| PARAMETER | SYMBOL | V_{CC} (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|--|---|--------------|---------------|-----|------|----------------|-----|------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Propagation Delay, \overline{OE} to \overline{Y} ' AC/CD74ACT258 | t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH} | 5 | 4.1 | - | 14.6 | 4 | - | 16.1 | ns |
| Three-State Output Capacitance | C_O | - | - | - | 15 | - | - | 15 | pF |
| Input Capacitance | C_I | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C_{PD} ⁽³⁾ | - | - | 130 | - | - | 130 | - | pF |

- (1) 3.3V Min is at 3.6V, Max is at 3V.
 (2) 5V Min is at 5.5V, Max is at 4.5V.
 (3) C_{PD} is used to determine the dynamic power consumption per multiplexer.

备注

$$\text{AC: } P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$$

$$\text{ACT: } P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency, } f_o = \text{output frequency, } C_L = \text{output load capacitance, } V_{CC} = \text{supply voltage.}$$

5 Parameter Measurement Information

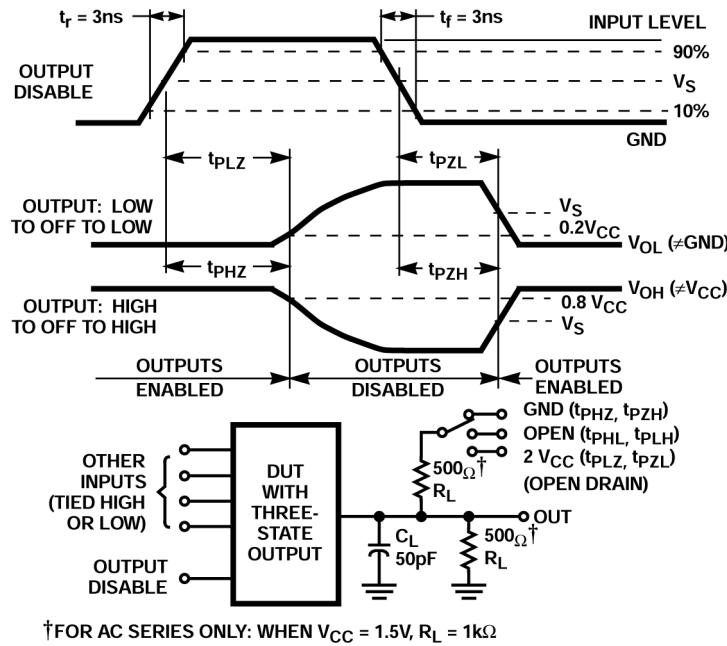


图 5-1. Three-State Propagation Delay Times and Test Circuit

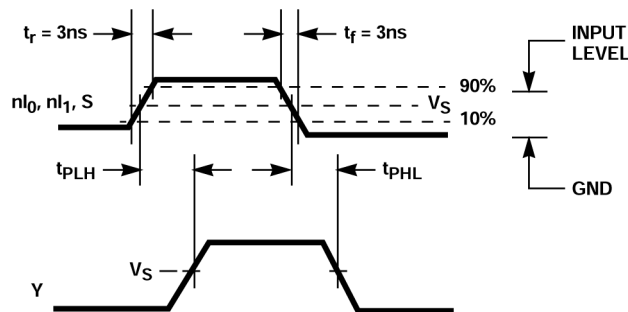


图 5-2. inputs or select to output propagation delays (ac/act257)

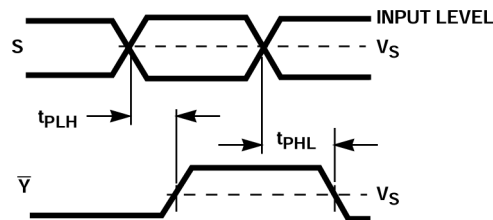


图 5-3. Select to Output Propagation Delays (CD74ACT258)

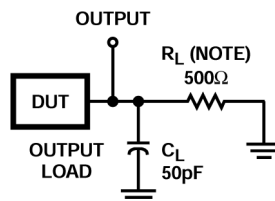


图 5-4.

For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

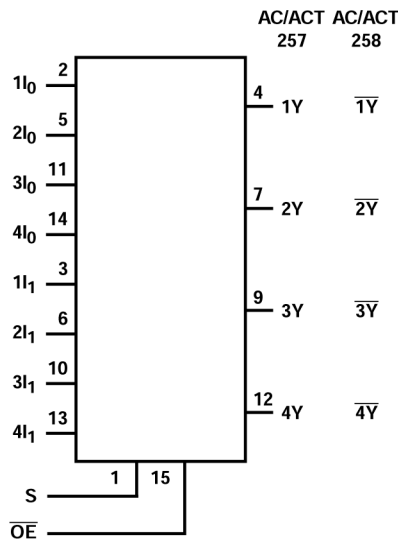
6 Detailed Description

6.1 Overview

Each of these devices selects four bits of data from two sources under the control of a common Select input (S). The Output Enable (\overline{OE}) is active LOW. When \overline{OE} is HIGH, all of the outputs (Y or \overline{Y}) are in the high-impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the ' AC257, ' ACT257, and CD74ACT258. The state of the Select input determines the particular register from which the data comes. The ' AC257, ' ACT257 and CD74ACT258 can also be used as function generators.

6.2 Functional Block Diagram



6.3 Device Functional Modes

表 6-1. Truth Table

| OUTPUT ENABLE | SELECT INPUT | DATA INPUTS | | 257 OUTPUTS | 258 OUTPUTS |
|-----------------|--------------|-------------|-------|-------------|----------------|
| \overline{OE} | S | I_0 | I_1 | Y | \overline{Y} |
| H | X | X | X | Z | Z |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\ \mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\ \mu\text{F}$ and $1\ \mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD54AC257 | Click here | Click here | Click here | Click here | Click here |
| CD54ACT257 | Click here | Click here | Click here | Click here | Click here |
| CD74AC257 | Click here | Click here | Click here | Click here | Click here |
| CD74ACT257 | Click here | Click here | Click here | Click here | Click here |
| CD74ACT258 | Click here | Click here | Click here | Click here | Click here |

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ [中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

| Changes from Revision A (May 2000) to Revision B (August 2024) | Page |
|--|------|
| • 添加了 封装信息表 、 引脚功能表 、 ESD 等级表 、 热性能信息表 、 器件功能模式 、“应用和实施”部分、 器件和文档支持 部分以及 机械、封装和可订购信息 部分..... | 1 |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD54AC257F3A | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54AC257F3A | Samples |
| CD54ACT257F3A | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54ACT257F3A | Samples |
| CD74AC257E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC257E | Samples |
| CD74AC257M | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -55 to 125 | AC257M | |
| CD74AC257M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC257M | Samples |
| CD74ACT257E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT257E | Samples |
| CD74ACT257EE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT257E | Samples |
| CD74ACT257M | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -55 to 125 | ACT257M | |
| CD74ACT257M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT257M | Samples |
| CD74ACT258M | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -55 to 125 | ACT258M | |
| CD74ACT258M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ACT258M | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54AC257, CD54ACT257, CD74AC257, CD74ACT257 :

- Catalog : [CD74AC257](#), [CD74ACT257](#)
- Military : [CD54AC257](#), [CD54ACT257](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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