

## 具有三态输出寄存器的 CD74HC595 8 位移位寄存器

### 1 特性

- 8 位串行输入/并行输出移位寄存器
- 2V 至 6V 的宽工作电压范围
- 高电流三态输出最多可驱动多达 15 个 LSTTL 负载
- 低功耗， $I_{CC}$  最大值为 80 $\mu$ A
- 典型值  $t_{PD} = 14$ ns
- 电压为 5V 时，输出驱动为  $\pm 6$ mA
- 低输出电流，最大值 1 $\mu$ A
- 移位寄存器具有直接清零功能

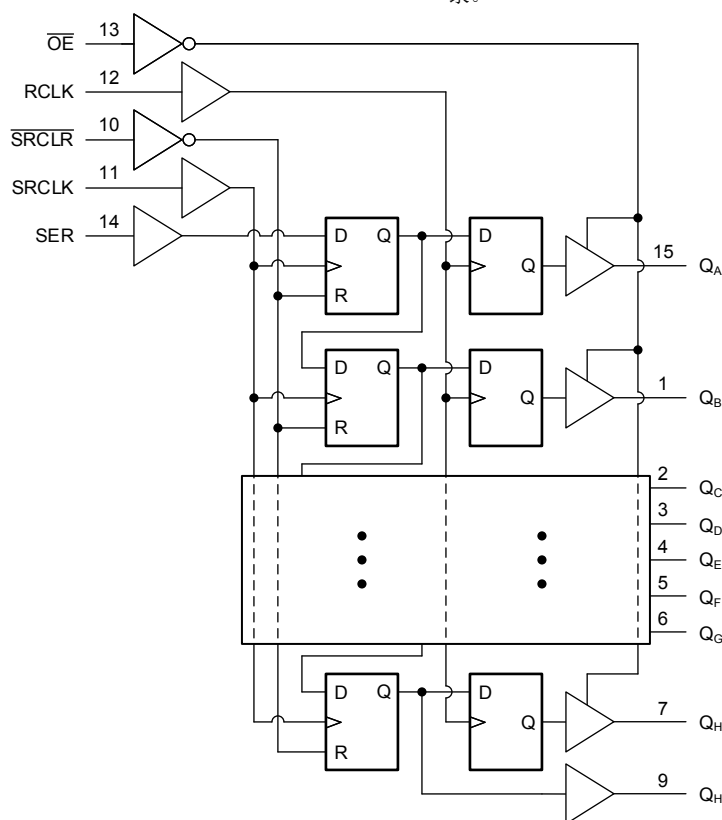
### 2 说明

CD74HC595 是一款具有输出寄存器和三态输出的 8 位串行输入并行输出移位寄存器。

#### 器件信息

零件编号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
CD74HC595E	PDIP (16)	19.31mm × 6.35mm
CD74HC595DW	SOIC-DW (16)	10.30mm × 7.50mm
CD74HC595M	SOIC-D (16)	9.90mm × 3.90mm
CD74HC595NS	SO (16)	10.20mm × 5.30mm
CD74HC595SM	SSOP (16)	6.20mm × 5.30mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能框图



## Table of Contents

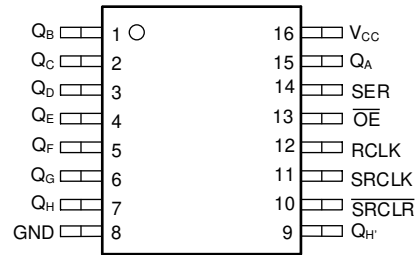
<b>1 特性</b> .....	1	7.2 Functional Block Diagram.....	11
<b>2 说明</b> .....	1	7.3 Device Functional Modes.....	12
<b>3 Revision History</b> .....	2	<b>8 Power Supply Recommendations</b> .....	13
<b>4 Pin Configuration and Functions</b> .....	3	<b>9 Layout</b> .....	13
<b>5 Specifications</b> .....	4	9.1 Layout Guidelines.....	13
5.1 Absolute Maximum Ratings.....	4	<b>10 Device and Documentation Support</b> .....	14
5.2 Recommended Operating Conditions <sup>(1)</sup> .....	4	10.1 Documentation Support.....	14
5.3 Thermal Information.....	4	10.2 接收文档更新通知.....	14
5.4 Electrical Characteristics.....	5	10.3 支持资源.....	14
5.5 Timing Requirements.....	6	10.4 Trademarks.....	14
5.6 Switching Characteristics.....	8	10.5 Electrostatic Discharge Caution.....	14
5.7 Operating Characteristics.....	9	10.6 术语表.....	14
<b>6 Parameter Measurement Information</b> .....	10	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	14
<b>7 Detailed Description</b> .....	11		
7.1 Overview.....	11		

### 3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (January 2004) to Revision A (February 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....	1

## 4 Pin Configuration and Functions



**D, DW, N, NS, or DB Package**  
**16-Pin SOIC, PDIP, SO, or SSOP**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	For V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	For V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current	For -0.5V < V <sub>O</sub> = 0 to V <sub>CC</sub>		±35 mA
	Continuous current through V <sub>CC</sub> or GND		±70	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2V 3.15			V
		V <sub>CC</sub> = 4.5V			
		V <sub>CC</sub> = 6V 4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2V 0.5			V
		V <sub>CC</sub> = 4.5V 1.35			
		V <sub>CC</sub> = 6V 1.8			
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
t <sub>t</sub> <sup>(2)</sup>	Input transition rise and fall time	V <sub>CC</sub> = 2V 500		1000	ns
		V <sub>CC</sub> = 4.5V 400			
		V <sub>CC</sub> = 6V			
T <sub>A</sub>	Operating free-air temperature	-55		125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) If this device is used in the threshold region (from V<sub>IL</sub> max = 0.5 V to V<sub>IH</sub> min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>t</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

### 5.3 Thermal Information

THERMAL METRIC		N (PDIP)	DW (SOIC)	D (SOIC)	NS (SO)	DB (SSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	67	57	73	64	82	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Electrical Characteristics

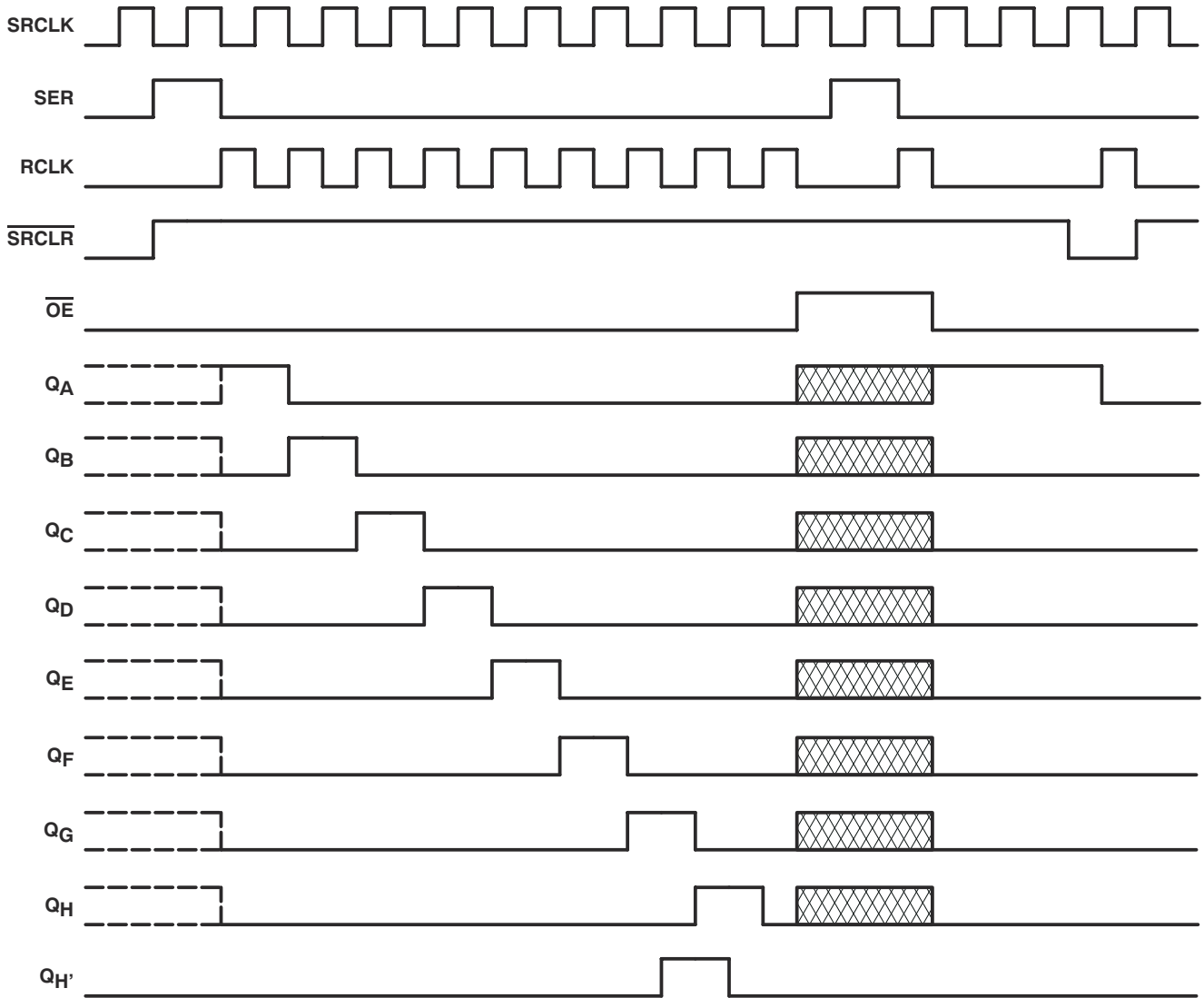
PARAMETER	TEST CONDITIONS <sup>(1)</sup>	V <sub>CC</sub> (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>											
V <sub>OH</sub>	I <sub>OH</sub> = - 20 μA	2	1.9	1.998		1.9		1.9	V		
		4.5	4.4	4.499		4.4		4.4			
		6	5.9	5.999		5.9		5.9			
	4.5	Q <sub>H</sub> , I <sub>OH</sub> = - 4 mA		3.98	4.3		3.84			3.7	
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = - 6 mA		3.98	4.3		3.84			3.7	
	6	Q <sub>H</sub> , I <sub>OH</sub> = - 5.2 mA		5.48	5.8		5.34			5.2	
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = - 57.8 mA		5.48	5.8		5.34			5.2	
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	2		0.002	0.1		0.1		0.1	V	
		4.5		0.001	0.1		0.1		0.1		
		6		0.001	0.1		0.1		0.1		
	4.5	Q <sub>H</sub> , I <sub>OL</sub> = 4 mA			0.17	0.26		0.33		0.4	V
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 6 mA			0.17	0.26		0.33		0.4	V
	6	Q <sub>H</sub> , I <sub>OL</sub> = 5.2 mA			0.15	0.26		0.33		0.4	V
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 7.8 mA			0.15	0.26		0.33		0.4	V
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6		±0.1	±100		±1000		±1000	nA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, Q <sub>A</sub> -Q <sub>H</sub>	6		±0.01	±0.5		±5		±10	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6			8		80		160	μA	
C <sub>i</sub>		2 to 6		3	10		10		10	pF	

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>

## 5.5 Timing Requirements

PARAMETER			V <sub>CC</sub> (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
f <sub>clock</sub>	Clock frequency		2	6		5		4.2	MHz	
			4.5	31		25		21		
			6	36		29		25		
t <sub>w</sub>	Pulse duration	SRCLK or RCLK high or low	2	80		100		120	ns	
			4.5	16		20		24		
			6	14		17		20		
		SRCLR low	2	80		100		120		
			4.5	16		20		24		
			6	14		17		20		
t <sub>su</sub>	Setup time	SER before SRCLK ↑	2	100		125		150	ns	
			4.5	20		25		30		
			6	17		21		25		
		SRCLK ↑ before RCLK ↑ <sup>(1)</sup>	2	75		94		113		
			4.5	15		19		23		
			6	13		16		19		
		SRCLR low before RCLK ↑	2	50		65		75		
			4.5	10		13		15		
			6	9		11		13		
		SRCLR high (inactive) before SRCLK ↑	2	50		60		75		
			4.5	10		12		15		
			6	9		11		13		
t <sub>h</sub>	Hold time, SER after SRCLK ↑		2	0		0		0	ns	
			4.5	0		0		0		
			6	0		0		0		

- (1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.



NOTE:  implies that the output is in 3-State mode.

### Timing Diagram

## 5.6 Switching Characteristics

over operating free-air temperature range,  $C_L = 50\text{pF}$  (unless otherwise noted) (Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			2	6	26		5		4.2	MHz	
			4.5	31	38		25		21		
			6	36	42		29		25		
$t_{pd}$	SRCLK	$Q_H$	2		50	160		200		240	ns
			4.5		17	32		40		48	
			6		14	27		34		41	
	RCLK	$Q_A-Q_H$	2		50	150		187		225	
			4.5		17	30		37		45	
			6		14	26		32		38	
$t_{PHL}$	$\overline{\text{SRCLR}}$	$Q_H$	2		51	175		219		261	ns
			4.5		18	35		44		52	
			6		15	30		37		44	
$t_{en}$	$\overline{\text{OE}}$	$Q_A-Q_H$	2		40	150		187		225	ns
			4.5		15	30		37		45	
			6		13	26		32		38	
$t_{dis}$	$\overline{\text{OE}}$	$Q_A-Q_H$	2		42	200		250		300	ns
			4.5		23	40		50		60	
			6		20	34		43		51	
$t_t$		$Q_A-Q_H$	2		28	60		75		90	ns
			4.5		8	12		15		18	
			6		6	10		13		15	
		$Q_H$	2		28	75		95		110	
			4.5		8	15		19		22	
			6		6	13		16		19	

## 5.6 Switching Characteristics

over operating free-air temperature range,  $C_L = 150\text{pF}$  (unless otherwise noted) (Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{pd}$	RCLK	$Q_A-Q_H$	2		60	200		250		300	MHz
			4.5		22	40		50		60	
			6		19	34		43		51	
$t_{en}$	$\overline{\text{OE}}$	$Q_A-Q_H$	2		70	200		250		298	ns
			4.5		2340	40		50		60	
			6		19	34		43		51	
$t_t$		$Q_A-Q_H$	2		45	210		265		315	ns
			4.5		17	42		53		63	
			6		13	36		45		53	

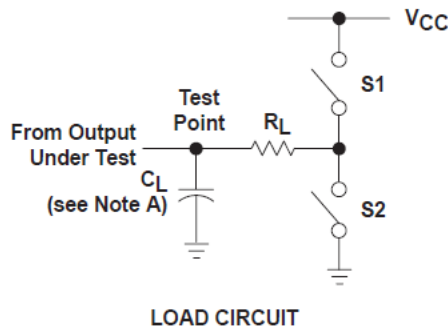


## 5.7 Operating Characteristics

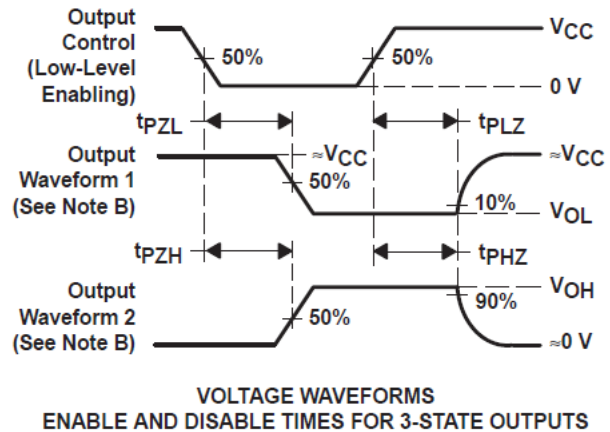
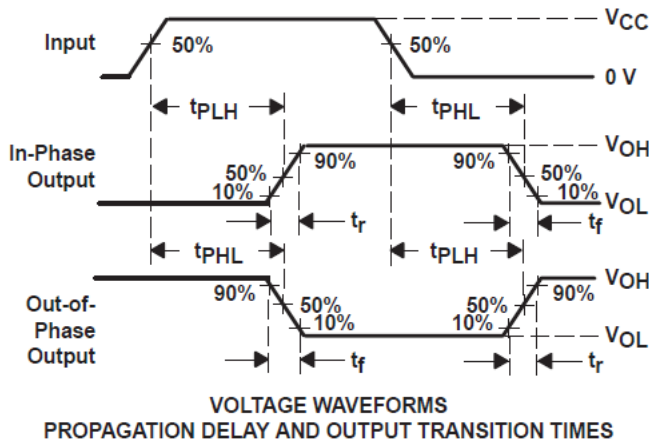
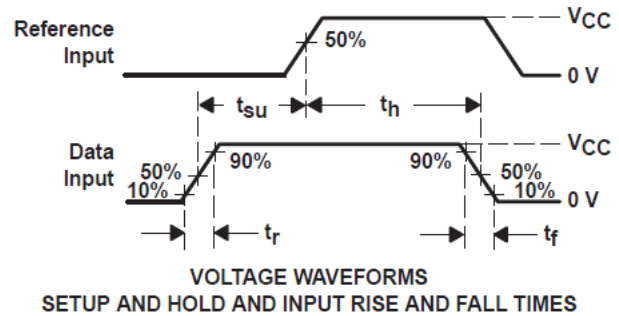
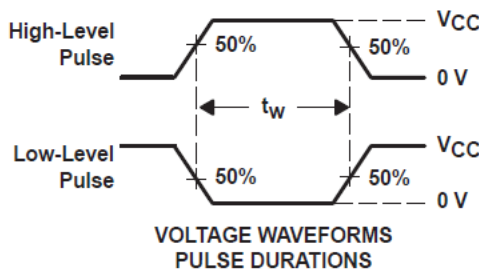
 $T_A = 25^\circ\text{C}$ 

		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	400	pF

## 6 Parameter Measurement Information



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	$t_{PZH}$	1 k $\Omega$ 50 pF or 150 pF	Open	Closed
	$t_{PZL}$		Closed	Open
$t_{dis}$	$t_{PHZ}$	1 k $\Omega$ 50 pF	Open	Closed
	$t_{PLZ}$		Closed	Open
$t_{pd}$ or $t_t$	--	50 pF or 150 pF	Open	Open



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 D. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.  
 E. The outputs are measured one at a time, with one input transition per measurement.  
 F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**图 6-1. Load Circuit and Voltage Waveforms**

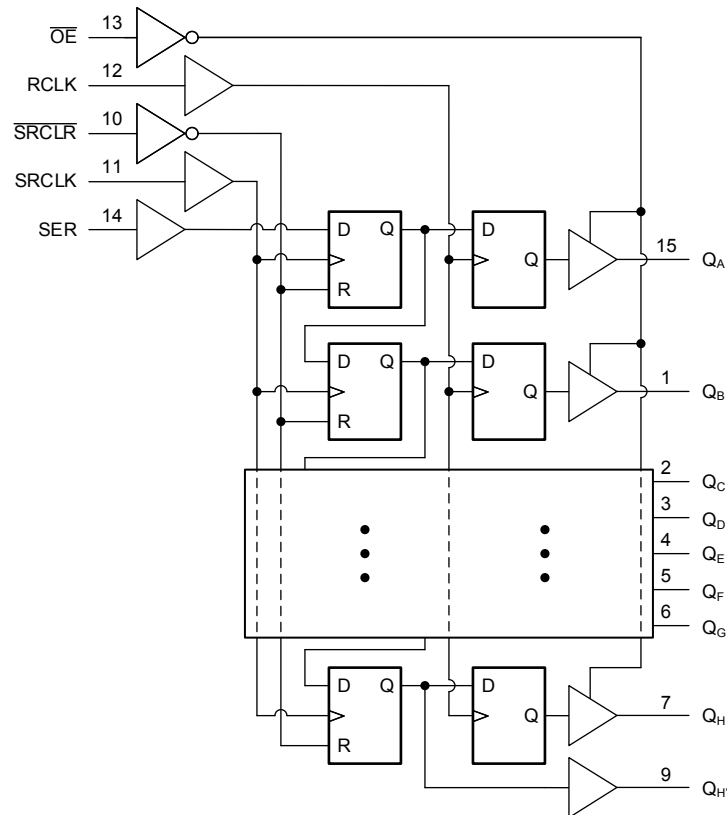
## 7 Detailed Description

### 7.1 Overview

The CD74HC595 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear ( $\overline{\text{SRCLR}}$ ) input, serial ( $\text{SER}$ ) input, and serial output for cascading. When the output-enable ( $\overline{\text{OE}}$ ) input is high, the outputs are in the high-impedance state.

Both the shift register clock ( $\text{SRCLK}$ ) and storage register clock ( $\text{RCLK}$ ) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

表 7-1 lists the functional modes of the CD74HC595.

表 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	
X	X	X	X	H	Outputs Q <sub>A</sub> - Q <sub>H</sub> are disabled
X	X	X	X	L	Outputs Q <sub>A</sub> - Q <sub>H</sub> are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register.
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through.

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 10.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 重要声明和免责声明

TI 提供技术和可靠性数据 (包括数据表)、设计资源 (包括参考设计)、应用或其他设计建议、网络工具、安全信息和其他资源, 不保证没有瑕疵且不做任何明示或暗示的担保, 包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任: (1) 针对您的应用选择合适的 TI 产品, (2) 设计、验证并测试您的应用, (3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更, 恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务, TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com/legal/termsofsale.html>) 或 [ti.com](https://www.ti.com) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, 德州仪器 (TI) 公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC595DW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-55 to 125	HC595M	
CD74HC595DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M	Samples
CD74HC595E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC595E	Samples
CD74HC595M	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	HC595M	
CD74HC595M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HC595M	Samples
CD74HC595MT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	HC595M	
CD74HC595NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M	Samples
CD74HC595SM96	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ595	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

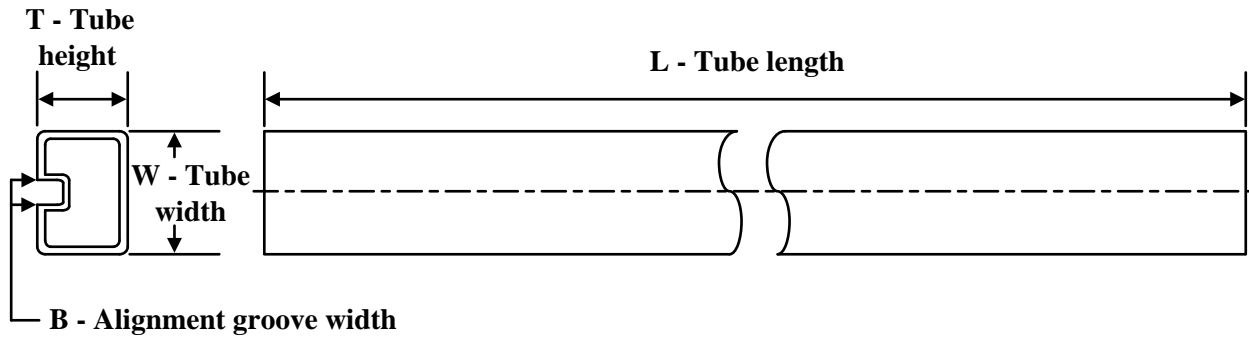
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC595DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD74HC595M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC595NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC595SM96	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC595DWR	SOIC	DW	16	2000	350.0	350.0	43.0
CD74HC595M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC595NSR	SO	NS	16	2000	356.0	356.0	35.0
CD74HC595SM96	SSOP	DB	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC595E	N	PDIP	16	25	506	13.97	11230	4.32



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

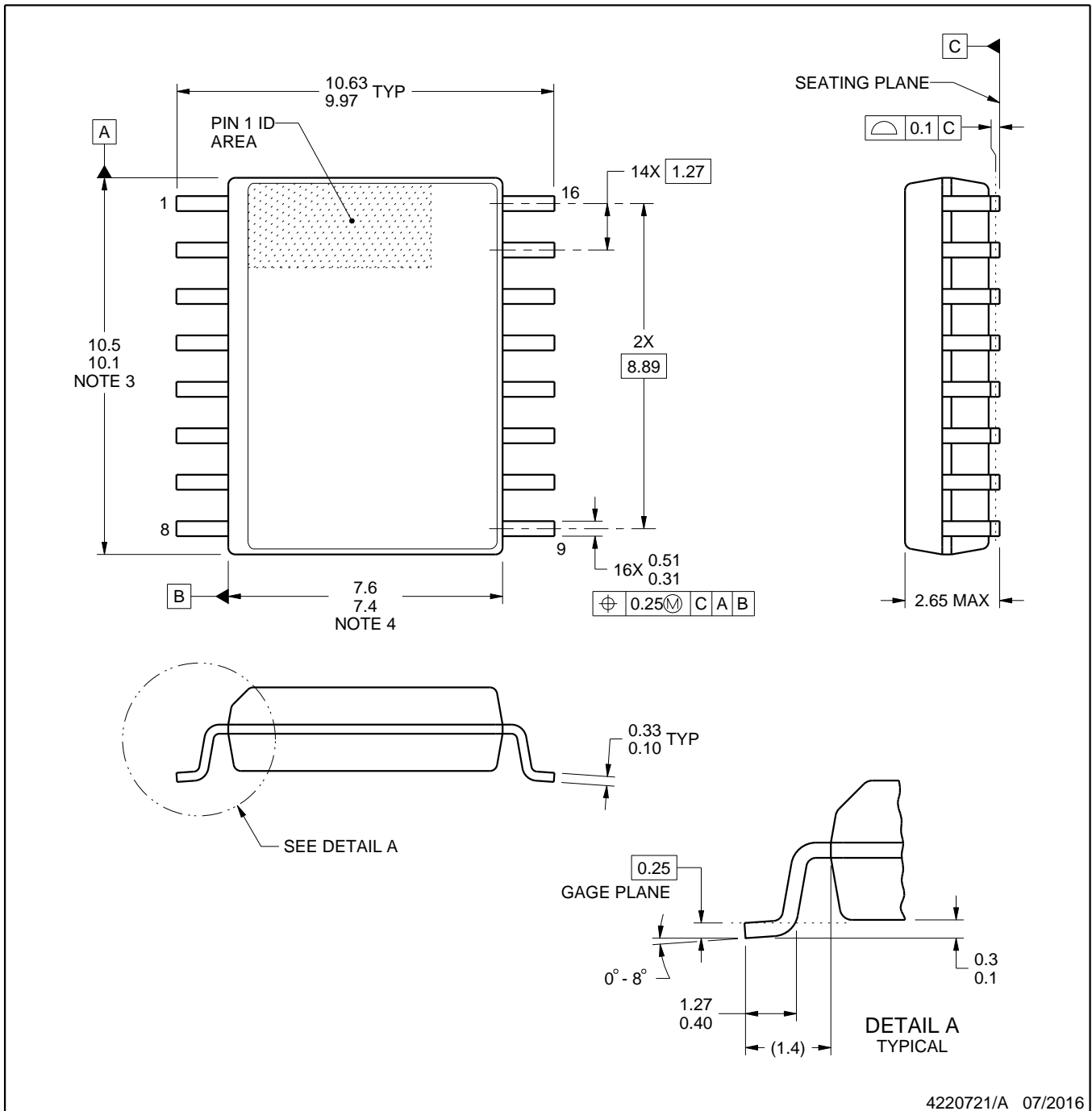


DW0016A

# PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司