INA141 G = 10V/V 或 100V/V 的低功耗精密仪表放大器

1 特性

- 低失调电压：
  - G = 100V/V 时为 50μV（最大值）
- 低温漂：
  - G = 100V/V 时为 0.5μV/°C（最大值）
- 准确增益：
  - G = 10V/V 时为 ±0.05%
- 低输入偏置电流：
  - 5nA（最大值）
- 高 CMR：
  - 117dB（最小值）
- 输入保护电压可达 ±40V
- 宽电源电压范围：±2.25V 至 ±18V
- 低静态电流：750μA

2 应用

- 温度变送器
- 医疗仪器
- 数据采集 (DAQ)
- 过程分析（pH、气体、浓度、力和湿度）

3 说明

INA141 是一款低功耗通用仪表放大器，可提供出色的准确性。此器件采用多功能三级运算放大器设计，尺寸小巧，适用于多种应用。即使在高增益（G = 100V/V 时为 200kHz）情况下，电流反馈输入电路也可提供宽带宽。

通过简单的引脚连接设置 10V/V 或 100V/V 的准确增益，无需外部电阻器。内部输入保护可经受高达 ±40V 的电压且无损坏。

INA141 经过激光修整，具有超低失调电压 (50 μ V)、超低温漂 (0.5 μ V/°C) 和高共模抑制（G ≥ 100V/V 时为 117dB）。该器件采用低至 ±2.25V 的电源电压，静态电流仅为 750μA。

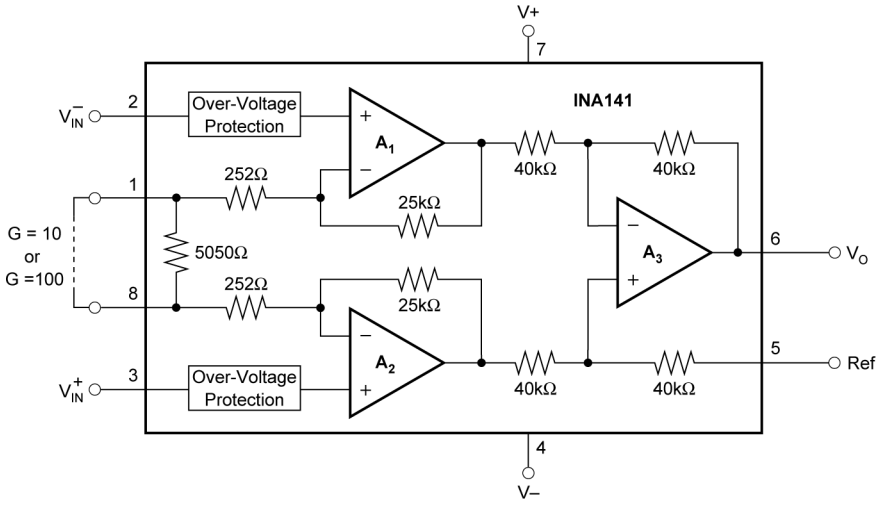
INA141 采用 8 引脚 SOIC 封装，额定温度范围为 −40°C 至 +85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
INA141	D（SOIC，8）	4.9mm × 6mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。



基本连接

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2000) to Revision A (August 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 删除了数据表中的 PDIP 封装	1
• Added single supply specification to Absolute Maximum Ratings	4
• Added note that output short-circuit (to ground) means short-circuit to $V_S/2$ in Absolute Maximum Ratings	4
• Added "TA = –40°C to +85°C" test condition to Offset voltage vs temperature specification in the Electrical Characteristics and renamed to Offset voltage drift	5
• Added test conditions "VREF = 0 V, VCM = VS / 2 and G = 10 below the title	5
• Deleted common-mode voltage typical values in the Electrical Characteristics and combined to one line	5
• Added "TA = –40°C to +85°C" test condition to Bias current vs temperature specification in the Electrical Characteristics and renamed to Input bias current drift for clarity	5
• Added "TA = –40°C to +85°C" test condition to Offset current vs temperature specification in Electrical Characteristics and renamed to Input offset current drift for clarity	5
• Added "TA = –40°C to +85°C" test condition for Gain error vs temperature in the Electrical Characteristics and renamed to Gain drift for clarity	5
• Changed parameter names from "Voltage - Positive" and "Voltage - Negative" to "Output voltage" in the Electrical Characteristics	5
• Added "Continuous to VS / 2" test condition short-circuit current specification in the Electrical Characteristics for clarity	5
• Changed short-circuit current typical value from +6/-15 mA ±20 mA	5
• Changed bandwidth typical value from 1 MHz to 610 kHz in the Electrical Characteristics	5
• Changed slew rate typical value from 4 V/µs to 2 V/µs in the Electrical Characteristics	5
• Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from Electrical Characteristics	5
• Changed Figure 6-2, *Common-Mode Rejection vs Frequency*	7
• Changed Figure 6-8, *Quiescent Current and Slew Rate vs Temperature*	7
• Changed *Output Voltage Swing vs Output Current* single plot to Figure 6-12, *Positive Output Voltage Swing vs Output Current* and Figure 6-12, *Negative Output Voltage Swing vs Output Current*	7
• Changed Figure 6-18, *Small-Signal Step Response*	7
• Changed Figure 6-19, *Large-Signal Step Response*	7
• Changed Figure 6-20, *0.1-Hz to 10-Hz Input-Referred Voltage Noise*	7
• Changed G from 1 to 10 V/V at the end of the *Application Information* section	11
• Deleted reference to *Input Bias Current vs Common-Mode Input Voltage* plot	13

5 Pin Configuration and Functions

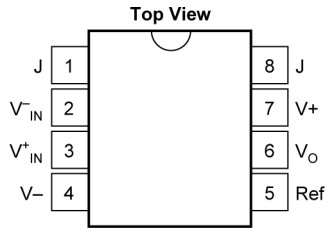


图 5-1. D Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
J	1, 8	Input	Gain selection. G = 10 V/V if not shorted G = 100 V/V if shorted A resistance of 0.5 Ω decreases gain by 0.1%.
Ref	5	Input	Reference input. This pin must be driven by low impedance
V –	4	—	Negative supply
V+	7	—	Positive supply
V^-_{IN}	2	Input	Negative (inverting) input
V^+_{IN}	3	Input	Positive (noninverting) input
V_O	6	Output	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, V_S = (V+) – (V–)		±18	V
		Single supply, V_S = (V+) – 0 V		36	
	Input voltage			±40	V
	Output short-circuit (to ground)(2)		Continuous		
T_A	Operating temperature		–40	125	°C
T_{stg}	Storage temperature		–40	125	°C
T_J	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			300	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
T_A	Specified temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA141 D (SOIC) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 10 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage (RTI)	INA141P, INA141U	G = 10 V/V			±50	±100	µV
			G = 100 V/V			±20	±50	
		INA141PA, INA141UA	G = 10 V/V			±50	±250	
			G = 100 V/V			±20	±125	
	Offset voltage drift (RTI)	T_A = –40°C to +85°C	INA141P, INA141U	G = 10 V/V		±0.5	±2	µV/℃
				G = 100 V/V		±0.2	±0.5	
			INA141PA, INA141UA	G = 10 V/V		±0.5	±2.5	
				G = 100 V/V		±0.2	±1.5	
PSRR	Power-supply rejection ratio (RTI)	V_S = ±2.25 V to ±18 V	INA141P, INA141U	G = 10 V/V		±2	±10	µV/V
				G = 100 V/V		±0.4	±1	
			INA141PA, INA141UA	G = 10 V/V		±2	±20	
				G = 100 V/V		±0.4	±3	
	Long-term stability	G = 10 V/V				0.5		µV/mo
		G = 100 V/V				0.2		µV/mo
	Input impedance	Differential				100 || 2		GΩ || pF
		Common-mode				100 || 9		
V_{CM}	Common-mode voltage[1]	V_O = 0 V			(V–) +2		(V+) – 2	V
CMRR	Common-mode rejection	V_{CM} = ±13 V, Δ R_S = 1 kΩ	INA141P, INA141U	G = 10 V/V	100	106		dB
				G = 100 V/V	117	125		
			INA141PA, INA141UA	G = 10 V/V	93	100		
				G = 100 V/V	110	120		
INPUT BIAS CURRENT								
I_B	Input bias current	INA141P, INA141U				±2	±5	nA
		INA141PA, INA141UA				±2	±10	
	Input bias current drift	T_A = –40°C to +85°C				±30		pA/℃
I_{OS}	Input offset current	INA141P, INA141U				±1	±5	nA
		INA141PA, INA141UA				±1	±10	nA
	Input offset current drift	T_A = –40°C to +85°C				±30		pA/℃
NOISE								
e_N	Voltage noise (RTI)	R_S = 0 Ω	G = 10 V/V	f = 10 Hz		22		nV/ √Hz
				f = 100 Hz		13		
				f = 1 kHz		12		
				f_B = 0.1 Hz to 10 Hz		0.6		$µV_{PP}$
			G = 100 V/V	f = 10 Hz		10		nV/ √Hz
				f = 100 Hz		8		
				f = 1 kHz		8		
				f_B = 0.1 Hz to 10 Hz		0.2		$µV_{PP}$
I_n	Current noise	f = 10 Hz				0.9		pA/ √Hz
		f = 1 kHz				0.3		
		f_B = 0.1 Hz to 10 Hz				30		pA_{PP}

6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 10 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
GAIN								
G	Gain				10		100	V/V
GE	Gain error	V_O = ±13.6 V	INA141P, INA141U	G = 10 V/V		±0.01	±0.05	%
				G = 100 V/V		±0.03	±0.075	
			INA141PA, INA141UA	G = 10 V/V		±0.01	±0.15	
				G = 100 V/V		±0.03	±0.15	
	Gain drift[6]	G = 10 V/V or 100 V/V, T_A = –40°C to +85°C				±2	±10	ppm/°C
	Gain nonlinearity	INA141P, INA141U	G = 10 V/V			±0.0003	±0.001	% of FSR
			G = 100 V/V			±0.0005	±0.002	
		INA141PA, INA141UA	G = 10 V/V			±0.0003	±0.002	
			G = 100 V/V			±0.0005	±0.004	
OUTPUT								
	Output voltage				(V–) + 1.4	(V±) ∓ 0.9	(V+) – 1.4	V
C_L	Load capacitance	Stable operation				1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2				±20		mA
FREQUENCY RESPONSE								
BW	Bandwidth, –3 dB	G = 10 V/V				610		kHz
		G = 100 V/V				200		kHz
SR	Slew rate	G = 10 V/V, V_O = ±10 V				2		V/µs
t_S	Settling time	To 0.01%, V_O = ±5 V	G = 10 V/V			7		µs
			G = 100 V/V			9		
	Overload recovery	50% input overload				4		µs
POWER SUPPLY								
I_Q	Quiescent current	V_{IN} = 0 V				±750	±800	µA

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ (unless otherwise noted)

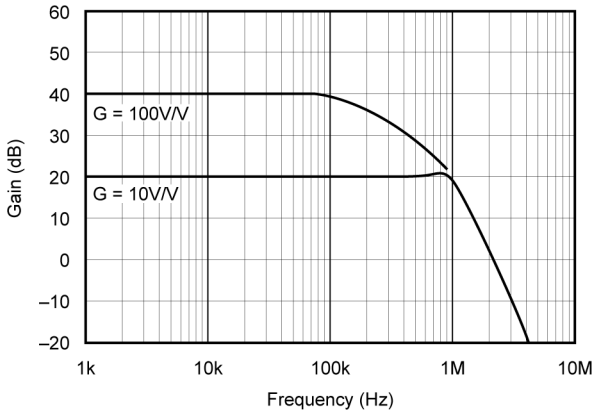


图 6-1. Gain vs Frequency

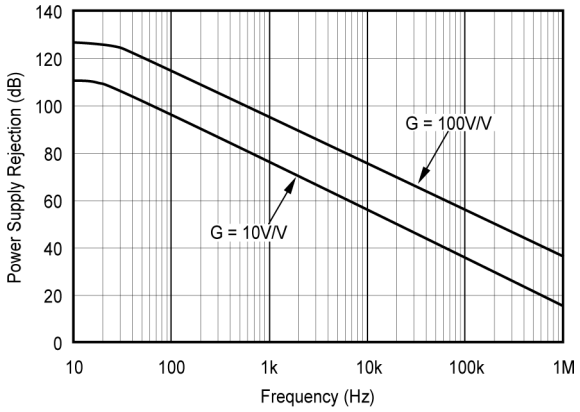


图 6-2. Common-Mode Rejection vs Frequency

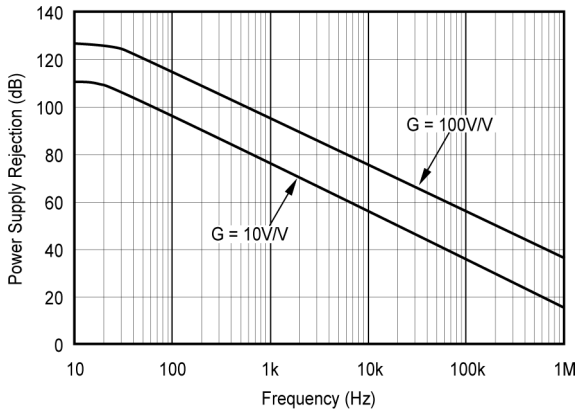


图 6-3. Positive Power Supply Rejection vs Frequency

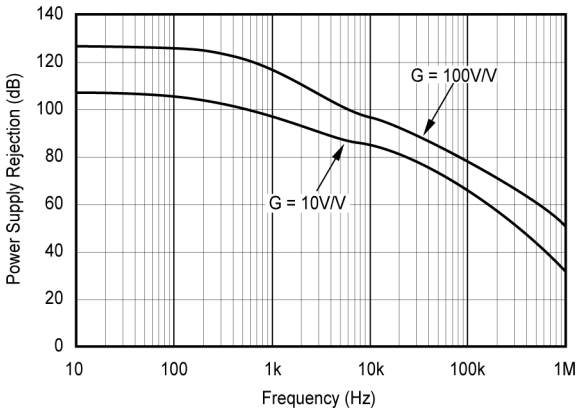
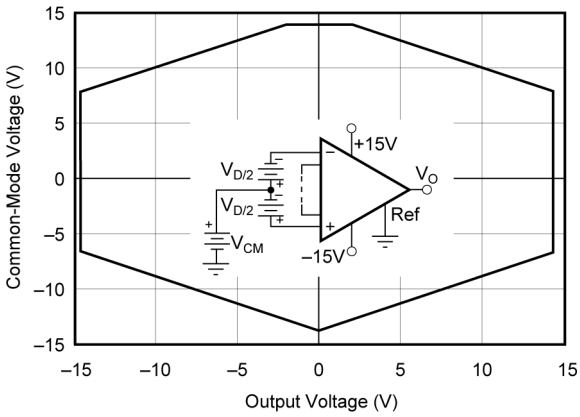
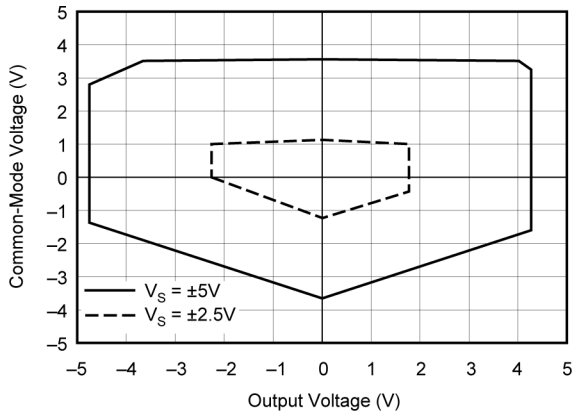


图 6-4. Negative Power Supply Rejection vs Frequency



V_S = ±15 V

图 6-5. Input Common-Mode Range vs Output Voltage



V_S = ±5 V, ±2.5 V

图 6-6. Input Common-Mode Range vs Output Voltage

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ (unless otherwise noted)

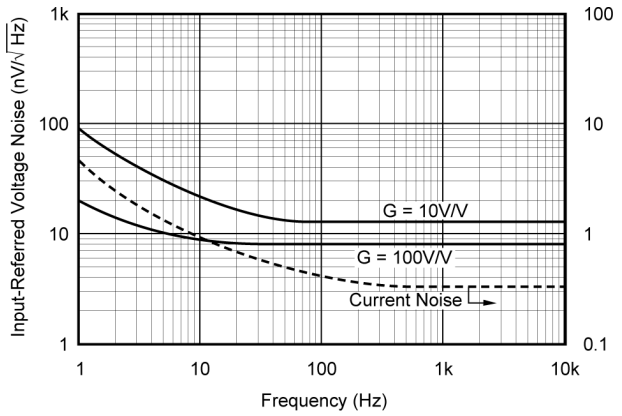


图 6-7. Input-Referred Noise vs Frequency

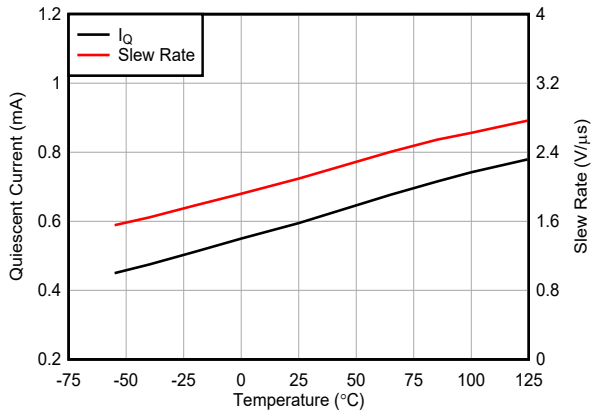


图 6-8. Quiescent Current and Slew Rate vs Temperature

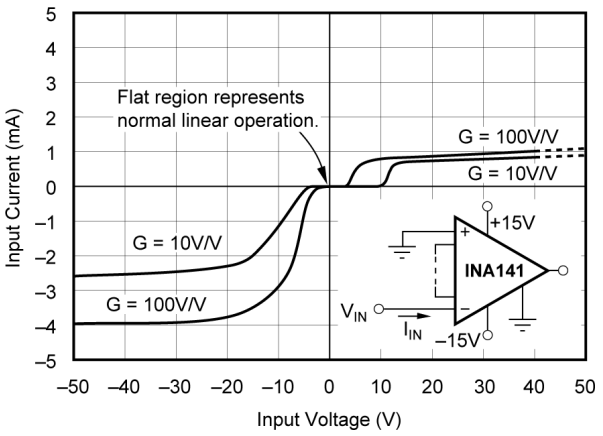


图 6-9. Input Overvoltage V/I Characteristics

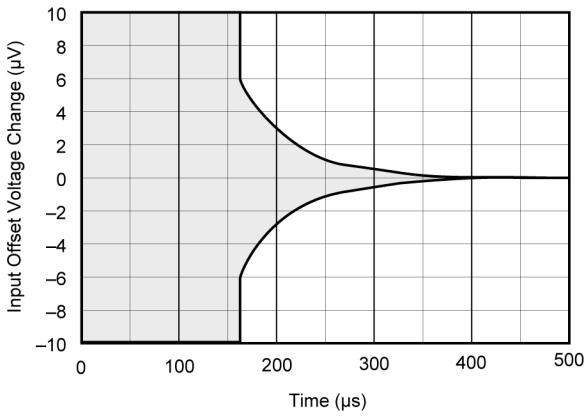


图 6-10. Input Offset Voltage Warmup

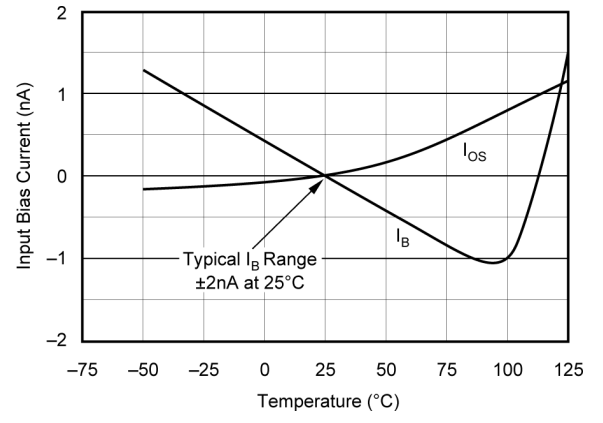


图 6-11. Input Bias Current vs Temperature

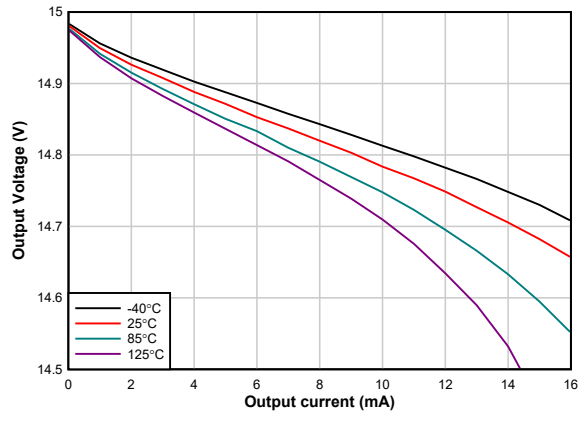


图 6-12. Positive Output Voltage Swing vs Output Current

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ (unless otherwise noted)

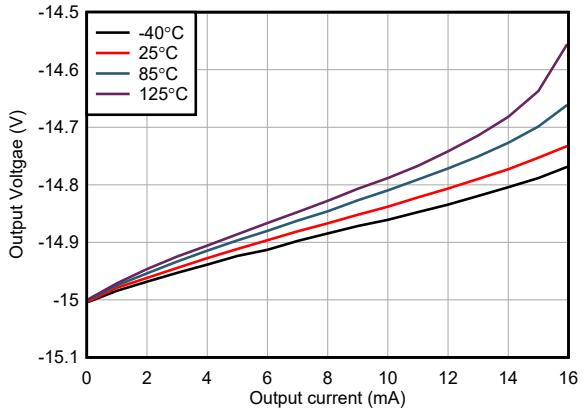


图 6-13. Negative Output Voltage Swing vs Output Current

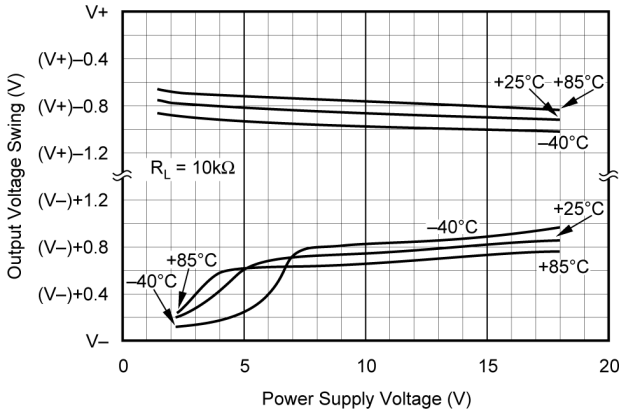


图 6-14. Output Voltage Swing vs Power Supply Voltage

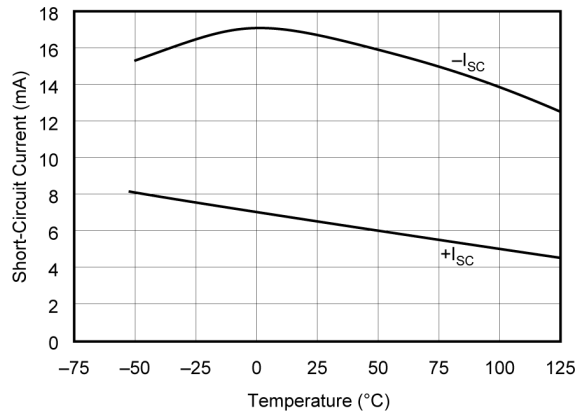


图 6-15. Short-circuit Output Current vs Temperature

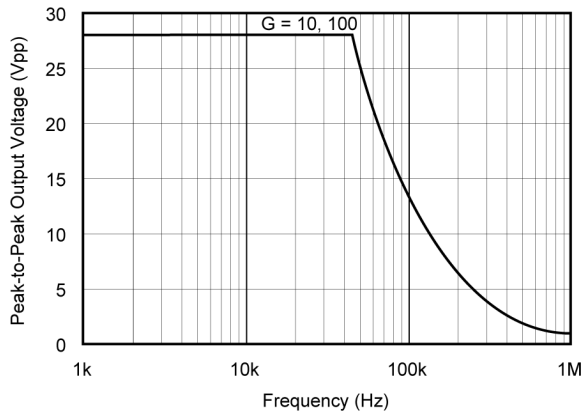


图 6-16. Maximum Output Voltage vs Frequency

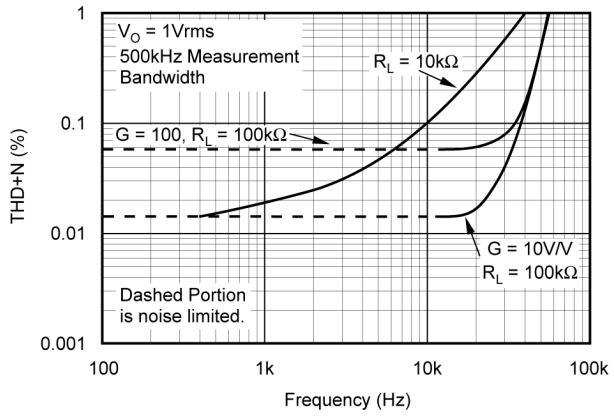


图 6-17. Total Harmonic Distortion + Noise vs Frequency

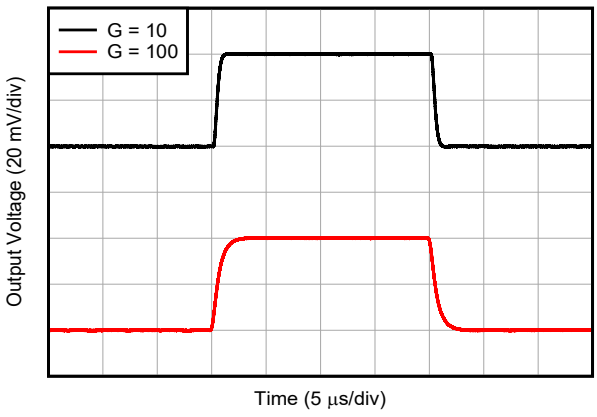


图 6-18. Small-Signal Step Response

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ (unless otherwise noted)

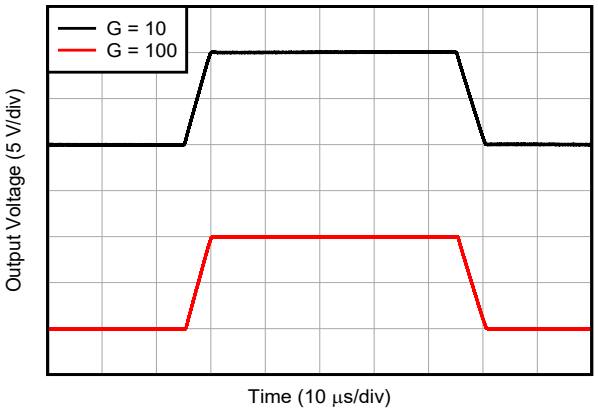


图 6-19. Large-Signal Step Response

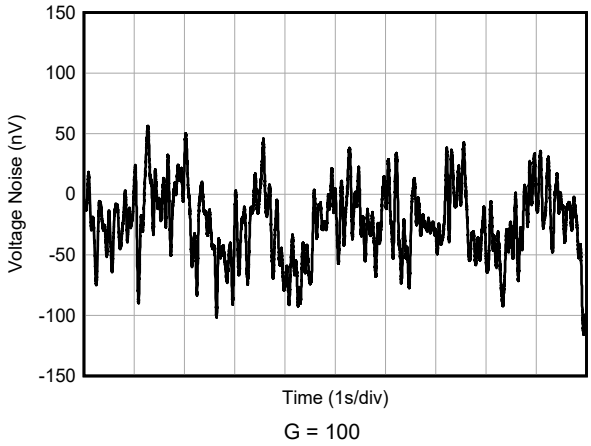


图 6-20. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

图 7-1 shows the basic connections required for operation of the INA141. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins as shown.

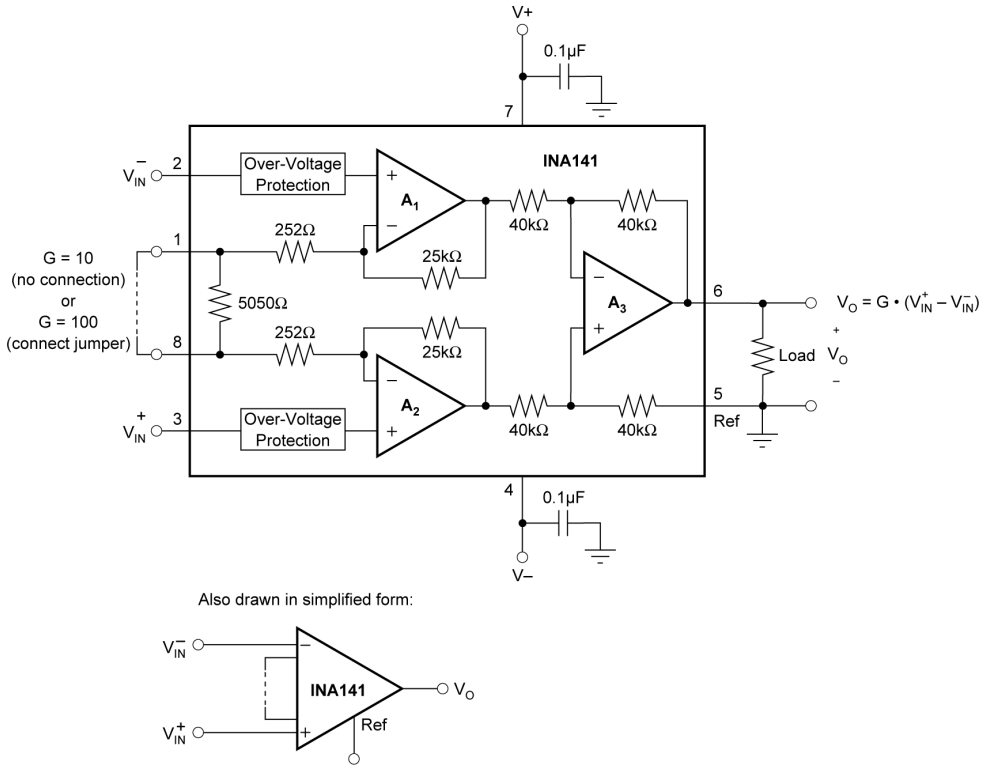


图 7-1. Basic Connections.

The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. A resistance of 8 Ω in series with the Ref pin causes a typical device to degrade to approximately 80 dB CMR (G = 10 V/V).

7.1.1 Setting the Gain

Gain is selected with a jumper connection (see 图 7-1). With no jumper installed, G = 10 V/V. With a jumper installed, G = 100 V/V. To preserve good gain accuracy, this jumper must have low series resistance. A resistance of 0.5 Ω in series with the jumper decreases the gain by 0.1%.

Internal resistor ratios are laser trimmed to provide excellent gain accuracy. Actual resistor values can vary by approximately ±25% from the nominal values shown.

Gains between 10 V/V and 100 V/V are achieved by connecting an external resistor to the jumper pins. However, this configuration is not recommended because the ±25% variation of internal resistor values makes the required external resistor value uncertain. A companion model, the INA128, features accurately trimmed internal resistors so that gains from 1 V/V to 10,000 V/V can be set with an external resistor.

7.1.2 Dynamic Performance

Typical performance curve *Gain vs Frequency* (图 6-1) shows that, despite the low quiescent current, the INA141 achieves wide bandwidth, even at G = 100 V/V. This wide bandwidth is a result of the current-feedback topology of the INA141. Settling time also remains excellent at G = 100 V/V.

7.1.3 Noise Performance

The INA141 provides very low noise in most applications. Low-frequency noise is approximately 0.2 μV_{PP} measured from 0.1 Hz to 10 Hz (G = 100 V/V). The INA141 provides dramatically improved noise when compared to state-of-the-art, chopper-stabilized amplifiers.

7.1.4 Offset Trimming

The INA141 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. 图 7-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref pin is summed with the output. The op-amp buffer provides low impedance at the Ref pin to preserve good common-mode rejection.

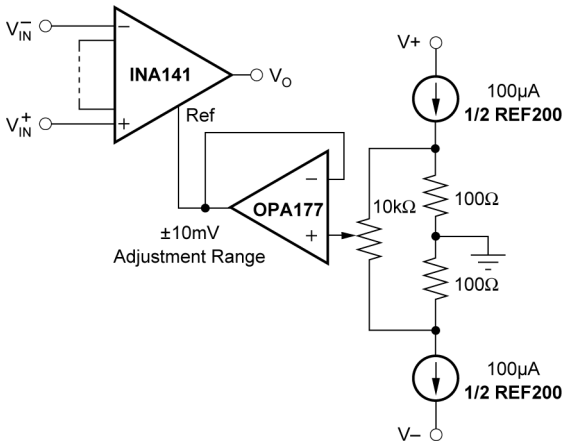


图 7-2. Optional Trimming of Output Offset Voltage.

7.1.5 Input Bias Current Return Path

The input impedance of the INA141 is extremely high—approximately 10^{10} Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 图 7-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA141 and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in 图 7-3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

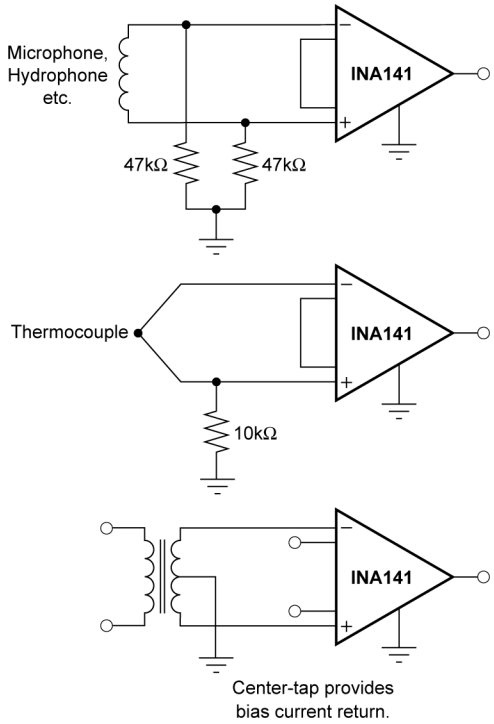


图 7-3. Providing an Input Common-Mode Current Path.

7.1.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA141 is from approximately 1.4 V less than the positive supply voltage to 1.7 V greater than the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Therefore, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see the *Input Common-Mode Range vs Output Voltage* plots, 图 6-5 and 图 6-6.

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA141 is near 0 V even though both inputs are overloaded.

7.1.7 Low-Voltage Operation

The INA141 operates on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly through this supply voltage range—see Typical Performance Curves. Operation at a very low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The *Input Common-Mode Range vs Output Voltage* typical characteristics plots, 图 6-5 and 图 6-6, show the range of linear operation for ±15-V, ±5-V, and ±2.5-V supplies.

7.1.8 Input Protection

The inputs of the INA141 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contributes excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.50 mA to 5 mA. The inputs are protected even if the power supplies are disconnected or turned off.

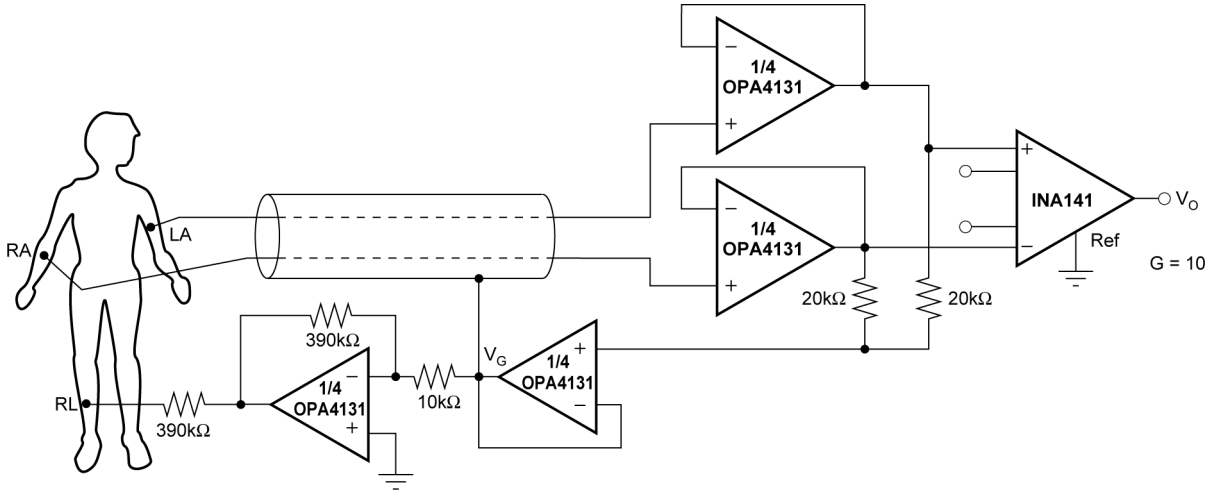


图 7-4. ECG Amplifier With Right-Leg Drive

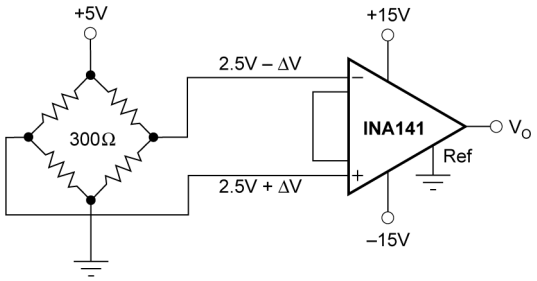


图 7-5. Bridge Amplifier

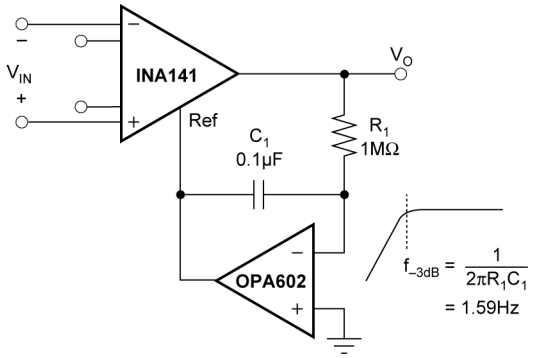
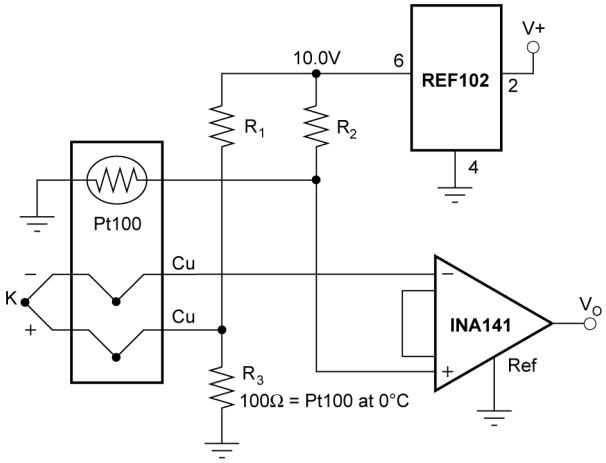
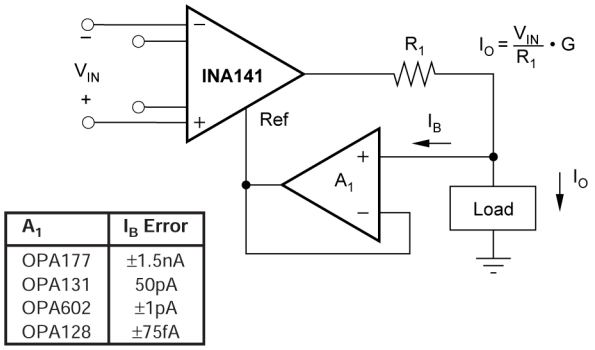


图 7-6. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

图 7-7. Thermocouple Amplifier With RTD Cold-Junction Compensation



A_1	I_B Error
OPA177	±1.5nA
OPA131	50pA
OPA602	±1pA
OPA128	±75fA

图 7-8. Differential Voltage-to-Current Converter

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

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8.4 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA141U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 141U	Samples
INA141U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 141U	Samples
INA141UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 141U A	Samples
INA141UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 141U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

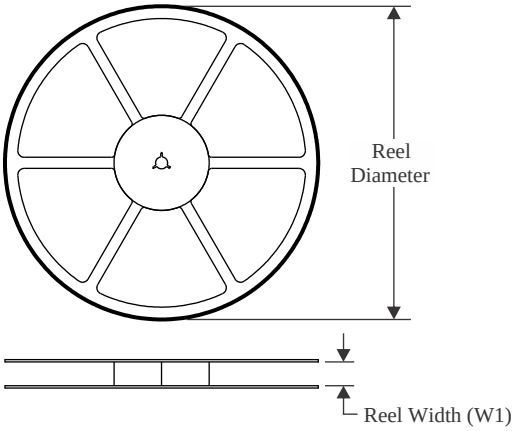
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

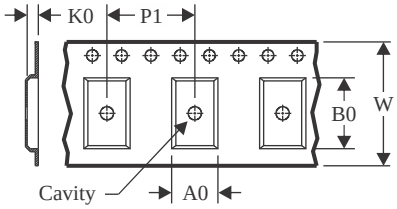
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

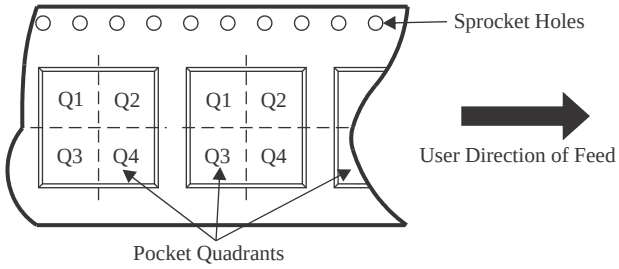


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

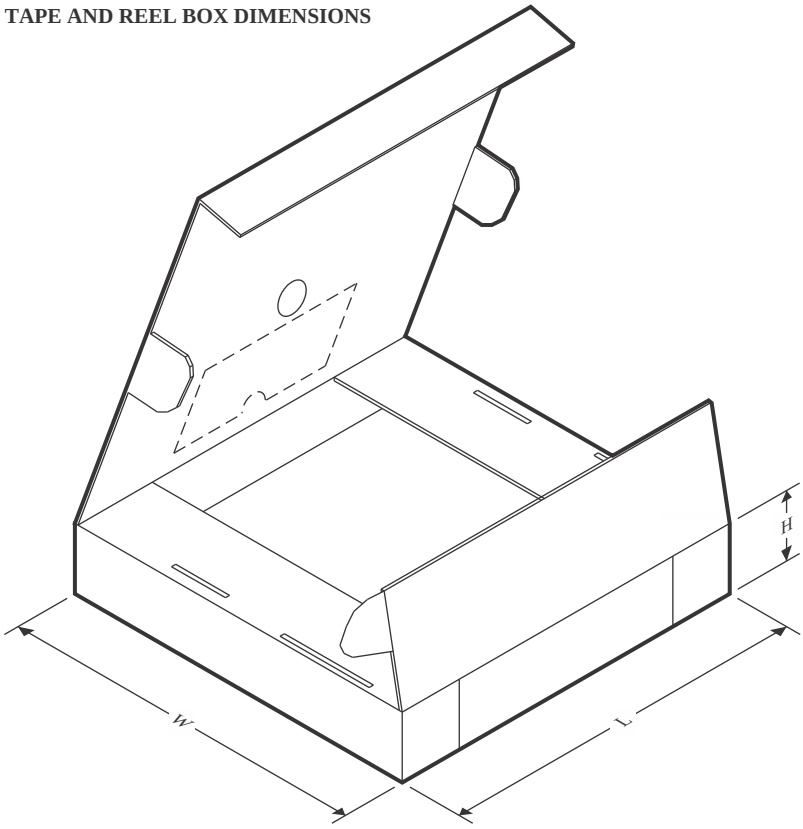
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA141U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA141U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA141UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

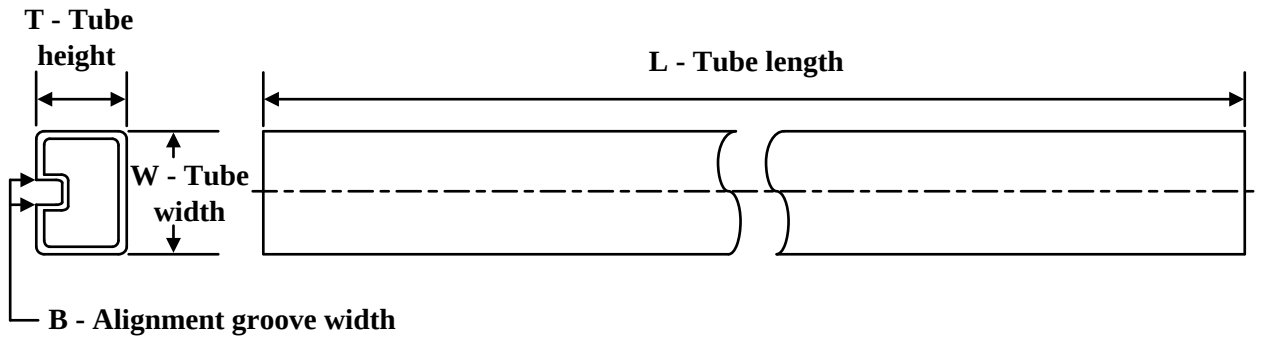
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA141U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA141U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA141UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA141U	D	SOIC	8	75	506.6	8	3940	4.32
INA141UA	D	SOIC	8	75	506.6	8	3940	4.32

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