LMH1981 Multi-Format Video Sync Separator

Check for Samples: LMH1981

FEATURES

- **Standard Analog Video Sync Separation for NTSC, PAL, 480I/P, 576I/P, 720P, and 1080I/P/PsF from Composite Video (CVBS), S-Video (Y/C), and Component Video (YP_BP_R/GBR) Interfaces**
- **Bi-Level & Tri-Level Sync Compatible**
- **Composite, Horizontal, and Vertical Sync Outputs**
- **Burst/Back Porch Timing, Odd/Even Field, and Video Format Outputs**
- **Superior Jitter Performance on Leading Edge of HSync**
- **Automatic Video Format Detection**
- **50% Sync Slicing for Video Inputs from 0.5 V_{PP} to 2 V_{PP}**
- **3.3V to 5V Supply Operation**

APPLICATIONS

- **Broadcast and Professional Video Equipment**
- **HDTV/DTV Systems**
- **Genlock Circuits**
- **Video Capture Devices**
- **Set-Top Boxes (STB) & Digital Video Recorders (DVR)**
- **Video Displays**

DESCRIPTION

The LMH1981 is a high performance multi-format sync separator ideal for use in a wide range of video applications, such as broadcast and professional video equipment and HDTV/DTV systems.

The input accepts standard analog SD/ED/HD video signals with either bi-level or tri-level sync, and the outputs provide all of the critical timing signals in CMOS logic, which swing from rail-to-rail (V_{CC} and GND) including Composite, Horizontal, and Vertical Syncs, Burst/Back Porch Timing, Odd/Even Field, and Video Format Outputs. HSync features very low jitter on its leading (falling) edge, minimizing external circuitry needed to clean and reduce jitter in subsequent clock generation stages.

The LMH1981 automatically detects the input video format, eliminating the need for programming using a microcontroller, and applies precise 50% sync slicing to ensure accurate sync extraction at O_H, even for inputs with irregular amplitude from improper termination or transmission loss. Its unique Video Format Output conveys the total horizontal line count per field as an 11-bit binary serial data stream, which can be decoded by the video system to determine the input video format and enable dynamic adjustment of system parameters, i.e.: color space or scaler conversions. The LMH1981 is available in a 14-pin TSSOP package and operates over a temperature range of −40°C to +85°C.

Connection Diagram

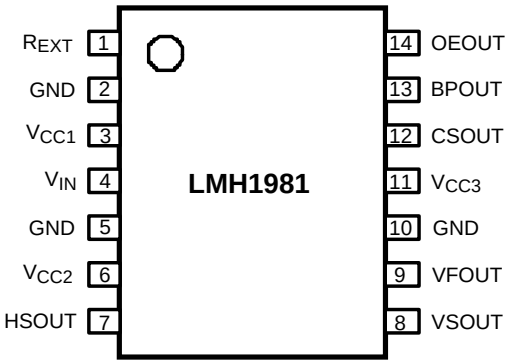


Figure 1. 14-Pin TSSOP - Top View
See PW Package

PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Description
1	R_{EXT}	Bias Current External Resistor
2, 5, 10	GND	Ground
3, 6, 11	V_{CC}	Supply Voltage
4	V_{IN}	Video Input
7	HSOUT	Horizontal Sync Output
8	VSOUT	Vertical Sync Output
9	VFOUT	Video Format Output
12	CSOUT	Composite Sync Output
13	BPOUT	Burst/Back Porch Timing Output
14	OEOUT	Odd/Even Field Output

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

ESD Tolerance (4)	Human Body Model	3.5 kV
	Machine Model	350V
	Charge-Device Model	1.0 kV
Supply Voltage, V_{CC}		0V to 5.5V
Video Input, V_{IN}		−0.3V to V_{CC} + 0.3V
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering 10 sec.)		300°C
Junction Temperature (T_{JMAX}) (5)		+150°C
Thermal Resistance (θ_{JA})		52°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) All voltages are measured with respect to GND, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Temperature Range (2)	−40°C to +85°C
V_{CC}	3.3V −5% to 5V +5%
Input Amplitude, $V_{IN-AMPL}$	140 mV to V_{CC}–$V_{IN-CLAMP}$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 3.3V, R_{EXT} = 10 kΩ 1%, R_L = 10 kΩ, C_L < 10 pF. **Boldface** limits apply at the temperature extremes. See Figure 2.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
I_{CC}	Supply Current	No input signal	V_{CC} = 3.3V		9.5	11.5	mA
			V_{CC} = 5V		11	13.5	
Video Input Specifications							
$V_{IN-SYNC}$	Input Sync Amplitude	Amplitude from negative sync tip to video blanking level for SD/EDTV bi-level sync (4)(5)(6)		0.14	0.30	0.60	V_{PP}
		Amplitude from negative to positive sync tips for HDTV tri-level sync (4)(7)(6)		0.30	0.60	1.20	
$V_{IN-CLAMP}$	Input Sync Tip Clamp Level				0.7		V
$V_{IN-SLICE}$	Input Sync Slice Level	Level between video blanking & sync tip for SD/EDTV and between negative & positive sync tips for HDTV			50		%
Logic Output Specifications (8)							
V_{OL}	Output Logic 0	See output load conditions above	V_{CC} = 3.3V			0.3	V
			V_{CC} = 5V			0.5	
V_{OH}	Output Logic 1	See output load conditions above	V_{CC} = 3.3V	3.0			V
			V_{CC} = 5V	4.5			
$T_{SYNC-LOCK}$	Sync Lock Time	Time for the output signals to be correct after the video signal settles at V_{IN} following a significant input change. See START-UP TIME for more information			2		V periods
T_{VSOUT}	Vertical Sync Output Pulse Width	See Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 for SDTV, EDTV & HDTV Vertical Interval Timing			3		H periods

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) $V_{IN-AMPL}$ plus $V_{IN-CLAMP}$ should not exceed V_{CC}.
(5) Tested with 480I signal.
(6) Maximum voltage offset between 2 consecutive input horizontal sync tips must be less than 25 mV_{PP}.
(7) Tested with 720P signal.
(8) Outputs are negative-polarity logic signal, except for odd/even field and video format outputs.

LMH1981 Test Circuit

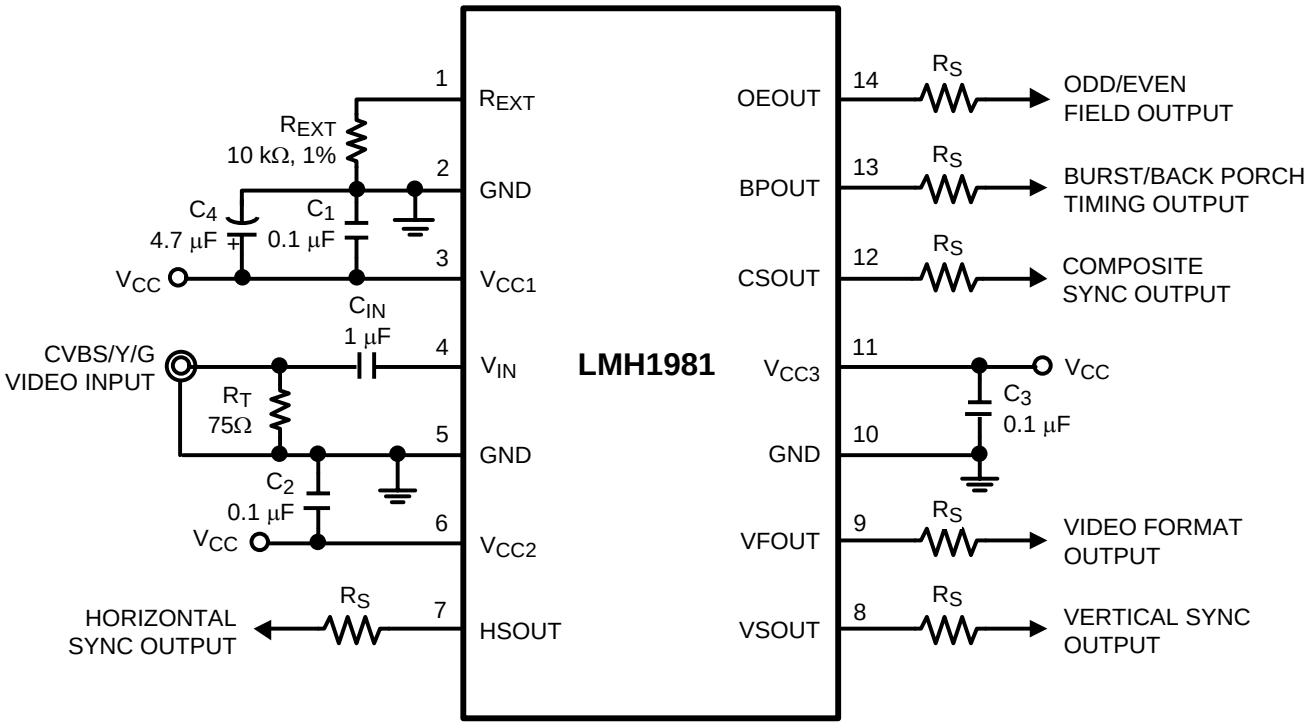


Figure 2. Test Circuit

The LMH1981 test circuit is shown in Figure 2. The video generator should provide a low-noise, broadcast-quality signal over 75Ω coaxial cable which should be impedance-matched with a 75Ω load termination resistor to prevent unwanted signal distortion. The output waveforms should be monitored using a low-capacitance probe on an oscilloscope with at least 500 MHz bandwidth. See PCB LAYOUT CONSIDERATIONS for more information about signal and supply trace routing and component placement.

SDTV Vertical Interval Timing (NTSC, PAL, 480I, 576I)

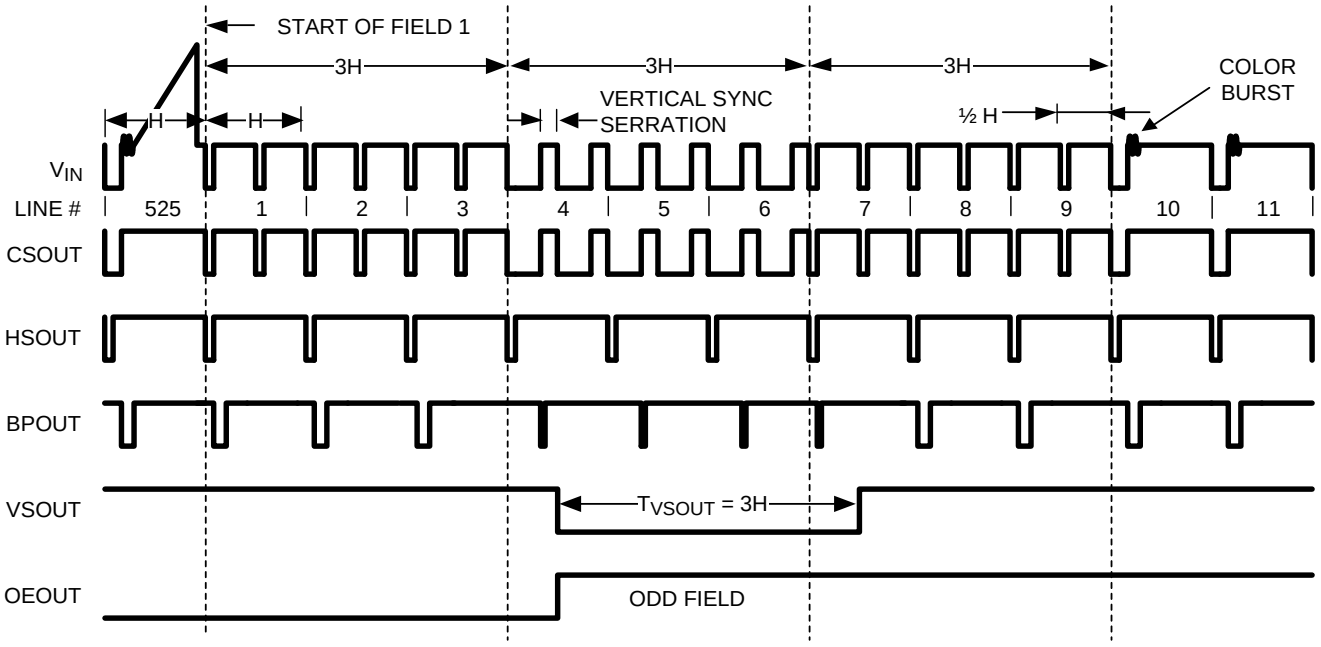


Figure 3. NTSC Odd Field Vertical Interval

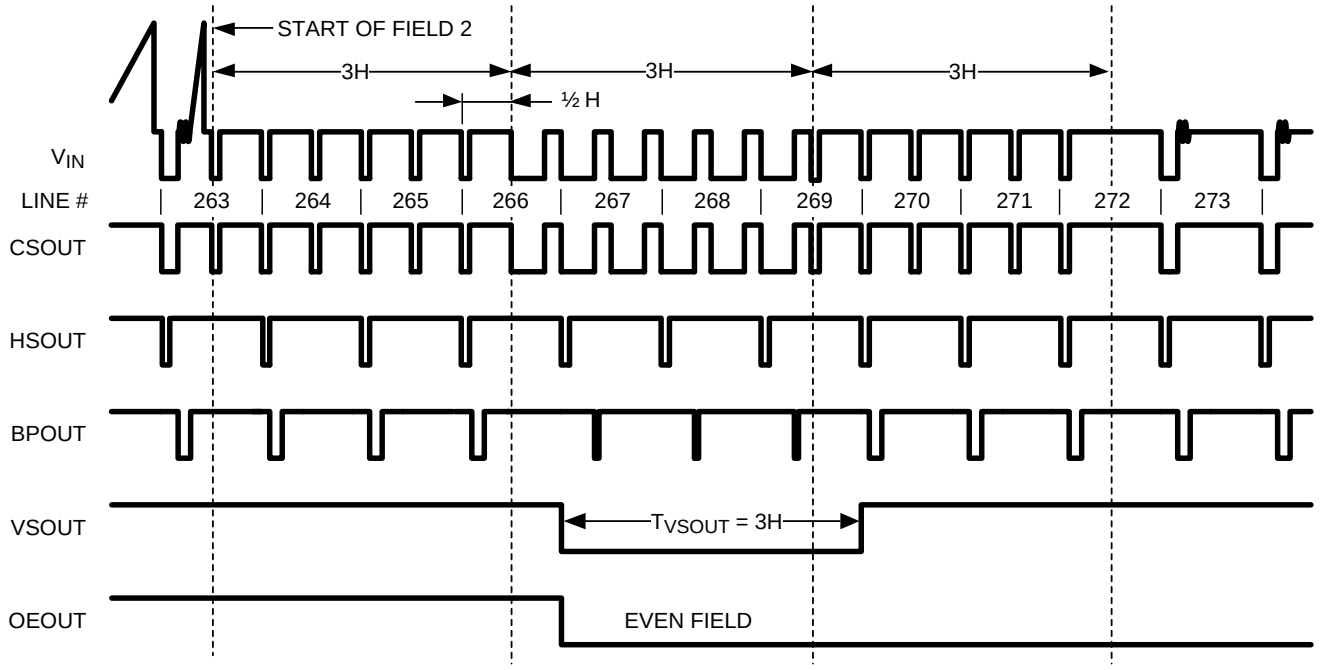


Figure 4. NTSC Even Field Vertical Interval

EDTV Vertical Interval Timing (480P, 576P)

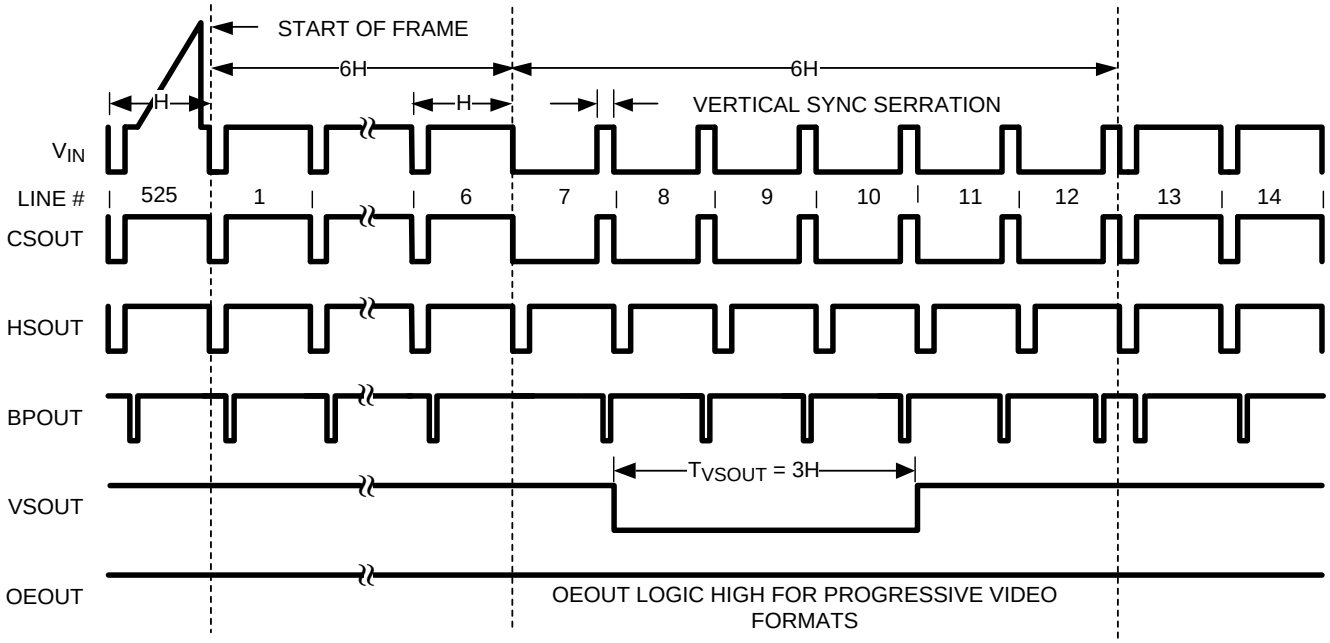


Figure 5. 480P Vertical Interval

HDTV Vertical Interval Timing (720P, 1080P)

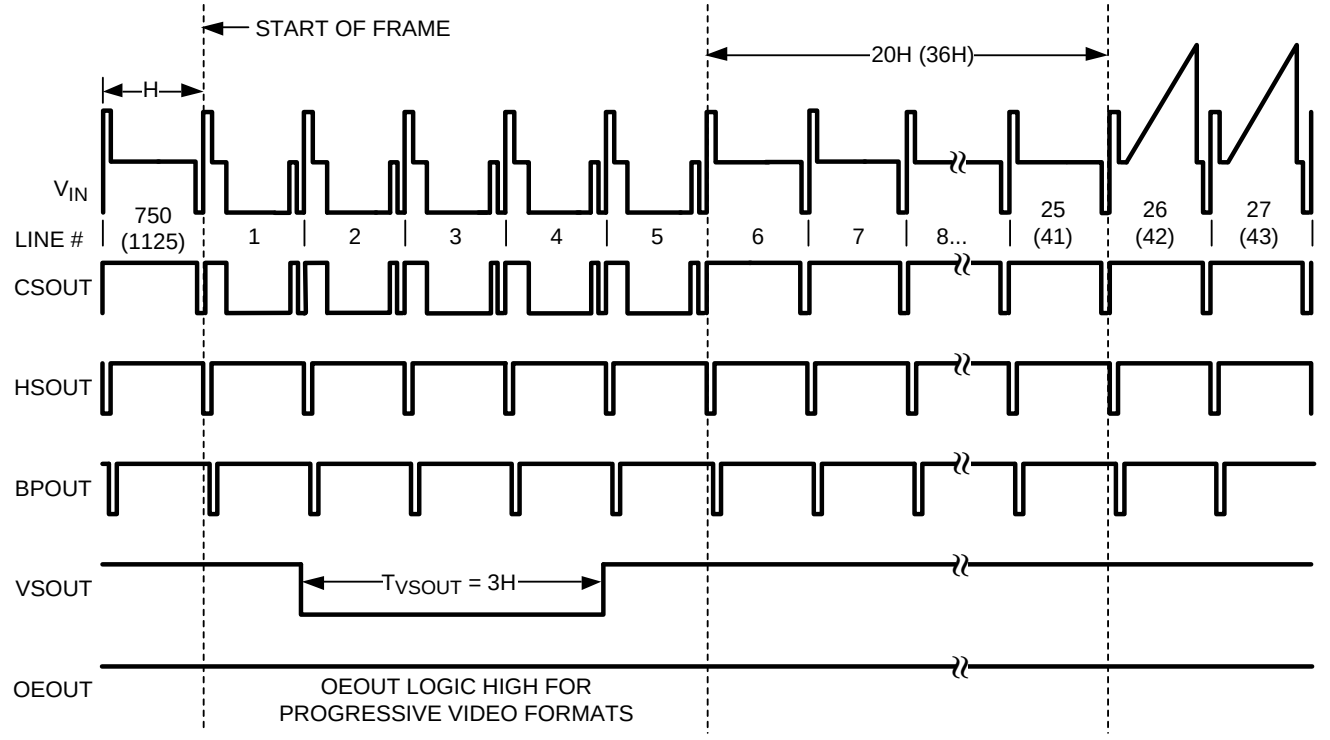


Figure 6. 720P (1080P) Vertical Interval

HDTV Vertical Interval Timing (1080I)

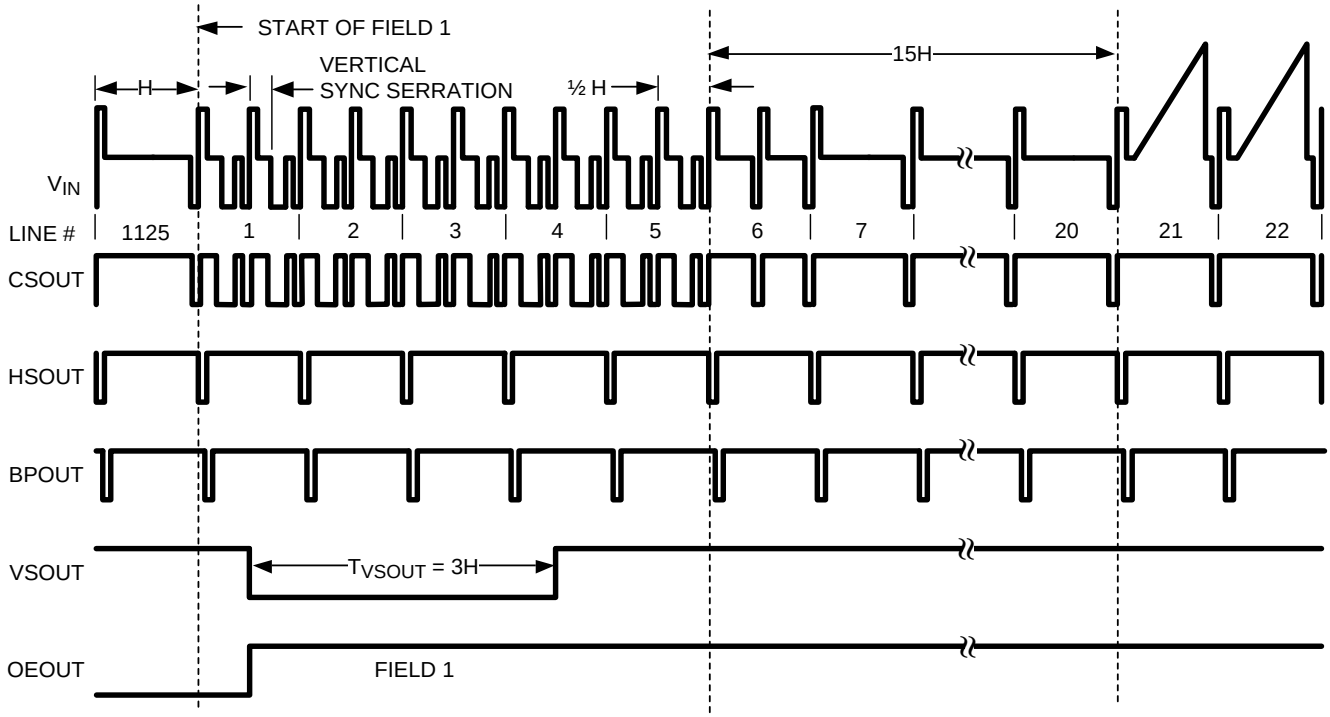


Figure 7. 1080I Field 1 Vertical Interval

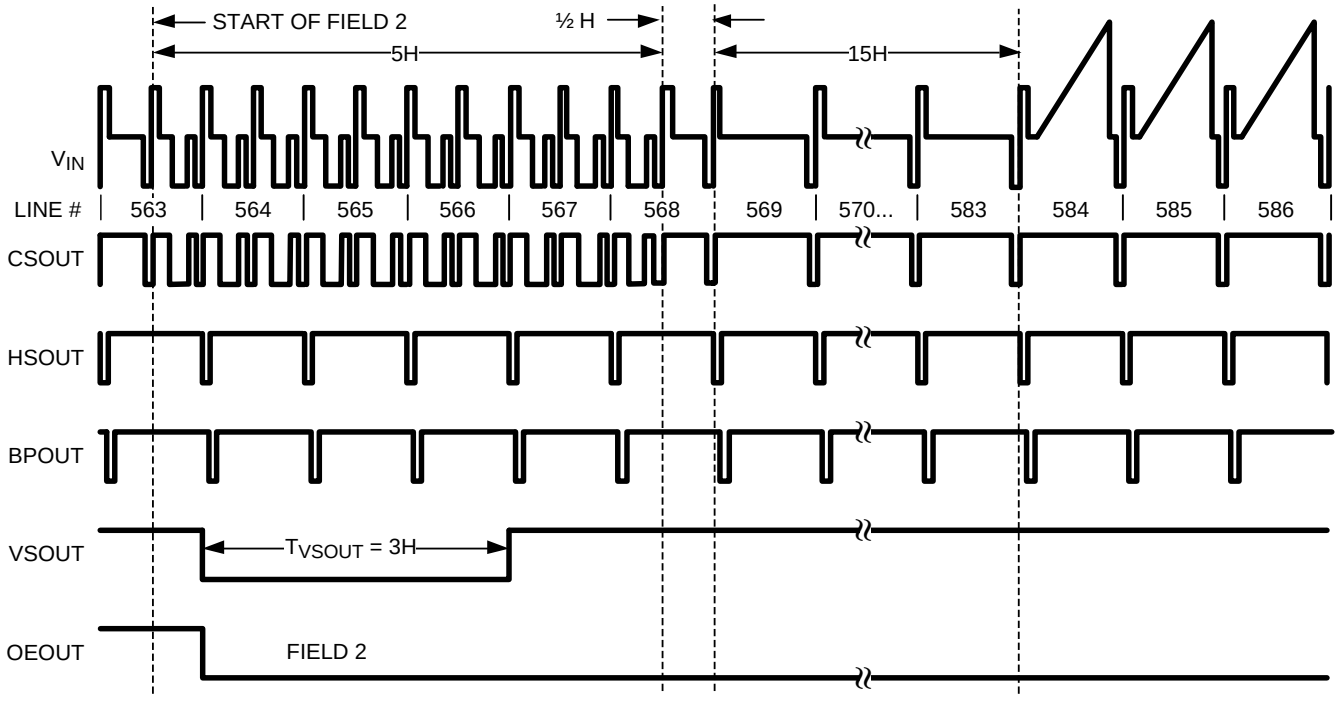


Figure 8. 1080I Field 2 Vertical Interval

SD/EDTV Horizontal Interval Timing

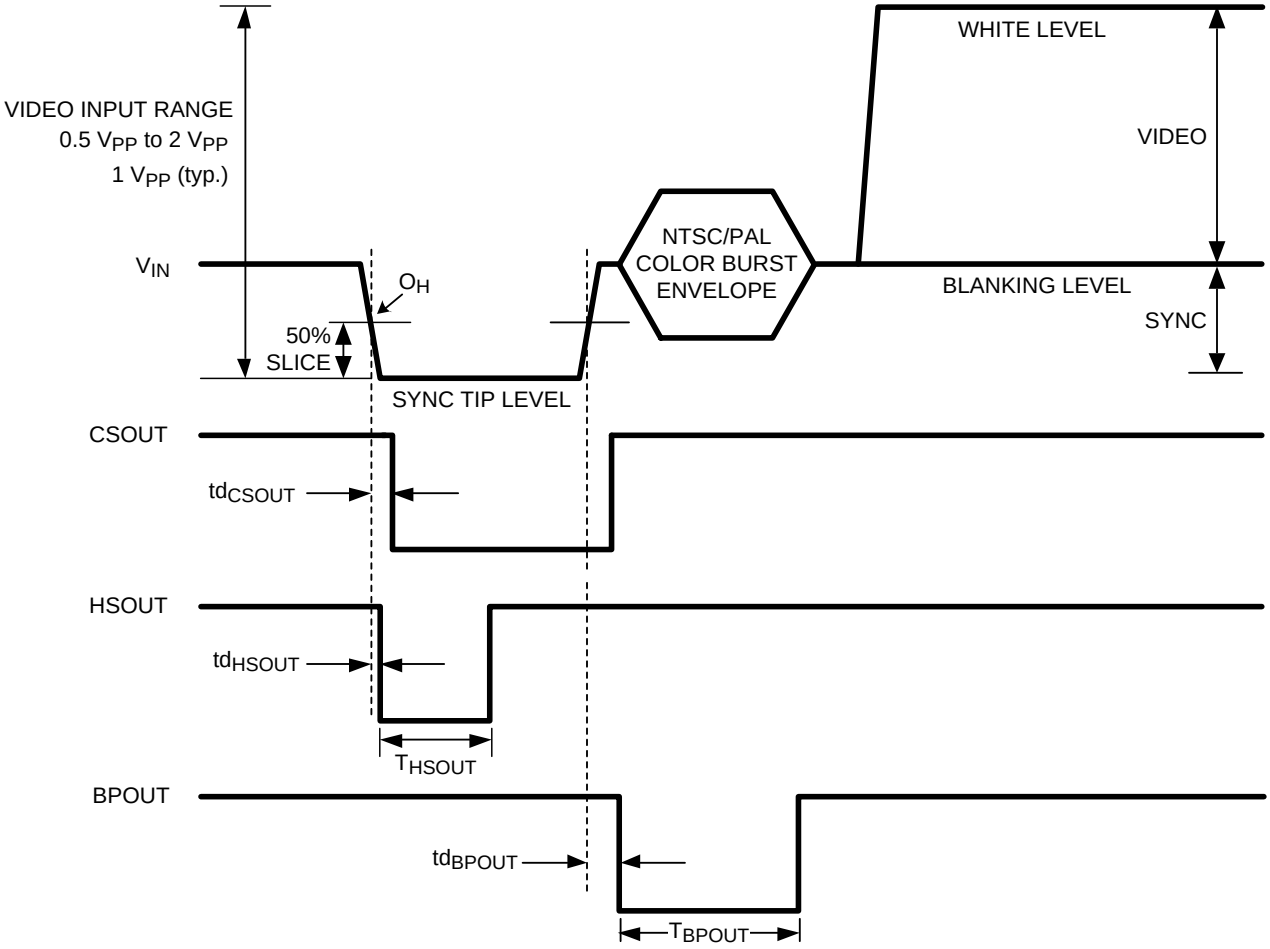


Figure 9. SD/EDTV Horizontal Interval with Bi-level Sync

Table 1. SDTV Horizontal Interval Timing Characteristics (NTSC, PAL, 480I, 576I)(1)(2)

Symbol	Parameter	Conditions		Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 9	NTSC, 480I	475	ns
			PAL, 576I	525	
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 9(1)	NTSC, 480I	40	ns
			PAL, 576I	60	
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 9		300	ns
T_{HSOUT}	Horizontal Sync Output Pulse Width	See Figure 9		2.5	µs
T_{BPOUT}	Burst/Back Porch Timing Output Pulse Width	See Figure 9		3.2	µs

(1) Note: HSync propagation delay variation less than ±3 ns (typ) over 0°C to 70°C temperature range.
(2) V_{CC} = 3.3V , T_A = 25°C

Table 2. EDTV Horizontal Interval Timing Characteristics (480P, 576P)

Symbol	Parameter	Conditions	Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 9	450	ns
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 9	35	ns
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 9	500	ns
T_{HSOUT}	Horizontal Sync Output Pulse Width	See Figure 9	2.3	µs
T_{BPOUT}	Burst/Back Porch Timing Output Pulse Width	See Figure 9	350	ns

HDTV Horizontal Interval Timing

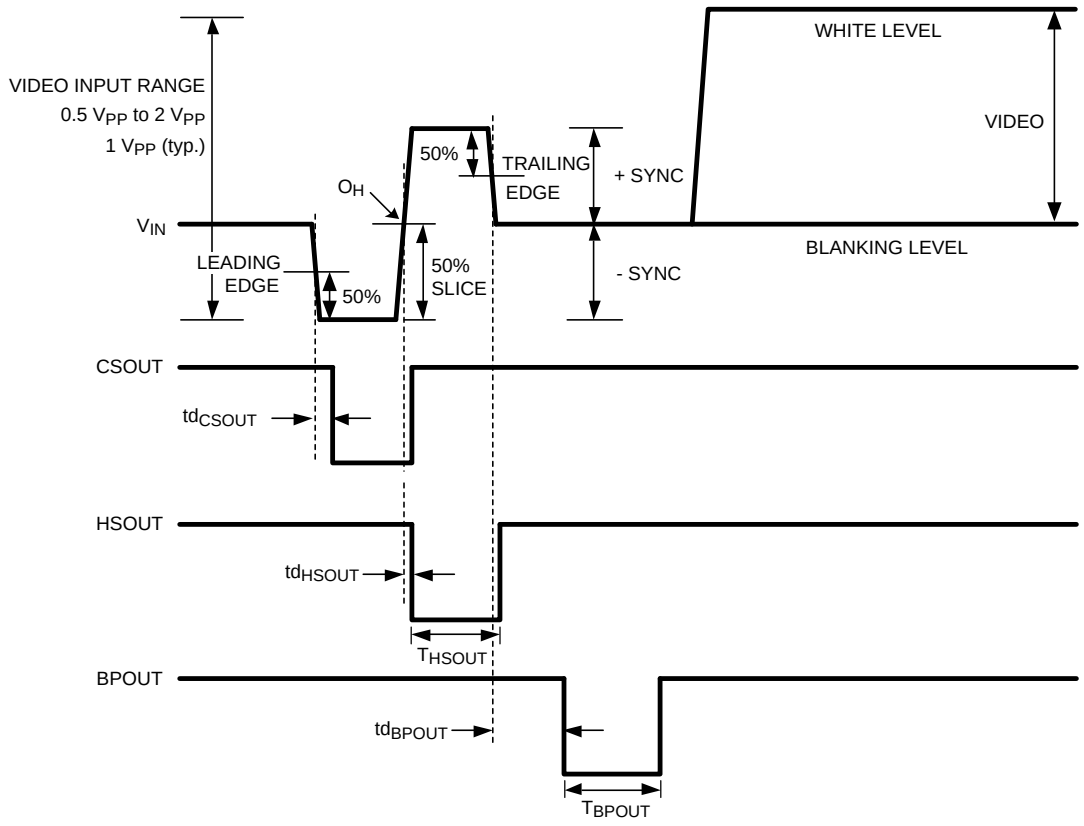


Figure 10. HDTV Horizontal Interval with Tri-level Sync

Table 3. HDTV Horizontal Interval Timing Characteristics (720P, 1080I)(1)

Symbol	Parameter	Conditions		Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Leading Edge	See Figure 10		150	ns
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 10		30	ns
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 10	720P	400	ns
			1080I, 1080P	300	
T_{HSOUT}	Horizontal Sync Output Pulse Width	See Figure 10	720P	525	ns
			1080I, 1080P	475	
T_{BPOUT}	Burst/Back Porch Timing Output Pulse Width	See Figure 10		350	ns

(1) V_{CC} = 3.3V , T_A = 25°C

APPLICATION INFORMATION

GENERAL DESCRIPTION

The LMH1981 is designed to extract the timing information from various video formats with vertical serration and output the syncs and relevant timing signals in CMOS logic. Its high performance, advanced features and easy application make it ideal for broadcast and professional video systems where low jitter is a crucial parameter. The device can operate from a supply voltage between 3.3V and 5V. The only required external components are bypass capacitors at the power supply pins, an input coupling capacitor at pin 4, and a precision R_{EXT} resistor at pin 1. Refer to the test circuit in Figure 2.

R_{EXT} Resistor

The R_{EXT} external resistor establishes the internal bias current and precise reference voltage for the LMH1981. For optimal performance, R_{EXT} should be a 10 kΩ 1% precision resistor with a low temperature coefficient to ensure proper operation over a wide temperature range. Using a R_{EXT} resistor with less precision may result in reduced performance (like worse jitter performance, increased propagation delay variation, or reduced input sync amplitude range) against temperature, supply voltage, input signal, or part-to-part variations.

NOTE

The R_{EXT} resistor serves a different function than the "R_{SET} resistor" used in the LM1881 sync separator. In the older LM1881, the R_{SET} value was adjusted to accommodate different input line rates. For the LMH1981, the R_{EXT} value is fixed, and the device automatically detects the input line rate to support various video formats without electrical or physical intervention.

Automatic Format Detection and Switching

Automatic format detection eliminates the need for external programming via a microcontroller or R_{SET} resistor. The device outputs will respond correctly to video format switching after a sufficient start-up time has been satisfied. Unlike other sync separators, the LMH1981 does not require the power to be cycled in order to ensure correct outputs after a significant change to the input signal. See START-UP TIME for more details.

50% Sync Slicing

The LMH1981 features 50% sync slicing on HSync to provide accurate sync separation for video input amplitudes from 0.5 V_{PP} to 2 V_{PP}, which enables excellent HSync jitter performance even for improperly terminated or attenuated source signals and stability against variations in temperature. The sync separator is compatible with SD/EDTV bi-level and HDTV tri-level sync inputs. Bi-level syncs will be sliced at the 50% point between the video blanking level and negative sync tip, indicated by the input's sync timing reference or "O_H" in Figure 9. Tri-level syncs will be sliced at the 50% point between the negative and positive sync tips (or positive zero-crossing), indicated by O_H in Figure 10.

VIDEO INPUT

The LMH1981 supports sync separation for CVBS, Y (luma) from Y/C and YP_BP_R and G (sync on green) from GBR with either bi-level or tri-level sync, as specified in the following video standards.

- Composite Video (CVBS) and S-Video (Y/C):
  - SDTV: SMPTE 170M (NTSC), ITU-R BT.470 (PAL)
- Component Video (YP_BP_R/GBR):
  - SDTV: SMPTE 125M, SMPTE 267M, ITU-R BT.601 (480I, 576I)
  - EDTV: ITU-R BT.1358 (480P, 576P)
  - HDTV: SMPTE 296M (720P), SMPTE 274M (1080I/P), SMPTE RP 211 (1080PsF)

The LMH1981 does not support RGB formats that conform to VESA standards used for PC graphics.

Input Termination

The video source should be load terminated with a 75Ω resistor to ensure correct video signal amplitude and minimize signal distortion due to reflections. In extreme cases, the LMH1981 can handle unterminated or double-terminated input conditions, assuming 1 V_{PP} signal amplitude for normal terminated video.

Input Coupling Capacitor

The input signal should be AC coupled to the V_{IN} (pin 4) of the LMH1981 with a properly chosen coupling capacitor, C_{IN}.

The primary consideration in choosing C_{IN} is whether the LMH1981 will interface with video sources using an AC-coupled output stage. If AC-coupled video sources are expected in the end-application, then it's recommended to choose a small C_{IN} value such as 0.01 µF as prescribed in the next section. Other considerations such as HSync jitter performance and start-up time are practically fixed by the limited range of small C_{IN} values. It's important to note that video sources with AC-coupled outputs will introduce video-dependent jitter that cannot be remedied by the sync separator; moreover, this type of jitter is not prevalent in sources with DC-coupled input/output stages.

When only DC-coupled video sources are expected, a larger C_{IN} value can be chosen to minimize voltage droop and thus improve HSync jitter at the expense of increased start-up time as explained in START-UP TIME. A typical C_{IN} value such as 1 µF will give excellent jitter performance and reasonable start-up time using a broadcast-quality DC-coupled video generator. For applications where low HSync jitter is not critical, C_{IN} can be a small value to reduce start-up time.

START-UP TIME

When there is a significant change to the video input signal, such as sudden signal switching, signal attenuation (i.e.: additional termination via loop through) or signal gain (i.e.: disconnected end-of-line termination), the quiescent operation of the LMH1981 will be disrupted. During this dynamic input condition, the LMH1981 outputs may not be correct but will recover to valid signals after a predictable start-up time, which consists of an adjustable input settling time and a predetermined "sync lock time".

Input Settling Time and Coupling Capacitor Selection

Following a significant input condition, the negative sync tip of the AC-coupled signal settles to the input clamp voltage as the coupling capacitor, C_{IN}, recovers a quiescent DC voltage via the dynamic clamp current. Because C_{IN} determines the input settling time, its capacitance value is critical when minimizing overall start-up time.

For example, a settling time of 8 ms can be expected for a typical C_{IN} value of 1 µF when switching in a standard NTSC signal with no prior input. A smaller value yields shorter settling time at the expense of increased line droop voltage and consequently higher HSync jitter, whereas a larger one gives lower jitter but longer settling time. Settling time is proportional to the value of C_{IN}, so doubling C_{IN} will also double the settling time.

The value of C_{IN} is a tradeoff between start-up time and jitter performance and therefore should be evaluated based on the application requirements. Figure 11 shows a graph of typical input-referred HSync jitter vs. C_{IN} values to use as a guideline. Refer to Horizontal Sync Output for more about jitter performance.

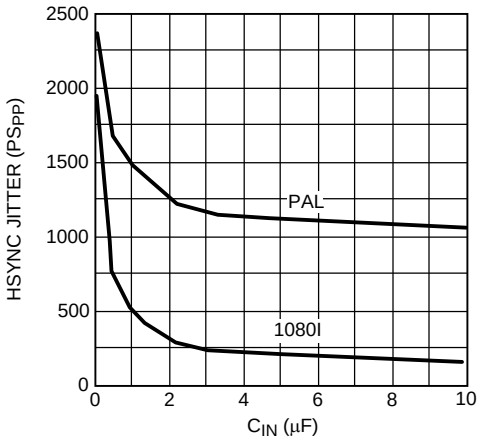


Figure 11. Typical HSync Jitter vs. C_{IN} Values

Sync Lock Time

In addition to settling time, the LMH1981 has a predetermined sync lock time, $T_{SYNC-LOCK}$, before the outputs are correct. Once the AC-coupled input has settled enough, the LMH1981 needs time to detect the valid video signal and resolve the blanking & sync tip levels for 50% sync slicing before the output signals are correct.

For practical values of C_{IN}, $T_{SYNC-LOCK}$ is typically less than 1 or 2 video fields in duration starting from the 1st valid VSync output pulse to the valid HSync pulses beginning thereafter. VSync and HSync pulses are considered valid when they align correctly with the input's vertical and horizontal sync intervals. Note that the start-up time may vary depending on the video duty cycle, average picture level variations, and start point of video relative to the vertical sync interval.

It is recommended for the outputs to be applied to the system after the start-up time is satisfied and outputs are valid. For example, the oscilloscope screenshot in Figure 12 shows a typical start-up time of about 13.5 ms from when an NTSC signal is switched in (no previous input) to when the LMH1981 outputs are valid.

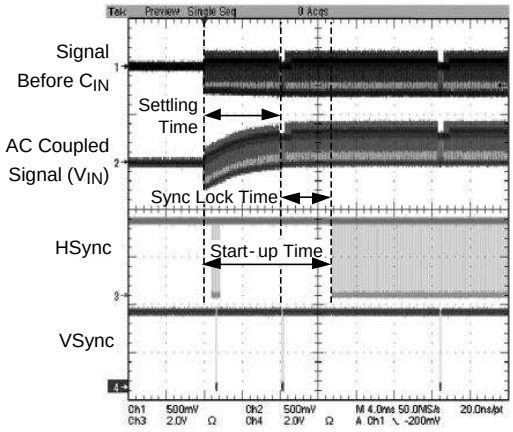


Figure 12. Typical Start-Up Time for NTSC Input to LMH1981 via 1 µF Coupling Capacitor

LOGIC OUTPUTS

In the absence of a video input signal, the LMH1981 outputs are logic high except for the odd/even field and video format outputs, which are both undefined, and the composite sync output.

Composite Sync Output

CSOUT (pin 12) simply reproduces the video input sync pulses below the video blanking level. This is obtained by clamping the video signal sync tip to the internal clamp voltage at V_{IN} and extracting the resultant composite sync signal, or CSync. For both bi-level and tri-level syncs, CSync's negative-going leading edge is derived from the input's negative-going leading edge with a propagation delay.

Horizontal Sync Output

HSOUT (pin 7) produces a negative-polarity horizontal sync signal, or HSync, with very low jitter on its negative-going leading edge (reference edge) using precise 50% sync slicing. For bi-level and tri-level sync signals, the horizontal sync leading edge is triggered from the input's sync reference, O_H, with a propagation delay.

HSync was optimized for excellent jitter performance on its leading edge because most video systems are negative-edge triggered. When HSync is used in a positive-edge triggered system, like an FPGA PLL input, it must be inverted beforehand to produce positive-going leading edges. The trailing edge of HSync should **never** be used as the reference or triggered edge. This is because the trailing edges of HSync are reconstructed for the broad serration pulses during the vertical interval.

HSync's typical peak-to-peak jitter can be measured using the input-referred jitter test methodology on a real-time digital oscilloscope by triggering at or near the input's O_H reference and monitoring HSync's leading edge with 4-sec. variable persistence. This is one way to measure HSync's typical peak-to-peak jitter in the time domain. Figure 13 and Figure 14 show oscilloscope screenshots demonstrating very low jitter on HSync's leading edge for 1080I tri-level sync and PAL Black Burst inputs, respectively, from a Tek TG700-AWVG7/AVG7 video generator with DC-coupled outputs and with LMH1981 V_{CC} = 3.3V.

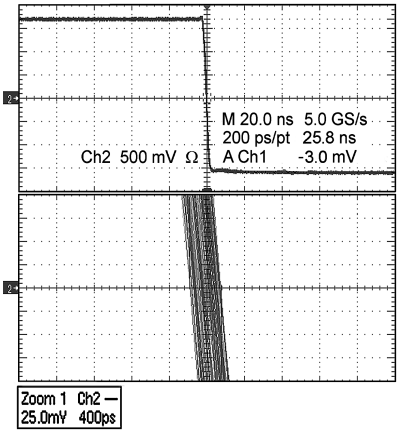


Figure 13. Typical HSync Jitter for 1080I Input
Upper: Horizontal Sync Leading Edge (Reference)
Lower: Zoomed In — 400 ps/DIV, 25 mV/DIV

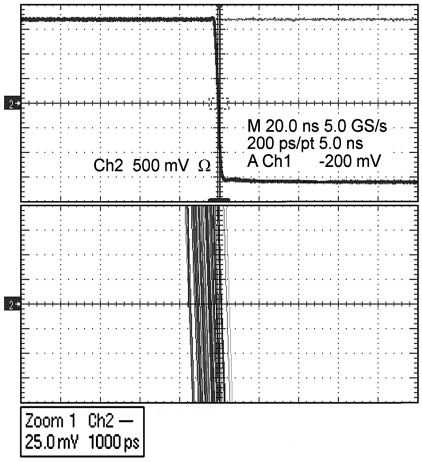


Figure 14. Typical HSync Jitter for PAL Input
Upper: Horizontal Sync Leading Edge (Reference)
Lower: Zoomed In — 1000 ps/DIV, 25 mV/DIV

Vertical Sync Output

VSOUT (pin 8) produces a negative-polarity vertical sync signal, or VSync. VSync's negative-going leading edge is derived from the 50% point of the first vertical serration pulse with a propagation delay, and its output pulse width, T_{VSOUT}, spans approximately three horizontal periods (3H).

Burst/Back Porch Timing Output

BPOUT (pin 13) provides a negative-polarity burst/back porch signal, which is pulsed low for a fixed width during the back porch interval following the input's sync pulse. The burst/back porch timing pulse is useful as a burst gate signal for NTSC/PAL color burst synchronization and as a clamp signal for black level clamping (DC restoration) and sync stripping applications.

For SDTV formats, the back porch pulse's negative-going leading edge is derived from the input's positive-going sync edge with a propagation delay, and the pulse width spans an appropriate duration of the color burst envelope for NTSC/PAL. During the vertical interval, its pulse width is shorter to correspond with the narrow serration pulses. For EDTV formats, the back porch pulse behaves similar to the SDTV case except that the shorter pulse width is always maintained. For HDTV formats, the pulse's leading edge is derived from the input's negative-going trailing sync edge with a propagation delay, and the pulse width is even narrower to correspond with the shortest back porch duration of HDTV formats.

Odd/Even Field Output

OEOUT (pin 14) provides an odd/even field output signal, which facilitates identification of odd and even fields for interlaced or segmented frame (sF) formats. For interlaced or segmented frame formats, the odd/even output is logic high during an odd field (field 1) and logic low during an even field (field 2). The odd/even output edge transitions align with VSync's leading edge to designate the start of odd and even fields. For progressive (non-interlaced) video formats, the output is held constantly at logic high.

Video Format Output (Lines-per-Field Data)

The LMH1981 counts the number of HSync pulses per field to approximate the total horizontal line count per field (vertical resolution). This can be used to identify the video format and enable dynamic adjustment of video system parameters, such as color space or scaler conversions. The line count per field is output to VFOUT (pin 9) as an 11-bit binary data stream. The video format data stream is clocked out on the 11 consecutive leading edges of HSync, starting at the 3rd HSync **after** each VSync leading edge. Outside of these active 11-bits of data, the video format output can be either 0 or 1 and should be treated as undefined. Refer to Figure 15 to see the VFOUT data timing for the 480P progressive format and Figure 16 and Figure 17 for the 1080I interlaced format. See Table 4 for a summary of VFOUT data for all supported formats.

A FPGA/MCU can be used to decode the 11-bit VFOUT data stream by using HSync as the clock source signal and VSync as the enable signal. Using the FPGA's clock delay capability, a delayed clock derived from HSync can be used as the sampling clock to latch the VFOUT data in the middle of the horizontal line period rather than near the VFOUT data-bit transitions in order to avoid setup time requirements.

Table 4. VFOUT Data Summary(1)

TV Format (Total Lines per Field)	**VFOUT Data Field 1**	**VFOUT Data Field 2**
NTSC/480I (262.5)	00100000100**b** 260**d**	00100000011**b** 259**d**
PAL/576I (312.5)	00100110110**b** 310**d**	00100110101**b** 309**d**
480P (525)	01000001010**b** 522**d**	N/A
576P (625)	01001101110**b** 622**d**	N/A
720P (750)	01011101011**b** 747**d**	N/A
1080I (562.5)	01000110000**b** 560**d**	01000101111**b** 559**d**
1080P (1125)	10001100010**b** 1122**d**	N/A

(1) Note: VFOUT Data has an average offset of −3 lines due to the HSync pulses uncounted during the VSync pulse interval.

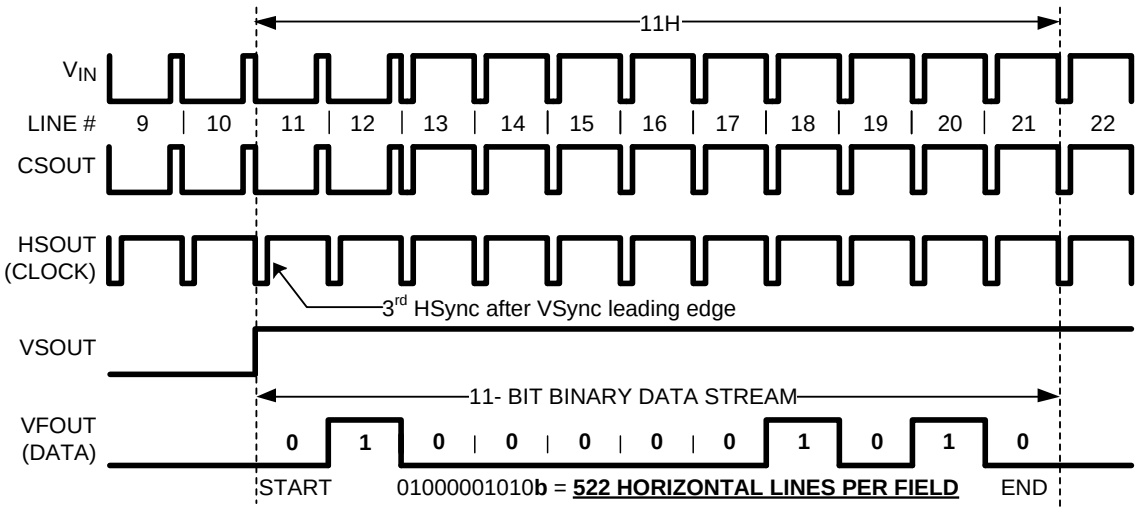


Figure 15. Video Format Output for Progressive Format, 480P

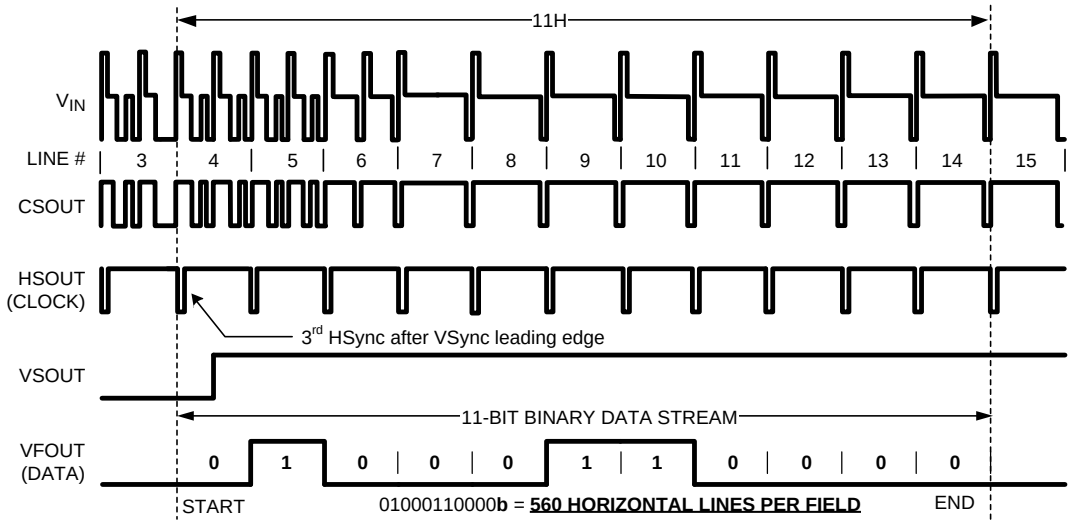


Figure 16. Video Format Output for Interlaced Format, 1080I Field 1

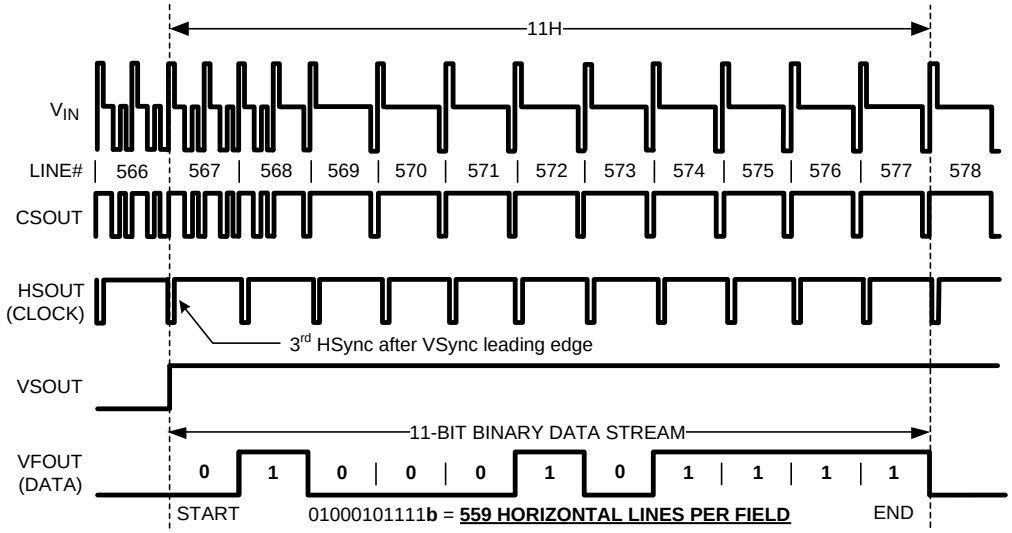


Figure 17. Video Format Output for Interlaced Format, 1080I Field 2

OPTIONAL CONSIDERATIONS

Optional Input Filtering

An external filter may be necessary if the video signal has considerable high-frequency noise or has large chroma amplitude that extends near the sync tip. A simple RC low-pass filter with a series resistor (R_S) and a capacitor (C_F) to ground can be used to improve the overall signal-to-noise ratio and sufficiently attenuate chroma such that minimum peak of its amplitude is above the 50% sync slice level. To achieve the desired filter cutoff frequency, it's advised to vary C_F and keep R_S small (ie. 100Ω) to minimize sync tip clipping due to the voltage drop across R_S. Note that using an external filter will increase the propagation delay from the input to the outputs.

In applications where the chroma filter needs to be disabled when non-composite video (ie: ED/HD video) is input, it is possible to use a transistor to switch open C_F's connection to ground as shown in Figure 18. This transistor can be switched off/on by logic circuitry to decode the lines-per-field data output (VFOUT). As shown in Table 4, NTSC and PAL both have 1 (logic high) for the 3rd bit of VFOUT. If the logic circuitry detects 0 (logic low) for this bit, indicating non-composite video, the transistor can be turned off to disable the chroma filter.

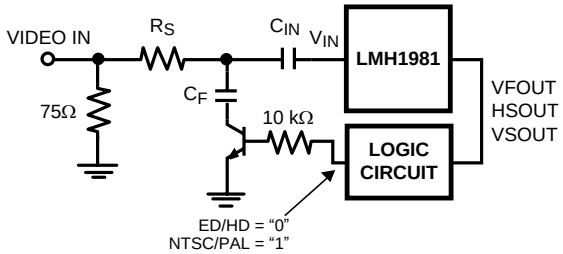


Figure 18. External Chroma Filter with Control Circuit

AC-Coupled Video Sources

An AC coupled video source typically has a 100 µF or larger output coupling capacitor (C_{OUT}) for protection and to remove the DC bias of the amplifier output from the video signal. When the video source is load terminated, the average value of the video signal will shift dynamically as the video duty cycle varies due to the averaging effect of the C_{OUT} and termination resistors. The average picture level or APL of the video content is closely related to the duty cycle.

For example, a significant decrease in APL such as a white-to-black field transition will cause a positive-going shift in the sync tips characterized by the source's RC time constant, $t_{RC\text{-}OUT}$ (150Ω*C_{OUT}). The LMH1981's input clamp circuitry may have difficulty stabilizing the input signal under this type of shifting; consequently, the unstable signal at V_{IN} may cause missing sync output pulses to result, **unless** a proper value for C_{IN} is chosen.

To avoid this potential problem when interfacing AC-coupled sources to the LMH1981, it's necessary to introduce a voltage droop component via C_{IN} to compensate for video signal shifting related to changes in the APL. This can be accomplished by selecting C_{IN} such that the effective time constant of the LMH1981's input circuit, $t_{RC\text{-}IN}$, is less than $t_{RC\text{-}OUT}$.

The effective time constant of the input circuit can be approximated as: $t_{RC\text{-}IN} = (R_S+R_I)*C_{IN}*T_{LINE}/T_{CLAMP}$, where R_S = 150Ω, R_I = 4000Ω (input resistance), T_{LINE} ~ 64 µs for NTSC, and T_{CLAMP} = 250 ns (internal clamp duration). A white-to-black field transition in NTSC video through C_{OUT} will exhibit the maximum sync tip shifting due to its long line period (T_{LINE}). By setting $t_{RC\text{-}IN} < t_{RC\text{-}OUT}$, the maximum value of C_{IN} can be calculated to ensure proper operation under this worst-case condition.

For instance, $t_{RC\text{-}OUT}$ is about 33 ms for C_{OUT} = 220 µF. To ensure $t_{RC\text{-}IN}$ < 33 ms, C_{IN} must be less than 31 nF. By choosing C_{IN} = 0.01 µF, the LMH1981 will function properly with AC-coupled video sources using C_{OUT} ≥ 220 µF.

PCB LAYOUT CONSIDERATIONS

LMH1981 IC Placement

The LMH1981 should be placed such that critical signal paths are short and direct to minimize PCB parasitics from degrading the high-speed video input and logic output signals.

Ground Plane

A two-layer, FR-4 PCB is sufficient for this device. One of the PCB layers should be dedicated to a single, solid ground plane that runs underneath the device and connects the device GND pins together. The ground plane should be used to connect other components and serve as the common ground reference. It also helps to reduce trace inductances and minimize ground loops. Try to route supply and signal traces on another layer to maintain as much ground plane continuity as possible.

Power Supply Pins

The power supply pins should be connected together using short traces with minimal inductance. When routing the supply traces, be careful not to disrupt the solid ground plane.

For high frequency bypassing, place 0.1 µF SMD ceramic bypass capacitors with very short connections to power supply and GND pins. Two or three ceramic bypass capacitors can be used depending on how the supply pins are connected together. Place a 4.7 µF SMD tantalum bypass capacitor nearby all three power supply pins for low frequency supply bypassing.

R_{EXT} Resistor

The R_{EXT} resistor should be a 10 kΩ 1% SMD precision resistor. Place R_{EXT} as close as possible to the device and connect to pin 1 and the ground plane using the shortest possible connections. All input and output signals must be kept away from this pin to prevent unwanted signals from coupling into this pin.

Video Input

The input signal path should be routed using short, direct traces between video source and input pin. Use a 75Ω input termination and a SMD capacitor for AC coupling the video input to pin 4.

Output Routing

The output signal paths should be routed using short, direct traces to minimize parasitic effects that may degrade these high-speed logic signals. All output signals should have a resistive load of about 10 kΩ and capacitive load of less than 10 pF, including parasitic capacitances for optimal signal quality. This is especially important for the horizontal sync output, in which it is critical to minimize timing jitter. Each output can be protected by current limiting with a small series resistor, like 100Ω.

REVISION HISTORY

Changes from Revision G (March 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH1981MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH19 81MT	Samples
LMH1981MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH19 81MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

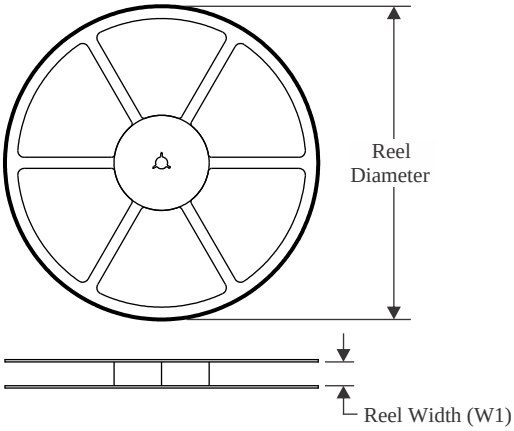
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

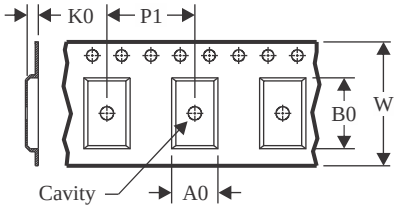
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

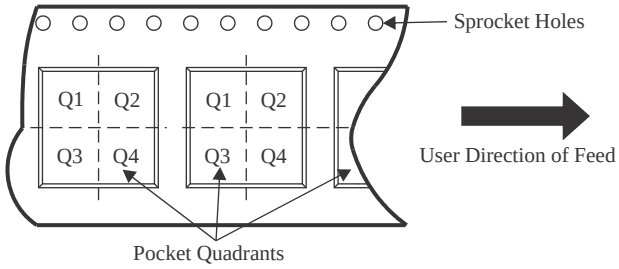


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

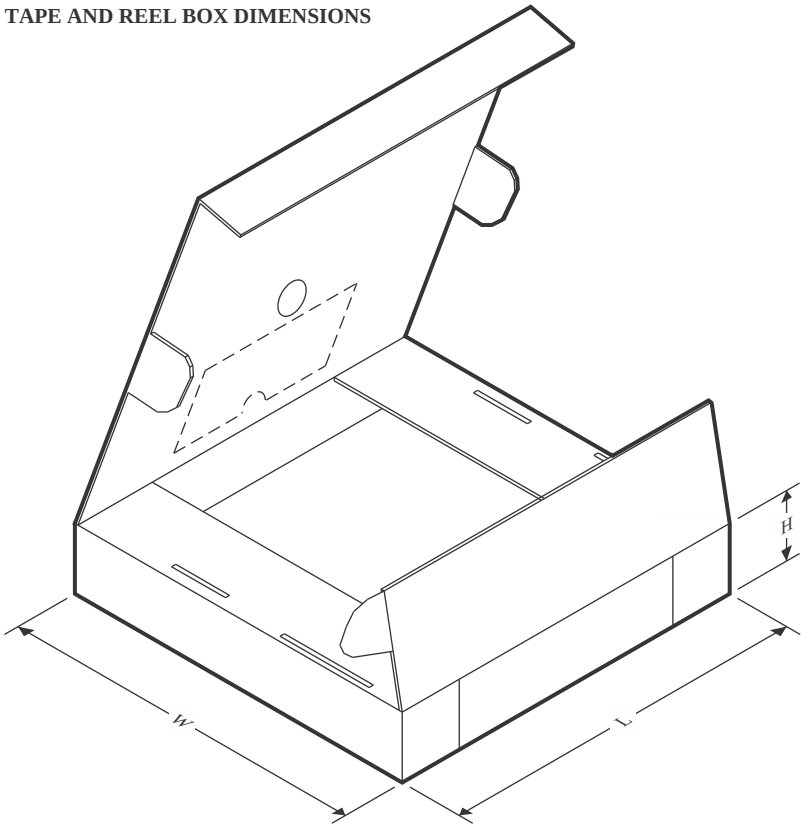
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1981MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

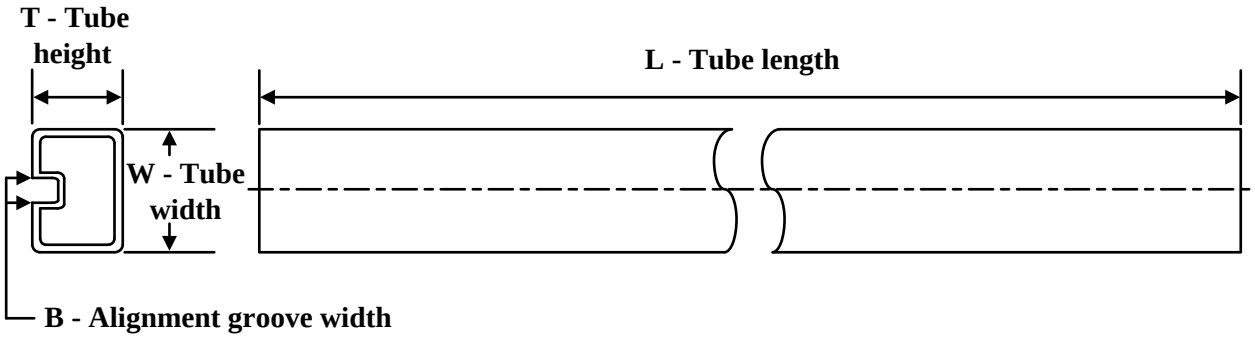
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1981MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

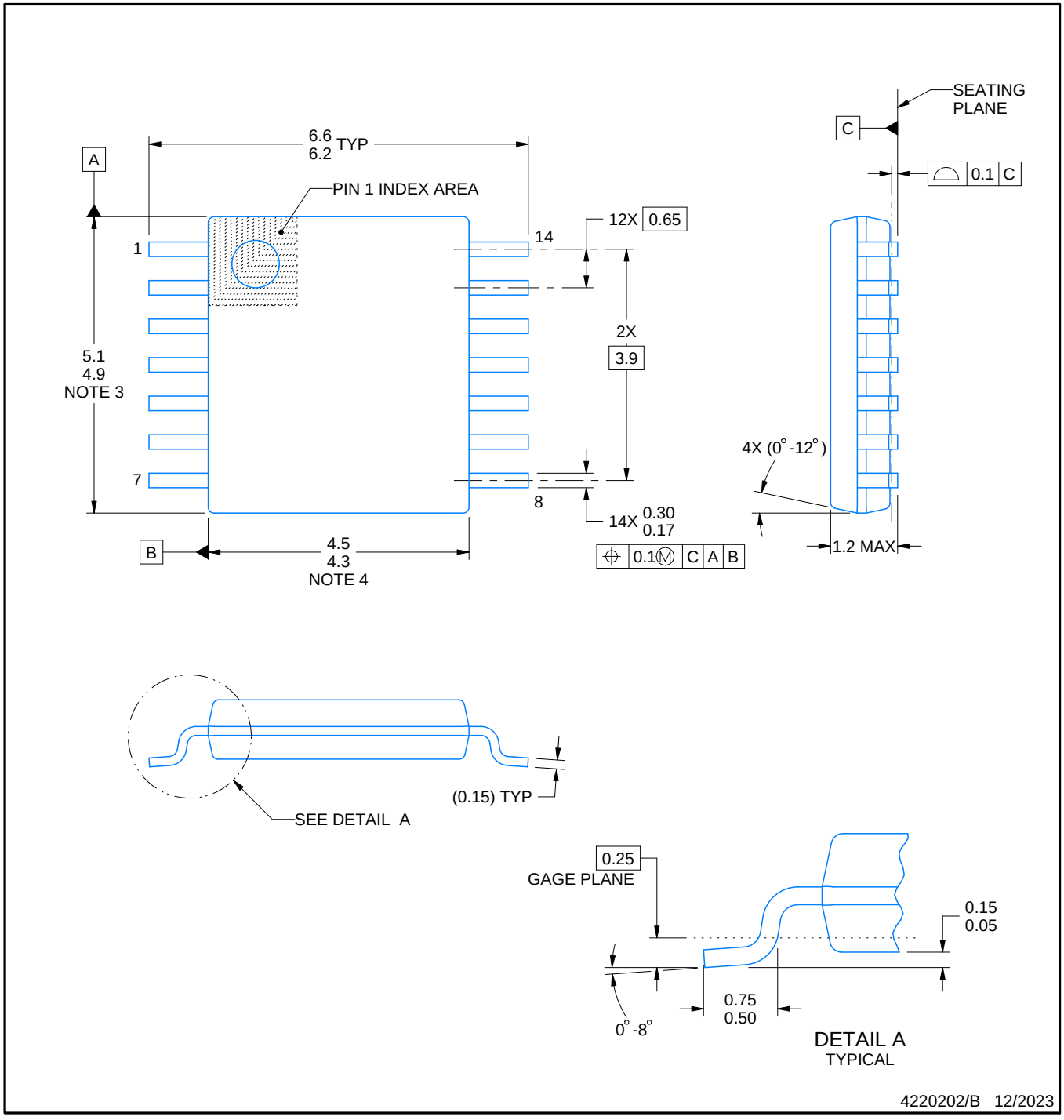
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH1981MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0014A

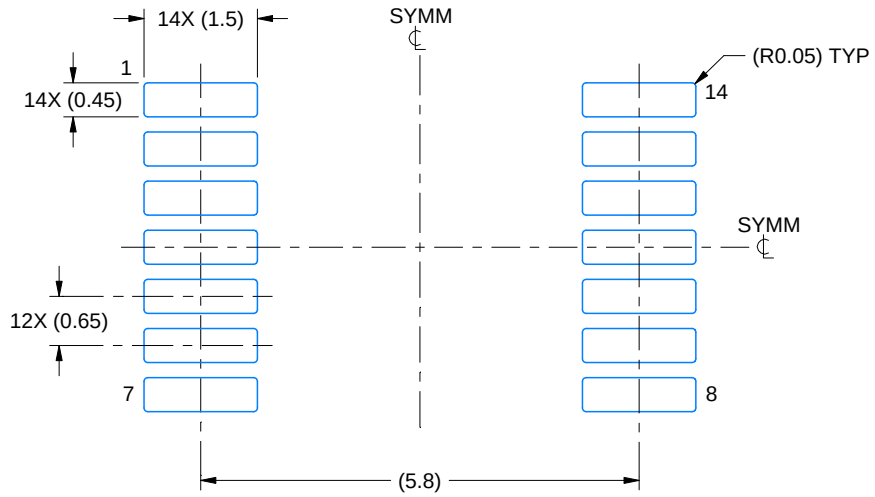
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

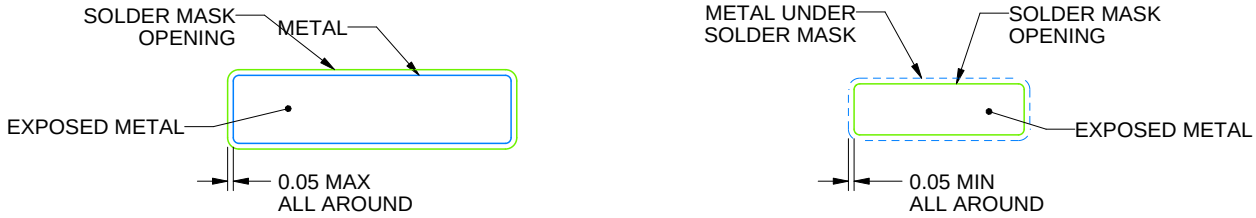


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

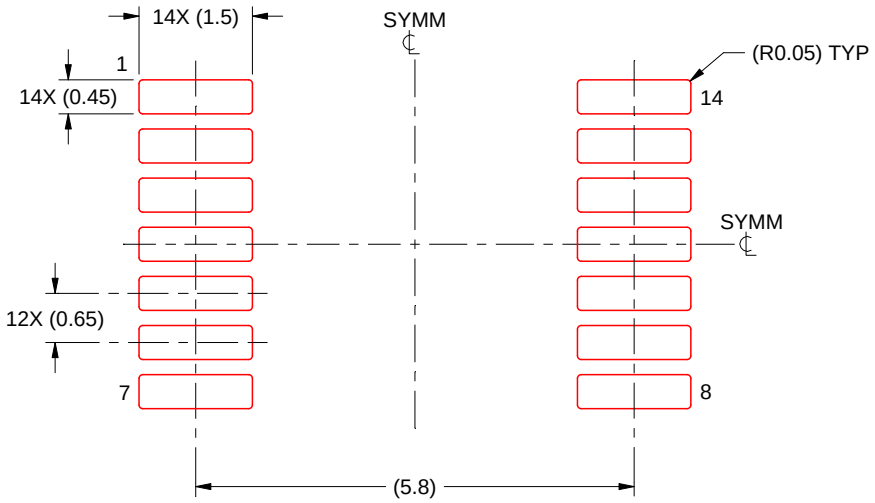


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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