LMH6503 Wideband, Low Power, Linear Variable Gain Amplifier

Check for Samples: LMH6503

FEATURES

- **V_S = ±5V, T_A = 25°C, R_F = 1kΩ, R_G = 174Ω, R_L = 100Ω, A_V = $A_{V(MAX)}$ = 10, Typical Values Unless Specified.**
- **-3dB BW 135MHz**
- **Gain Control BW 100MHz**
- **Adjustment Range (Typical Over Temp) 70dB**
- **Gain Matching (Limit) ±0.7dB**
- **Slew Rate 1800V/µs**
- **Supply Current (No Load) 37mA**
- **Linear Output Current ±75mA**
- **Output Voltage (R_L = 100Ω) ±3.2V**
- **Input Voltage Noise 6.6nV/$\sqrt{Hz}$**
- **Input Current Noise 2.4pA/$\sqrt{Hz}$**
- **THD (20MHz, R_L = 100Ω, V_O = $2V_{PP}$) −57dBc**
- **Replacement for CLC522**

APPLICATIONS

- **Variable Attenuator**
- **AGC**
- **Voltage Controller Filter**
- **Multiplier**

DESCRIPTION

The LMH™6503 is a wideband, DC coupled, differential input, voltage controlled gain stage followed by a high-speed current feedback Op Amp which can directly drive a low impedance load. Gain adjustment range is more than 70dB for up to 10MHz.

Maximum gain is set by external components and the gain can be reduced all the way to cut-off. Power consumption is 370mW with a speed of 135MHz . Output referred DC offset voltage is less than 350mV over the entire gain control voltage range. Device-to-device Gain matching is within 0.7dB at maximum gain. Furthermore, gain at any V_G is tested and the tolerance is ensured. The output current feedback Op Amp allows high frequency large signals (Slew Rate = 1800V/µs) and can also drive heavy load current (75mA). Differential inputs allow common mode rejection in low level amplification or in applications where signals are carried over relatively long wires. For single ended operation, the unused input can easily be tied to ground (or to a virtual half-supply in single supply application). Inverting or non-inverting gains could be obtained by choosing one input polarity or the other.

To further increase versatility when used in a single supply application, gain control range is set to be from −1V to +1V relative to pin 11 potential (ground pin). In single supply operation, this ground pin is tied to a "virtual" half supply. Gain control pin has high input impedance to simplify its drive requirement. Gain control is linear in V/V throughout the gain adjustment range. Maximum gain can be set to be anywhere between 1V/V to 100V/V or higher. For linear in dB gain control applications, see LMH6502 datasheet.

The LMH6503 is available in the SOIC-14 and TSSOP-14 package.

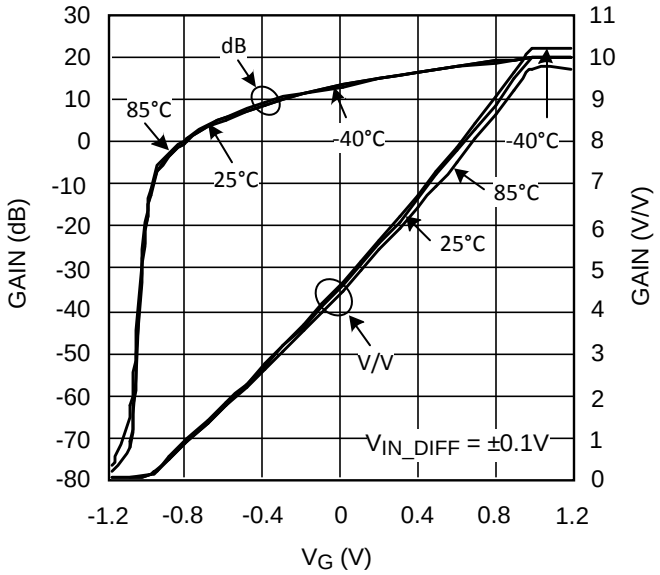


Figure 1. Gain vs. V_G for Various Temperature

Typical Application

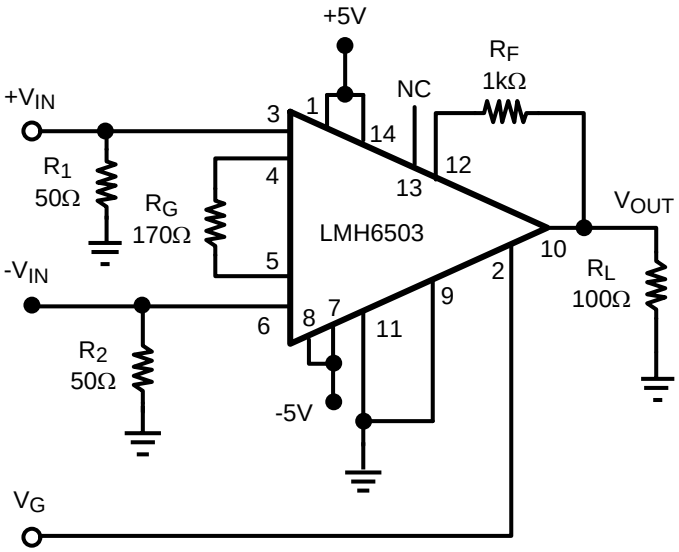


Figure 2. A_{VMAX} = 10V/V

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance:(3)	Human Body	2KV
	Machine Model	200V
Input Current		±10mA
V_{IN} Differential		±(V^+ −V^-)
Output Current		120mA(4)
Supply Voltages (V^+ - V^-)		12.6V
Voltage at Input/ Output pins		V^+ +0.8V,V^- - 0.8V
Soldering Information:	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C
Storage Temperature Range		−65°C to +150°C
Junction Temperature		+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations or value specified, whichever is lower.

Operating Ratings(1)

Supply Voltages (V^+ - V^-)		5V to 12V
Temperature Range		−40°C to +85°C
Thermal Resistance:	θ_{JA}	θ_{JC}
14-Pin SOIC	138°C/W	45°C/W
14-Pin TSSOP	160°C/W	51°C/W

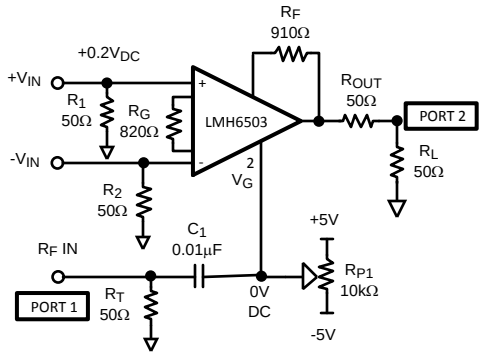
(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

Electrical Characteristics(1)

Unless otherwise specified, all limits ensured for T_J = 25°C, V_S = ±5V, $A_{V(MAX)}$ = 10, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, V_{IN_DIFF} = ±0.1V, R_L = 100Ω, V_G = +1V. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min(2)	Typ(2)	Max(2)	Units
Frequency Domain Response						
BW	-3dB Bandwidth	V_{OUT} < 0.5_{PP}		135		MHz
		V_{OUT} < 0.5_{PP}, $A_{V(MAX)}$ = 100		50		
GF	Gain Flatness	V_{OUT} < $0.5V_{PP}$, −1V < V_G < 1V, ±0.2dB		40		MHz
Att Range	Flat Band (Relative to Max Gain) Attenuation Range(3)	±0.2dB Flatness, f < 30MHZ		20		MHz
		±0.1dB, f < 30MHZ		6.6		
BW Control	Gain Control Bandwidth	V_G = 0V(4)		100		MHz
PL	Linear Phase Deviation	DC to 60MHz		1.6		deg
G Delay	Group Delay	DC to 130MHz		2.6		ns
CT (dB)	Feed-through	V_G = −1.2V, 30MHz (Output Referred)		−48		dB
GR	Gain Adjustment Range	f < 10MHz		79		dB
		f < 30MHz		68		
Time Domain Response						
t_r , t_f	Rise and Fall Time	0.5V Step		2.2		ns
OS%	Overshoot	0.5V Step		10		%
SR	Slew Rate	4V Step(5)		1800		V/µs
ΔG Rate	Gain Change Rate	V_{IN} = 0.3V, 10%−90% of final output		4.6		dB/ns
Distortion & Noise performance						
HD2	2nd Harmonic Distortion	$2V_{PP}$, 20MHz		−60		dBc
HD3	3rdHarmonic Distortion	$2V_{PP}$, 20MHz		−61		dBc
THD	Total Harmonic Distortion	$2V_{PP}$, 20MHz		−57		dBc
En tot	Total Equivalent Input Noise	1MHz to 150MHz		6.6		nV/√Hz
I_n	Input Noise Current	1MHz to 150MHz		2.4		pA/√Hz
DG	Differential Gain	f = 4.43MHz, R_L = 150Ω, Neg. Sync		0.15		%
DP	Differential Phase	f = 4.43MHz, R_L = 150Ω, Neg. Sync		0.22		deg

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm. Bold numbers refer to over temperature limits.
(3) Flat Band Attenuation (Relative To Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either ±0.2dB or ±0.1dB), relative to A_{VMAX} gain. For example, for f<30MHz, here are the Flat Band Attenuation ranges:±0.2dB: 10V/V down to 1V/V=20dB range±0.1dB: 10V/V down to 4.7V/V=6.5dB range
(4) Gain Control Frequency Response Schematic:



(5) Slew Rate is the average of the rising and falling rates.

Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V_S = ±5V, $A_{V(MAX)}$ = 10, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, V_{IN_DIFF} = ±0.1V, R_L = 100Ω, V_G = +1V. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[2]	Max[2]	Units
DC & Miscellaneous Performance						
GACCU	Gain Accuracy (see Application Information)	V_G =1.0V		+0.25	+0.9/−0.4	dB
		0V < V_G < 1V		±0.3	+1.3/−1.5	
		−0.7V < V_G < 1V		±0.4	+4.4/−4.3	
G Match	Gain Matching (see Application Information)	V_G = 1.0		–	±0.7	dB
		0 < V_G < 1V		–	+1.7/−1.1	
		−0.7V < V_G < 1V		–	+4.0/−4.7	
K	Gain Multiplier (see Application Information)		1.58 **1.58**	1.72	1.87 **1.91**	V/V
V_{CM}	Input Voltage Range	Pin 3 & 6 Common Mode, |CMRR| > 50dB[6]	±2.0 **±1.80**	±2.2		V
V_{IN_DIFF}	Differential Input Voltage	Across pins 3 & 6	±0.34 **±0.28**	±0.37		V
$I_{RG\ MAX}$	R_G Current	Pins 4 & 5	±1.70 **±1.60**	±2.30		mA
I_{BIAS}	Bias Current	Pins 3 & 6[7]		11	18 **20**	µA
		Pins 3 & 6[7], V_S= ±2.5V		3	10 **13**	
TC_{BIAS}	Bias Current Drift	Pin 3 & 6[8]		100		nA/°C
I_{OFF}	Offset Current	Pin 3 & 6		0.01	2.0 **2.5**	µA
TC I_{OFF}	Offset Current Drift	See[8]		5		nA/°C
R_{IN}	Input Resistance	Pin 3 & 6		750		kΩ
C_{IN}	Input Capacitance	Pin 3 & 6		5		pF
IV_G	V_G Bias Current	Pin 2, V_G = 1.4V[7]		45		µA
TC IV_G	V_G Bias Drift	Pin 2[8]		20		nA/°C
R V_G	V_G Input Resistance	Pin 2		70		KΩ
C V_G	V_G Input Capacitance	Pin 2		1.3		pF
V_{OUT}	Output Voltage Range	R_L = 100Ω	±3.00 **±2.97**	±3.20		V
		R_L Open	±3.95 **±3.90**	±4.05		
R_{OUT}	Output Impedance	DC		0.1		Ω
I_{OUT}	Output Current	V_{OUT} ±4V from Rails	±75 **±70**	±90		mA
$V_{O\ OFFSET}$	Output Offset Voltage	−1V < V_G < 1V		±80	±350 **±380**	mV
+PSRR	+Power Supply Rejection Ratio (See[9])	Input Referred, 1V change, V_G = 1.4V		−80	−58 **−56**	dB
−PSRR	−Power Supply Rejection Ratio (See[9])	Input Referred, 1V change, V_G = 1.4V		−67	−57 **−51**	dB
CMRR	Common Mode Rejection Ratio (See[10])	Input Referred, V_G = 1V −1.8V < V_{CM} < 1.8V		−67		dB

(6) CMRR definition: $[|\Delta V_{OUT}/\Delta V_{CM}|/A_V]$ with 0.1V differential input voltage. ΔV_{OUT} is the change in output voltage with offset shift subtracted out.
(7) Positive current correspondes to current flowing in the device.
(8) Drift determined by dividing the change in parameter distribution at temperature extremes by the total temperature change.
(9) +PSRR definition: $[|\Delta V_{OUT}/\Delta V^+|\ /A_V]$, -PSRR definition: $[|\Delta V_{OUT}/\Delta V^-|\ /A_V]$ with 0.1V differential input voltage. ΔV_{OUT} is the change in output voltage with offset shift subtracted out.
(10) CMRR definition: $[|\Delta V_{OUT}/\Delta V_{CM}|/A_V]$ with 0.1V differential input voltage. ΔV_{OUT} is the change in output voltage with offset shift subtracted out.

Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V_S = ±5V, $A_{V(MAX)}$ = 10, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, V_{IN_DIFF} = ±0.1V, R_L = 100Ω, V_G = +1V. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[2]	Max[2]	Units
I_S	Supply Current	R_L = Open		37	50 **53**	mA
		R_L = Open, V_S = ±2.5V		12	20 **23**	

Connection Diagram

Top View

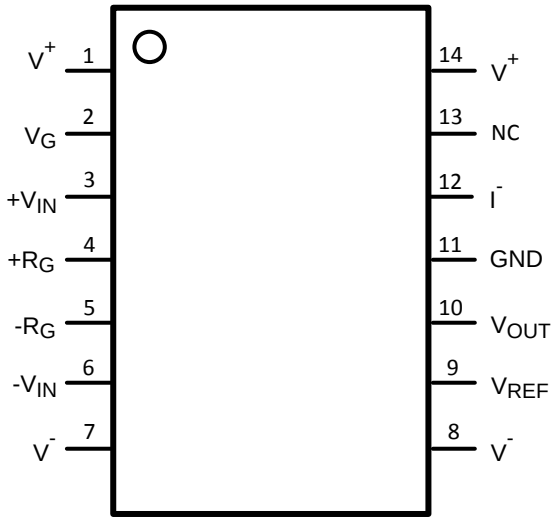


Figure 3. 14-Pin SOIC AND TSSOP Packages
See Package Numbers D0014A and PW0014A

Typical Performance Charateristics

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{G\_MAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

Small Signal Frequency Response (A_V = 2)

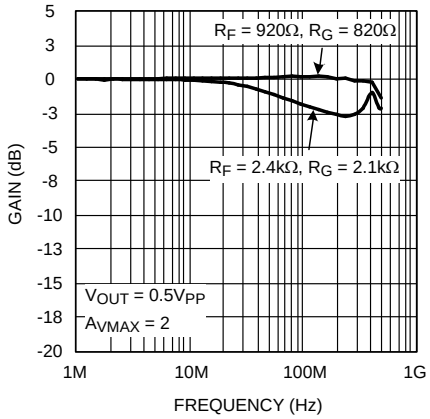


Figure 4.

Large Signal Frequency Response (A_V = 2)

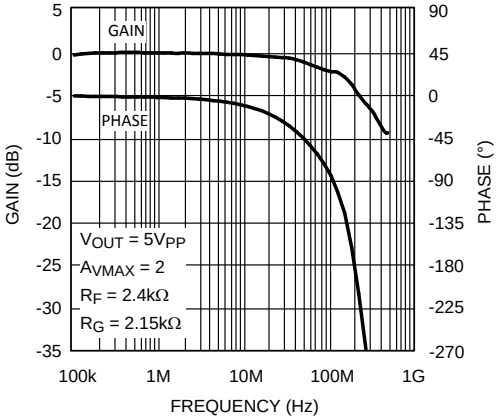


Figure 5.

Frequency Response over Temperature (A_V = 10)

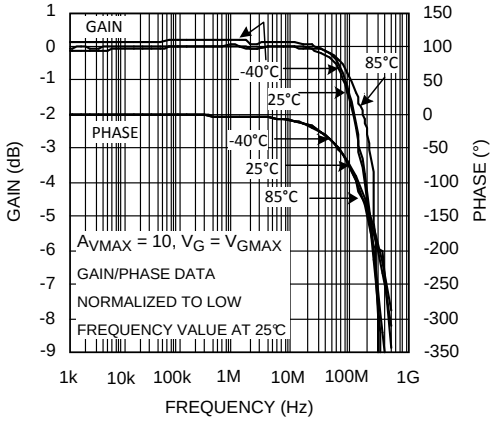


Figure 6.

Frequency Response for Various V_G (A_{VMAX} = 10)

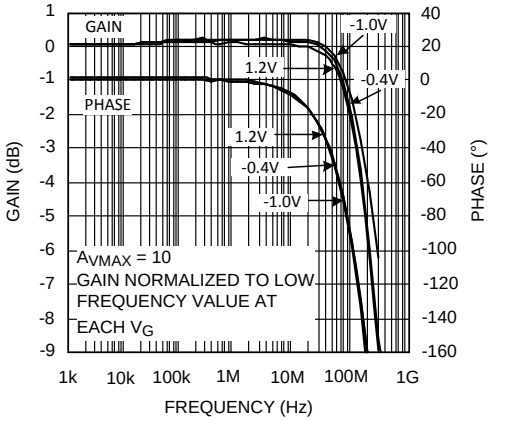


Figure 7.

Frequency Response for Various V_G (A_{VMAX} = 10) (±2.5V)

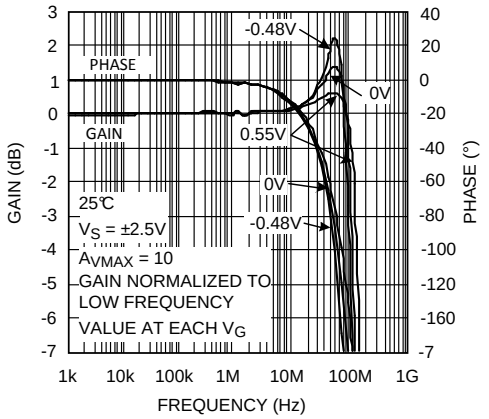


Figure 8.

Small Signal Frequency Response

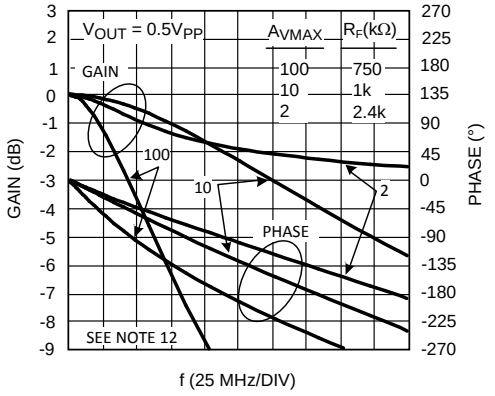


Figure 9.

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{G\_MAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

Large Signal Frequency Response

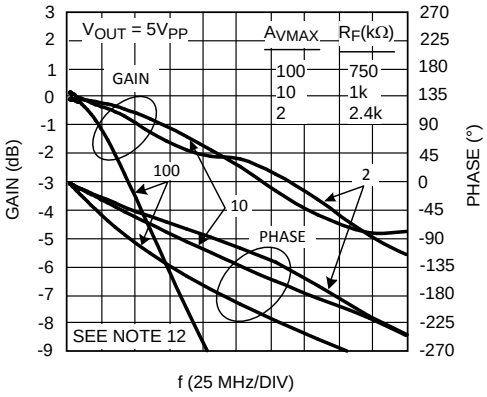


Figure 10.

Frequency Response for Various V_G (A_{VMAX} = 100) (Small Signal)

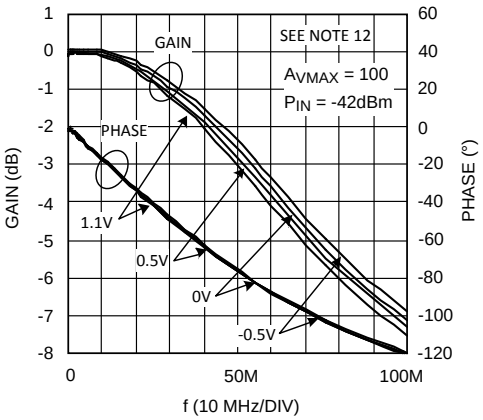


Figure 11.

Frequency Response for Various V_G (A_{VMAX} = 100) (Large Signal)

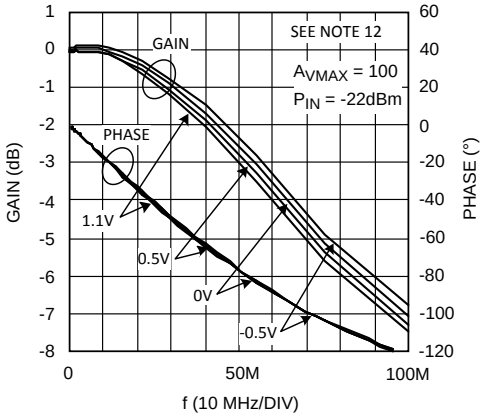


Figure 12.

Gain Control Frequency Response

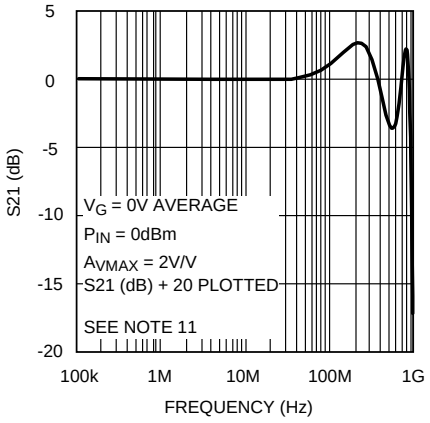


Figure 13.

I_S vs. V_S

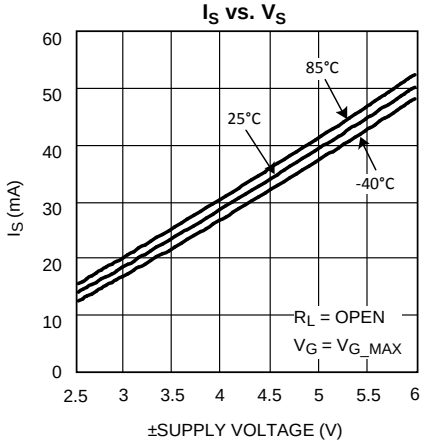


Figure 14.

I_S vs. V_S

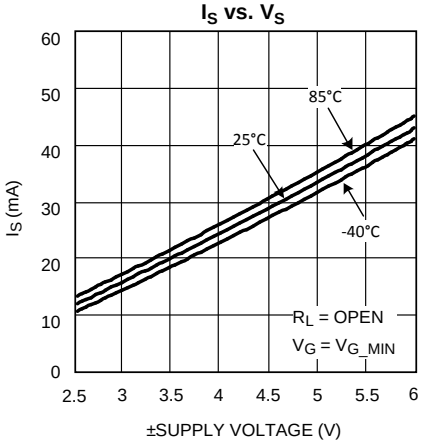


Figure 15.

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{G\_MAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

Input Bias Current vs. V_S

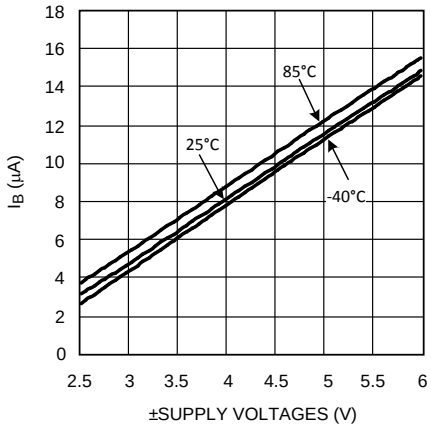


Figure 16.

A_{VMAX} vs. V_S

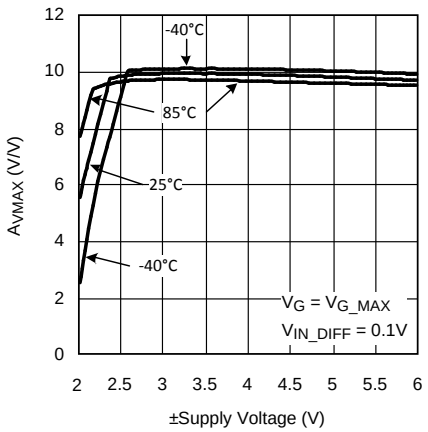


Figure 17.

PSRR ±5V

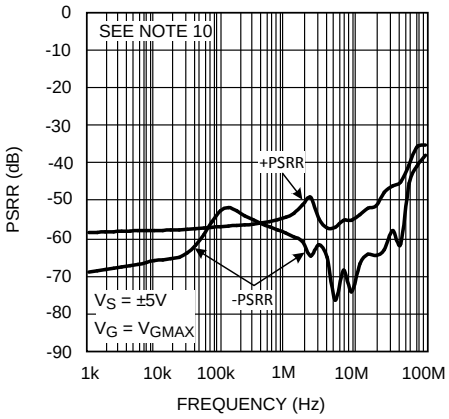


Figure 18.

PSRR ±2.5V

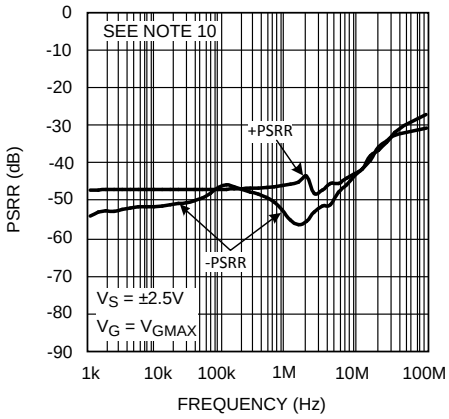


Figure 19.

CMRR ±5V

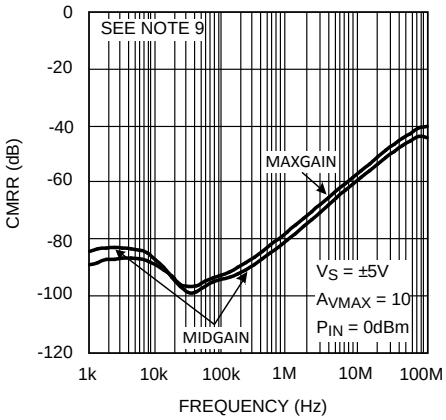


Figure 20.

CMRR ±2.5V

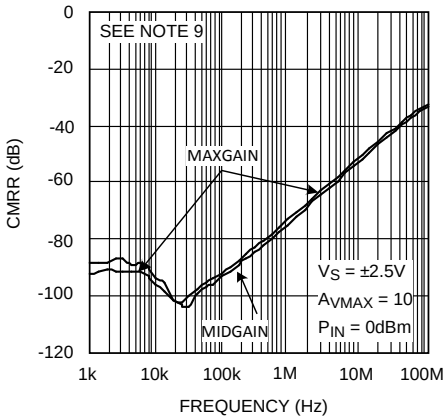


Figure 21.

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{G\_MAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

A_{VMAX} vs. V_{CM}

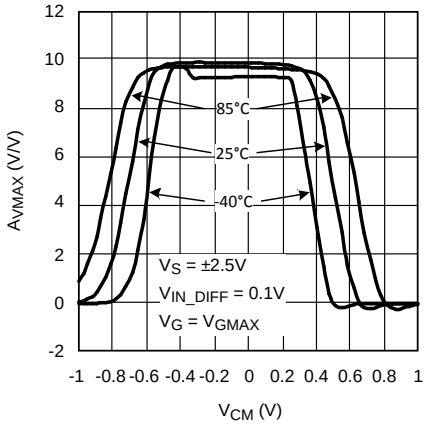


Figure 22.

A_{VMAX} vs. V_{CM}

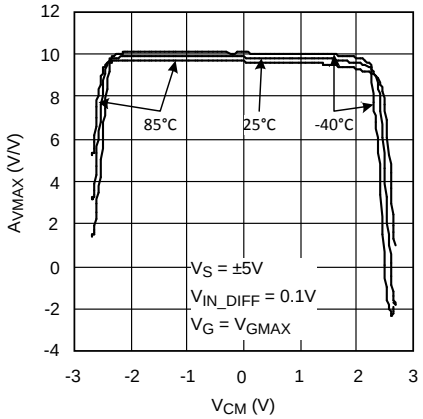


Figure 23.

Supply Current vs. V_{CM}

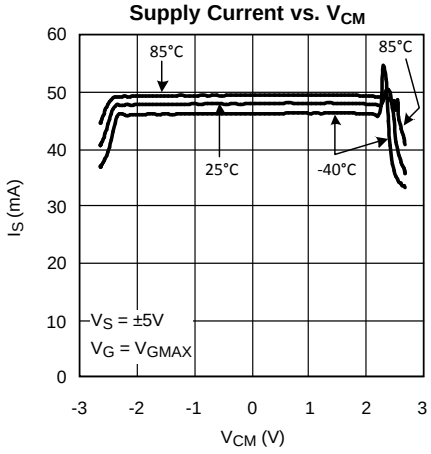


Figure 24.

Supply Current vs. V_{CM}

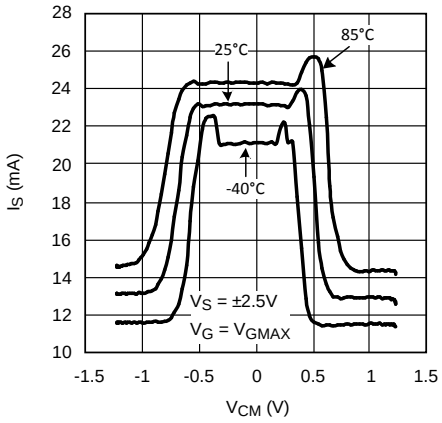


Figure 25.

Output Offset Voltage vs.V_{CM} (Typical Unit 1)

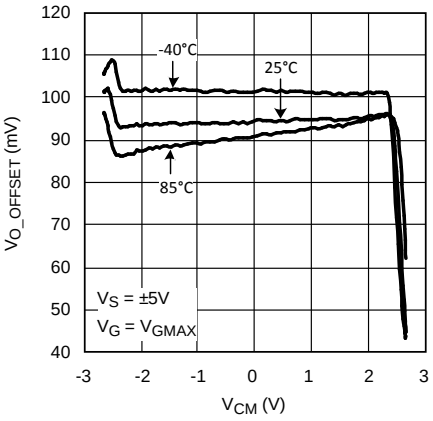


Figure 26.

Output Offset Voltage vs.V_{CM} (Typical Unit 2)

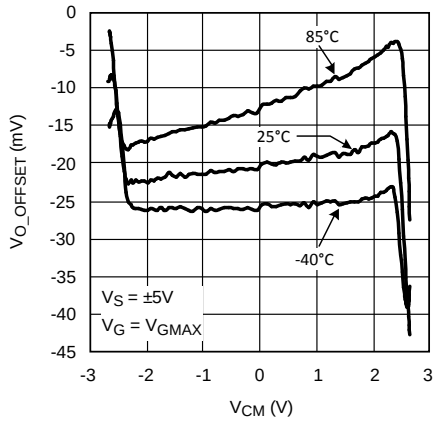


Figure 27.

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

Output Offset Voltage vs.V_{CM} (Typical Unit 3)

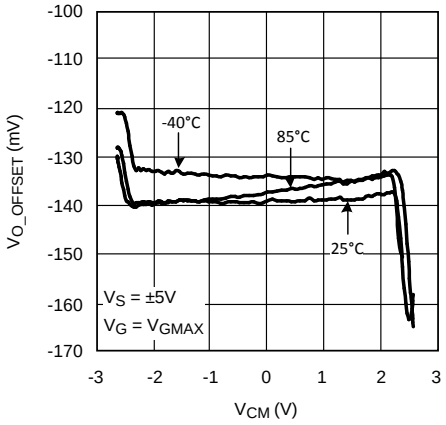


Figure 28.

Feed through Isolation

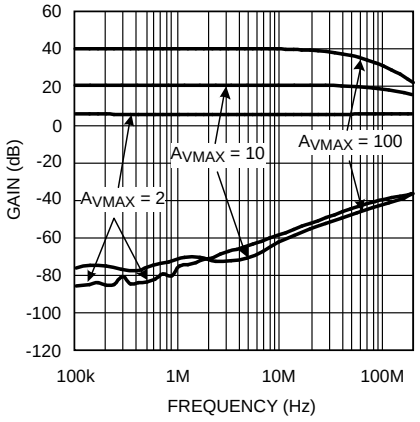


Figure 29.

Gain Flatness and Linear Phase Deviation

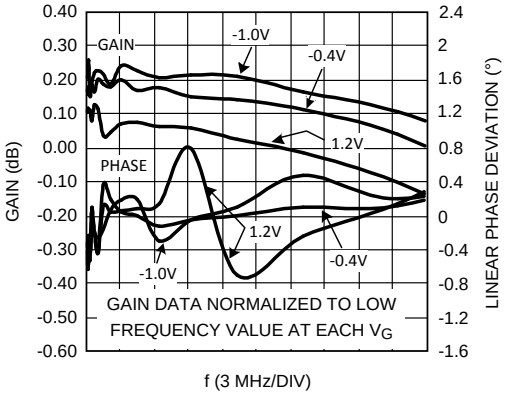


Figure 30.

Gain Flatness Frequency vs. Gain (1)

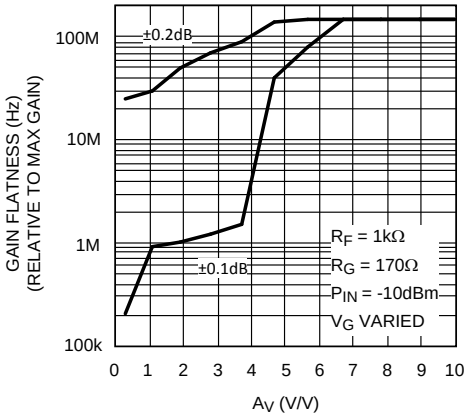


Figure 31.

Group Delay vs. Frequency

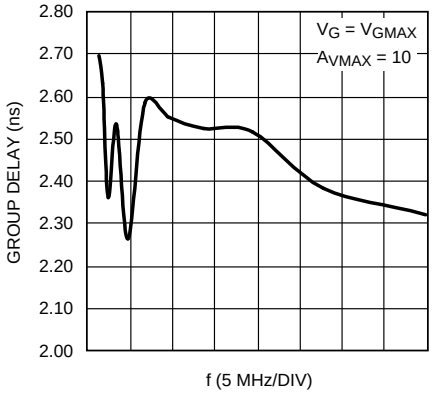


Figure 32.

K Factor vs. R_G

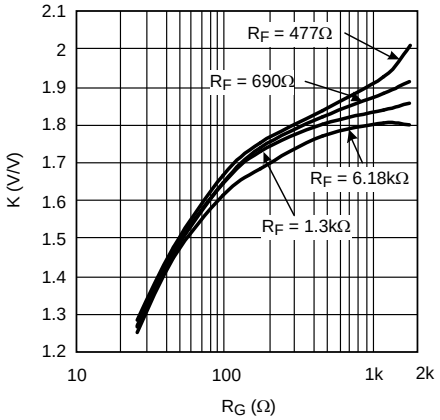


Figure 33.

(1) Flat Band Attenuation (Relative To Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either ±0.2dB or ±0.1dB), relative to A_{VMAX} gain. For example, for f<30MHz, here are the Flat Band Attenuation ranges:±0.2dB: 10V/V down to 1V/V=20dB range±0.1dB: 10V/V down to 4.7V/V=6.5dB range

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

Gain vs. V_G Including Limits

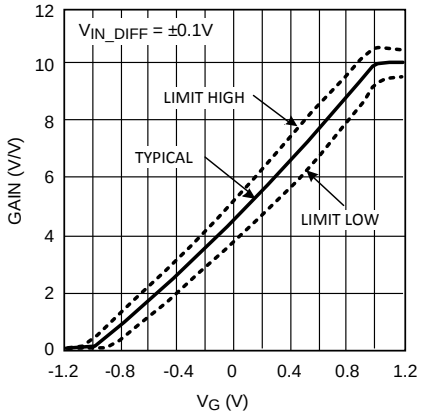


Figure 34.

BW vs. R_F for Various R_G

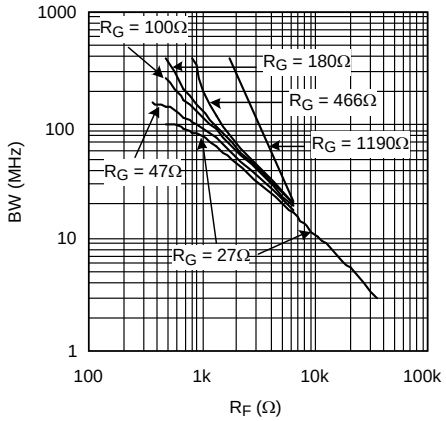


Figure 35.

Gain vs. V_G (±5V)

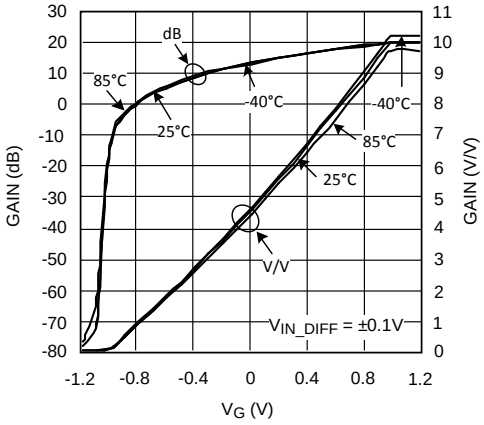


Figure 36.

Output Offset Voltage vs. V_G (Typical Unit 1)

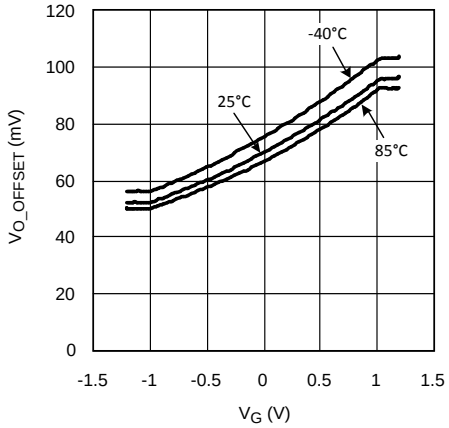


Figure 37.

Output Offset Voltage vs. V_G (Typical Unit 2)

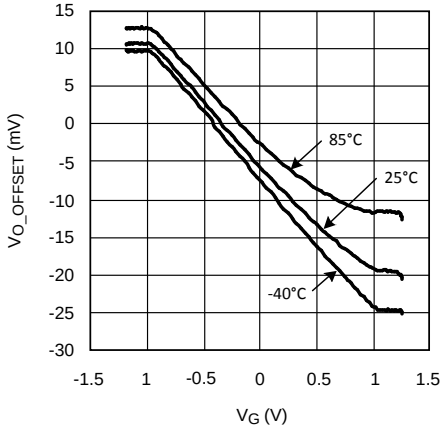


Figure 38.

Output Offset Voltage vs. V_G (Typical Unit 3)

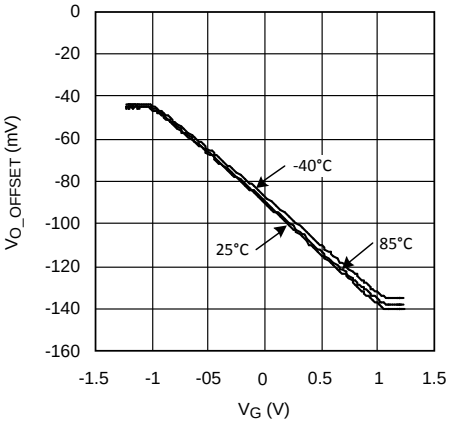


Figure 39.

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

Output Offset Voltage vs. ±V_S for Various V_G (Typical Unit 1)

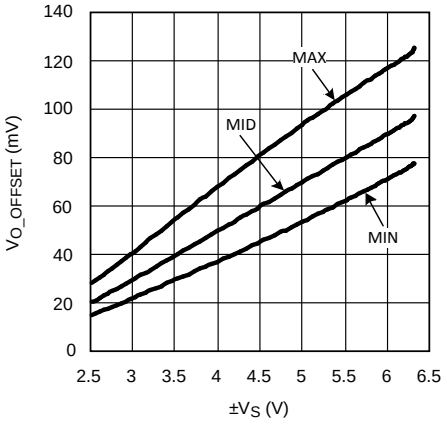


Figure 40.

Output Offset Voltage vs. ±V_S for Various V_G (Typical Unit 2)

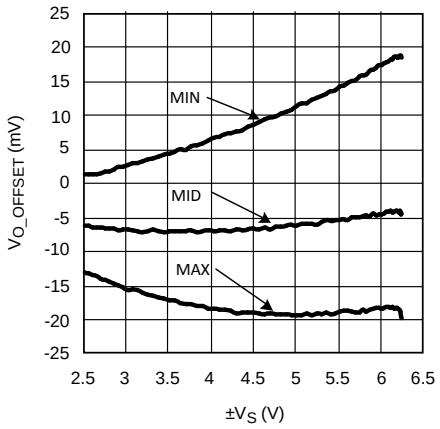


Figure 41.

Output Offset Voltage vs. ±V_S for Various V_G (Typical Unit 3)

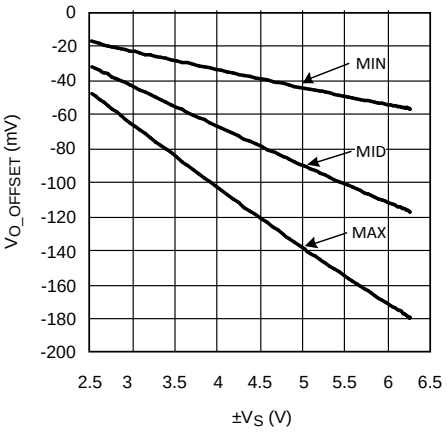


Figure 42.

Gain vs. V_G (±2.5V)

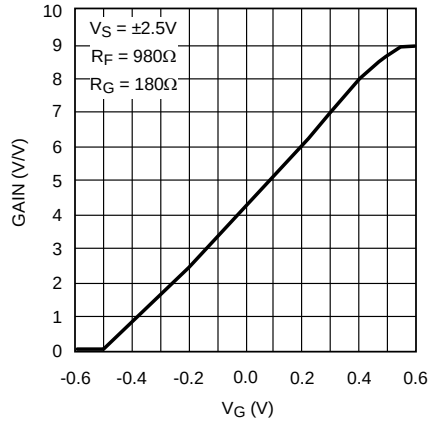


Figure 43.

Noise vs. Frequency (A_{VMAX} = 2)

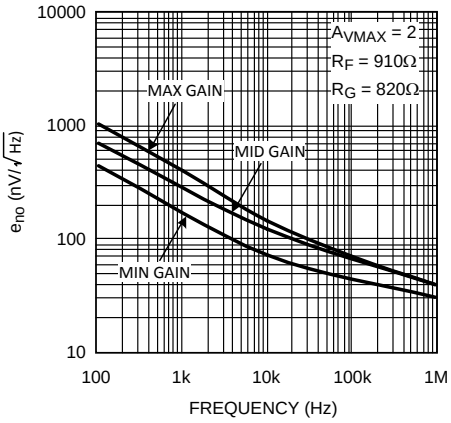


Figure 44.

Noise vs. Frequency (A_{VMAX} = 10)

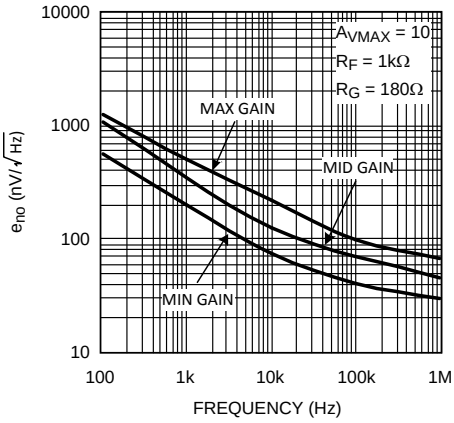


Figure 45.

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{G\_MAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

Noise vs. Frequency (A_{VMAX} = 100)

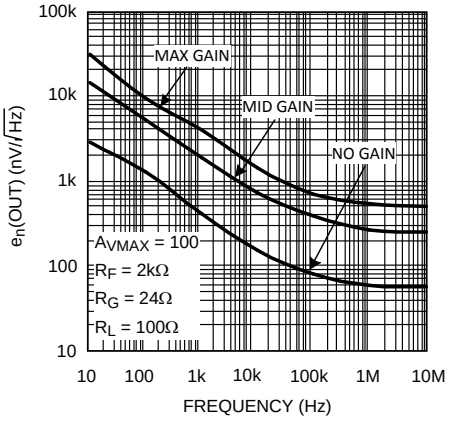


Figure 46.

−1dB Compression

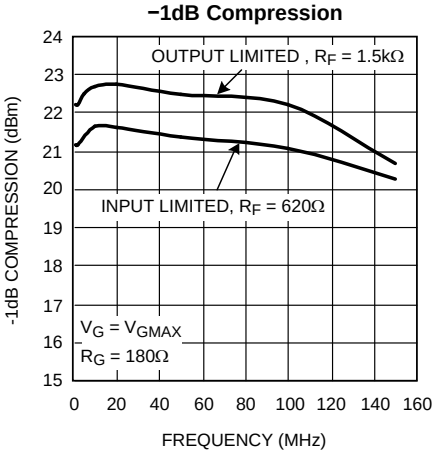


Figure 47.

Output Voltage vs. Output Current

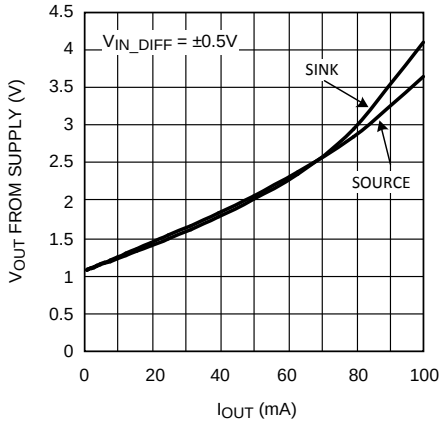


Figure 48.

HD2 vs. P_{OUT}

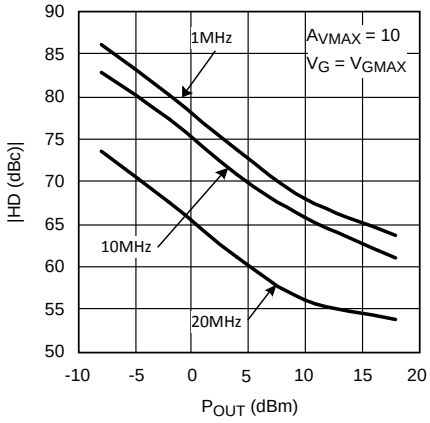


Figure 49.

HD3 vs. P_{OUT}

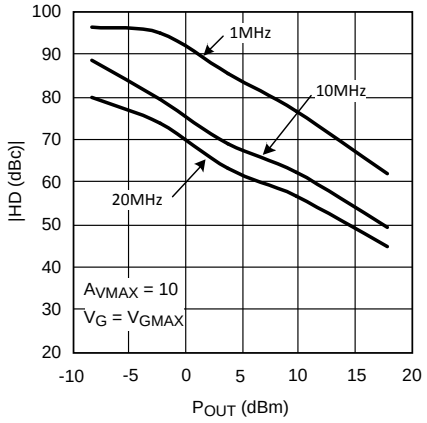


Figure 50.

THD vs. P_{OUT}

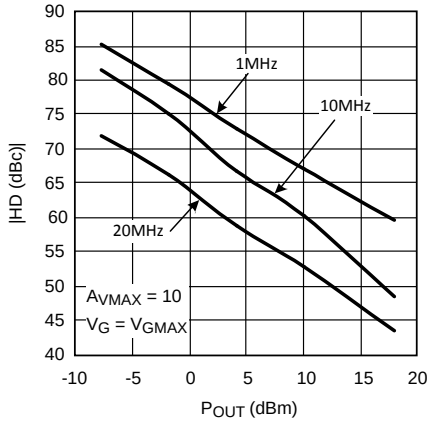


Figure 51.

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

HD2 & HD3 vs. V_G

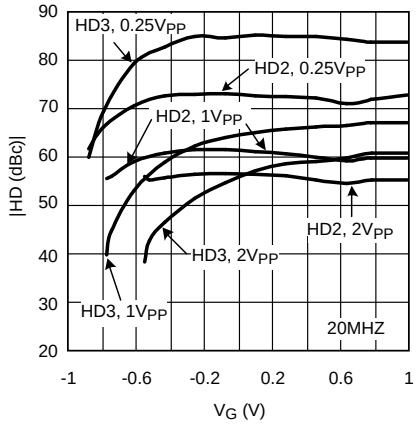


Figure 52.

THD vs. V_G

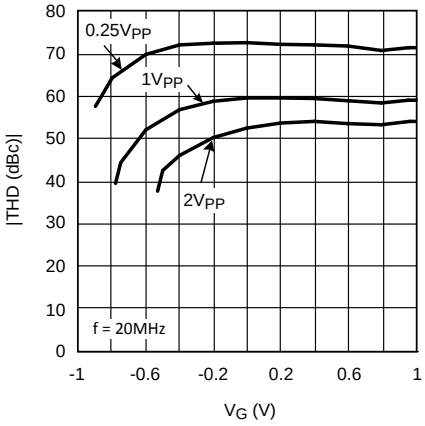


Figure 53.

V_G Bias Current vs. V_G

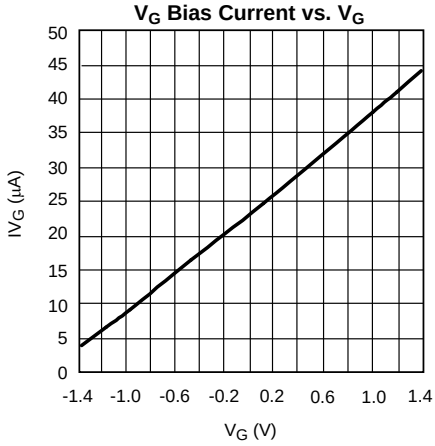


Figure 54.

Step Response Plot

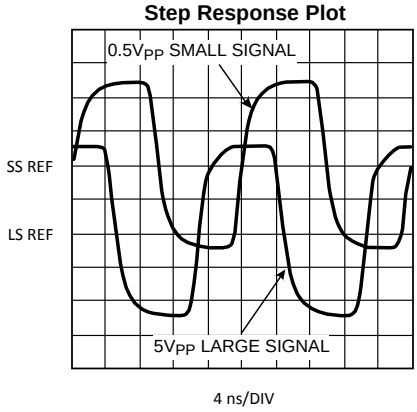


Figure 55.

Step Response Plot

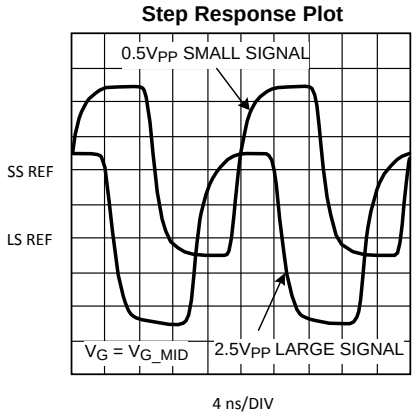


Figure 56.

Gain vs. V_G Step

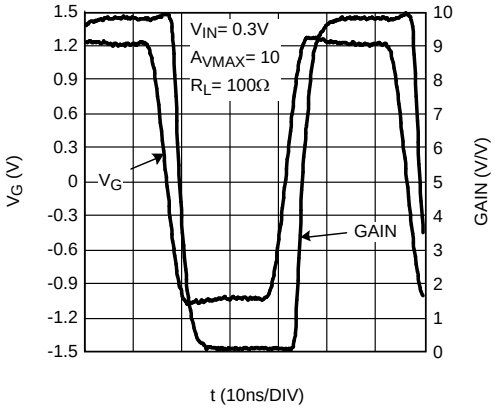


Figure 57.

Typical Performance Charateristics (continued)

Unless otherwise specified: V_S = ±5V, 25°C, $V_G = V_{G\_MAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

V_G Feedthrough

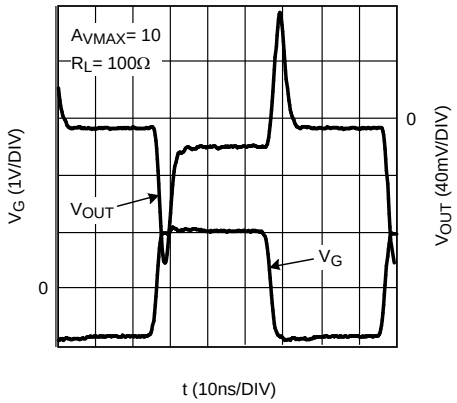


Figure 58.

APPLICATION INFORMATION

THEORY OF OPERATION

The LMH6503 is a linear wideband variable-gain amplifier as illustrated in Figure 59. A voltage input signal may be applied differentially between the two inputs ($+V_{IN}$, $-V_{IN}$), or single-endedly by grounding one of the two unused inputs. The LMH6503 input buffers convert the input voltage to a current (I_{RG}) that is a function of the differential input voltage ($V_{INPUT} = (+V_{IN}) - (-V_{IN})$) and the value of the gain setting resistor (R_G). This current (I_{RG}) is then mirrored to a gain stage with a current gain of K (1.72 nominal). The voltage controlled two-quadrant multiplier attenuates this current which is then converted to a voltage via the output amplifier. This output amplifier is a current feedback op amp configured as a Transimpedance amplifier. Its Transimpedance gain is the feedback resistor (R_F). The input signal, output, and gain control are all voltages. The output voltage can easily be calculated as shown in Equation 1:

$$V_{OUT} = I_{RG} \times K \times \left[\frac{V_G + 1}{2}\right] \times R_F \quad \text{FOR } -1 < V_G < +1 \tag{1}$$

Where K = 1.72 (Nominal)

since:

$$I_{RG} = \frac{V_{INPUT}}{R_G} \tag{2}$$

The gain of the LMH6503 is therefore a function of three external variables: R_G, R_F, and V_G as expressed in Equation 3:

$$A_V = \frac{R_F}{R_G} \times 1.72 \times \left[\frac{V_G + 1}{2}\right] \tag{3}$$

The gain control voltage (V_G) has an ideal input range of $-1V < V_G < +1V$. At $V_G = +1V$, the gain of the LMH6503 is at its maximum as expressed in Equation 4:

$$A_V = 1.72 \frac{R_F}{R_G} \tag{4}$$

Notice also that Equation 4 holds for both differential and single-ended operation.

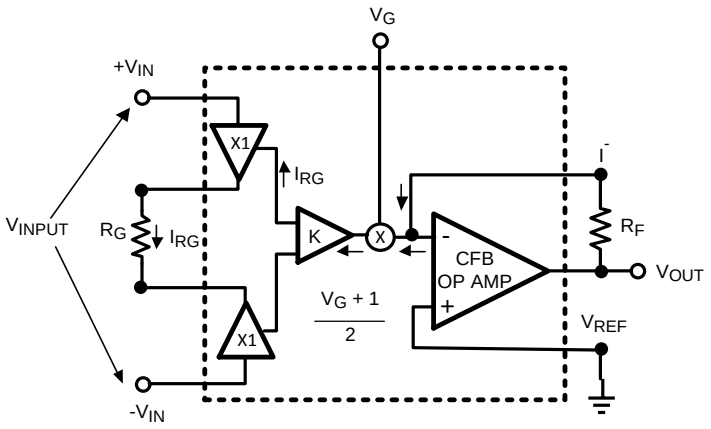


Figure 59. LMH6503 Functional Block Diagram

CHOOSING R_F AND R_G

R_G is calculated using Equation 5. $V_{INPUTMAX}$ is the maximum peak input voltage (V_{pk}) determined by the application. I_{RGMAX} is the maximum allowable current through R_G and is typically 2.3mA. Once A_{VMAX} is determined from the minimum input and desired output voltages, R_F is then determined using Equation 6. These values of R_F and R_G are the minimum possible values that meet the input voltage and maximum gain constraints. Scaling the resistor values will decrease bandwidth and improve stability.

$$R_G = \frac{V_{INPUT_{MAX}}}{I_{R_{GMAX}}} \tag{5}$$

$$R_F = \frac{1}{K} * R_G * A_{VMAX} \tag{6}$$

Figure 60 illustrates the resulting LMH6503 bandwidths as a function of the maximum (y axis) and minimum (related to x axis) input voltages when V_{OUT} is held constant at $1V_{PP}$.

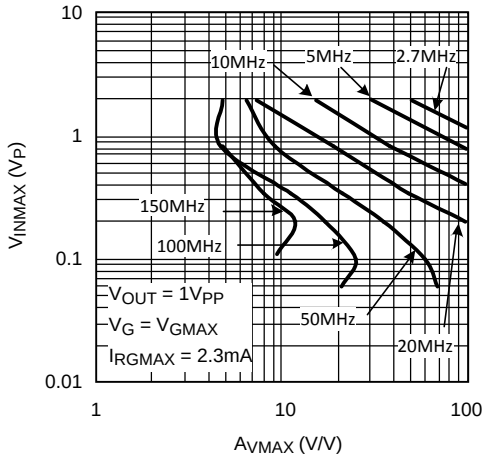


Figure 60. Bandwidth vs. V_{INMAX} and A_{VMAX}

ADJUSTING OFFSETS

Treating the offsets introduced by the input and output stages of the LMH6503 is accomplished with a two step process. The offset voltage of the output stage is treated by first applying −1.1V on V_G, which effectively isolates the input stage and multiplier core from the output stage. As illustrated in Figure 61, the trim pot located at R14 on the LMH6503 Evaluation Board (LMH730033) should then be adjusted in order to null the offset voltage seen at the LMH6503's output (pin 10).

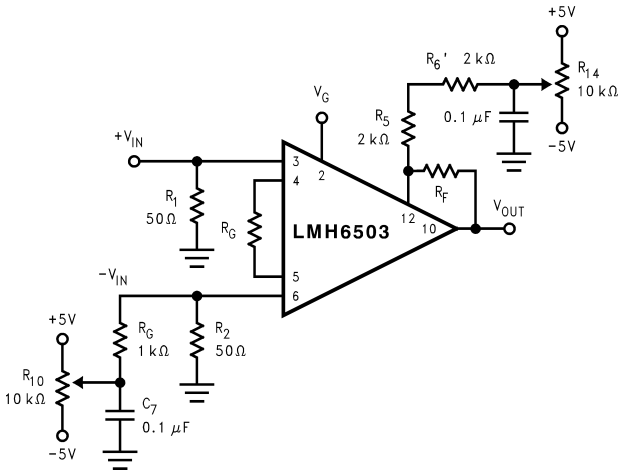


Figure 61. Nulling the Output Offset Voltage

Once this is accomplished, the offset errors introduced by the input stage and multiplier core can then be treated. The second step requires the absence of an input signal and matched source impedances on the two input pins in order to cancel the bias current errors. This done, then +1.1V should be applied to V_G and the trim pot located at R_{10} adjusted in order to null the offset voltage seen at the LMH6503's output. If a more limited gain range is anticipated, the above adjustments should be made at these operating points. These steps will minimize the output offset voltage. However, since the offset term itself varies with the gain setting, the correction is not perfect and some residual output offset will remain.

GAIN ACCURACY

Defined as the ratio of measured gain (V/V), at a certain V_G, to the best fit line drawn through the typical gain (V/V) distribution for $-1V < V_G < 1V$ (results expressed in dB) (See Figure 62). The best fit gain (A_V) is given by:

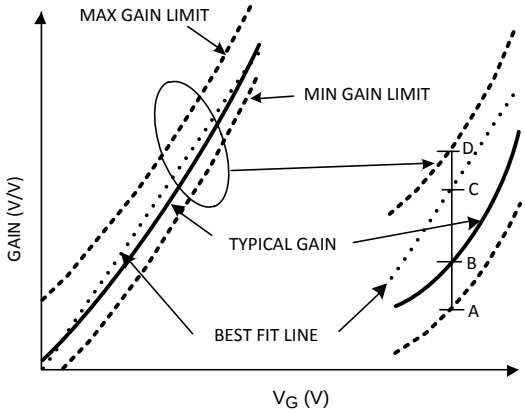
$$A_V \text{ (V/V)} = 4.87V_G + 4.61 \quad (7)$$

$$\text{For: } -1V \le V_G \le +1V,\ R_F = 1k\Omega,\ R_G = 174\Omega \quad (8)$$

For a V_G range, the value specified in the tables represents the worst case accuracy over the entire range. The "Typical" value would be the worst case ratio between the "Typical Gain" and the best fit line. The "Max" value would be the worst case between the max/min gain limit and the best fit line.

GAIN MATCHING

Defined as the limit on gain variation at a certain V_G (expressed in dB) (See Figure 62). Specified as "Max" only (no "Typical"). For a V_G range, the value specified represents the worst case matching over the entire range. The "Max" value would be the worst case ratio between the max/min gain limit and the typical gain.



PARAMETER:
GAIN ACCURACY (TYPICAL) = B/C (dB)
GAIN ACCURACY (+ & - LIMIT) = D/C & A/C (dB)
GAIN MATCHING (+ & - LIMIT) = D/B & A/B (dB)

Figure 62. Gain Accuracy and Gain Matching Parameters Defined

NOISE

Figure 63 describes the LMH6503's output-referred spot noise density as a function of frequency with A_{VMAX} = 10V/V. The plot includes all the noise contributing terms. However, with both inputs terminated in 50Ω, the input noise contribution is minimal. At A_{VMAX} = 10V/V, the LMH6503 has a typical flat-band input-referred spot noise density (e_{in}) of 6.6nV/√Hz. For applications with −3dB BW extending well into the flat-band region, the input RMS voltage noise can be determined from the following single-pole model:

$$V_{RMS} = e_{in} * \sqrt{1.57 * (\text{-3dB BANDWIDTH})} \quad (9)$$

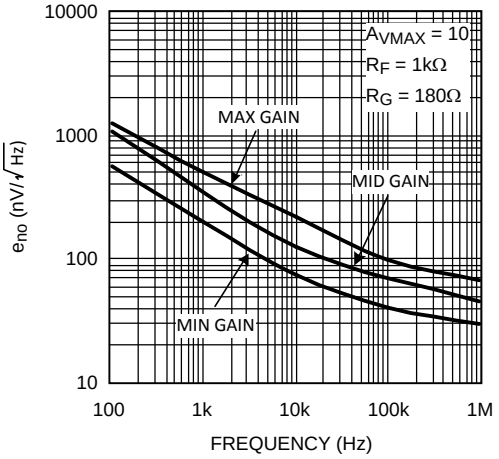


Figure 63. Output Referred Voltage Noise vs. Frequency

CIRCUIT LAYOUT CONSIDERATIONS

Good high-frequency operation requires all of the de-coupling capacitors shown in Figure 64 to be placed as close as possible to the power supply pins in order to insure a proper high-frequency low-impedance bypass. Adequate ground plane and low inductive power returns are also required of the layout. Minimizing the parasitic capacitances at pins 3, 4, 5, 6, 9, 10 and 12 will assure best high frequency performance. The parasitic inductance of component leads or traces to pins 4, 5 and 9 should also be kept to a minimum. Parasitic or load capacitance, C_L, on the output (pin 10) degrades phase margin and can lead to frequency response peaking or circuit oscillation. The LMH6503 is fully stable when driving a 100Ω load. With reduced load (e.g. 1kΩ) there is a possibility of instability at very high frequencies beyond 400MHz especially with a capacitive load. When the LMH6503 is connected to a light load as such, it is recommended to add a snubber network to the output (e.g. 100Ω and 39pF in series tied between the LMH6503 output and ground). C_L can also be isolated from the output by placing a small resistor in series with the output (pin 10).

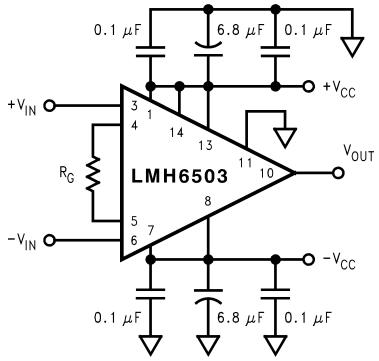


Figure 64. Required Power Supply Decoupling

Component parasitics also influence high frequency results. Therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended.

Texas Instruments suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6503MA	SOIC-14	LMH730033

SINGLE SUPPLY OPERATION

It is possible to operate the LMH6503 with a single supply. To do so, tie pin 11 (GND) to a potential about mid point between V^+ and V^-. Two examples are shown in Figure 65 & Figure 66.

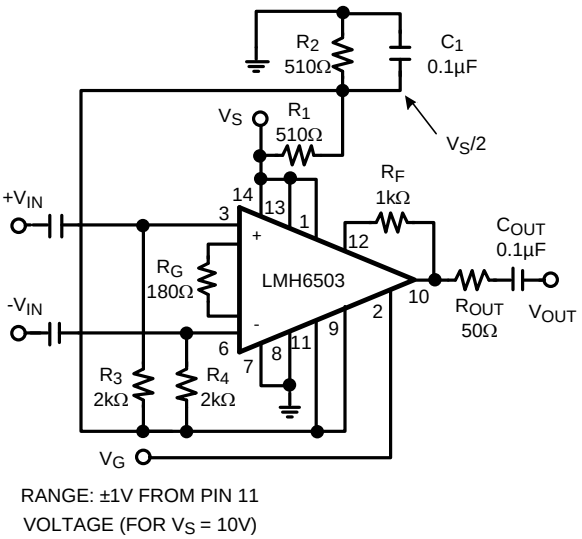


Figure 65. AC Coupled Single Supply VGA

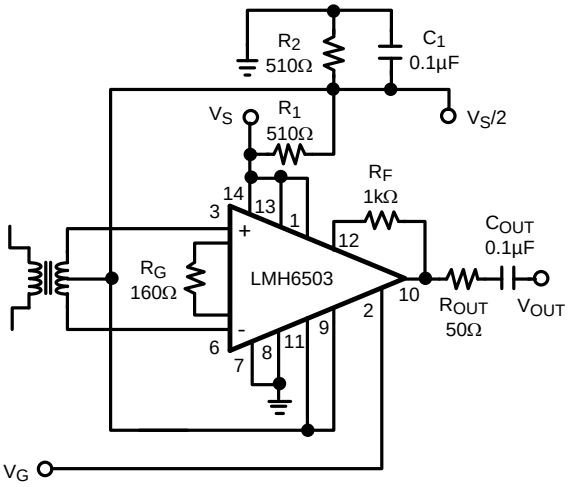


Figure 66. Transformer Coupled Single Supply VGA

OPERATING AT LOWER SUPPLY VOLTAGES

The LMH6503 is rated for operation down to 5V supplies (V^+ - V^-). There are some specifications shown for operation at ±2.5V within the data sheet (i.e. Frequency Response, CMRR, PSRR, Gain vs. V_G, etc.). Compared to ±5V operation, at lower supplies:

a) V_G range constricts. Referring to Figure 67, note that V_{G_MAX} (V_G voltage required to get maximum gain) is 0.5V (V_S = ±2.5V) compared to 1.0V for V_S = ±5V. At the same time, gain cut-off (V_{G_MIN}) would shift to −0.5V from - 1V with V_S = ±5V.
Table 1 shows the approximate expressions for various V_G voltages as a function of V^-:

Table 1. V_G Definition Based on V^-

V_G	Definition	Expression (V)
V_{G_MIN}	Gain Cut-off	0.2 x V^-
V_{G_MID}	$A_{VMAX}/2$	0
V_{G_MAX}	A_{VMAX}	−0.2 x V^-

b) V_{G_LIMIT} (maximum permissible voltage on V_G) is reduced. This is due to limitations within the device arising from transistor headroom. Beyond this limit, device performance will be affected (non-destructive). Referring to Figure 67, note that with V^+ = 2.5V, and V^- = −4V, V_{G_LIMIT} is approaching V_{G_MAX} and already "Max gain" is reduced by 1dB. This means that operating under these conditions has reduced the maximum permissible voltage on V_G to a level below what is needed to get Max gain. If supply voltages are asymmetrical, reference Figure 67 and Figure 68 plots to make sure the region of operation is not overly restricted by the "pinching" of V_{G_LIMIT}, and V_{G_MAX} curves.

c) "Max_gain" reduces. There is an intrinsic reduction in max gain when the total supply voltage is reduced (see Figure 43). In addition, there is the more drastic mechanism described in "b" above and shown in Figure 67.

Similar plots for V^+ = 5V operation are shown in Figure 68 for comparison and reference.

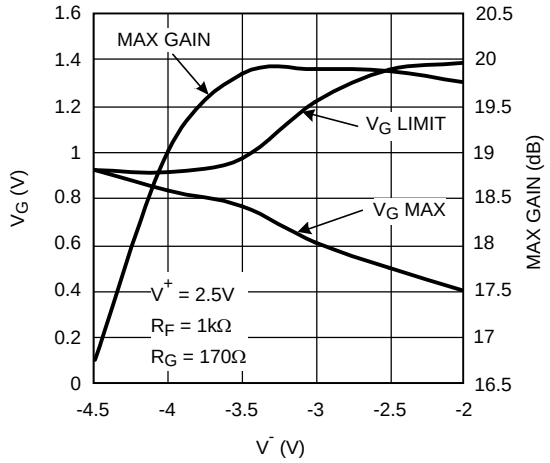


Figure 67. V_{G_MAX}, V_{G_LIMIT}, & Max-gain vs. V^- (V^+ = 2.5V)

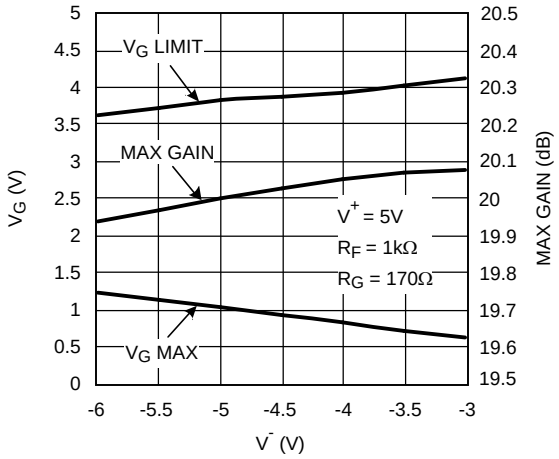


Figure 68. V_{G_MAX}, V_{G_LIMIT}, & Max-gain vs. V^- (V^+ = 5V)

Application Circuits

FOUR-QUADRANT MULTIPLIER

Applications requiring multiplication, squaring or other non-linear functions can be implemented with four-quadrant multipliers. The LMH6503 implements a four-quadrant multiplier as illustrated in Figure 69:

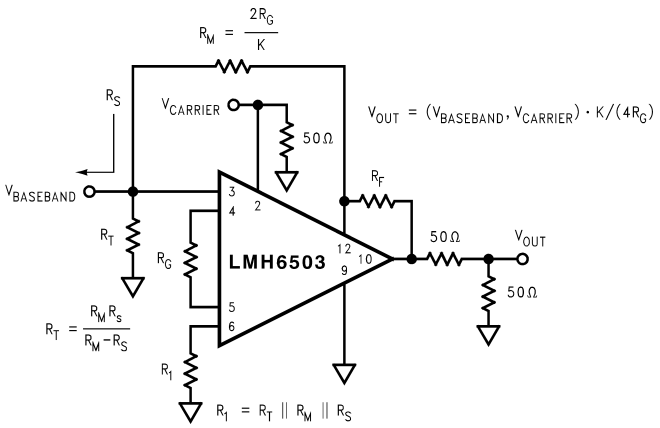


Figure 69. Four Quadrant Multiplier

FREQUENCY SHAPING

Frequency shaping and bandwidth extension of the LMH6503 can be accomplished using parallel networks connected across the R_G ports. The network shown in the Figure 70 schematic will effectively extend the LMH6503's bandwidth.

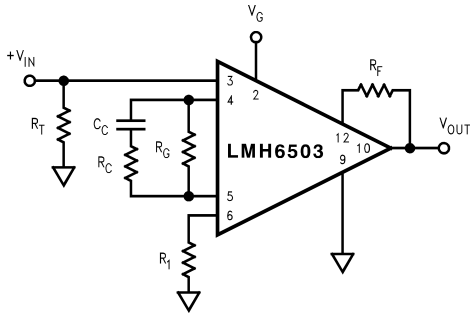
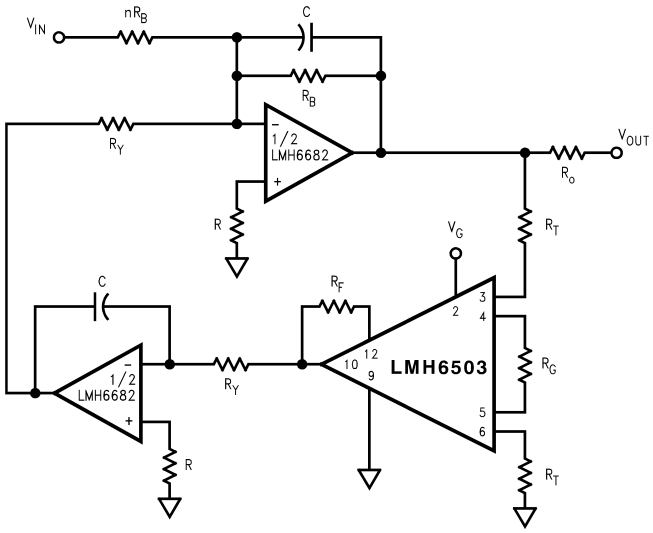


Figure 70. Frequency Shaping

2nd ORDER TUNABLE BANDPASS FILTER

The LMH6503 Variable-Gain Amplifier placed into a feedback loop provides signal processing function such as in a 2nd order tunable bandpass filter. The center frequency of the 2nd order bandpass shown in Figure 71 is adjusted through the use of the LMH6503's gain control voltage, V_G. The integrators implemented with two sections of a LMH6682, provide the coefficients for the transfer function.



$$\frac{V_O}{V_{IN}} = \left[-\frac{1}{n}\right] \frac{s\frac{1}{CR_B}}{s^2 + s\frac{1}{CR_B} + \frac{p}{C^2R_Y^2}}$$

$$p = 1.72\,\frac{R_F}{R_Y},\ Q = \frac{\sqrt{pR_B}}{R_Y},\ \omega_O = \frac{\sqrt{p}}{CR_Y}$$

Figure 71. Tunable Bandpass Filter

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6503MA/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH6503MA	Samples
LMH6503MAX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH6503MA	Samples
LMH6503MT	LIFEBUY	TSSOP	PW	14	94	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LMH65 03MT	
LMH6503MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 03MT	Samples
LMH6503MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 03MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

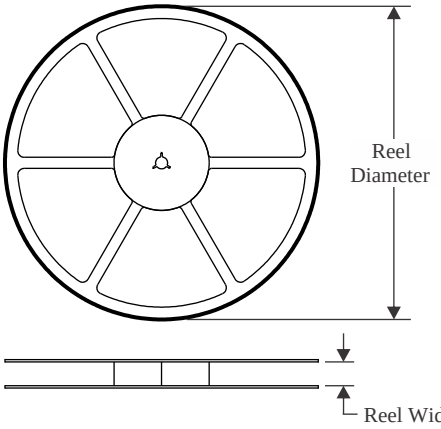
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

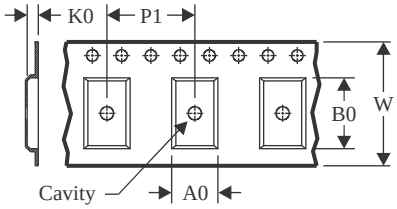
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

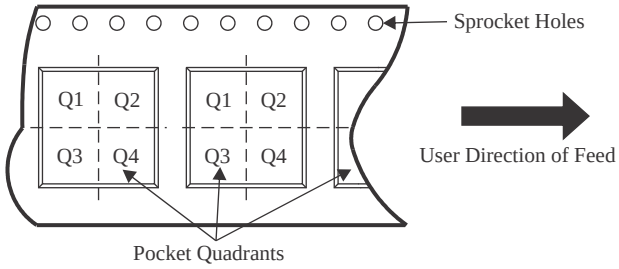


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

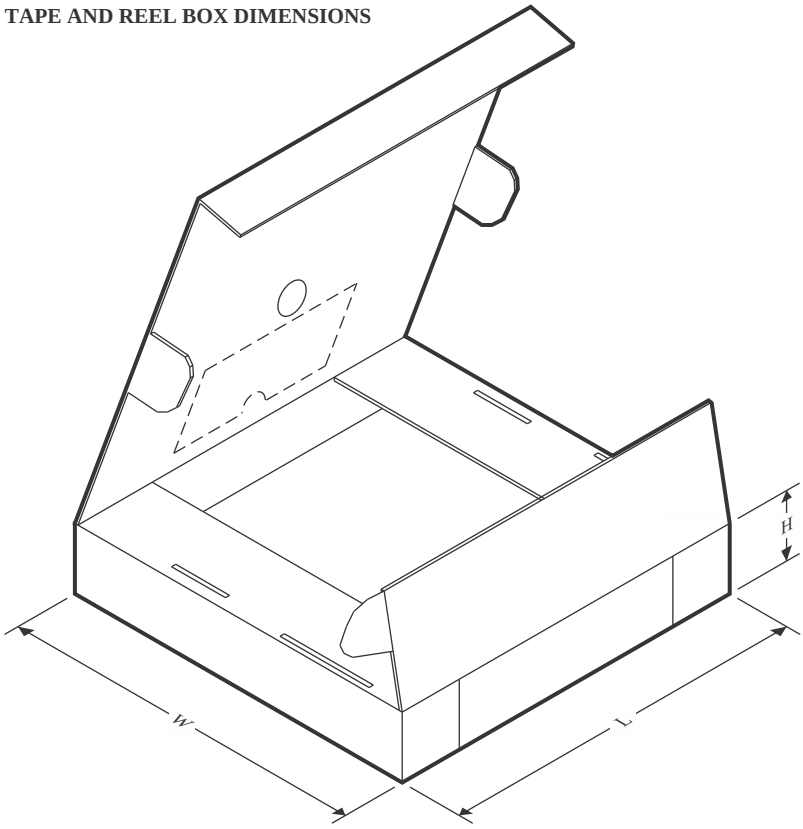
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6503MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMH6503MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

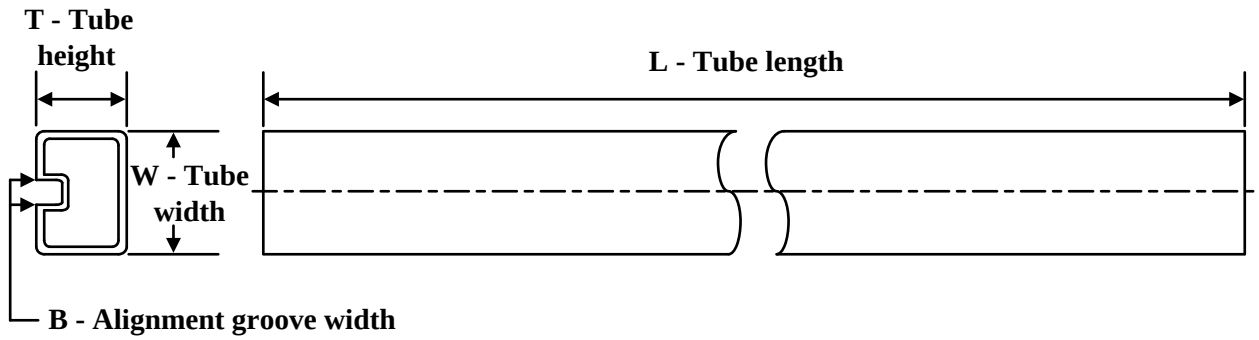
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

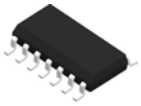
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6503MAX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LMH6503MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6503MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMH6503MT	PW	TSSOP	14	94	495	8	2514.6	4.06
LMH6503MT	PW	TSSOP	14	94	495	8	2514.6	4.06
LMH6503MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

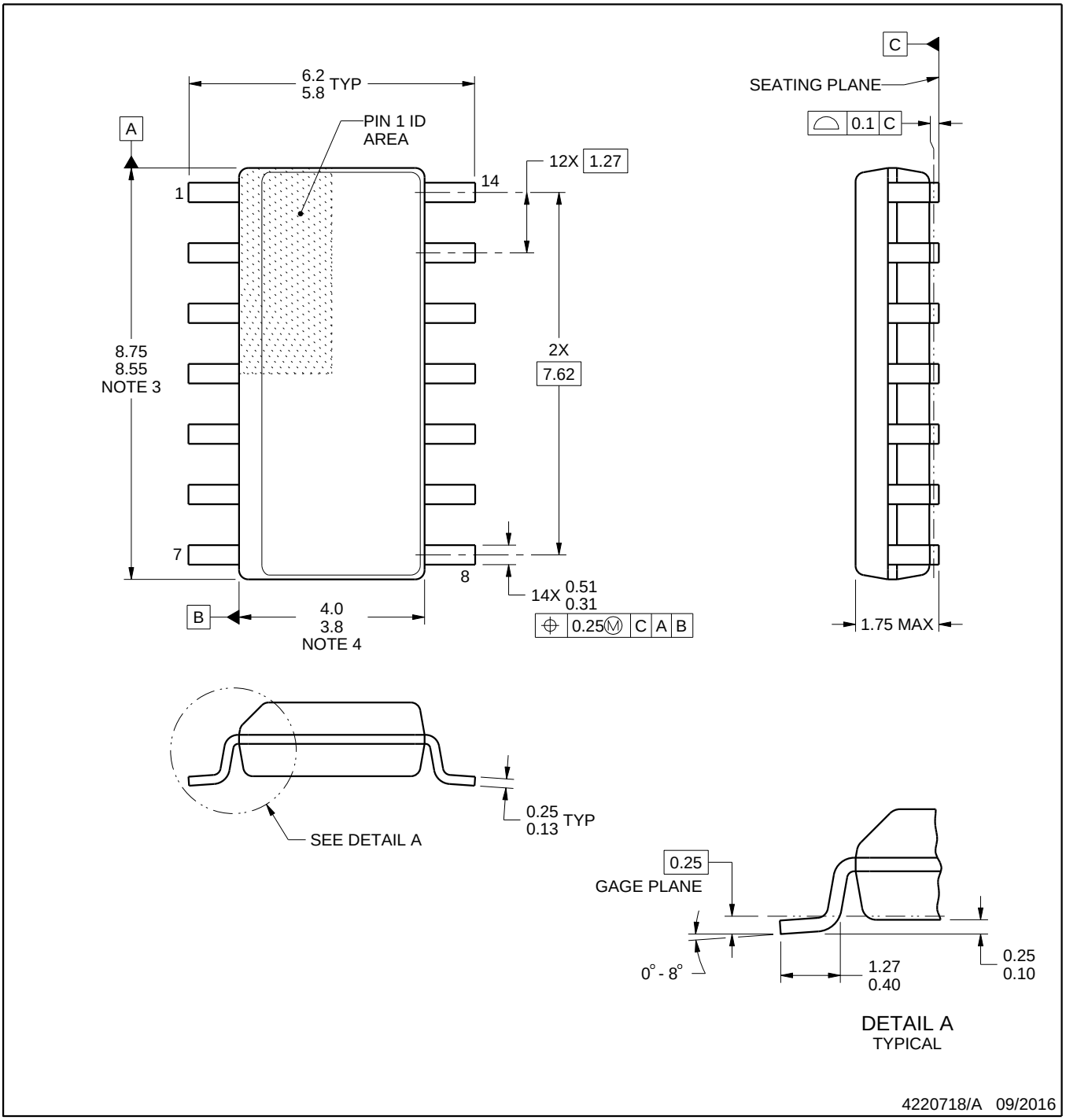


PACKAGE OUTLINE

D0014A

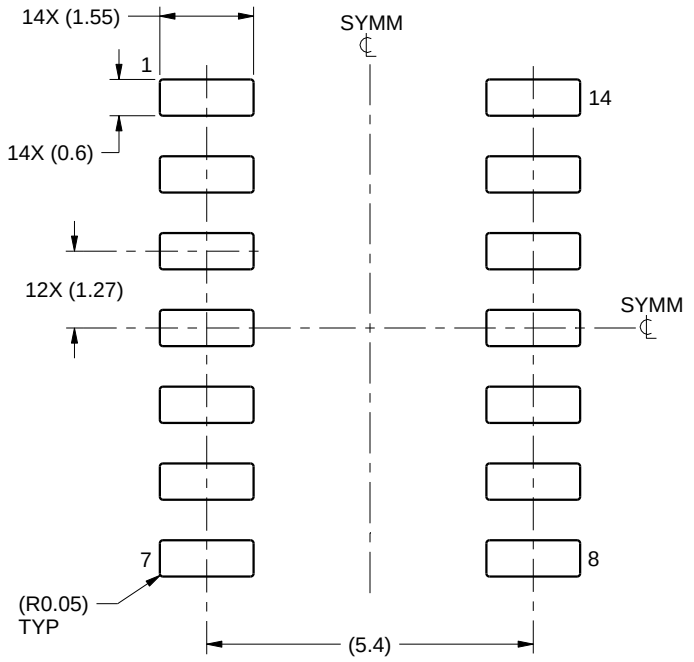
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

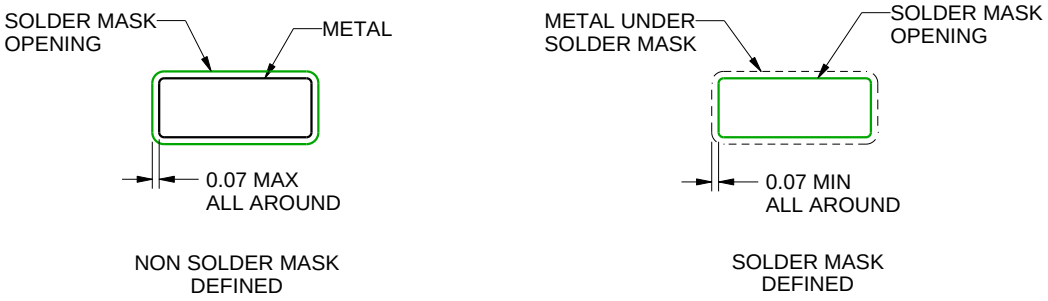


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

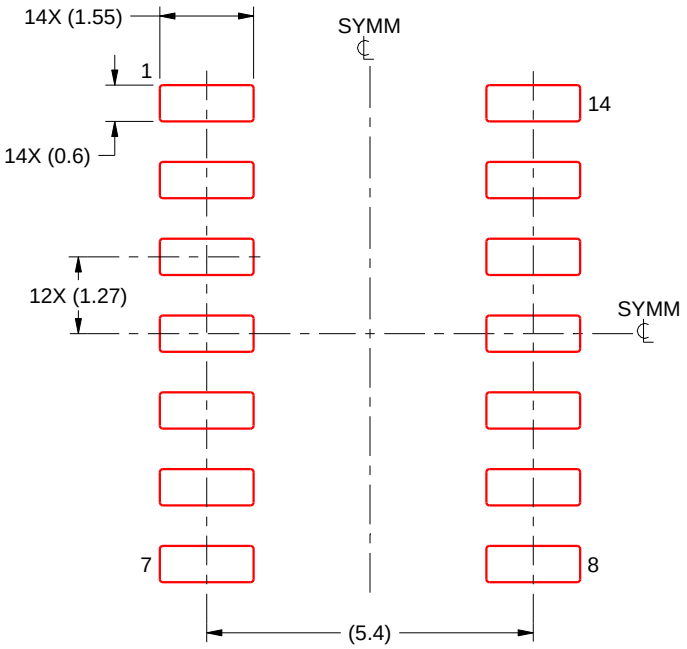
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

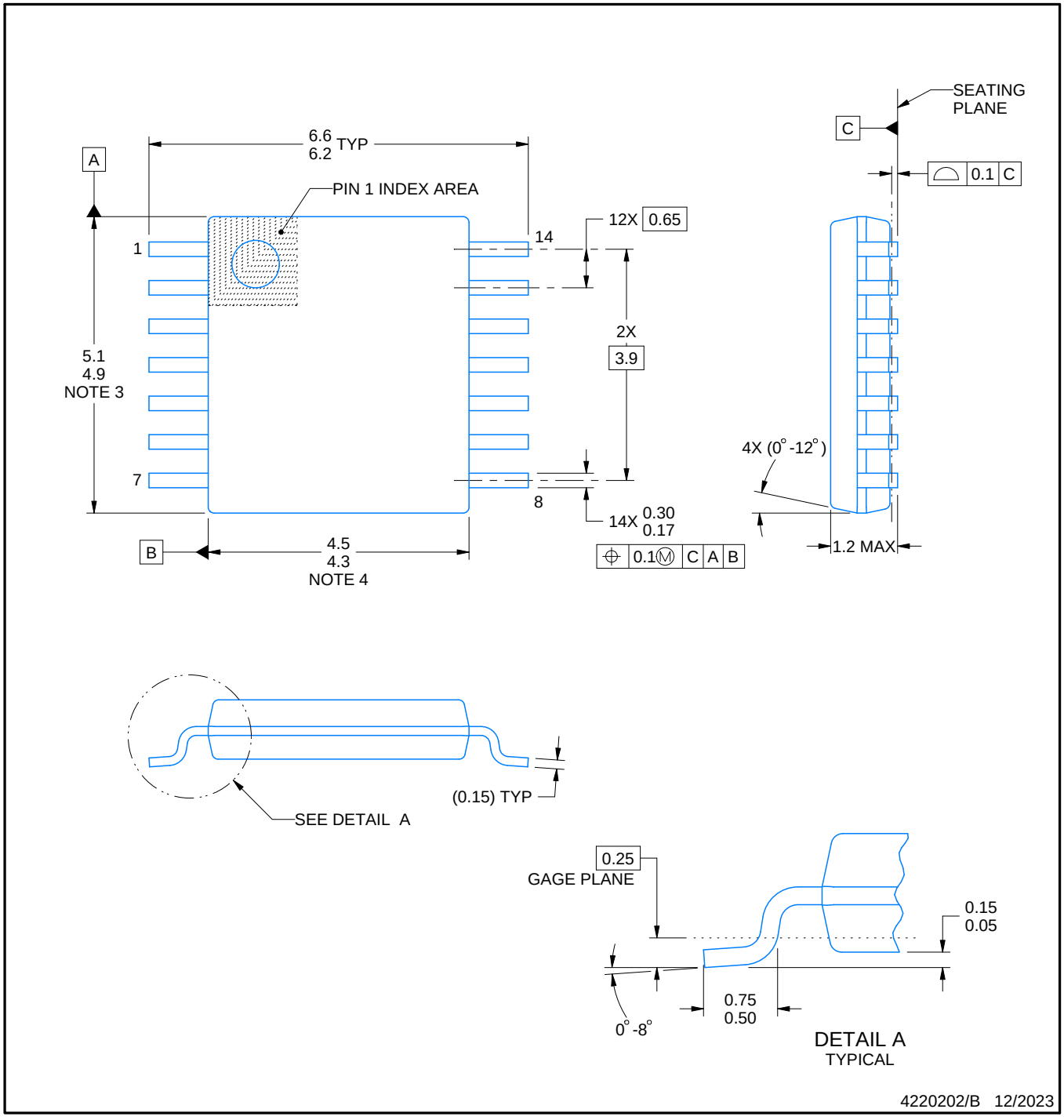
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

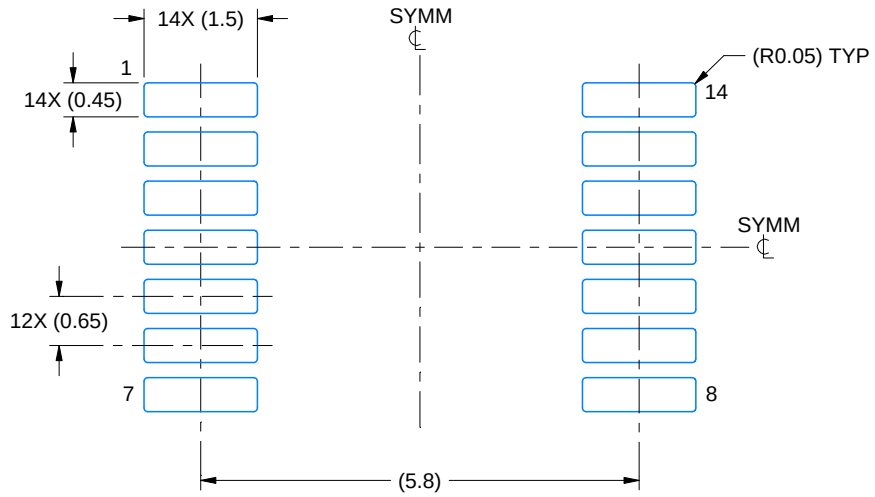
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

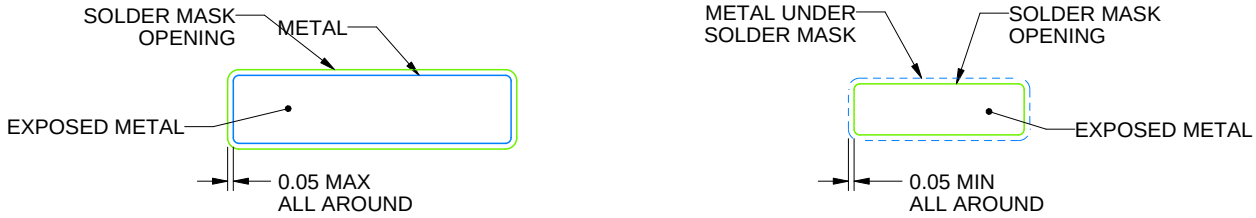


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

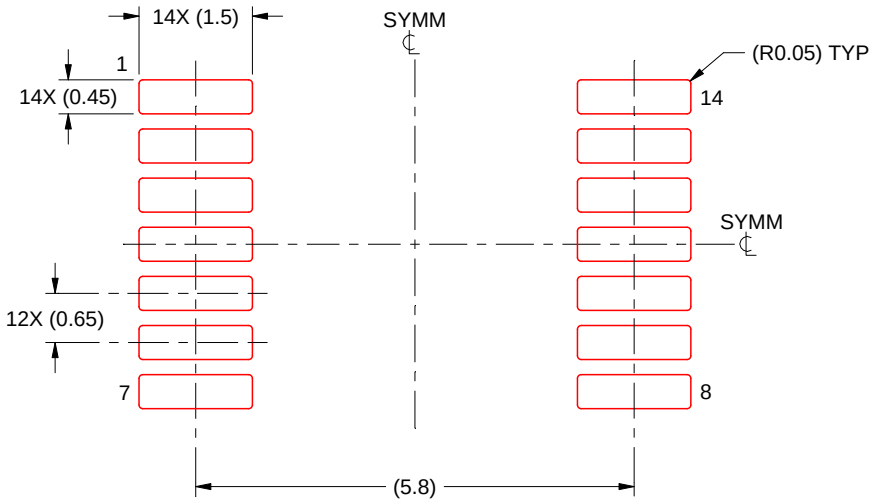


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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