MAX202 具有 ±15kV ESD 保护功能的 5V 双路 RS-232 线路驱动器和接收器

1 特性

- 符合或超出 TIA/EIA-232-F 和 ITU v.28 标准的要求
- 为 RS-232 总线引脚提供 ESD 保护：±15kV 人体放电模型
- 由 5V V_{CC} 电源供电
- 速率高达 120kbit/s
- 两个驱动器和两个接收器
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 电池供电型系统
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

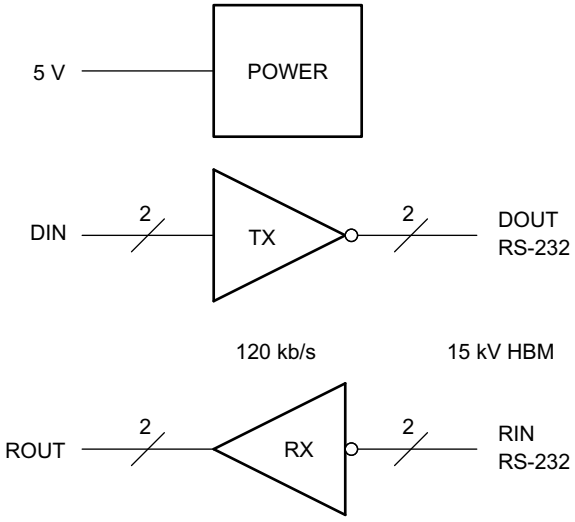
3 说明

MAX202 器件由两个线路驱动器、两个线路接收器和一个双电荷泵电路组成，具有引脚对引脚（串行端口连接引脚，包括 GND）±15kV ESD 保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 5V 单电源供电。这些器件以高达 120kbit/s 的数据信号传输速率和最高 30V/µs 的驱动器输出压摆率运行。

封装信息

器件型号	封装(1)	封装尺寸(2)
MAX202	SOIC (D) (16)	9.9mm x 6mm
	SOIC WIDE (DW) (16)	10.4mm x 10.3mm
	TSSOP (PW) (16)	5mm x 6.4mm

(1) 如需更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



方框图

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4 Pin Configuration and Functions

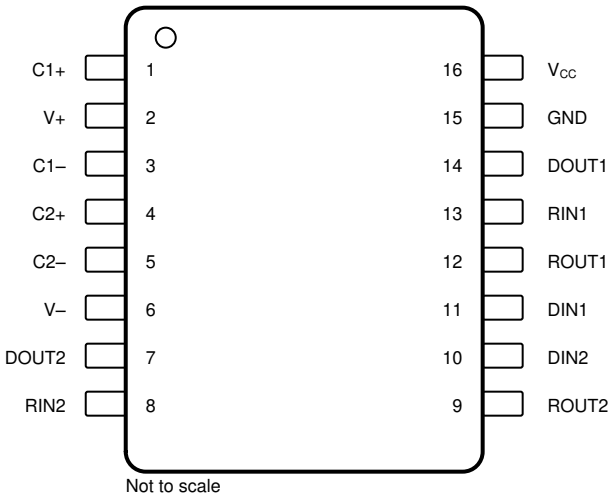


图 4-1. D, DW, or PW Package, 16-Pin SOIC or TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	V+	O	Positive charge pump output for storage capacitor only
3	C1 –	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2 –	—	Negative lead of C2 capacitor
6	V –	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	V_{CC}	—	Supply voltage, connect to external 5V power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		–0.3	6	V
Positive charge pump voltage, V+(2)		V_{CC} – 0.3	14	V
Negative charge pump voltage, V– (2)		–14	0.3	V
Input voltage, V_I	Drivers	–0.3	V+ + 0.3	V
	Receivers		±30	
Output voltage, V_O	Drivers	V– – 0.3	V+ + 0.3	V
	Receivers	–0.3	V_{CC} + 0.3	
Short-circuit duration, D_{OUT}		Continuous		
Operating junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 7, 8, 13, and 14	±15000	V
			All other pins	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted(1); see 图 7-1)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage (D_{IN})		2			V
V_{IL}	Driver low-level input voltage (D_{IN})				0.8	V
V_I	Driver input voltage (D_{IN})		0		5.5	V
	Receiver input voltage		–30		30	
T_A	Operating free-air temperature	MAX202C	0		70	°C
		MAX202I	–40		85	

(1) Test conditions are C1 – C4 = 0.1µF at V_{CC} = 5V ±0.5V.

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC)	DW (SOIC)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	71.7	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	37.6	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	36.8	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.	3.2	°C/W

5.4 Thermal Information（续）

THERMAL METRIC[1]		D (SOIC) 16 PINS	DW (SOIC) 16 PINS	PW (TSSOP) 16 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	42.8	36.4	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see 图 7-1)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 5V		8	15	mA
DRIVER SECTION						
V_{OH}	High-level output voltage	D_{OUT} at R_L = 3kΩ to GND, D_{IN} = GND	5	9		V
V_{OL}	Low-level output voltage	D_{OUT} at R_L = 3kΩ to GND, D_{IN} = V_{CC}	–5	–9		V
I_{IH}	High-level input current	V_I = V_{CC}		0	200	μA
I_{IL}	Low-level input current	V_I at 0V		0	–200	μA
I_{OS} [3]	Short-circuit output current	V_{CC} = 5.5V, V_O = 0V		±10	±60	mA
r_O	Output resistance	V_{CC}, V+, and V– = 0V, V_O = ±2V	300			Ω
RECEIVER SECTION						
V_{OH}	High-level output voltage	I_{OH} = –1mA	3.5	V_{CC} – 0.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5V, T_A = 25°C		1.7	2.4	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 5V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})		0.2	0.5	1	V
r_i	Input resistance	V_I = ±3V to ±25V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

5.6 Switching Characteristics

over recommended ranges of suply voltage and operating free-air temperature (unless otherwise noted; see 图 7-1)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
DRIVER SECTION						
	Maximum data rate	C_L = 50pF to 1000pF, R_L = 3kΩ to 7kΩ one D_{OUT} switching, see 图 6-1	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	C_L = 2500pF, R_L = 3kΩ, all drivers loaded, see 图 6-1		2		μs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	C_L = 2500pF, R_L = 3kΩ, all drivers loaded, see 图 6-1		2		μs
$t_{sk(p)}$	Pulse skew[3]	C_L = 150 to 2500pF, R_L = 3kΩ to 7 kΩ, see 图 6-2		300		ns
SR(tr)	Slew rate, transition region	C_L = 50 to 1000pF, R_L = 3kΩ to 7 kΩ, V_{CC} = 5V, see 图 6-1	3	6	30	V/μs
RECEIVER SECTION (SEE 图 6-3)						
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150pF		0.5	10	μs
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150pF		0.5	10	μs

5.6 Switching Characteristics（续）

over recommended ranges of suply voltage and operating free-air temperature (unless otherwise noted; see 图 7-1)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
$t_{sk(p)}$	Pulse skew(3)	C_L = 150pF		300		ns

(1) Test conditions are C1 – C4 = 0.1μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.7 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

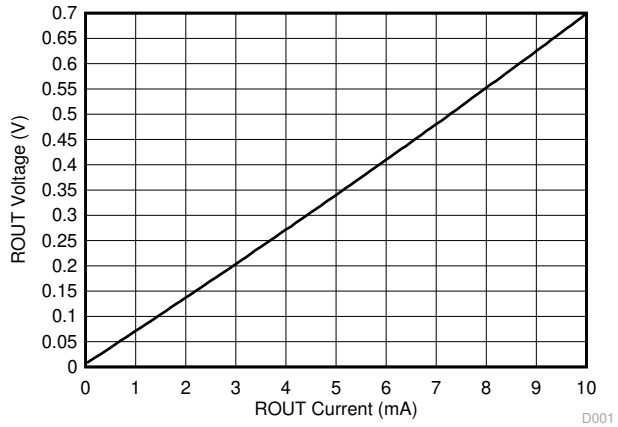


图 5-1. Receiver VOL vs Output Current

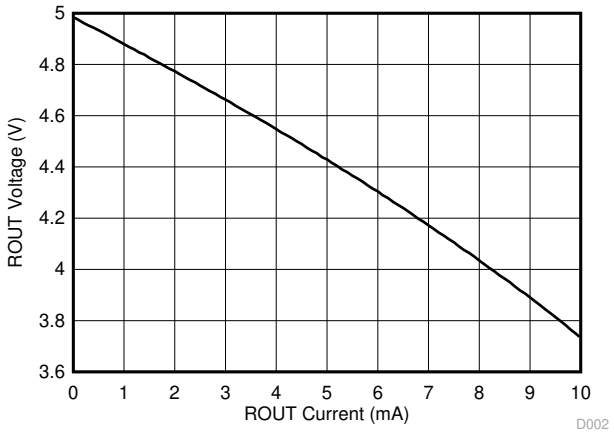


图 5-2. Receiver VOH vs Output Current

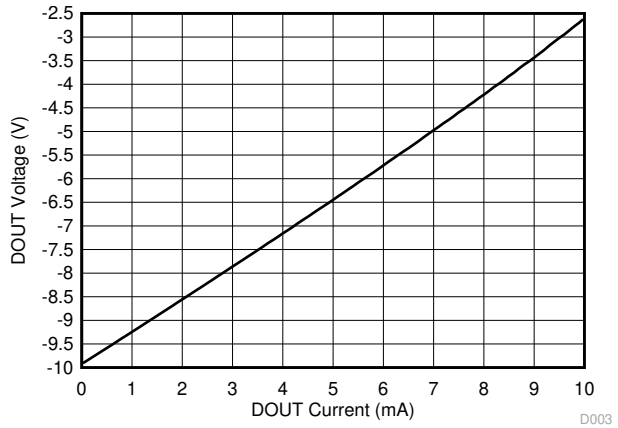


图 5-3. Driver VOL vs Output Current

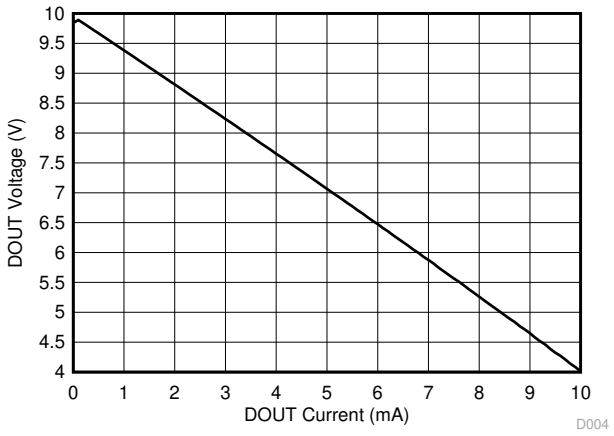


图 5-4. Driver VOH vs Output Current

5.7 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

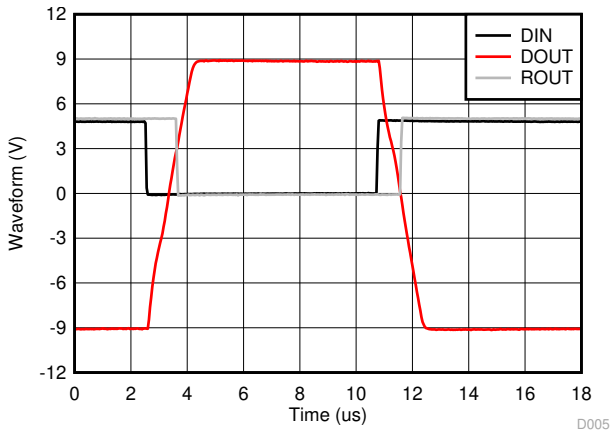
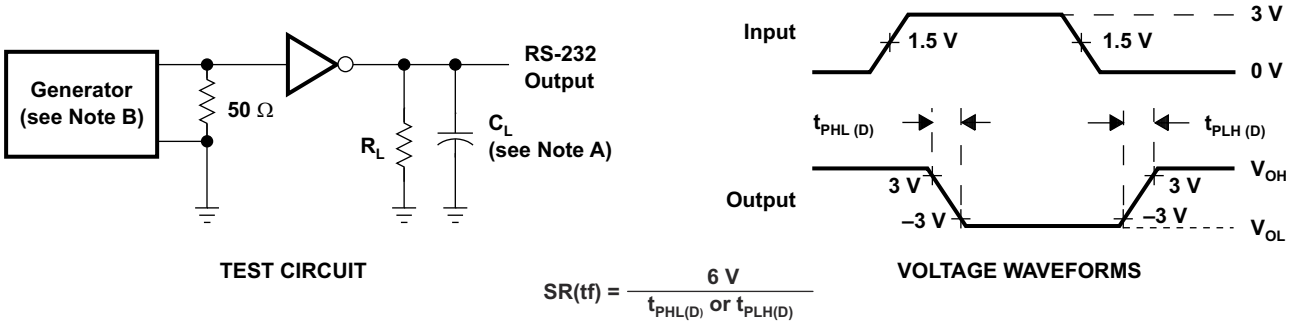


图 5-5. Driver and Receiver Loopback Waveforms

Parameter Measurement Information



TEST CIRCUIT

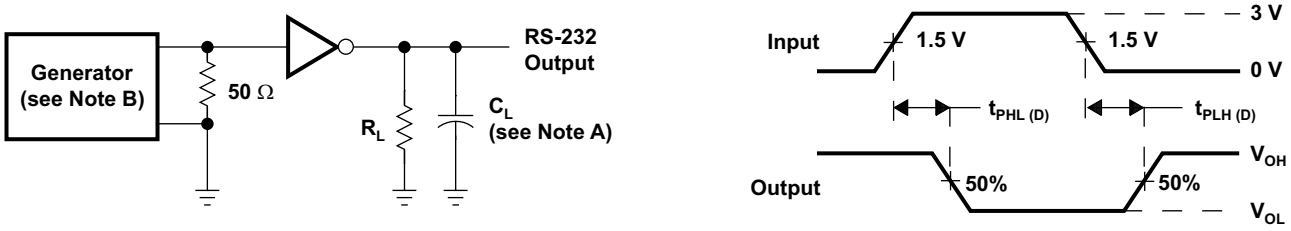
$$SR(tf) = \frac{6\ V}{t_{PHL(D)} \text{ or } t_{PLH(D)}}$$

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leqslant$ 10ns, $t_f \leqslant$ 10ns.

图 6-1. Driver Slew Rate



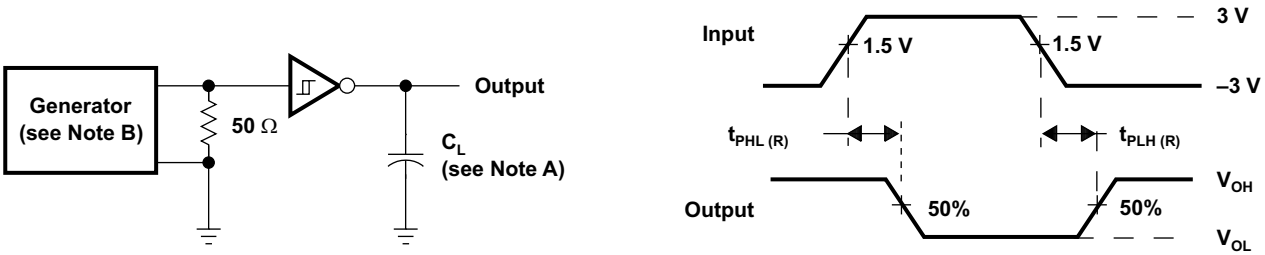
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leqslant$ 10ns, $t_f \leqslant$ 10ns.

图 6-2. Driver Pulse Skew



TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leqslant$ 10ns, $t_f \leqslant$ 10ns.

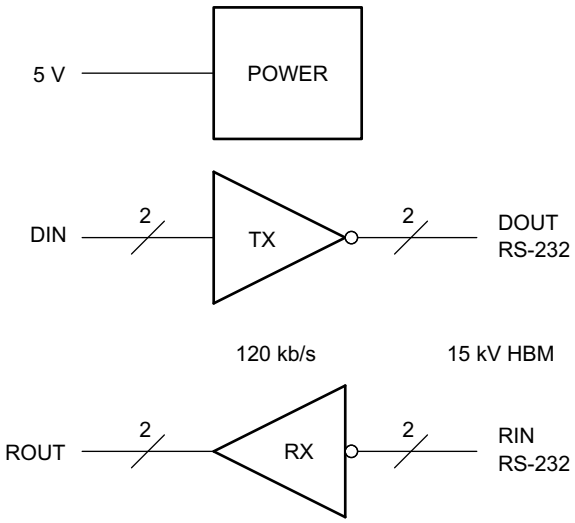
图 6-3. Receiver Propagation Delay Times

6 Detailed Description

6.1 Overview

The MAX202 is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5V supply. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to ±30V inputs and decode inputs as low as ±3V. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power

The power block increases and inverts the 5V supply for the RS-232 driver using a charge pump that requires four 0.1µF external capacitors.

6.3.2 RS-232 Driver

Two drivers interface standard logic levels to RS-232 levels. The driver inputs do not have internal pullup resistors. Do not float the driver inputs.

6.3.3 RS-232 Receiver

Two Schmitt trigger receivers interface RS-232 levels to standard logic levels. Each receiver has an internal 5-kΩ load to ground. An open input results in a high output on ROUT.

6.4 Device Functional Modes

6.4.1 V_{CC} Powered by 5V

The device is in normal operation when powered by 5V.

6.4.2 V_{CC} Unpowered

When MAX202 is unpowered, it can be safely connected to an active remote RS-232 device.

6.4.3 Truth Tables

表 6-1 and 表 6-2 list the function for each driver and receiver (respectively).

表 6-1. Function Table for Each Driver

INPUT DIN(1)	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

表 6-2. Function Table for Each Receiver

INPUT RIN(1)	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

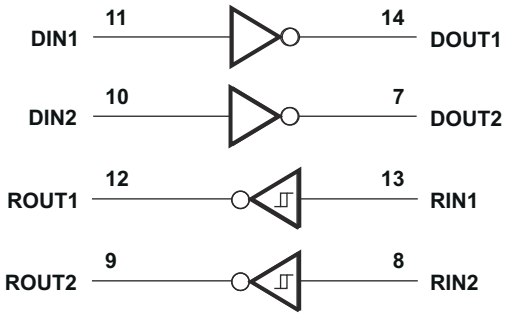


图 6-1. Logic Diagram (Positive Logic)

7 Application and Implementation

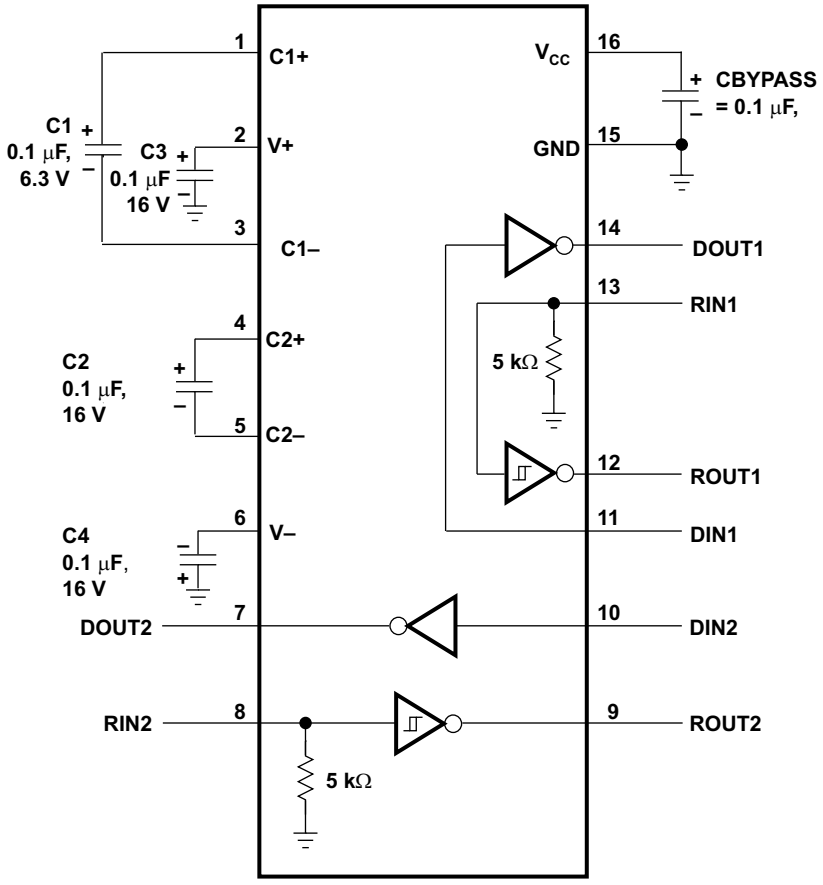
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

For proper operation, add capacitors as shown in 图 7-1. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

7.2 Typical Application



A. C3 can be connected to V_{CC} or GND.
B. Resistor values shown are nominal.
C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

图 7-1. Typical Operating Circuit and Capacitor Values

7.2.1 Design Requirements

- V_{CC} minimum is 4.5V and maximum is 5.5V.
- Maximum recommended bit rate is 120kbps.

7.2.2 Detailed Design Procedure

7.2.2.1 Capacitor Selection

The capacitor type used for C1 through C4 is not critical for proper operation. The MAX202 requires 0.1µF capacitors. Capacitors up to 10µF can be used without harm. Ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V – .

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V – .

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

7.2.2.2 ESD Protection

MAX202 devices have standard ESD protection structures incorporated on all pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15kV when powered down.

7.2.2.3 ESD Test Conditions

Stringent ESD testing is performed by TI based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

7.2.2.4 Human-Body Model (HBM)

The HBM of ESD testing is shown in 图 7-2. 图 7-3 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-kΩ resistor.

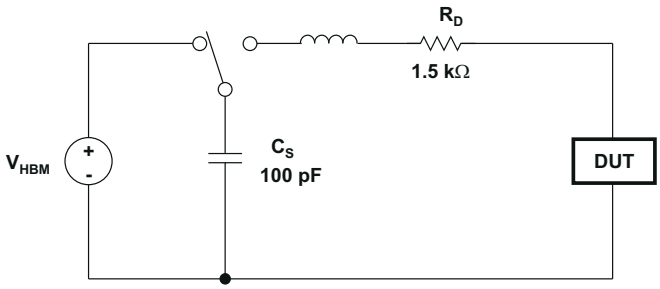


图 7-2. HBM ESD Test Circuit

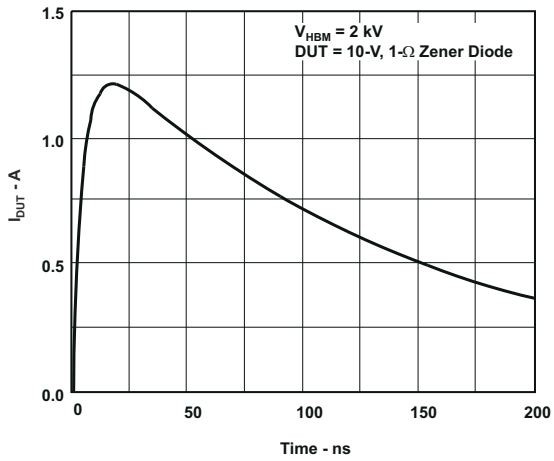
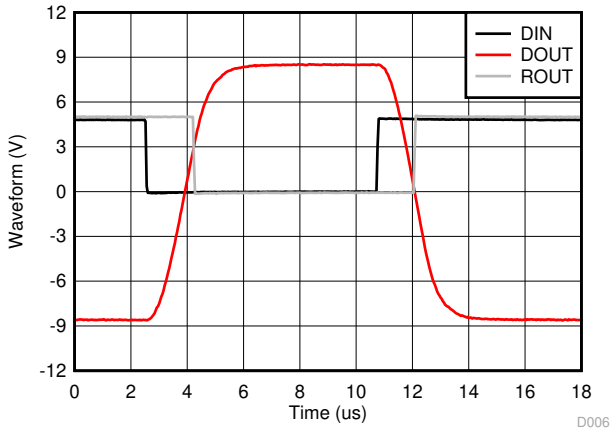


图 7-3. Typical HBM Current Waveform

7.2.3 Application Curve



120 kbit/s, 1-nF load

图 7-4. Driver and Receiver Loopback Signal

7.3 Power Supply Recommendations

The V_{CC} voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} must be between 4.5 V and 5.5 V.

7.4 Layout

7.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. For best ESD performance, make the impedance from MAX202 ground pin to the ground plane of the circuit board as low as possible. Use wide metal and multiple vias on both sides of ground pin.

7.4.2 Layout Example

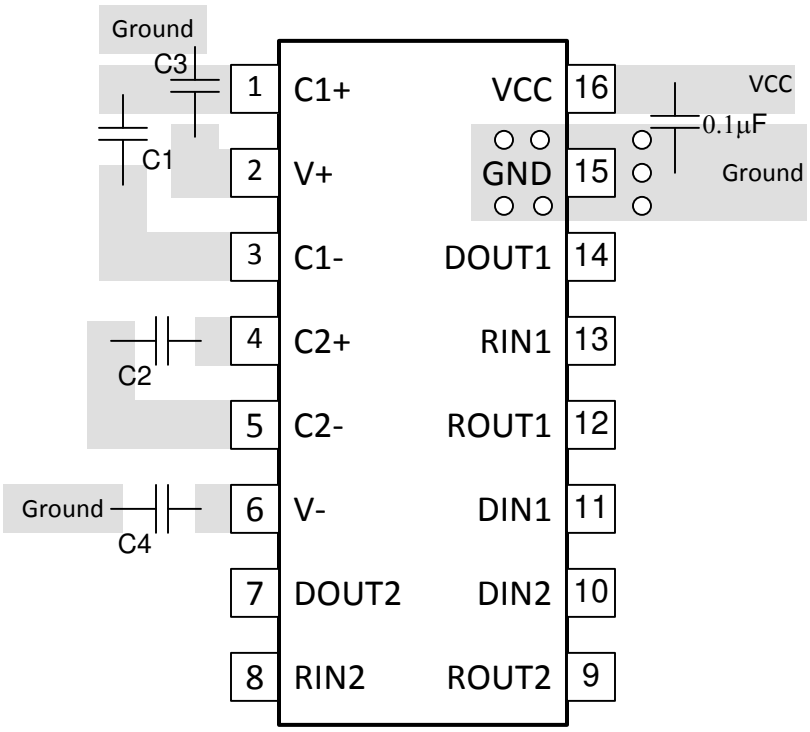


图 7-5. MAX202 Circuit Board Layout

8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (September 2016) to Revision G (February 2024)	Page
• 更改了 *封装信息* 表	1
• Changed values in the *Thermal Information* table	4

Changes from Revision E (April 2007) to Revision F (September 2016)	Page
• 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实现* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分	1
• 删除了 *订购信息* 表；请参阅数据表末尾的 POA	1
• Changed values in the *Thermal Information* table to align with JEDEC standards	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX202CD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	MAX202C	
MAX202CDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	MAX202C	
MAX202CDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70	MAX202C	
MAX202CPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	MA202C	
MAX202CPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	MA202C	
MAX202ID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	MAX202I	
MAX202IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IDRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85	MAX202I	
MAX202IDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX202I	Samples
MAX202IPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	MB202I	
MAX202IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB202I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

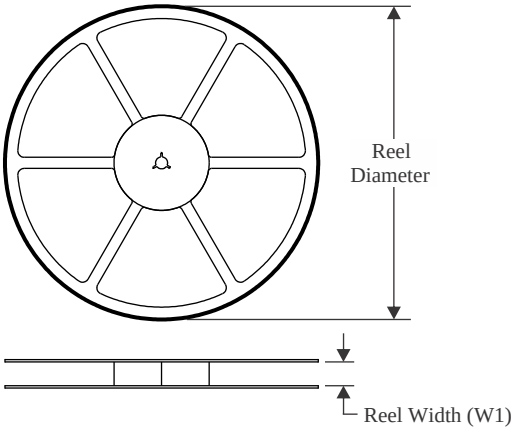
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

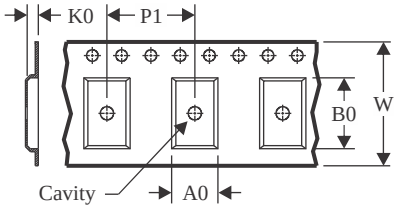
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

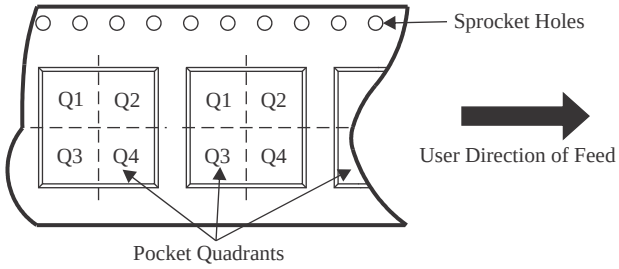


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

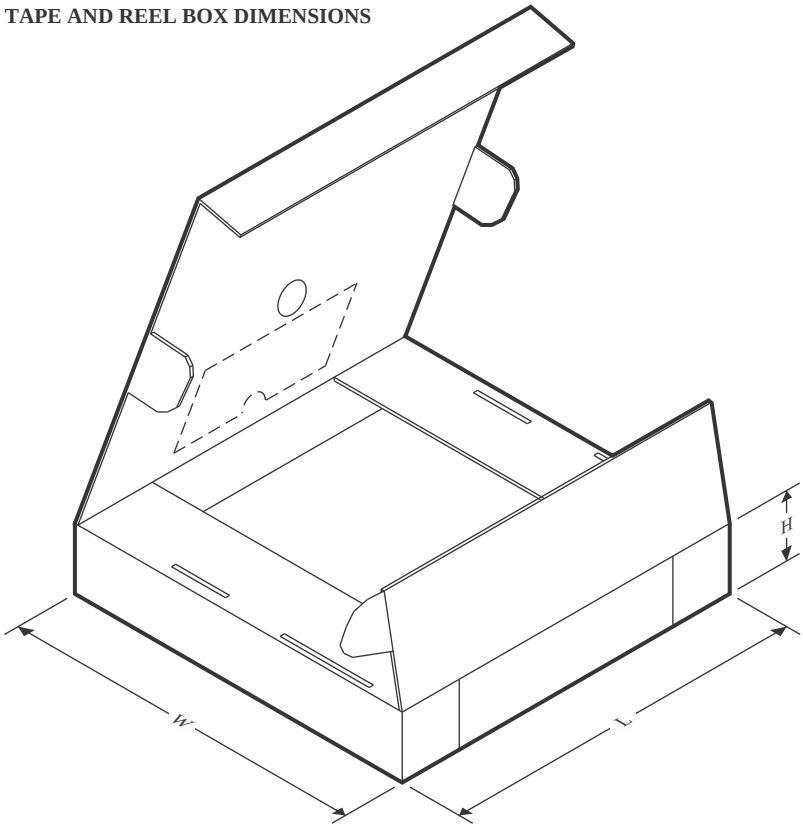
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX202IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX202IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX202IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX202IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX202IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX202IDR	SOIC	D	16	2500	340.5	336.1	32.0
MAX202IDR	SOIC	D	16	2500	353.0	353.0	32.0
MAX202IDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX202IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX202IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

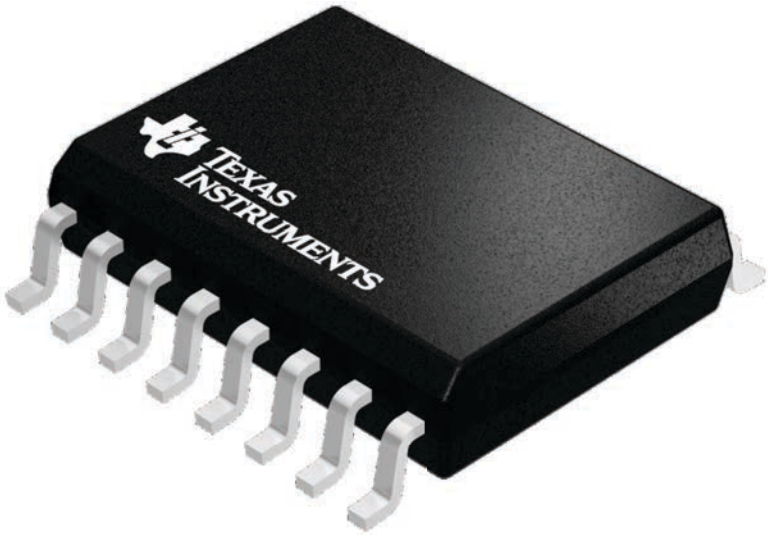
DW 16

SOIC - 2.65 mm max height

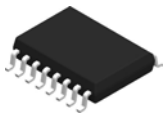
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

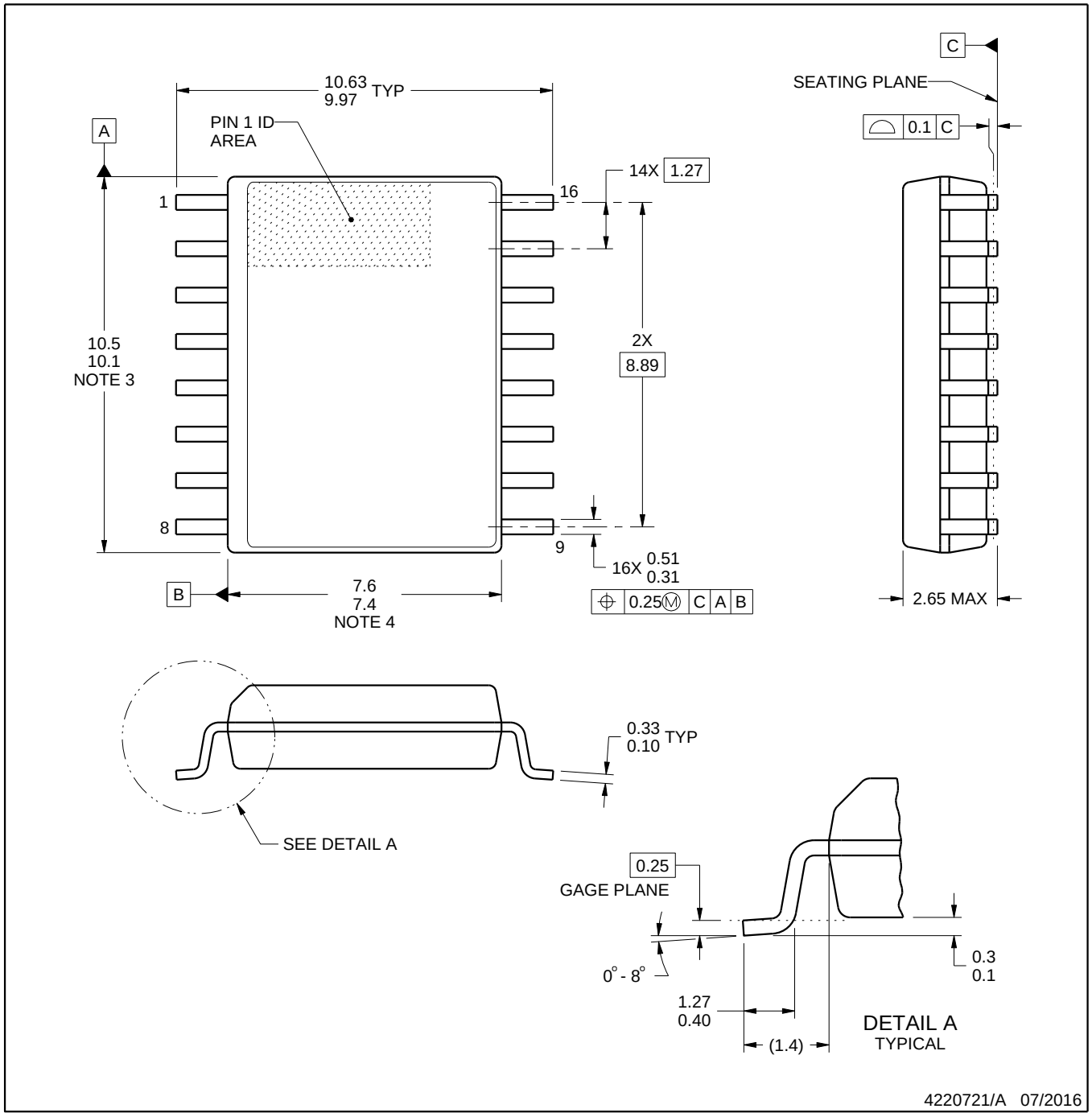


PACKAGE OUTLINE

DW0016A

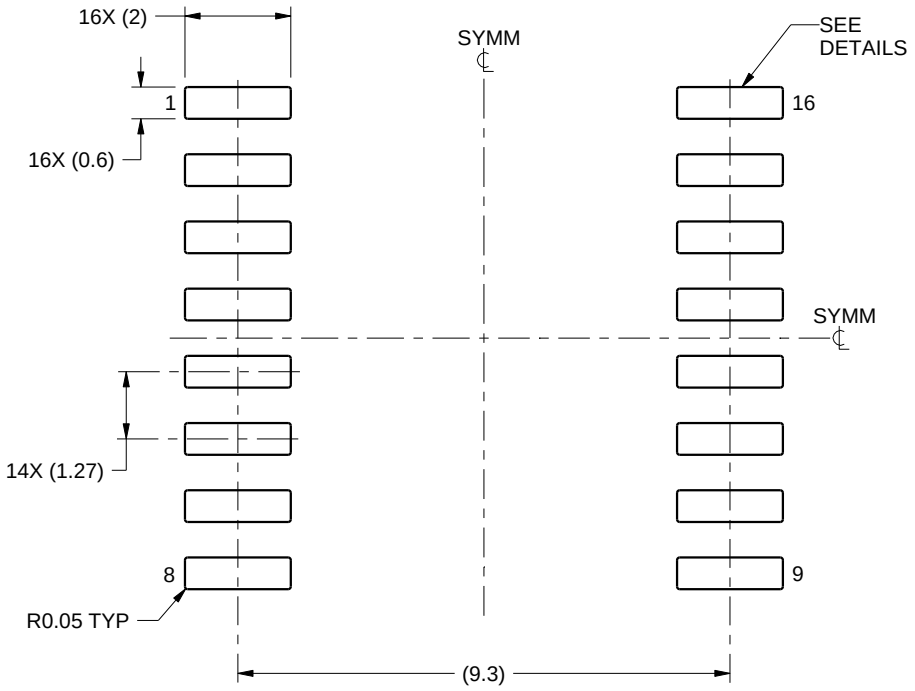
SOIC - 2.65 mm max height

SOIC

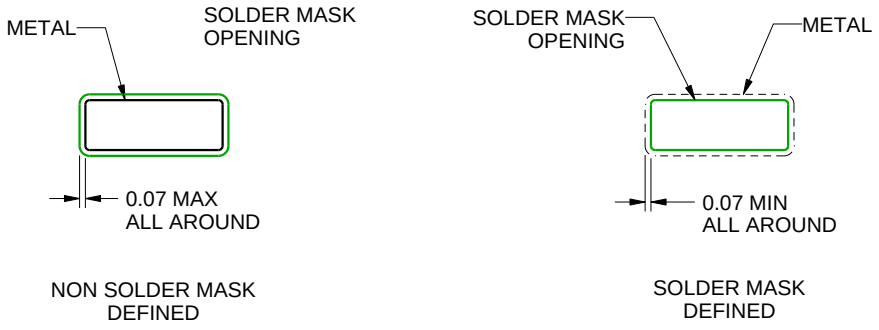


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

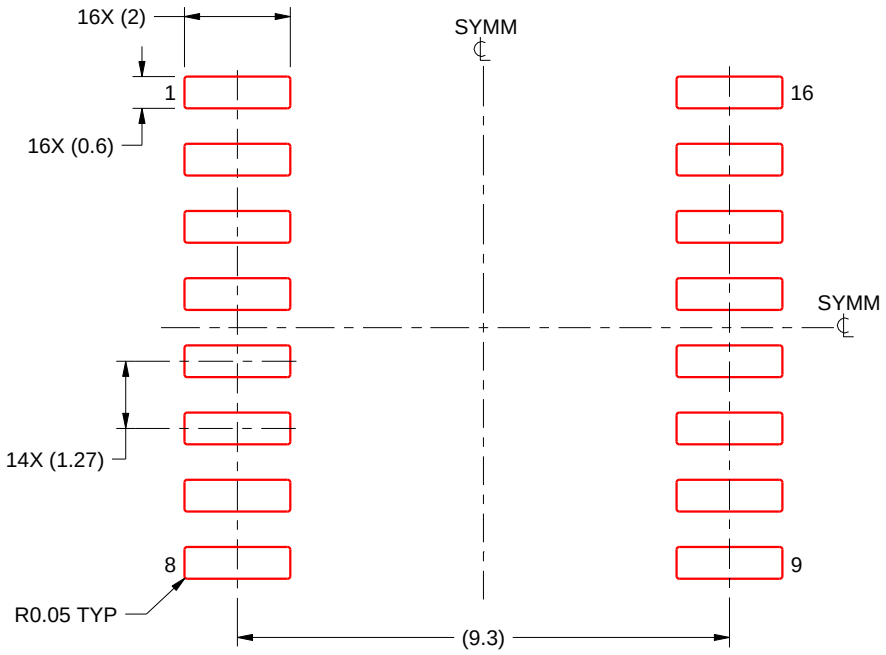


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



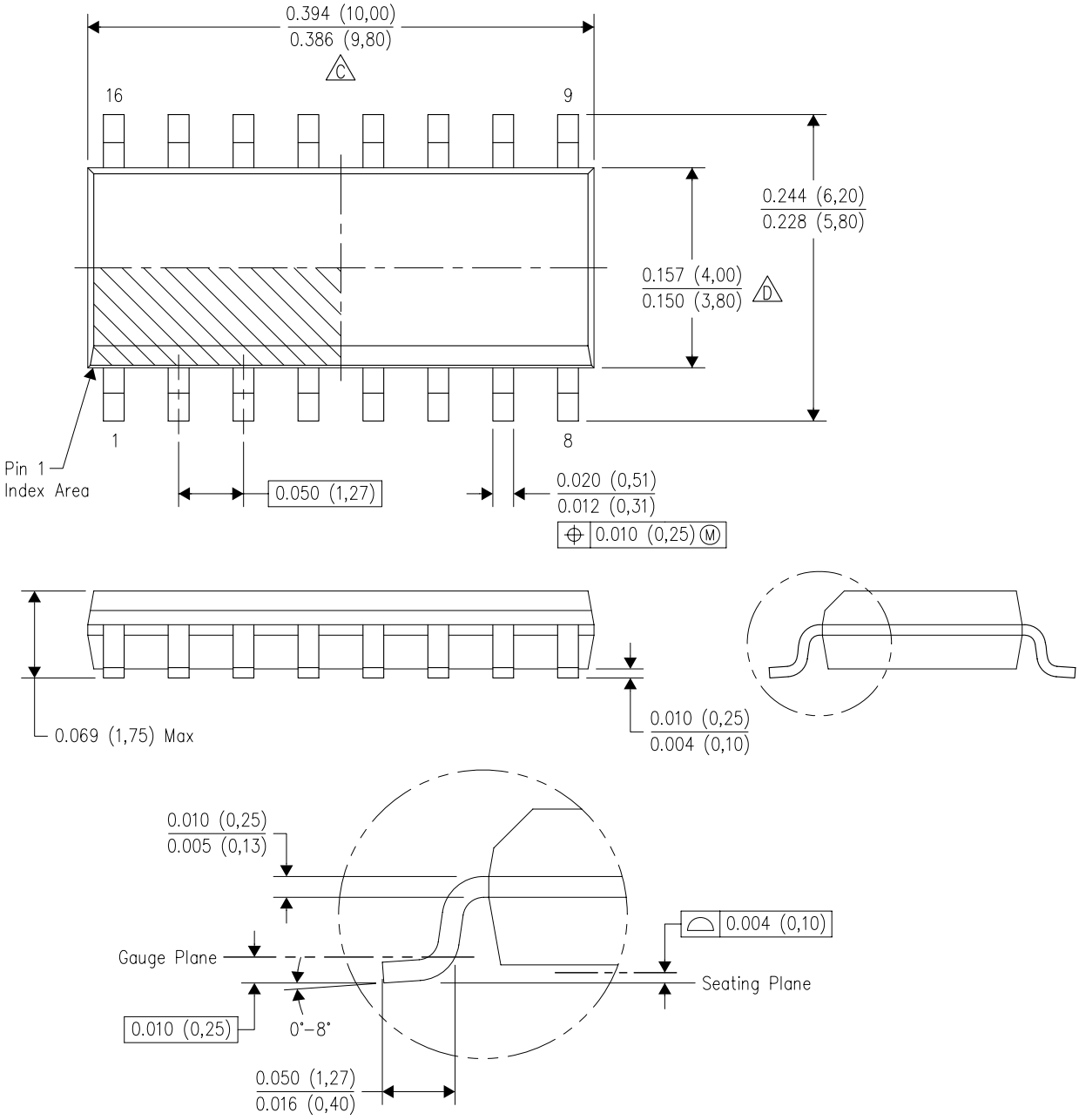
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



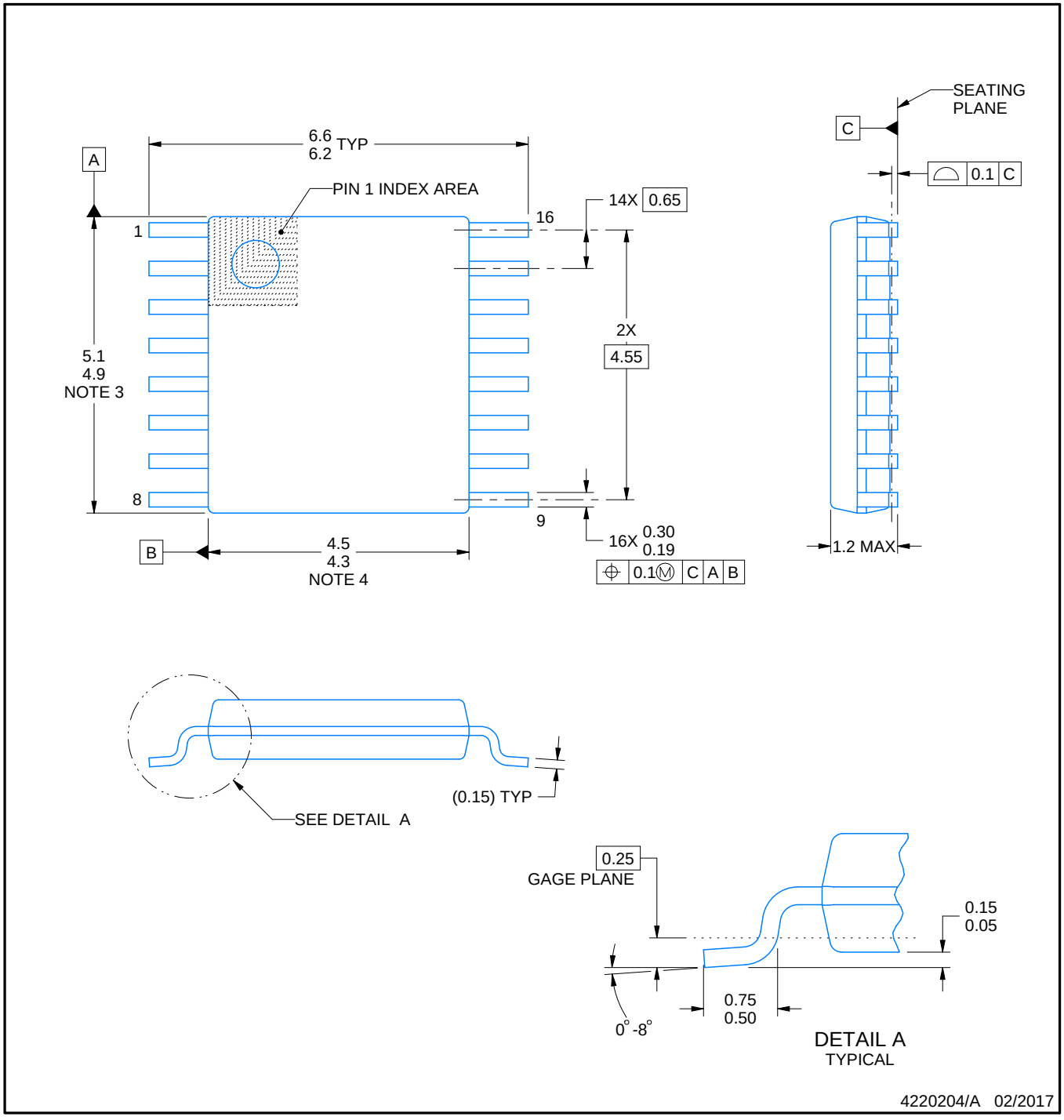
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

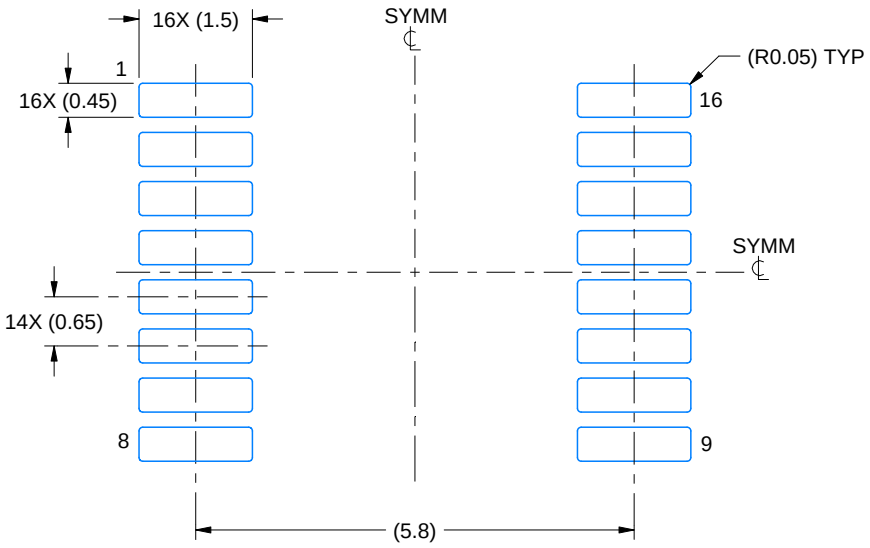
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

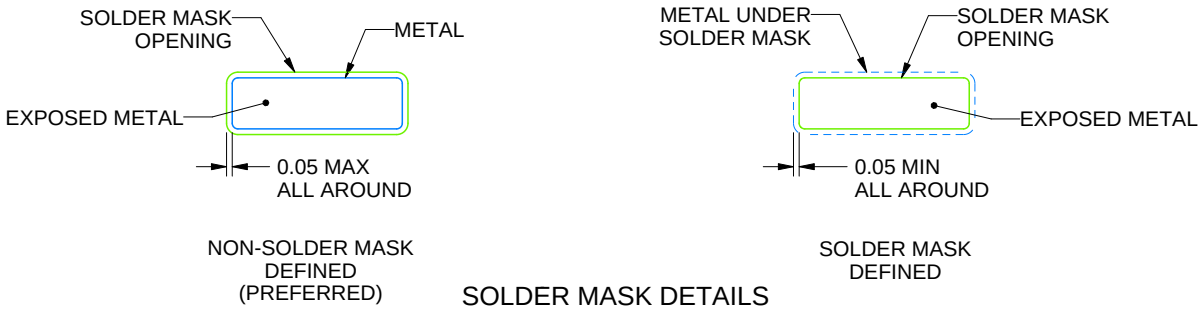


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

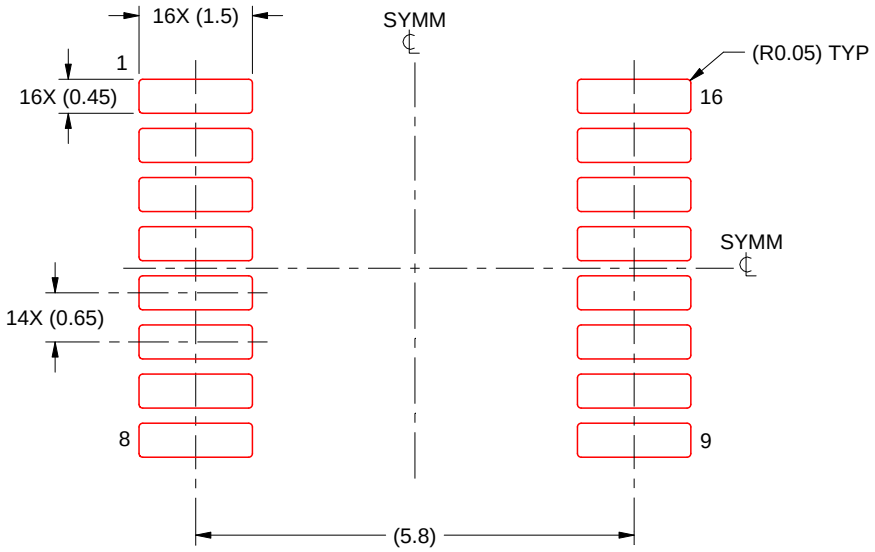


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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