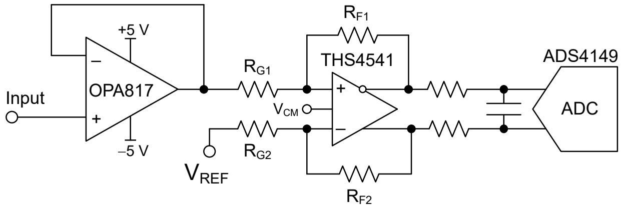
OPA817 800MHz、高精度、单位增益稳定、FET 输入运算放大器

1 特性

- 高带宽：
  - 增益带宽积：400MHz
  - 带宽 (G = 1V/V)：800MHz
  - 大信号带宽 (2V_{PP})：250MHz
  - 压摆率：1000V/µs
- 高精度：
  - 输入失调电压：250μV（最大值）
  - 输入失调电压温漂：3.5μV/°C（最大值）
- 输入电压噪声：4.5nV/√Hz
- 输入偏置电流：2pA
- 低失真（R_L = 100Ω，V_O = 2V_{PP}）：
  - 10MHz 时的 HD2、HD3：－86dBc、－100dBc
- 电源电压范围：6V 至 12.6V
- 电源电流：23.5mA
- 关断电流：55µA
- 性能提升至 OPA656

2 应用

- 高速数据采集 (DAQ)
- 有源探头
- 示波器
- 宽带跨阻放大器 (TIA)
- 晶圆扫描设备
- 光学通信模块
- 光时域反射法 (OTDR)
- 测试和测量前端
- 医学和化学分析器



高输入阻抗数字转换器前端

3 说明

OPA817 是一款单位增益稳定的电压反馈运算放大器、适用于高速、高精度和宽动态范围的应用。

OPA817 具有一个低噪声结型栅场效应管 (JFET) 输入级，该输入级具有 400MHz 的宽增益带宽和 6V 至 12.6V 的电源电压范围。当在高速数字转换器、有源探头及其他测试和测量应用中用作高阻抗缓冲器时，1000V/µs 的快速压摆率可实现大信号宽带宽和低失真。

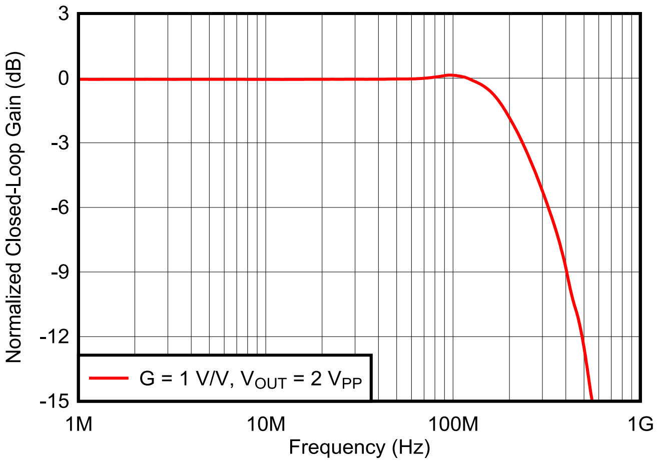
OPA817 提供 ±250μV 的超低输入失调电压和 ±3.5μV/°C 的失调电压温漂。皮安级输入偏置电流和低输入电压噪声 (4.5nV/√Hz) 相结合，使得 OPA817 十分适合在光学测试和通信设备以及医疗和科学仪器中用作宽带跨阻放大器。

OPA817 采用带有裸露散热垫的 8 引脚 WSON 封装。此器件可在 –40°C 至 +105°C 的工业温度范围内正常运行。

封装信息(1)(2)

器件型号	封装	封装尺寸（标称值）
OPA817	DTK（WSON，8）	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。
(2) 请参阅*器件比较表*。



大信号频率响应

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4 Revision History

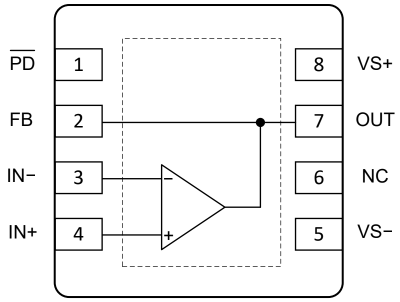
Changes from Revision * (July 2022) to Revision A (December 2022) **Page**

- 将数据表的状态从*预告信息* 更改为*“量产数据”* 1

5 Device Comparison Table

DEVICE	Supply Voltage (V)	BW (MHz)	Input	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	MINIMUM STABLE GAIN (V/V)
OPA817	±6.3	400	FET	1000	4.5	1
OPA818	±6.5	2700	FET	1400	2.2	7
OPA657	±5	1600	FET	700	4.8	7
OPA656	±5	230	FET	290	7	1
OPA659	±6	350	FET	2550	8.9	1
OPA858	±2.5	5500	CMOS	2000	2.5	7
THS4631	±15	210	FET	1000	7	1

6 Pin Configuration and Functions



Not to scale

NC - no internal connection

图 6-1. DTK Package, 8-Pin WSON With Thermal Pad (Top View)

表 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
FB	2	O	Feedback resistor connection (optional)
IN –	3	I	Inverting input
IN+	4	I	Noninverting input
NC	6	—	No connect (no internal connection to die)
OUT	7	O	Output of amplifier
$\overline{PD}$	1	I	Power down (low = amplifier enabled, high = amplifier disabled); internal 2-MΩ pull-up allows floating this pin
VS –	5	P	Negative power supply
VS+	8	P	Positive power supply
Thermal pad		—	Electrically isolated from the die substrate. The thermal pad can be connected to any potential between the device power-supplies, but it is recommended to connect it to a heat-spreading plane, typically ground.

(1) I = input, O = output, P = power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} – V_{S-})		13	V
	Maximum dV_S/dT for supply turn-on and turn-off(2)		1	V/µs
V_I	Input voltage	V_{S-}	V_{S+}	V
V_{ID}	Differential input voltage		$\pm V_S$	V
I_I	Continuous input current		±10	mA
I_O	Continuous output current(3)		±30	mA
	Continuous power dissipation	See Thermal Information		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	−40	105	°C
T_{stg}	Storage temperature	−65	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Staying below this specification ensures that the edge-triggered ESD absorption devices across the supply pins remain off
(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+} – V_{S-}	Total supply voltage	6	10	12.6	V
T_A	Ambient temperature	−40	25	105	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA817	UNIT
		DTK (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	32.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: $V_S = \pm 5$ V

At G = 1 V/V, R_F = 0, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and $T_A \approx$ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 200 mV_{PP}		800		MHz
		V_{OUT} = 200 mV_{PP}, G = 2 V/V		400		
		V_{OUT} = 200 mV_{PP}, G = 5 V/V		100		
		V_{OUT} = 200 mV_{PP}, G = 10 V/V		40		
GBWP	Gain-bandwidth product	V_{OUT} = 200 mV_{PP}, G = 100 V/V		400		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		250		MHz
		V_{OUT} = 4 V_{PP}		140		
	Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}		100		MHz
SR	Slew rate (10% to 90%)	V_{OUT} = 4-V step		1000		V/µs
	Slew rate (10% to 90%)	V_{OUT} = 1-V step, Gain = 2 V/V		750		
t_R, t_F	Rise, fall time	V_{OUT} = 200-mV step		0.7		ns
	Settling time to 0.1%,	V_{OUT} = 2-V step		6		ns
	Overshoot and undershoot	V_{OUT} = 2-V step		8		%
	Output Overdrive recovery time	V_{OUT} = V_{S-} to V_{S+}, G = 2 V/V,		15		ns
HD2	Second-order harmonic distortion	f = 1 MHz, V_{OUT} = 2 V_{PP}		–110		dBc
		f = 10 MHz, V_{OUT} = 2 V_{PP}		–86		
		f = 50 MHz, V_{OUT} = 2 V_{PP}		–76		
		f = 10 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		–97		
HD3	Third-order harmonic distortion	f = 1 MHz, V_{OUT} = 2 V_{PP}		–120		dBc
		f = 10 MHz, V_{OUT} = 2 V_{PP}		–100		
		f = 50 MHz, V_{OUT} = 2 V_{PP}		–68		
		f = 10 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		–102		
e_N	Input voltage noise	f ⩾ 200 kHz		4.5		nV/√Hz
	Voltage noise 1/f corner frequency			2.6		kHz
	Input current noise			18		fA/√Hz
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±1 V	78	85		dB
		T_A = –40°C to +85°C	72			
		T_A = –40°C to +105°C	69			
V_{OS}	Input-referred offset voltage			50	±250	µV
		T_A = –40°C to +85°C			±500	
		T_A = –40°C to +105°C			±600	
	Input offset voltage drift	T_A = –40°C to +85°C		1	±3.5	µV/°C
		T_A = –40°C to +105°C		1	±3.5	
I_B	Input bias current			2	±20	pA
		T_A = –40°C to +85°C			±1000	
		T_A = –40°C to +105°C			±1500	
I_{OS}	Input offset current			1	±20	pA
		T_A = –40°C to +85°C			±500	
		T_A = –40°C to +105°C			±750	

7.5 Electrical Characteristics: V_S = ±5 V (continued)

At G = 1 V/V, R_F = 0, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal feedback trace resistance	Device turned OFF, OUT to FB pin resistance		0.7		Ω
INPUT						
	Most positive input voltage[1]		2.1	2.7		V
		T_A = –40°C to +85°C	2.0			
		T_A = –40°C to +105°C	2.0			
	Most negative input voltage[1]			-3.9	-3.5	V
		T_A = –40°C to +85°C			-3.4	
		T_A = –40°C to +105°C			-3.4	
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V	84	110		dB
		T_A = –40°C to 85°C	83			
		T_A = –40°C to 105°C	82			
	Input impedance common-mode			60 || 2.9		GΩ || pF
	Input capacitance differential mode			0.1		pF
OUTPUT						
V_{OL}	Output voltage, low	no-load		-3.9	-3.6	V
		R_L = 100 Ω		-3.7	-3.4	
		T_A = –40°C to +85°C			-3.3	
		T_A = –40°C to +105°C			-3.2	
V_{OH}	Output voltage, high	no-load	3.7	3.9		V
		R_L = 100 Ω	3.4	3.7		
		T_A = –40°C to +85°C	3.3			
		T_A = –40°C to +105°C,	3.2			
	Linear output drive (sourcing/sinking)	V_{OUT} = ±1 V, ΔV_{OS} < 2 mV	±58	80		mA
		T_A = –40 to 85°C, ΔV_{OS} < 3 mV	±40			
		T_A = –40 to 105°C, ΔV_{OS} < 3 mV	±35			
	Short-circuit current			±100		mA
Z_O	Closed loop output Impedance	f = 100 kHz		0.04		Ω
POWER SUPPLY						
I_Q	Quiescent current			23.5	24.5	mA
		T_A = –40°C to +85°C			24.7	
		T_A = –40°C to +105°C			24.9	
PSRR+	Power-supply rejection ratio	ΔV_{S+} = ±0.5 V	80	100		dB
		T_A = –40°C to +85°C	77			
		T_A = –40°C to +105°C	76			
PSRR-	Power-supply rejection ratio	ΔV_{S-} = ±0.5 V,	80	100		dB
		T_A = –40°C to +85°C	77			
		T_A = –40°C to +105°C	76			

7.5 Electrical Characteristics: V_S = ±5 V (continued)

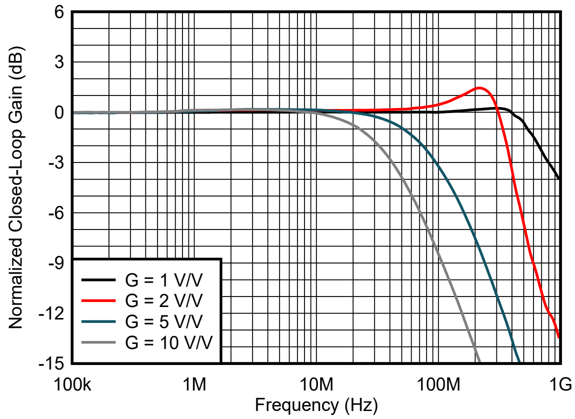
At G = 1 V/V, R_F = 0, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER DOWN						
	Enable voltage threshold	Specified *on* above (V_{S+}) – 1 V			4	V
	Disable voltage threshold	Specified *off* below (V_{S+}) – 3 V	2			V
	Power-down quiescent current	$\overline{PD}$ ≤ (V_{S+}) – 3V		55	100	uA
	Power-down pin bias current in shutdown mode	$\overline{PD}$ = 0 V to (V_{S+}) – 3 V		9	12	uA
	Power-down pin bias current in active mode	$\overline{PD}$ = (V_{S+}) – 1 V to (V_{S+})		0.5	1	uA
	Turn-on time delay	Time from $\overline{PD}$ voltage exceeds threshold to V_{OUT} = 90% of final value, V_{IN} = 1V		0.3		µs
	Turn-off time delay	Time from $\overline{PD}$ voltage reduces below threshold to I_Q = 10% of active mode value		0.1		µs

(1) Input range for CMRR > 77-dB.

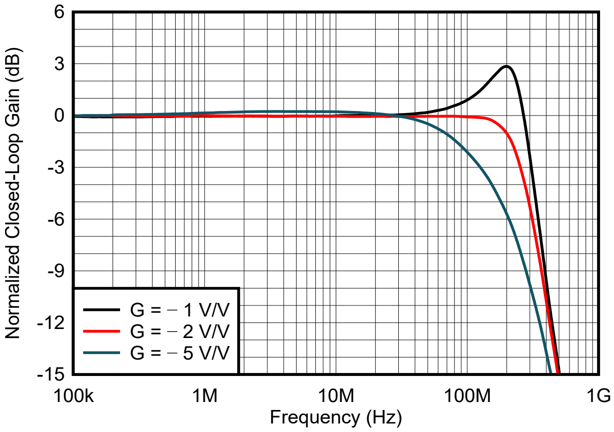
7.6 Typical Characteristics: V_S = ±5 V

At G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted).



V_{OUT} = 200 mV_{PP}

图 7-1. Noninverting Small-Signal Frequency Response



V_{OUT} = 200 mV_{PP}

图 7-2. Inverting Small-Signal Frequency Response

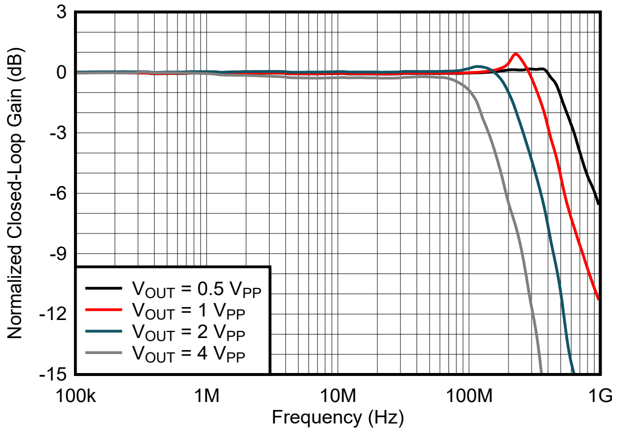


图 7-3. Noninverting Large-Signal Frequency Response

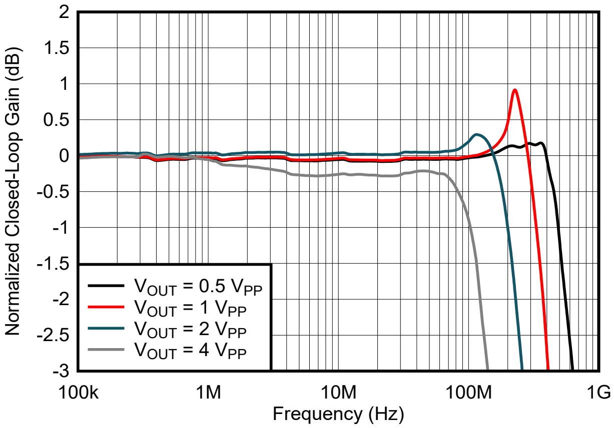
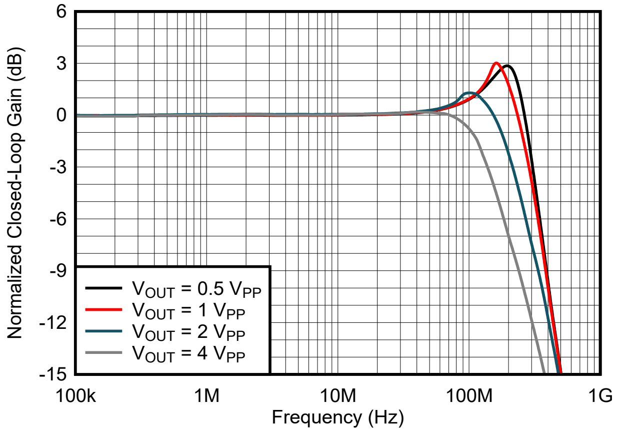
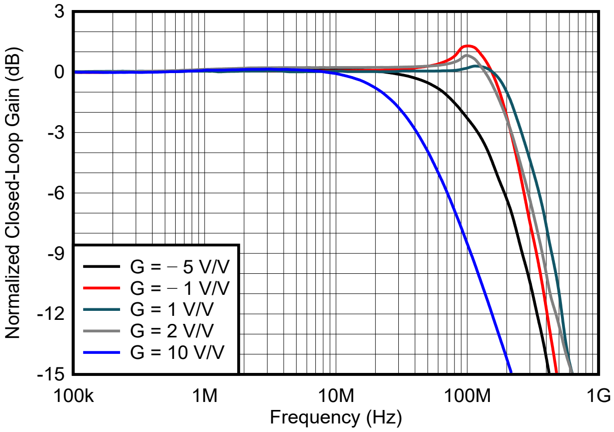


图 7-4. Gain Flatness vs Frequency



G = - 1 V/V

图 7-5. Inverting Large-Signal Frequency Response

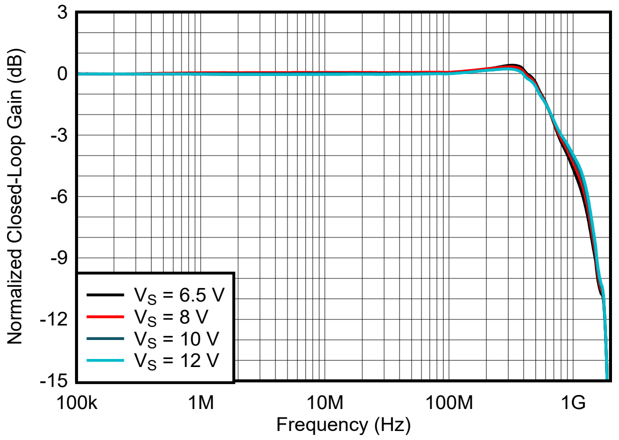


V_{OUT} = 2 V_{PP}

图 7-6. Large-Signal Frequency Response Over Gain

7.6 Typical Characteristics: V_S = ±5 V (continued)

At G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted).



V_{OUT} = 200 mV_{PP}

图 7-7. Noninverting Small-Signal Frequency Response Over Supply

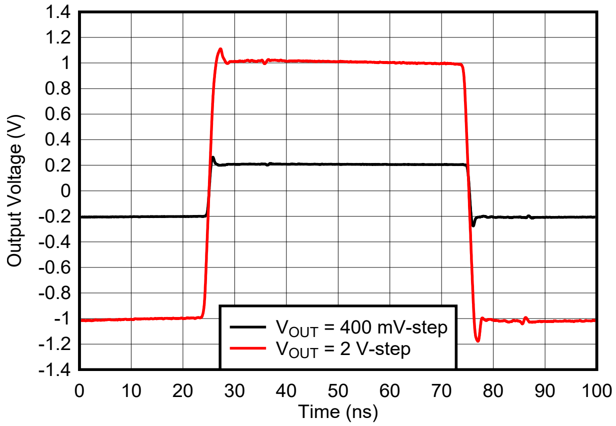
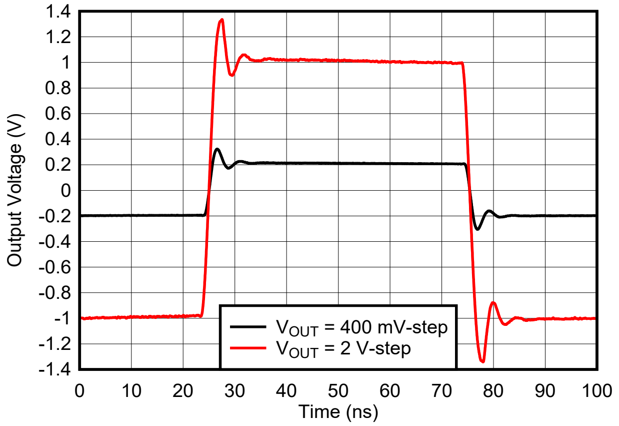
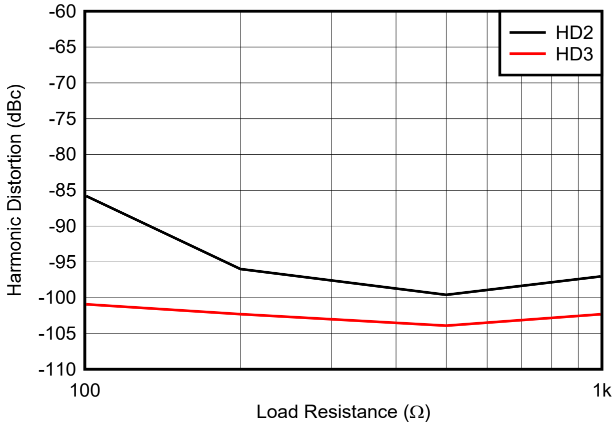


图 7-8. Noninverting Large-Signal Pulse Response



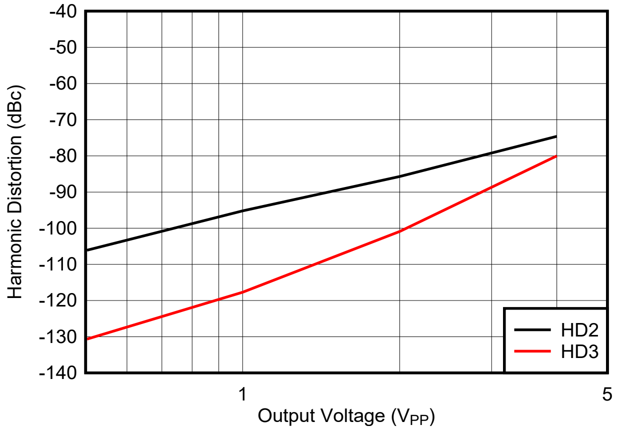
G = - 1 V/V

图 7-9. Inverting Large-Signal Pulse Response



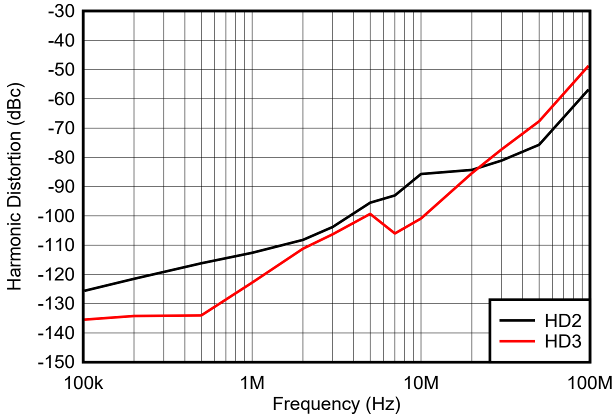
f = 10 MHz V_{OUT} = 2 V_{PP}

图 7-10. Harmonic Distortion vs Load Resistance



f = 10 MHz

图 7-11. Harmonic Distortion vs Output Voltage

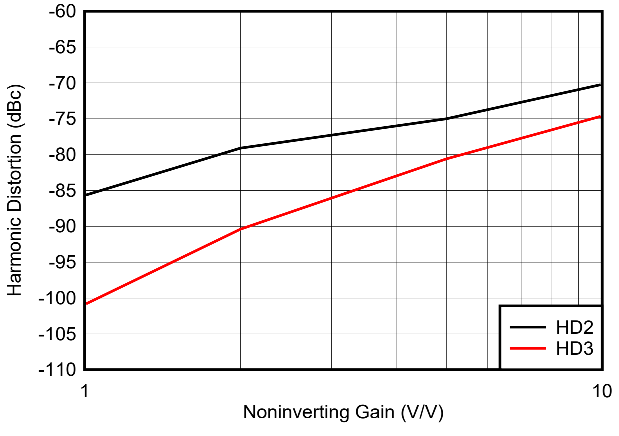


V_{OUT} = 2 V_{PP}

图 7-12. Harmonic Distortion vs Frequency

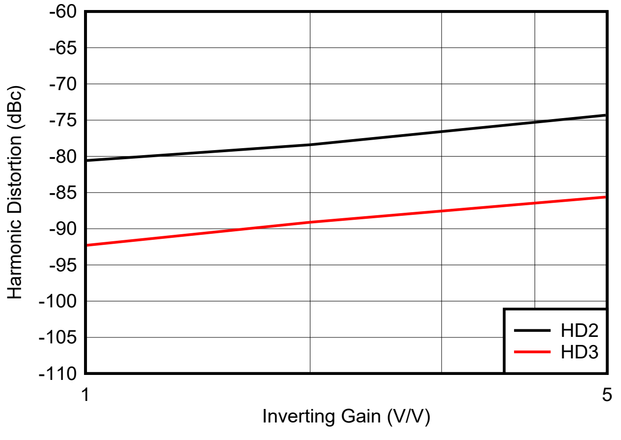
7.6 Typical Characteristics: V_S = ±5 V (continued)

At G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted).



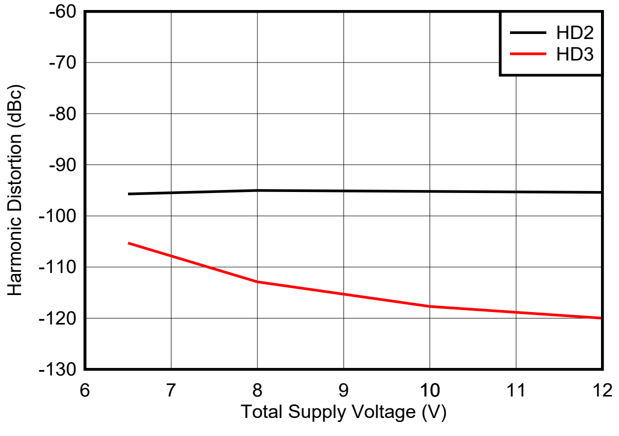
f = 10 MHz V_{OUT} = 2 V_{PP}

图 7-13. Harmonic Distortion vs Noninverting Gain



f = 10 MHz V_{OUT} = 2 V_{PP}

图 7-14. Harmonic Distortion vs Inverting Gain



f = 10 MHz V_{OUT} = 2 V_{PP}

图 7-15. Harmonic Distortion vs Supply Voltage

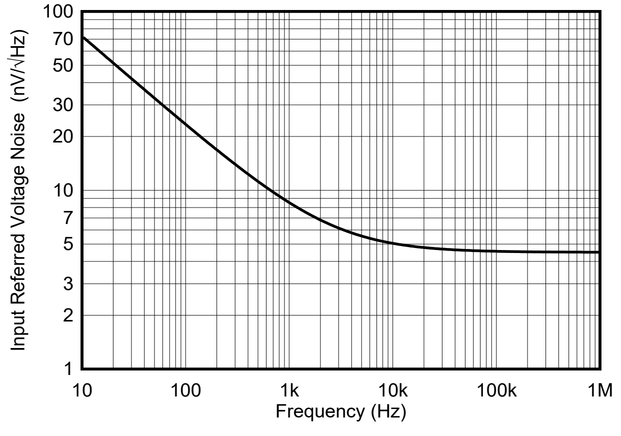


图 7-16. Voltage Noise Density vs Frequency

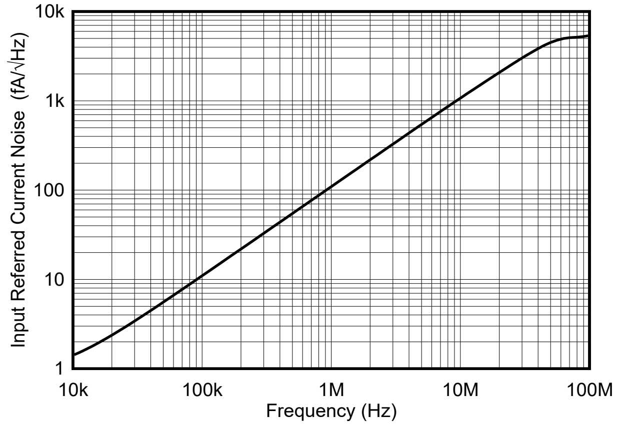


图 7-17. Current Noise Density vs Frequency

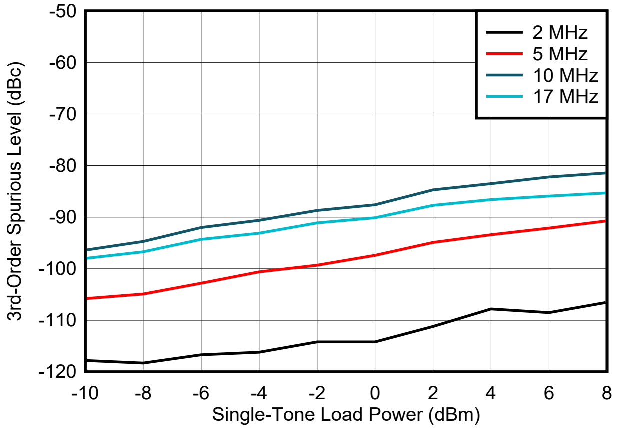


图 7-18. Intermodulation Distortion vs Load Power

7.6 Typical Characteristics: V_S = ±5 V (continued)

At G = 1 V/V, $R_F = 0\ \Omega$, $R_F = 250\ \Omega$ for other gains, $R_L = 100\ \Omega$, input and output referenced to mid-supply, and $T_A \cong 25°C$ (unless otherwise noted).

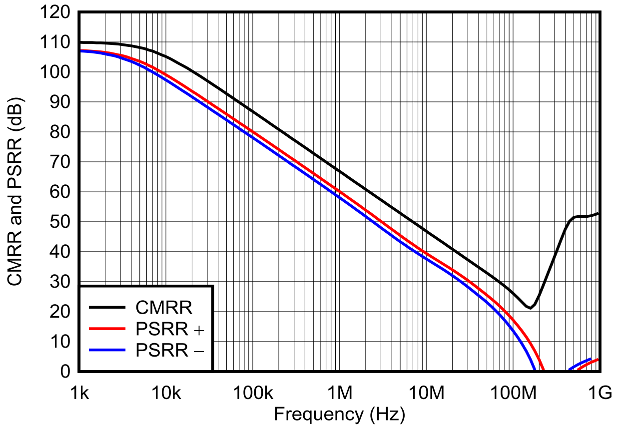


图 7-19. Common-Mode and Power-Supply Rejection Ratio vs Frequency

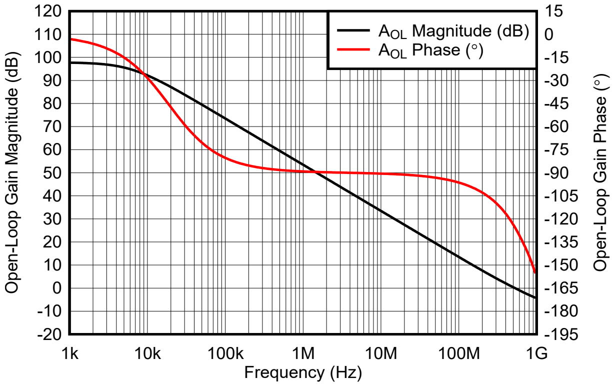
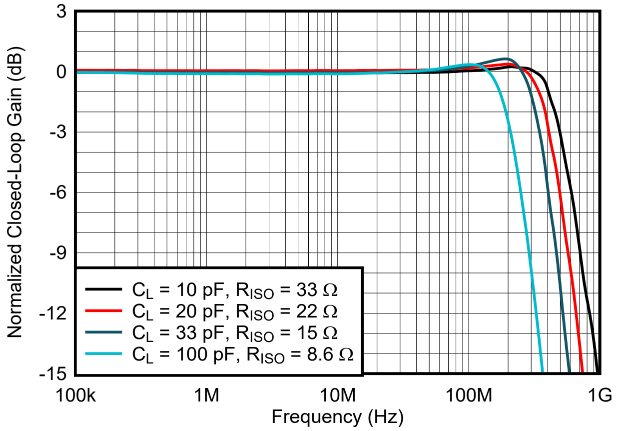


图 7-20. Open-Loop Gain Magnitude and Phase vs Frequency



V_{OUT} = 200 mV_{PP}

图 7-21. Frequency Response vs Capacitive Load

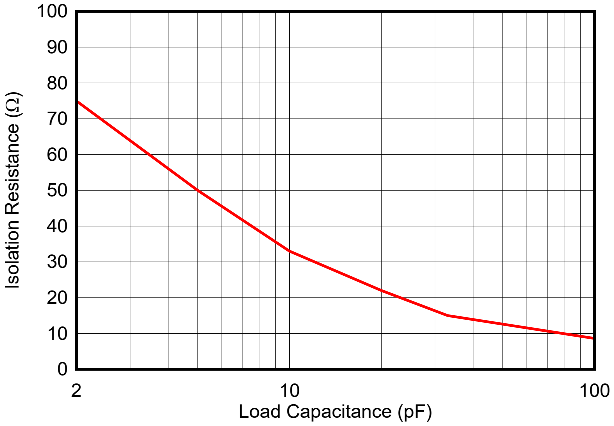


图 7-22. Recommended Isolation Resistor vs Capacitive Load

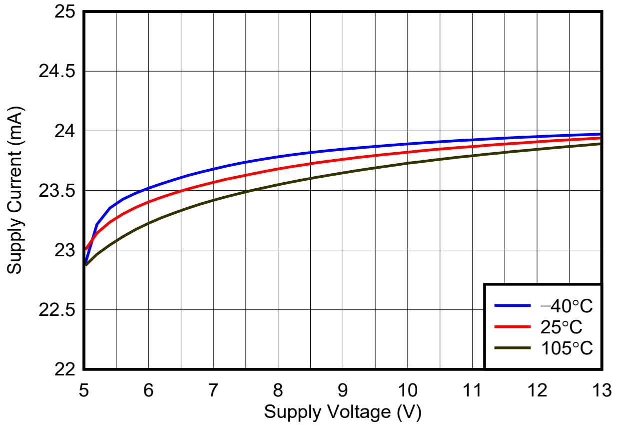


图 7-23. Quiescent Current vs Voltage Supply Over Temperature

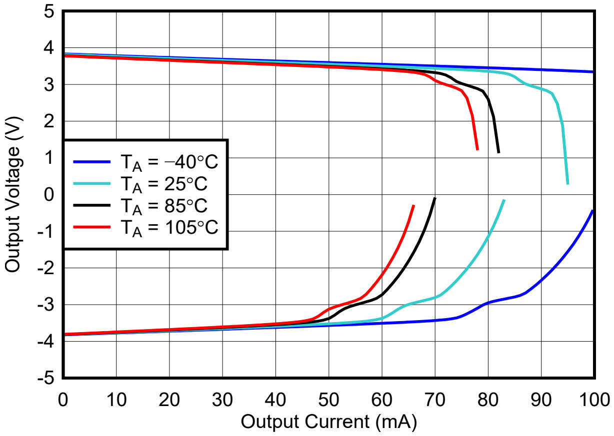
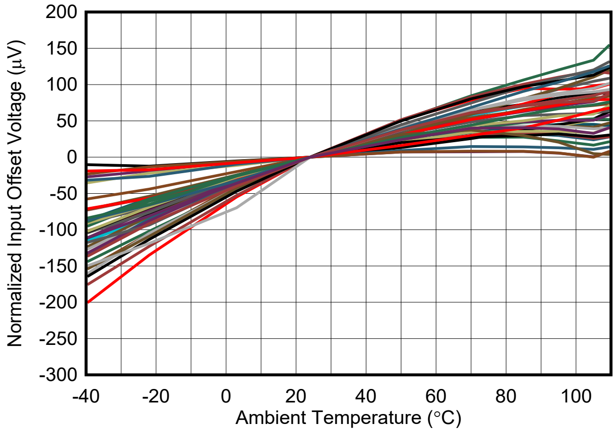


图 7-24. Output Voltage vs Output Current Over Temperature

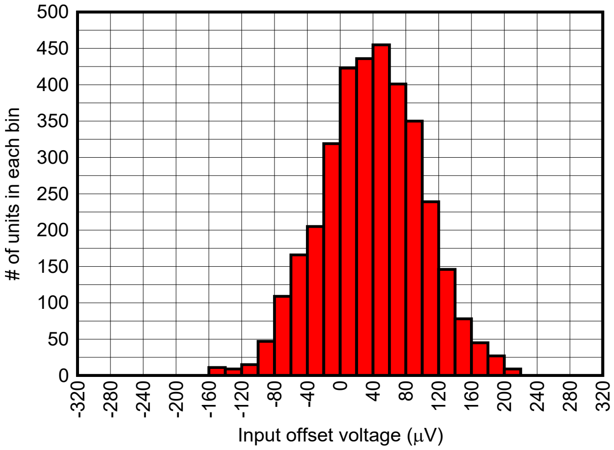
7.6 Typical Characteristics: V_S = ±5 V (continued)

At G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted).



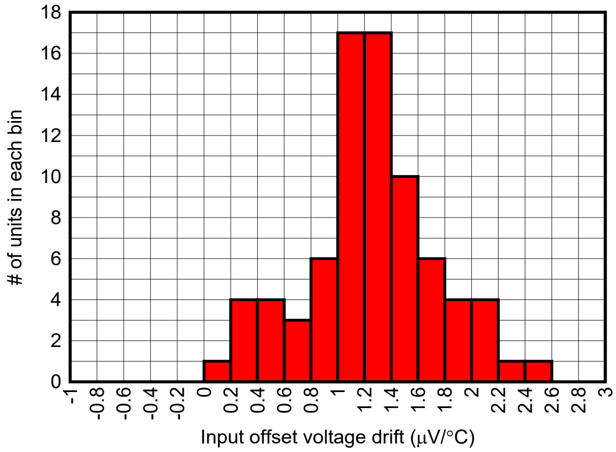
40 units, delta from 25°C

图 7-25. Input Offset Voltage vs Temperature



4000 units, μ = 40 μV, σ = 60 μV

图 7-26. Input Offset Voltage Histogram



40 units, μ = 1.2 μV/°C, σ = 0.5 μV/°C

图 7-27. Input Offset Voltage Drift Histogram

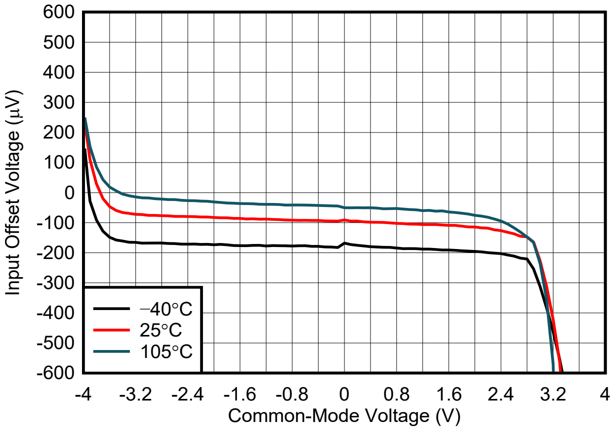
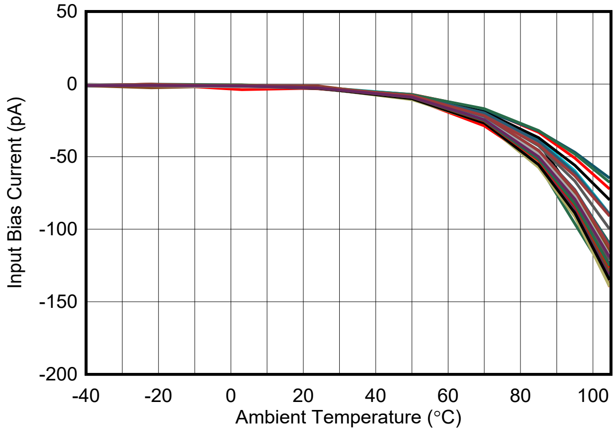
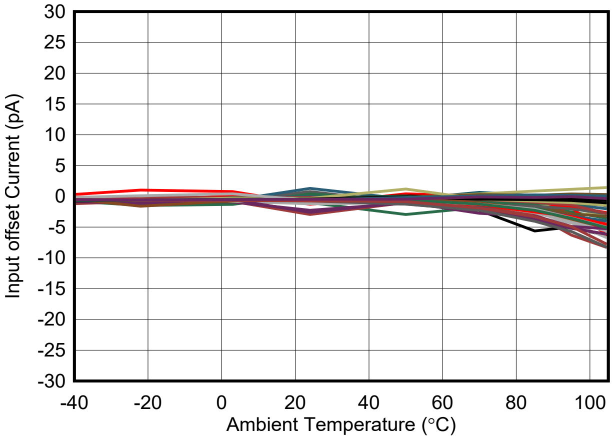


图 7-28. Input Offset Voltage vs Common-Mode Voltage Over Temperature



40 units

图 7-29. Input Bias Current vs Temperature



40 units

图 7-30. Input Offset Current vs Temperature

7.6 Typical Characteristics: V_S = ±5 V (continued)

At G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted).

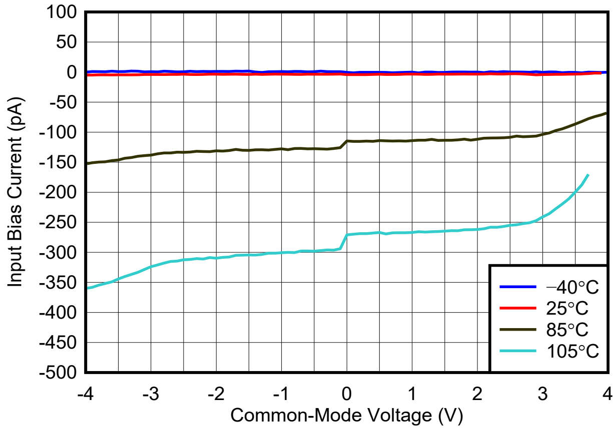
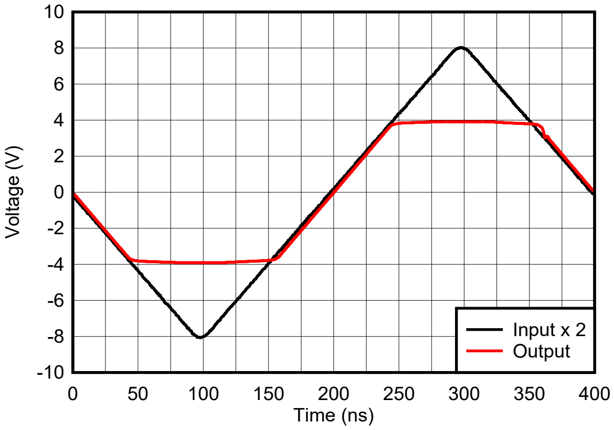
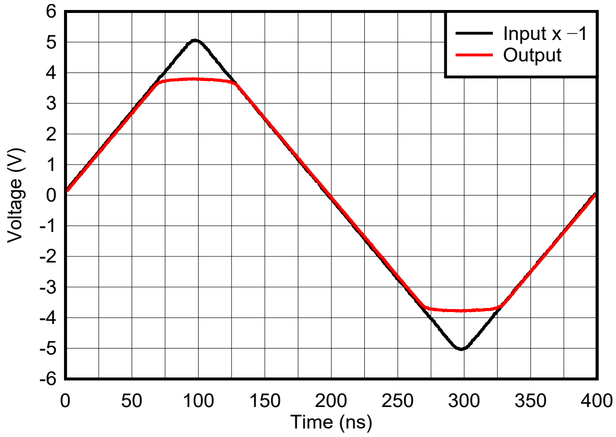


图 7-31. Input Bias Current vs Common-Mode Voltage Over Temperature



G = 2 V/V

图 7-32. Noninverting Output Overdrive Recovery



G = - 1 V/V

图 7-33. Inverting Output Overdrive Recovery

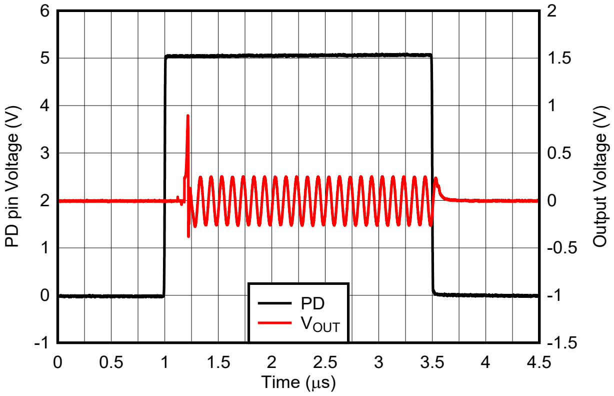


图 7-34. Turn-On and Turn-Off Waveform

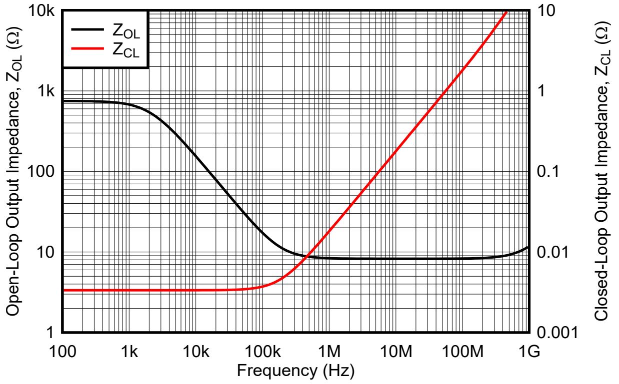


图 7-35. Open-Loop and Closed-Loop Output Impedance vs Frequency

8 Detailed Description

8.1 Overview

The OPA817 is a high voltage, unity gain stable, 400 MHz gain-bandwidth product (GBWP), voltage feedback operational amplifier (op amp) featuring a 4.5 nV/ √ Hz low noise JFET input stage. The low offset voltage (250 μV maximum), offset voltage drift (3.5 μV/°C maximum), and unity gain bandwidth of 800 MHz makes it ideal for high input impedance, high-speed data acquisition front-ends. The high voltage capability combined with 1000 V/µs slew rate enables applications needing wide output swings (9 V_{PP} at V_S = 12 V) for high-frequency signals such as those often found in medical instrumentation, optical front-end, test, and measurement applications. The low noise JFET input with pico-amperes of bias current makes the device attractive in high-gain TIA applications and in test and measurement front-ends. OPA817 also features a power-down mode that disables the core amplifier for power savings.

The OPA817 is built using TI's proprietary high-voltage, high-speed, complementary bipolar SiGe process.

8.2 Functional Block Diagram

The OPA817 is a conventional voltage feedback op amp with two high-impedance inputs and a low-impedance output. 图 8-1 and 图 8-2 shows two standard amplifier configuration examples that are supported for this device. The reference voltage (V_{REF}) level shifts the DC operating point for each configuration, which is typically set to mid-supply in single-supply operation. V_{REF} is typically set to ground in split-supply applications.

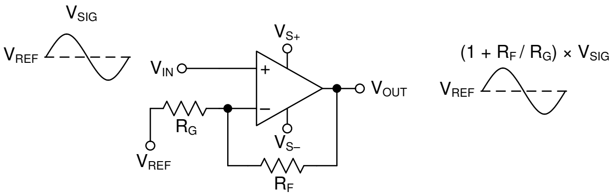


图 8-1. Noninverting Amplifier

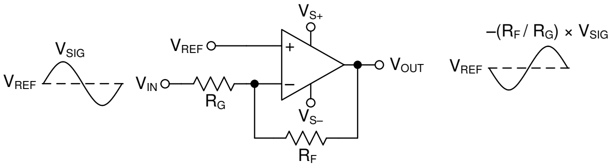


图 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input and ESD Protection

The OPA817 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings*. As 图 8-3 shows, all device pins are protected with internal ESD protection diodes to the power supplies.

The diodes provide moderate protection to input overdrive voltages beyond the supplies as well. The protection diodes can typically support a 10-mA continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA817), current limiting series resistors should be added in series with the two inputs to limit the current. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response. There are no back-to-back ESD diodes between V_{IN+} and V_{IN-}. As a result, the differential input voltage between V_{IN+} and V_{IN-} is entirely absorbed by the V_{GS} of the input JFET differential pair and must not exceed the voltage ratings shown in the *Absolute Maximum Ratings*.

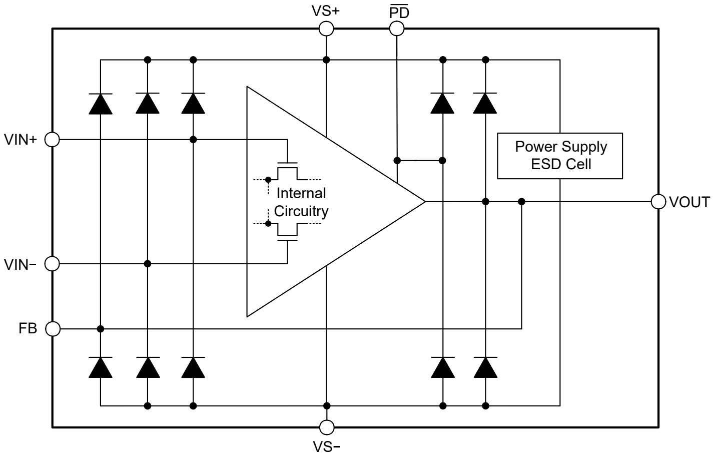


图 8-3. Internal ESD Protection

8.3.2 Feedback Pin

For high speed analog design, minimizing parasitic capacitances and inductances is critical to get the best performance from a high-speed amplifier such as the OPA817. Parasitic capacitance and inductance are especially detrimental in the feedback path and at the inverting input. They result in undesired poles and zeroes in the feedback that could result in reduced phase margin or instability. Techniques used to correct this phase margin reduction often result in reduced application bandwidth. To keep system engineers from making these tradeoff choices and to simplify the PCB layout, OPA817 features an FB pin on the same side as the inverting input pin (IN –). 图 8-4 shows how this feature allows for a very short feedback resistor (R_F) connection between the FB and the IN – pin, which minimizes parasitic capacitance and inductance with minimal PCB design effort. Internally the FB pin is connected to OUT pin through metal routing on the silicon. Due to the fixed metal sizing of this connection, the FB pin has limited current carrying capability. Therefore, the specifications in the *Absolute Maximum Ratings* section must be adhered to for continuous operation. For applications requiring high accuracy, the metal routing resistance from OUT to FB can be considered and added to R_F to set the desired gain. For more information, see 节 7.5.

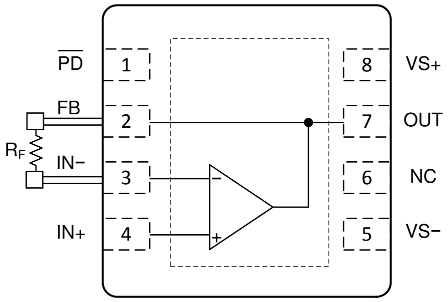
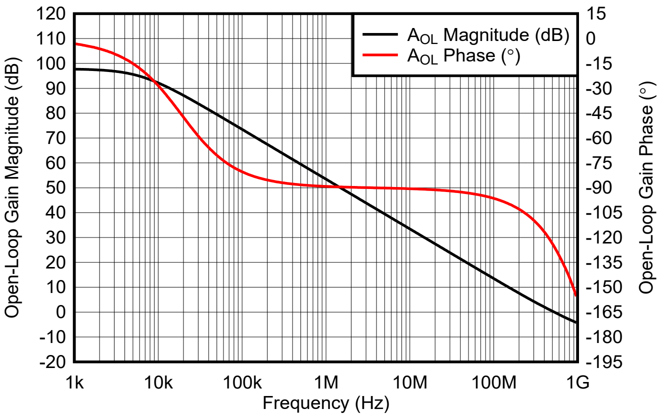


图 8-4. R_F Connection Between FB and IN – Pins

8.3.3 FET-Input Architecture with Wide Gain-Bandwidth Product

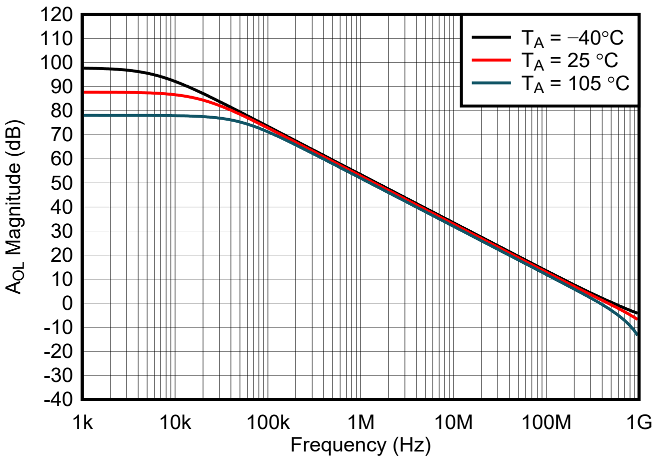
图 8-5 shows the open-loop gain and phase response of the OPA817. The GBWP of an op amp is measured in the 20 dB/decade constant slope region of the A_{OL} magnitude plot. The open-loop gain of 60 dB for the OPA817 is along this 20 dB/decade slope and the corresponding frequency intercept is at 400 kHz. Converting 60 dB to linear units (1000 V/V) and multiplying it with the 400 kHz frequency intercept gives the GBWP of OPA817 as 400 MHz. As can be inferred from the A_{OL} Bode plot, the second pole in the A_{OL} response occurs after A_{OL} magnitude drops below 0 dB (1 V/V). This results in phase change of less than 180° at 0 dB A_{OL} indicating that the amplifier will be stable in a gain of 1 V/V. Amplifiers like OPA817 that are JFET-input, low noise and unity-gain stable can be used as high input impedance buffers and gain stages with minimal degradation in SNR. It has 800 MHz of SSBW in gain of 1V/V configuration with approximately 55° phase margin.

The low input offset voltage and offset voltage drift of OPA817 makes it a very suitable amplifier for high precision, high input impedance, wideband data acquisition system front-ends. As 图 9-2 shows, the system benefits from the low noise JFET input stage with pico-amperes of input bias current to achieve higher precision at 1-MΩ input impedance settings and higher SNR at 50-Ω input impedance setting simultaneously in a typical data acquisition front-end circuit.



R_L = 100 Ω

图 8-5. Open-Loop Gain Magnitude and Phase Vs Frequency



R_L = 100 Ω

图 8-6. Open-Loop Gain Magnitude vs Temperature

8.3.4 Device Functional Modes

8.3.4.1 Power-Down ($\overline{PD}$) Pin

The OPA817 includes a power-down mode for low-power or standby operation and only consumes 55 µA (typical) of current when placed in power-down mode. Low-power systems that are only active for small periods of time benefit from this feature. The OPA817 can transition from low-power mode to active-mode in 300 ns (typical). For power-down pin control thresholds, refer to 节 7.5. An internal pull-up resistor of 2-MΩ provides a weak pull-up to V_{S+} if $\overline{PD}$ is left unconnected. An external 1-nF capacitor to V_{S+} may be used to avoid external noise coupling and false triggering. If the power-down mode is not used in an application, then connect the $\overline{PD}$ pin to V_{S+}.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 Wideband, High-Input Impedance DAQ Front-End

The OPA817 features a unique combination of high GBWP, low-input voltage noise, and the DC precision of a trimmed JFET-input stage to provide a high input impedance for a voltage-feedback amplifier. 图 9-2 shows how its very high GBWP of 400 MHz and high large signal bandwidth of 250 Mhz can be used to either deliver wide signal bandwidths at high gains or to extend the achievable bandwidth or gain in typical high-speed, high-input impedance data acquisition front-end applications. To achieve the full performance of the OPA817, careful attention to the printed circuit board (PCB) layout and component selection is required as discussed in the following sections of this data sheet. OPA817 also features a wider supply range thereby enabling a wider common-mode input range to support higher input signal swings.

图 9-1 shows the noninverting gain of +2 V/V circuit used as the basis for most of the *Typical Characteristics*. Most of the curves were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. As 图 9-1 shows, the 49.9-Ω shunt resistor at the V_{IN} terminal matches the source impedance of the test generator, while the 49.9-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in 图 9-1) while output power specifications are at the matched 50-Ω load. As shown in 图 9-1, the total 100-Ω load at the output combined with the 250-Ω total feedback network load presents the OPA817 with an effective output load of 83.3 Ω for the circuit.

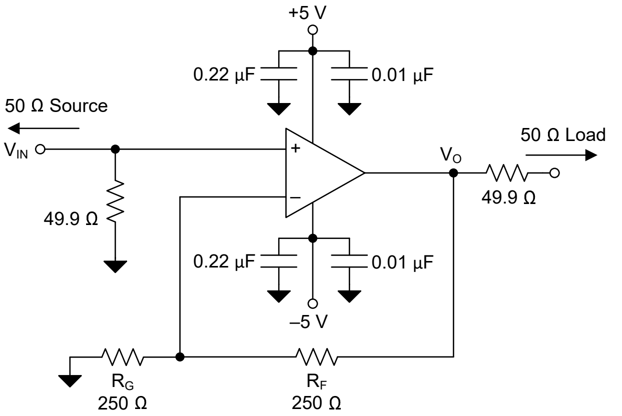


图 9-1. Noninverting G = +2 V/V Configuration and Test Circuit

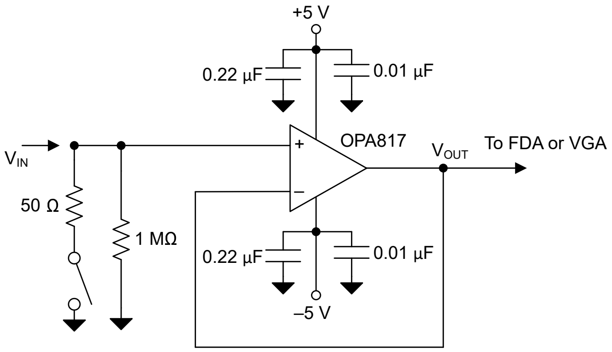


图 9-2. High Input Impedance DAQ Front-End

Voltage-feedback operational amplifiers, unlike current feedback amplifiers, can use a wide range of resistor values to set their gain. As 图 9-1 shows, the parallel combination of $R_F \parallel R_G$ should always be kept to a lower value to retain a controlled frequency response for the noninverting voltage amplifier. In the noninverting configuration, the parallel combination of $R_F \parallel R_G$ will form a pole with the parasitic input capacitance at the inverting node of the OPA817 (including layout parasitic capacitance). For best performance, this pole should be at a frequency greater than the closed loop bandwidth for the OPA817.

9.2 Typical Applications

9.2.1 High Input Impedance, 200 MHz, Digitizer Front-End Amplifier Design

The OPA817 offers a wide large-signal bandwidth, high-slew rate along with high-input impedance making it ideal for data acquisition systems. The trimmed DC precision of the OPA817 enables its use directly as front-end amplifier where low offset and offset voltage drift is needed.

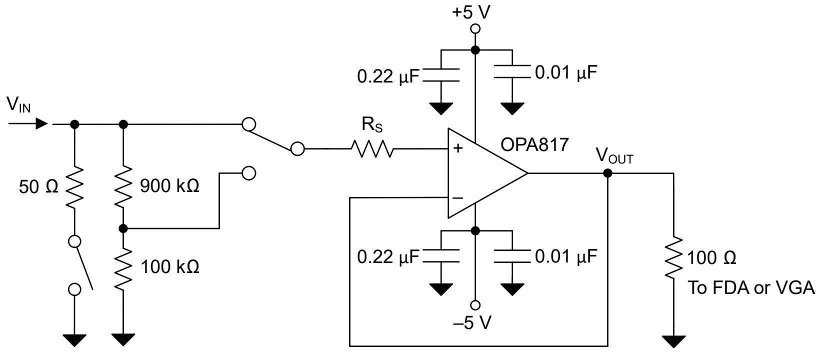


图 9-3. High Input Impedance, 200 MHz, Digitizer Front-End Amplifier

9.2.2 Design Requirements

表 9-1 lists the design requirements for a High Input Impedance, 200 MHz, Digitizer Front-End Amplifier.

表 9-1. Design Requirements

Specification	Value
Input Impedance	1 MΩ / 50 Ω
Input Range (1 MΩ / 50 Ω)	$20\ V_{PP}$ / $2\ V_{PP}$
Offset Drift	3.5 µV/°C maximum
Noise at Highest Resolution (50 Ω Input)	$80\ \mu V_{RMS}$

9.2.3 Detailed Design Procedure

- **Input Impedance:** The JFET-input stage of the OPA817 offers giga ohm's of input impedance and therefore enables the front-end to be terminated with a 1 MΩ resistor while achieving excellent precision. A 50 Ω resistance can also be switched in offering matched termination for high-frequency signals. The OPA817 therefore enables the designer to use both 1 MΩ and 50 Ω termination in the same signal chain.
- **Noise**: The total noise of the front-end amplifier is the function of the voltage and current noise of the OPA817, input termination, and the resistors thermal noise. In 50 Ω mode, the dominant noise source, however, is contributed by the voltage noise of the OPA817 due to its presence across the complete bandwidth. Thus, the total RMS noise of the front-end amplifier shall be approximately equal to the voltage noise of OPA817 over 200 MHz.

  The specified input referred voltage noise of the OPA817 is $4.5\ nV/\sqrt{Hz}$; for more information see 节 7.5. The total integrated RMS noise at the input in a bandwidth of 200 MHz is given by the following equation:

  $$En_{RMS} = 4.5\ nV/\sqrt{Hz} \times \sqrt{(200\ MHz \times 1.57)} = 80\ \mu V_{RMS}. \tag{1}$$

  The Brickwall correction factor of 1.57 is applied assuming the bandwidth will be limited to 200 MHz with a single pole RC-filter before digitizing the signal with the ADC. Detailed calculations can be found on TI Precision Labs – Op Amps: Noise – Spectral Density.

- **Optimizing Overshoot:** The OPA817 features an internal slew-boost circuit to deliver fast rise-time in applications needing high slew rates such as when configured as a transimpedance amplifier. For applications where overshoot needs to be limited, the input slew rates can be limited with introducing a series resistance (R_S) as shown in 图 9-3. The resistance R_S forms a low pass filter with the input capacitance of approximately 2.6 pF at the noninverting pin of the OPA817 limiting the input slew rate to the amplifier. 图 9-4 shows how limiting the input slew rate to the amplifier results in good overshoot performance, and 图 9-5 shows how this achieves a small signal and large signal bandwidth of 200 MHz.

9.2.4 Application Curves

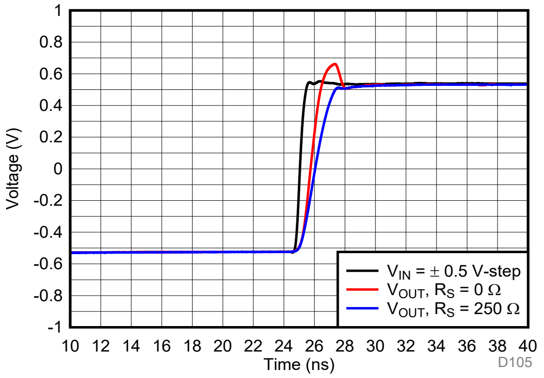


图 9-4. Step Response of Digitizer Front-End

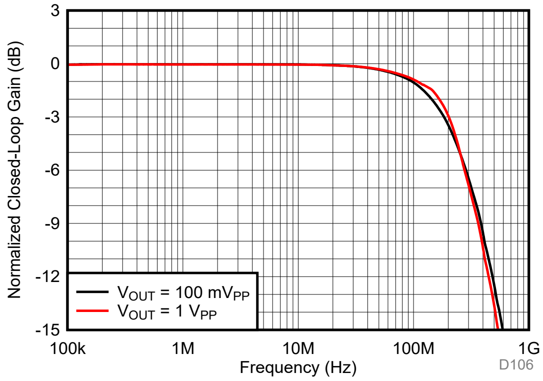


图 9-5. Frequency Response for R_S = 250 Ω

10 Power Supply Recommendations

The OPA817 is intended to operate on supplies ranging from 6 V to 12.6 V. OPA817 supports single-supply, split, balanced, and unbalanced bipolar supplies. When operating at supplies below 8 V, consideration must be given to the input common-mode range of the amplifier. Under these supply conditions, the common-mode must be biased appropriately for linear operation. Thus, the limit to lower supply voltage operation is the usable input voltage range for the JFET-input stage.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA817 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include the following:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability. On the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional bandlimiting. Ground and power metal planes act as one of the plates of a capacitor while the signal trace metal acts as the other separated by PCB dielectric. To reduce this unwanted capacitance, care must be taken to minimize the routing of the feedback network. A plane cutout around and underneath the inverting input pin on all ground and power planes is recommended. Otherwise, ground and power planes should be unbroken elsewhere on the board.

2. **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency decoupling capacitors.** Use high quality, 100-pF to 0.1-μF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies to ensure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2-μF to 6.8-μF) decoupling capacitors, effective at lower frequency, must be used on the supply pins. These can be placed further from the device and are shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components will preserve the high frequency performance of the OPA817.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wirewound type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the inverting input and the output pin, respectively.
   Other network components, such as noninverting input termination resistors, should also be placed close to the package. Even with a low parasitic capacitance at the noninverting input, high external resistor values can create significant time constants that can degrade performance. When OPA817 is configured as a conventional voltage amplifier, keep the resistor values as low as possible and consistent with the load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.
4. **Heat dissipation is important for a high voltage device like OPA817**. For good thermal relief, the thermal pad should be connected to a heat spreading plane that is preferably on the same layer as OPA817 or connected by as many vias as possible, if the plane is on a different layer. It is recommended to have at least one heat spreading plane on the same layer as the OPA817 that makes a direct connection to the thermal pad with wide metal for good thermal conduction when operating at high ambient temperatures. If more than one heat spreading plane is available, then connect them by a number of vias to further improve the thermal conduction.

11.1.1 Thermal Considerations

The OPA817 will not require heatsinking or airflow in most applications. Maximum allowed junction temperature will set the maximum allowed internal power dissipation as described in the following paragraph. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times R_{\theta JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load, but for a grounded resistive load the P_{DL} will be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced bipolar supplies). Under this condition $P_{DL} = V_S{}^2/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

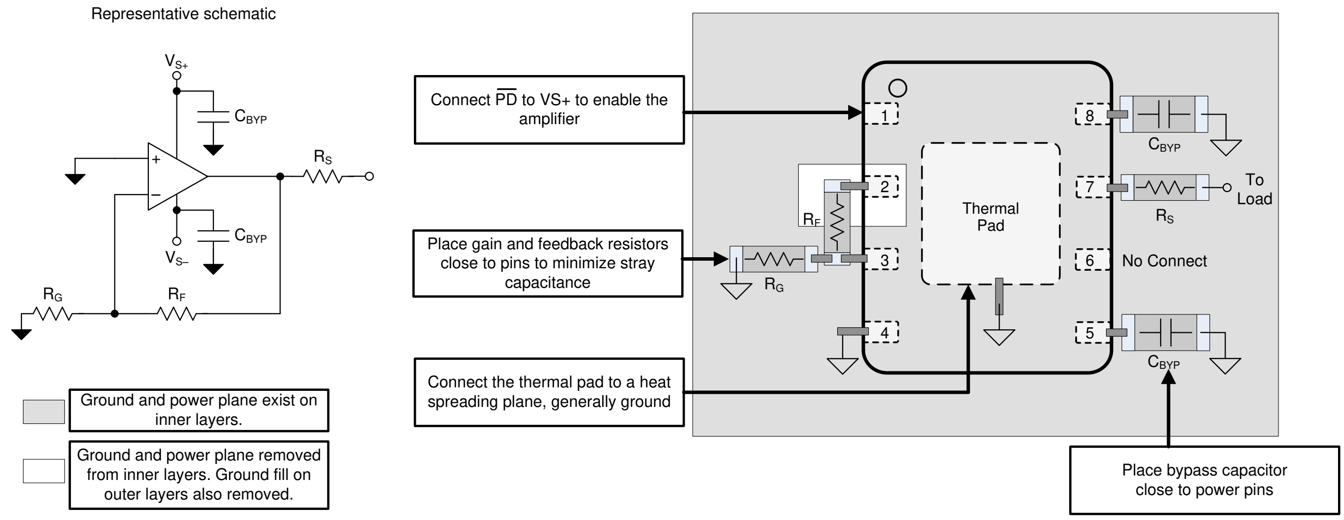
As a worst-case example, compute the maximum T_J using OPA817 in the circuit of 图 9-1 operating at the maximum specified ambient temperature of +105°C and driving a grounded 100-Ω load.

$P_D = 10\ \text{V} \times 23.5\ \text{mA} + 5^2/(4 \times (100\ \Omega \parallel 500\ \Omega)) \cong 310\ \text{mW}$

Maximum $T_J = 105°\text{C} + (0.310\ \text{W} \times 64.9°\text{C/W}) = 125.1°\text{C}$.

All actual applications will be operating at lower internal power and junction temperature.

11.2 Layout Example



Connect PD to VS+ to enable the amplifier

Place gain and feedback resistors close to pins to minimize stray capacitance

Connect the thermal pad to a heat spreading plane, generally ground

Place bypass capacitor close to power pins

▨ Ground and power plane exist on inner layers.

☐ Ground and power plane removed from inner layers. Ground fill on outer layers also removed.

图 11-1. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- Texas Instruments, *Wide Bandwidth Optical Front-end Reference Design*

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA817EVM User's Guide*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *Maximizing the Dynamic Range of Analog TIA Front-End* techincal brief
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA817DTKR	ACTIVE	WSON	DTK	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	817	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

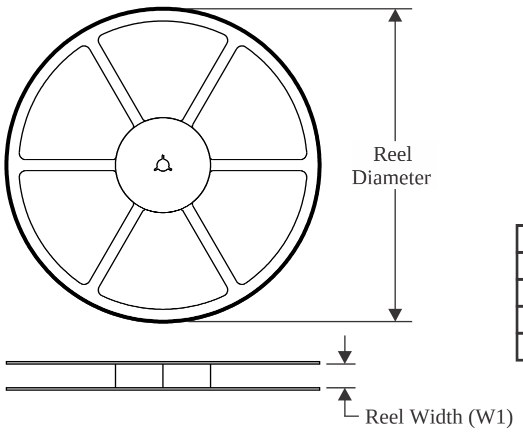
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

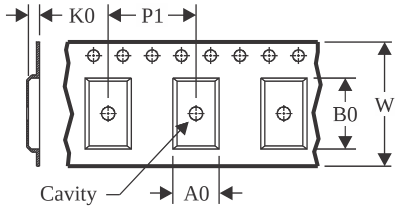
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

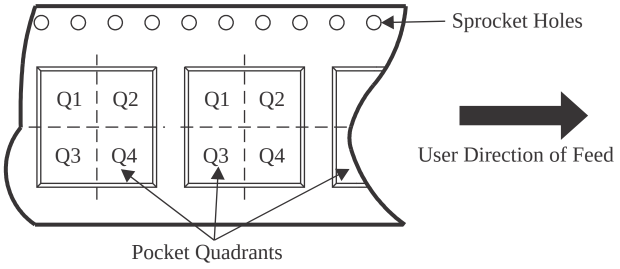


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

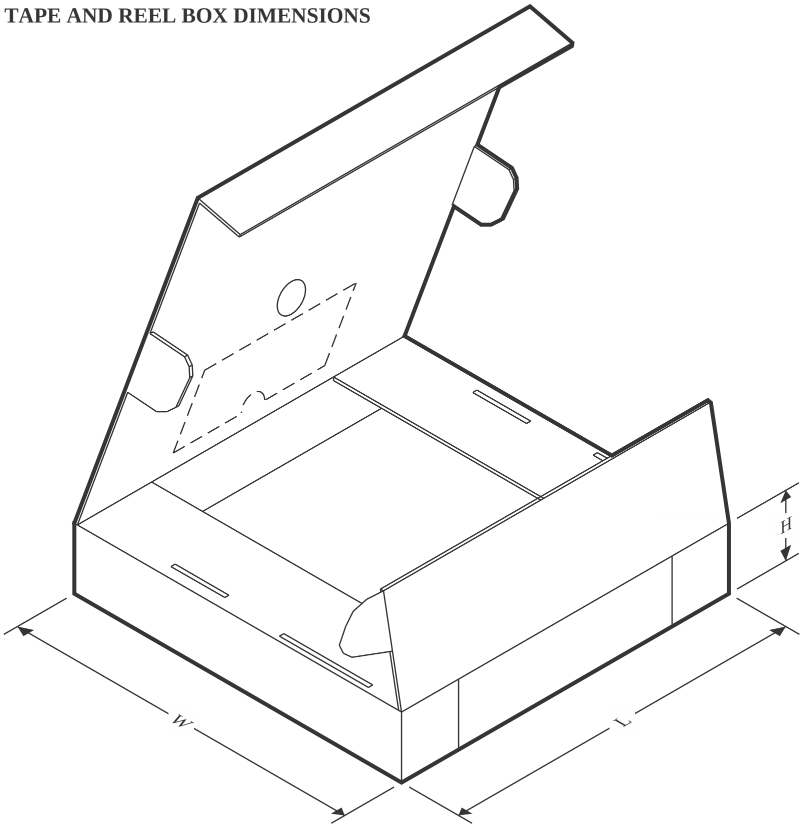
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

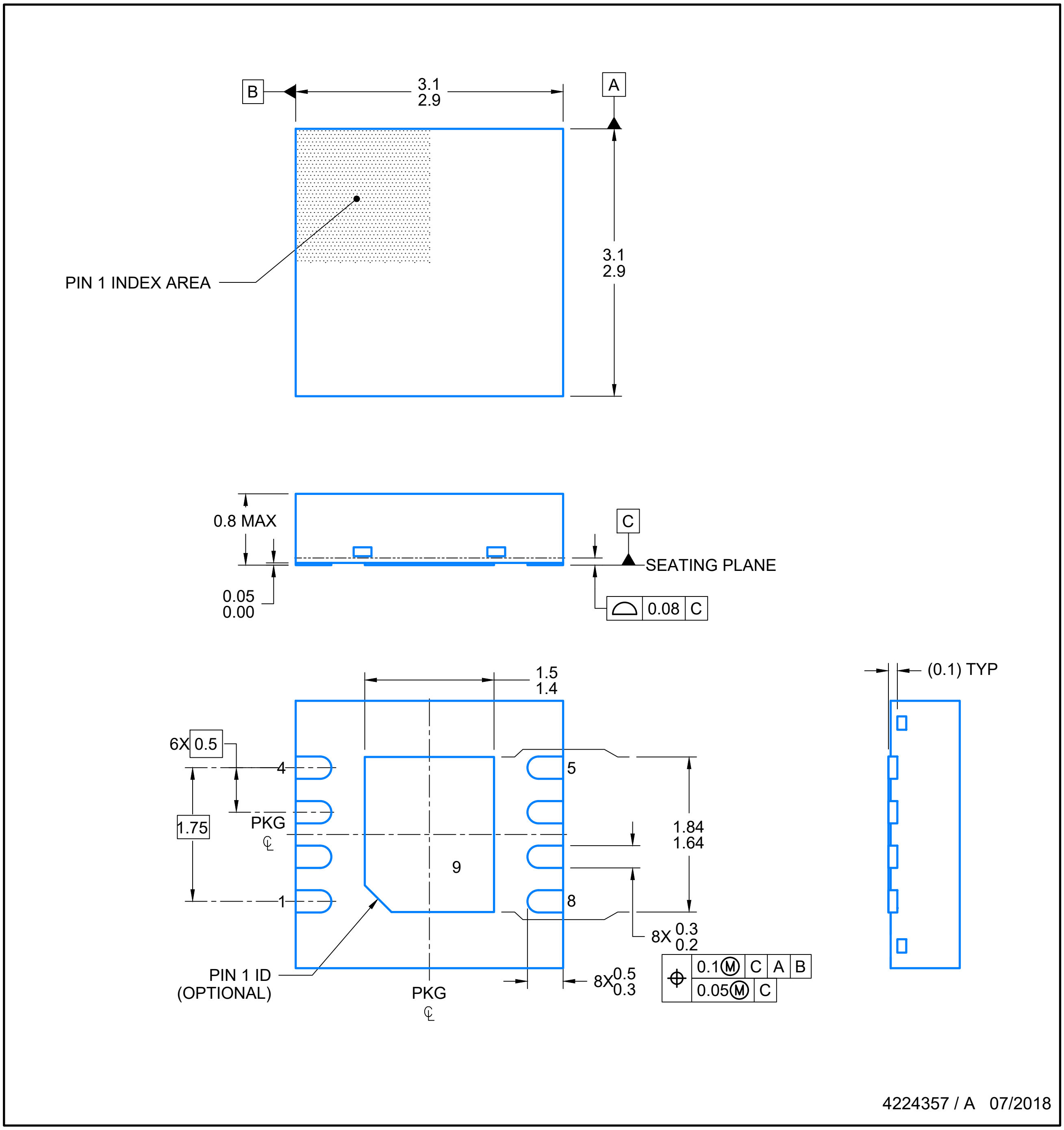
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA817DTKR	WSON	DTK	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA817DTKR	WSON	DTK	8	3000	367.0	367.0	35.0



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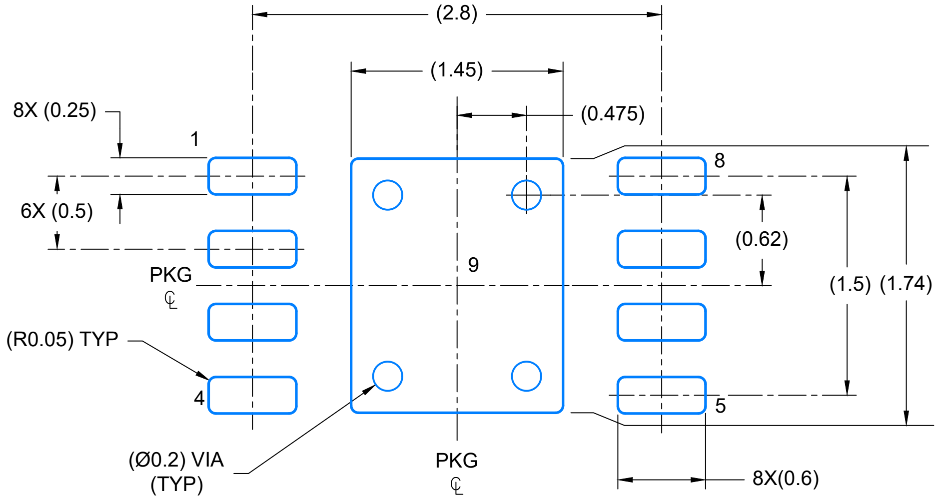
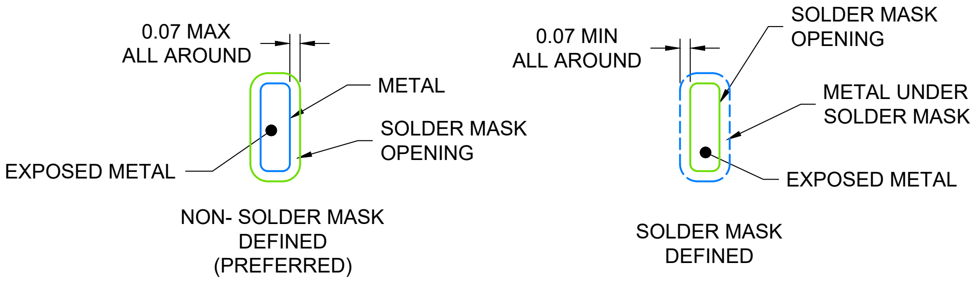
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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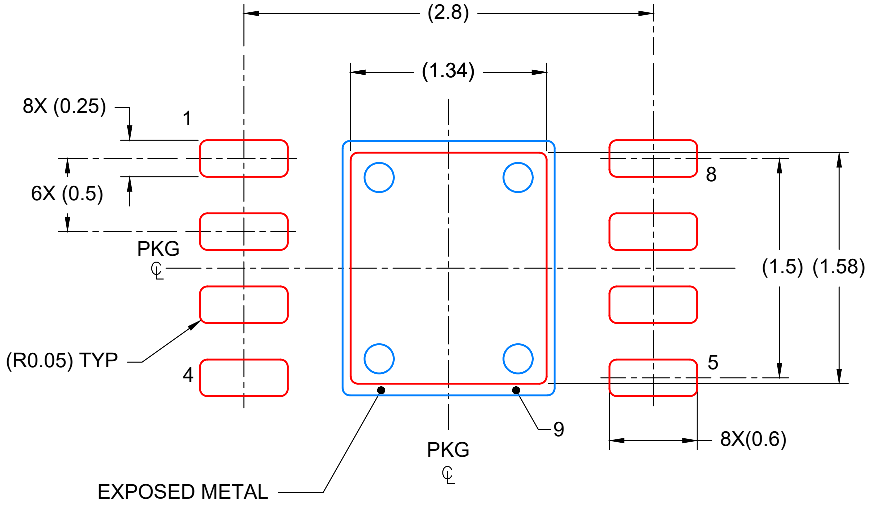
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 9: 84%
SCALE: 20X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

重要声明和免责声明

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