具有扩展共模范围的故障保护 RS-485 收发器

查询样品: **SN65HVD1792-EP**

特性

- 总线引脚故障保护达到 **> ±70V**
- 共模电压范围（**-20V** 至 **25V**），此范围超过 **TIA/EIA 485** 要求的两倍
- 总线 **I/O** 保护
  - **±16kV JEDEC** 人体模型 **(HBM)** 保护
- 减少了高达 **256** 个节点的单位负载
- 针对开路、短路和空闲总线情况下的故障安全接收器
- 低功耗
  - 低待机电源电流，典型值 **1μA**
  - 运行期间 I_{CC}静态电流为 **5mA**
- 加电、断电无毛刺脉冲运行

应用范围

- 设计用于 **RS-485** 和 **RS-422** 网络

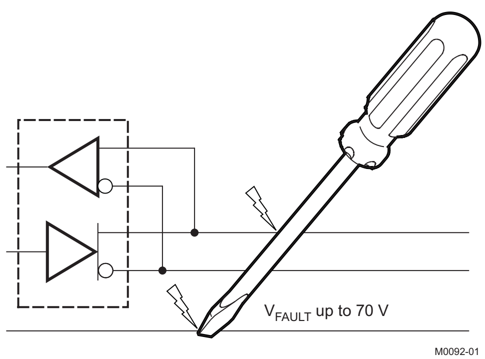
支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

说明

SN65HVD1792 被设计成在诸如电源直接短接、错误接线故障、接头故障、电缆破损和工具误用等所造成的过压故障情况下不受损坏。 它还借助于对人体模型技术规范的高级保护在静电放电 (ESD) 事件发生时稳定耐用。

SN65HVD1792 将一个差动驱动器和一个差动接收器组合在一起，这两个器件由一个单电源供电。 SN65HVD1792 额定工作温度范围 -40°C 至 105°C。



ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 105°C	SOIC - D	SN65HVD1792TDREP	1792EP	V62/13620-01XE
		SN65HVD1792TDEP		V62/13620-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

English Data Sheet: SLLSEG8

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

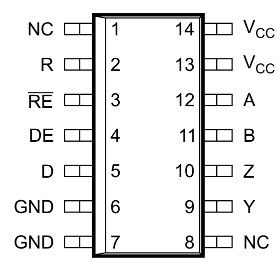
DRIVER FUNCTION TABLE

Input	Enable	Outputs		
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

RECEIVER FUNCTION TABLE

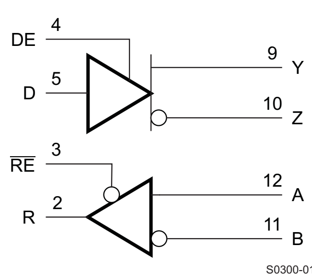
Differential Input	Enable	Output	
$V_{ID} = V_A – V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

D Package
(Top View)



NC - No internal connection
Pins 6 and 7 are connected together internally.
Pins 13 and 14 are connected together internally.

Logic Diagram (Positive Logic)



ABSOLUTE MAXIMUM RATINGS(1)

			VALUE	UNIT
V_{CC}	Supply voltage		–0.5 to 7	V
	Voltage range at bus pins	A, B pins	–70 to 70	V
	Input voltage range at any logic pin		–0.3 to V_{CC} + 0.3	V
	Transient overvoltage pulse through 100 Ω per TIA-485		–100 to 100	V
	Receiver output current		–24 to 24	mA
T_J	Junction temperature		170	°C
	IEC 60749-26 ESD (human-body model), bus terminals and GND		±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND		±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), all pins		±4	kV
	JEDEC Standard 22, Test Method C101 (charged-device model), all pins		±2	kV
	JEDEC Standard 22, Test Method A115 (machine model), all pins		±400	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		SN65HVD1792-EP	UNITS
		D	
		14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	70.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	29.4	
θ_{JB}	Junction-to-board thermal resistance(4)	25.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	8.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	25	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)	–20		25	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	–25		25	V
I_O	Output current, driver	–60		60	mA
	Output current, receiver	–8		8	mA
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
$1/t_{UI}$	Signaling rate			1	Mbps
T_A	Operating free-air temperature (see application section for thermal information)	–40		105	°C
T_J	Junction temperature	–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	RS-485 with common-mode load, V_{CC} > 4.75 V, See Figure 1		1.37			V
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V		1.5	2		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V		2	2.5		
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω		–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage			1	$V_{CC}/2$	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–100	0	100	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 2			500		mV
C_{OD}	Differential output capacitance				23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold	V_{CM} = –20 V to 25 V			–100	–10	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			–205	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – V_{IT-})			30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
		I_{OH} = –400 µA		4			
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.5	V
I_I	Driver input, driver enable, and receiver enable input current			–100		100	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_{OS}	Driver short-circuit output current			–250		250	mA
I_I	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V		75	125	µA
			V_I = –7 V	–100	–40		

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load			4	6.3	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load			3	5.2	mA
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load			2	4.3	mA
		Driver and receiver disabled	DE = GND, D = open RE = V_{CC}, no load	T_J = -40°C to 105°C		0.5	5.2	µA
				T_J = 150°C		15	29	µA
	Supply current (dynamic)	See TYPICAL CHARACTERISTICS section						

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See Figure 3				200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} – t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See Figure 3				29	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 4 and Figure 5			300	ns
		Receiver disabled	See Figure 4 and Figure 5			10	µs
		Receiver enabled	$V_{CM} > V_{CC}$		500		ns
RECEIVER							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, See Figure 6			4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	C_L = 15 pF, See Figure 6			100	200	ns
$t_{SK(P)}$	Receiver output pulse skew, $\|t_{PHL} – t_{PLH}\|$	C_L = 15 pF, See Figure 6			6	20	ns
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, See Figure 7			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 7			80	300	ns
		Driver disabled, See Figure 8			3	9	µs

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

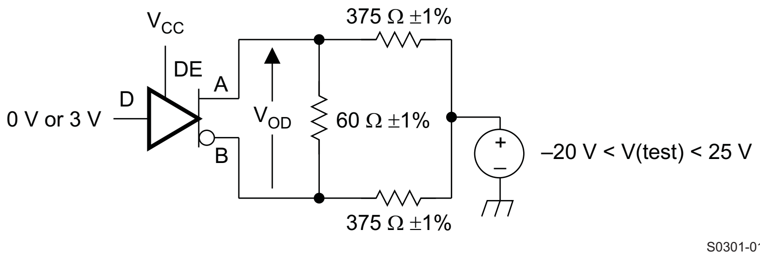


Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load

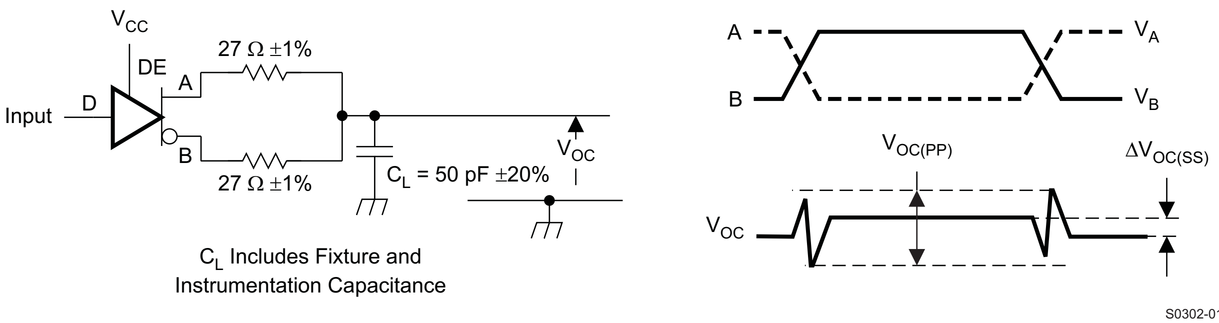


Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

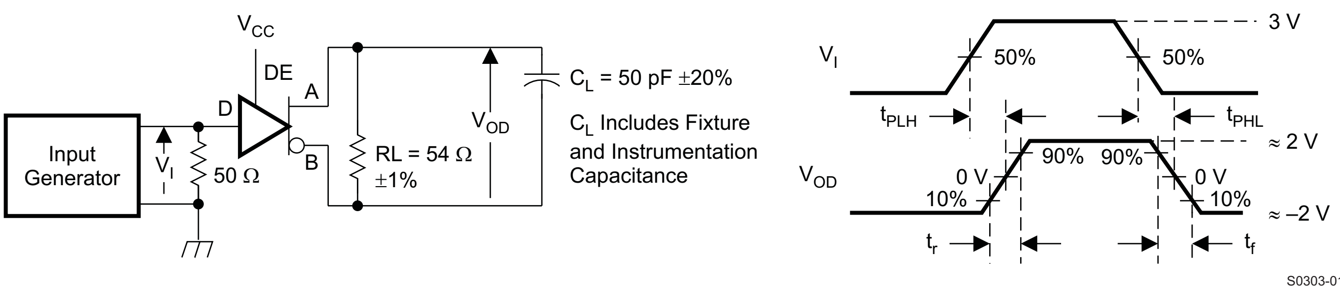
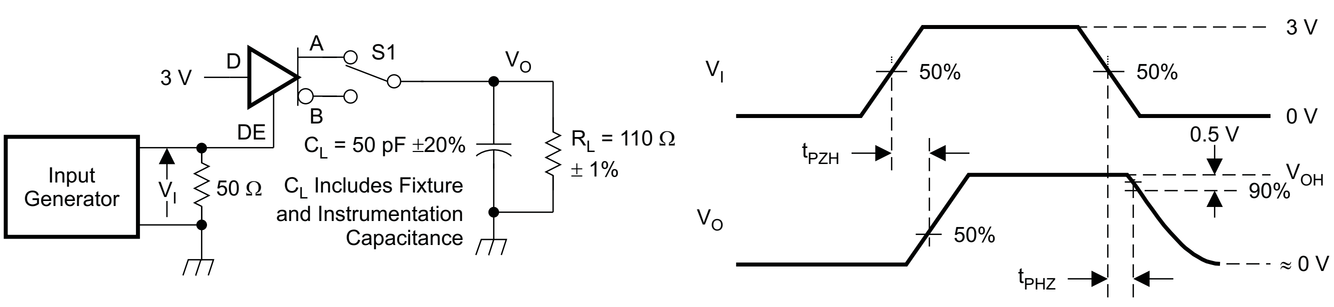


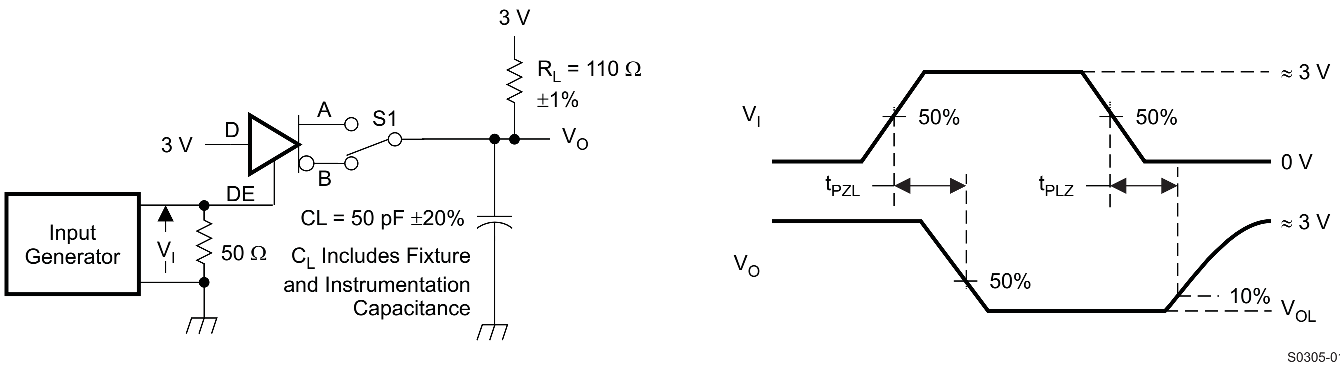
Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

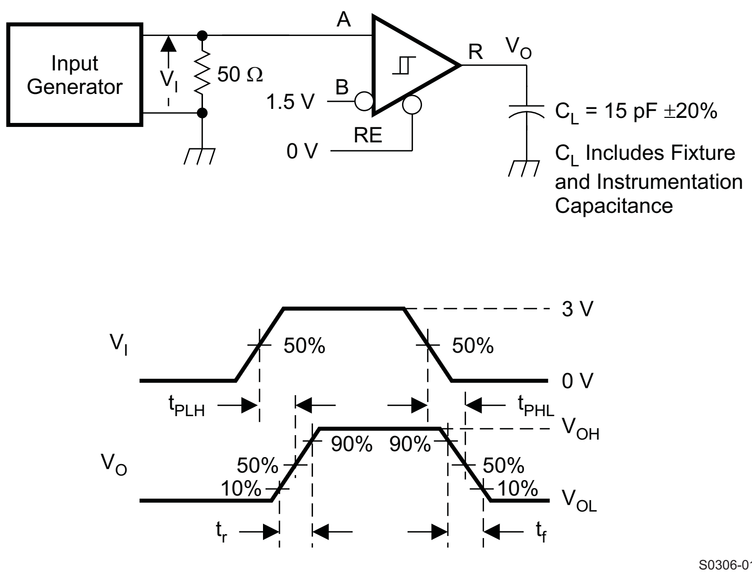


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

PARAMETER MEASUREMENT INFORMATION (continued)

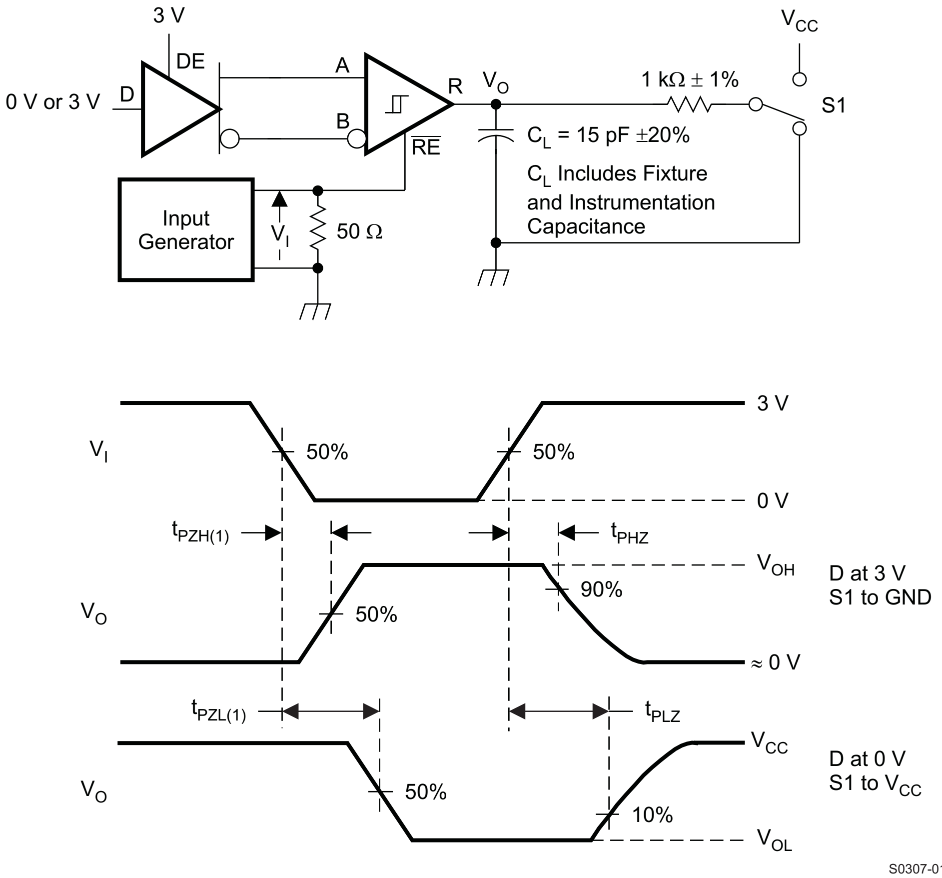


Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

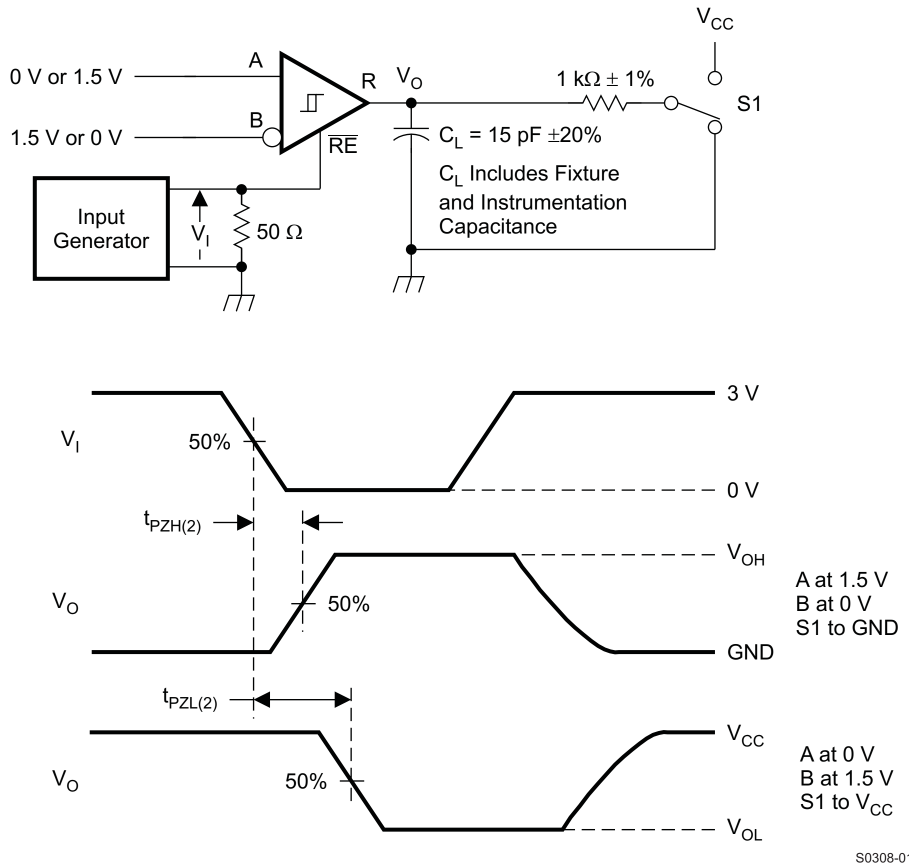


Figure 8. Measurement of Receiver Enable Times With Driver Disabled

TYPICAL CHARACTERISTICS

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

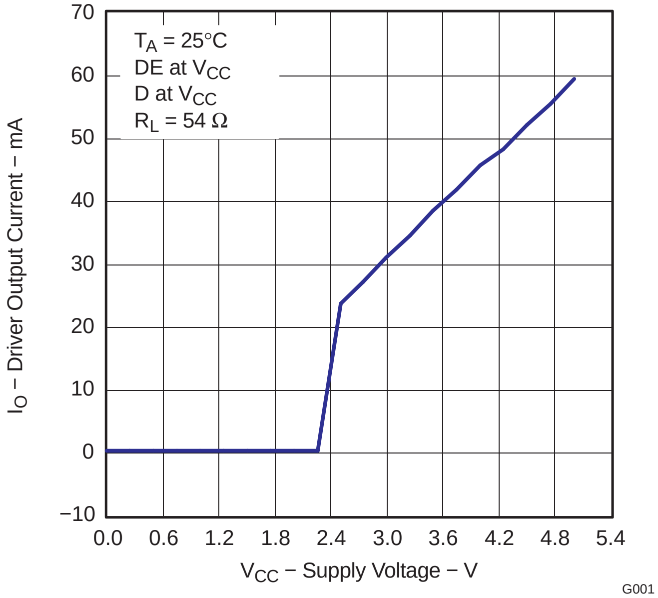


Figure 9.

HVD1787 RMS SUPPLY CURRENT vs SIGNALING RATE

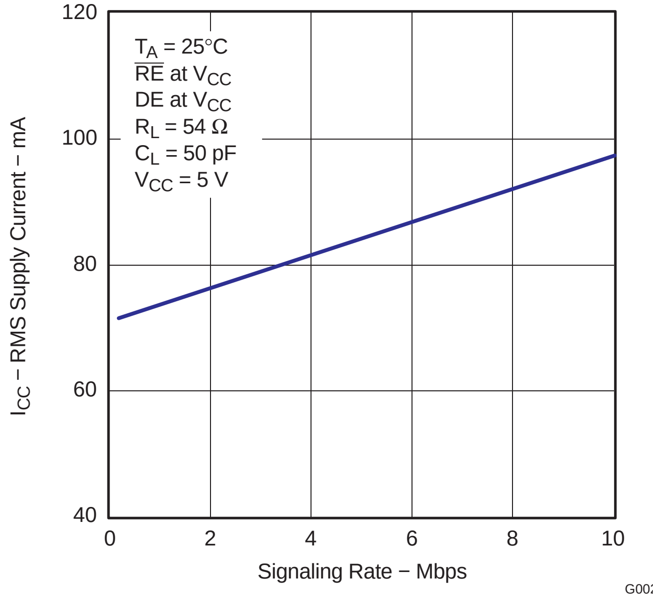


Figure 10.

BUS PIN CURRENT vs BUS PIN VOLTAGE

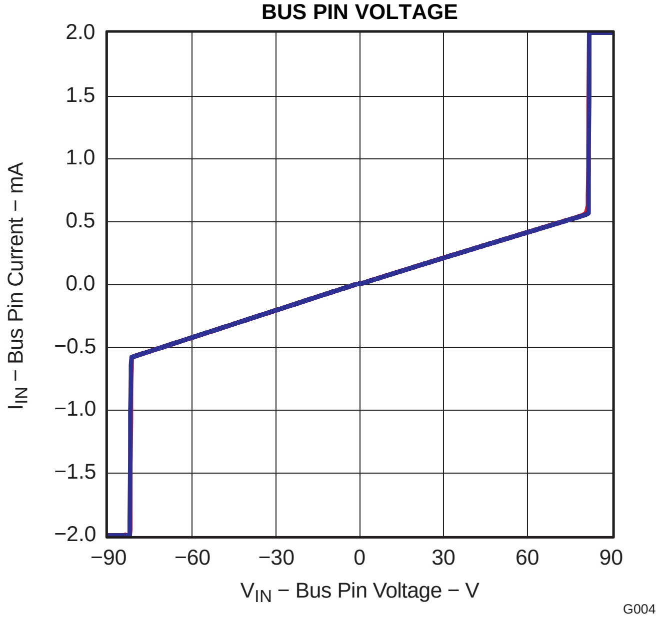


Figure 11.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL LOAD CURRENT

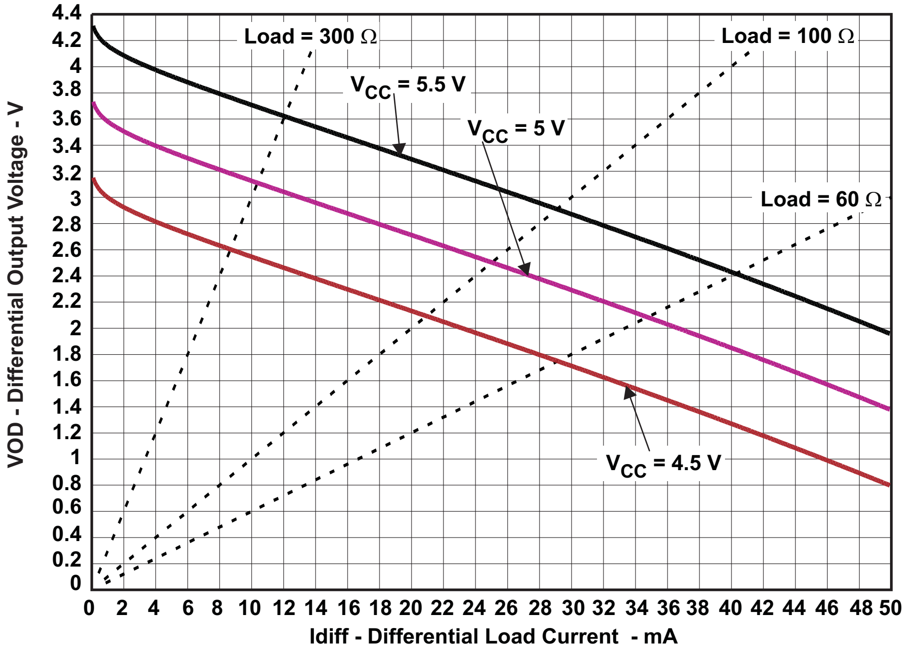


Figure 12.

ADDITIONAL OPTIONS

The SN65HVD1792 also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard SN65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring. Contact your local Texas Instruments representative for information on these options.

PART NUMBER	SN65HVD1792		
FOOTPRINT/FUNCTION	**SLOW**	**MEDIUM**	**FAST**
Half-duplex (176 pinout)	85	86	87
Full-duplex no enables (179 pinout)	88	89	90
Full-duplex with enables (180 pinout)	91	92	93
Half-duplex with cable invert	94	95	96
Full-duplex with cable invert and enables	97	98	99
J1708	08	09	10

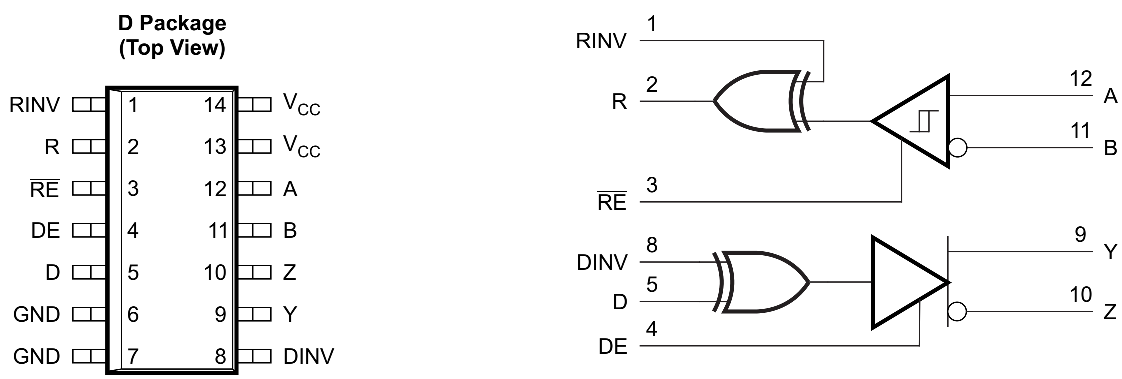


Figure 13. SN65HVD1792 With Inverting Feature to Correct for Miswired Cables

APPLICATION INFORMATION

Hot-Plugging

The SN65HVD1792 is designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 9, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device **FUNCTION TABLE**, the *ENABLE* inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together,
- or idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

In the SN65HVD1792, receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The SN65HVD1792 receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. In the *Electrical Characteristics* table, V_{IT-} has a typical value of -150 mV and a minimum (most negative) value of -200 mV, so differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output, because the typical value of V_{IT+} is -100mV, and V_{IT+} is never more positive than -10 mV under any conditions of temperature, supply voltage, or common-mode offset.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

For the SN65HVD1792, the typical noise immunity is typically about 150 mV, which is the negative noise level needed to exceed the V_{IT-} threshold (V_{IT-} TYP = -150 mV). In the worst case, the failsafe noise immunity is never less than 40 mV, which is set by the maximum positive threshold (V_{IT+} MAX = -10mV) plus the minimum hysteresis voltage (V_{HYS} MIN = 30 mV).

70-V Fault-Protection

The SN65HVD1792 is designed to survive bus pin faults up to ±70V. The devices designed for fast signaling rate (10 Mbps) will not survive a bus pin fault with a direct short to voltages above 30V when:

1. the device is powered on AND

2a. the driver is enabled (DE=HIGH) AND D=HIGH AND the bus fault is applied to the A pin OR

2b. the driver is enabled (DE=HIGH) AND D=LOW AND the bus fault is applied to the B pin

Under other conditions, the device will survive shorts to bus pin faults up to 70V. Table 1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

Table 1. Device Conditions

POWER	DE	D	A	B	RESULTS
OFF	X	X	$-70V < V_A < 70V$	$-70V < V_B < 70V$	Device survives
ON	LO	X	$-70V < V_A < 70V$	$-70V < V_B < 70V$	Device survives
ON	HI	L	$-70V < V_A < 70V$	$-70V < V_B < 30V$	Device survives
ON	HI	L	$-70V < V_A < 70V$	$30V < V_B$	Damage may occur
ON	HI	H	$-70V < V_A < 30V$	$-70V < V_B < 30V$	Device survives
ON	HI	H	$30V < V_A$	$-70V < V_B < 30V$	Damage may occur

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1792TDEP	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1792EP	Samples
SN65HVD1792TDREP	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1792EP	Samples
V62/13620-01XE	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1792EP	Samples
V62/13620-01XE-T	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1792EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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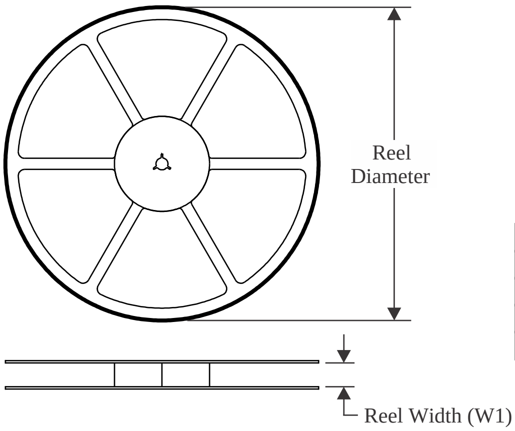
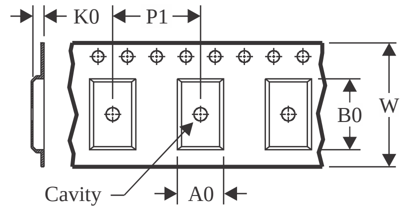
TAPE AND REEL INFORMATION

REEL DIMENSIONS

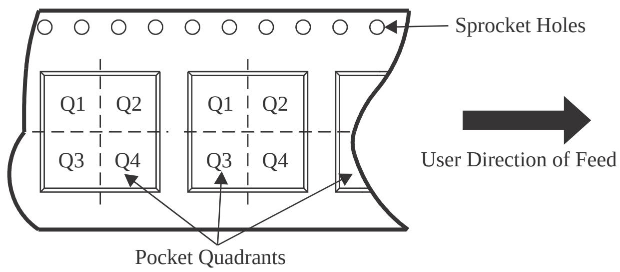


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

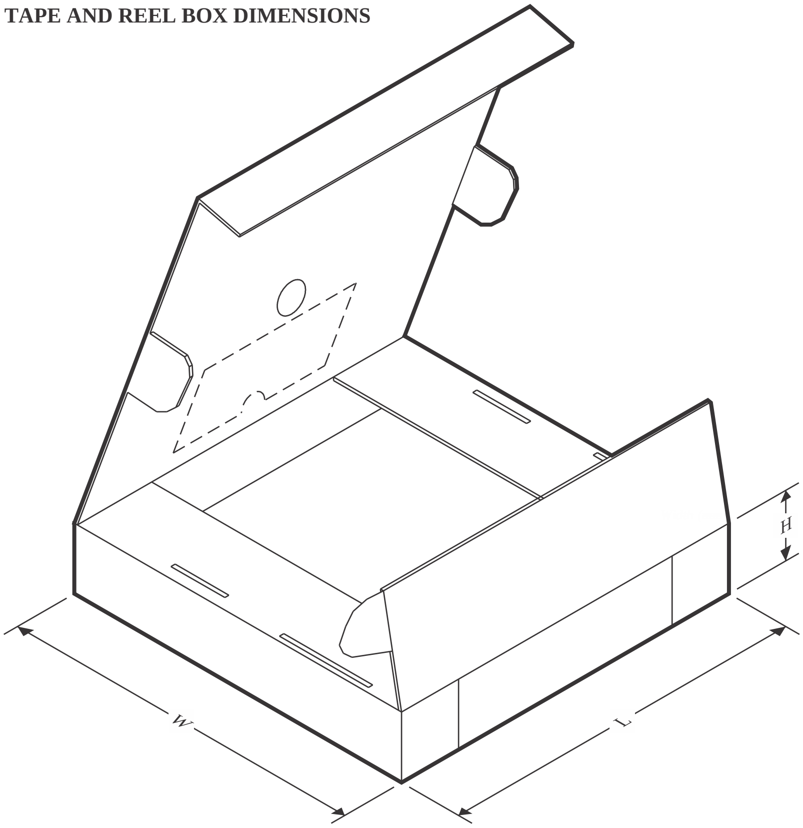
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1792TDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

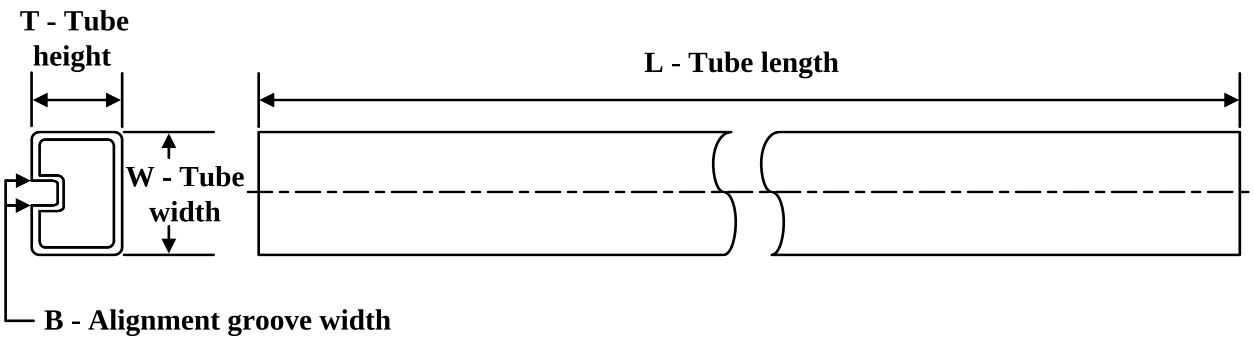
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1792TDREP	SOIC	D	14	2500	356.0	356.0	35.0

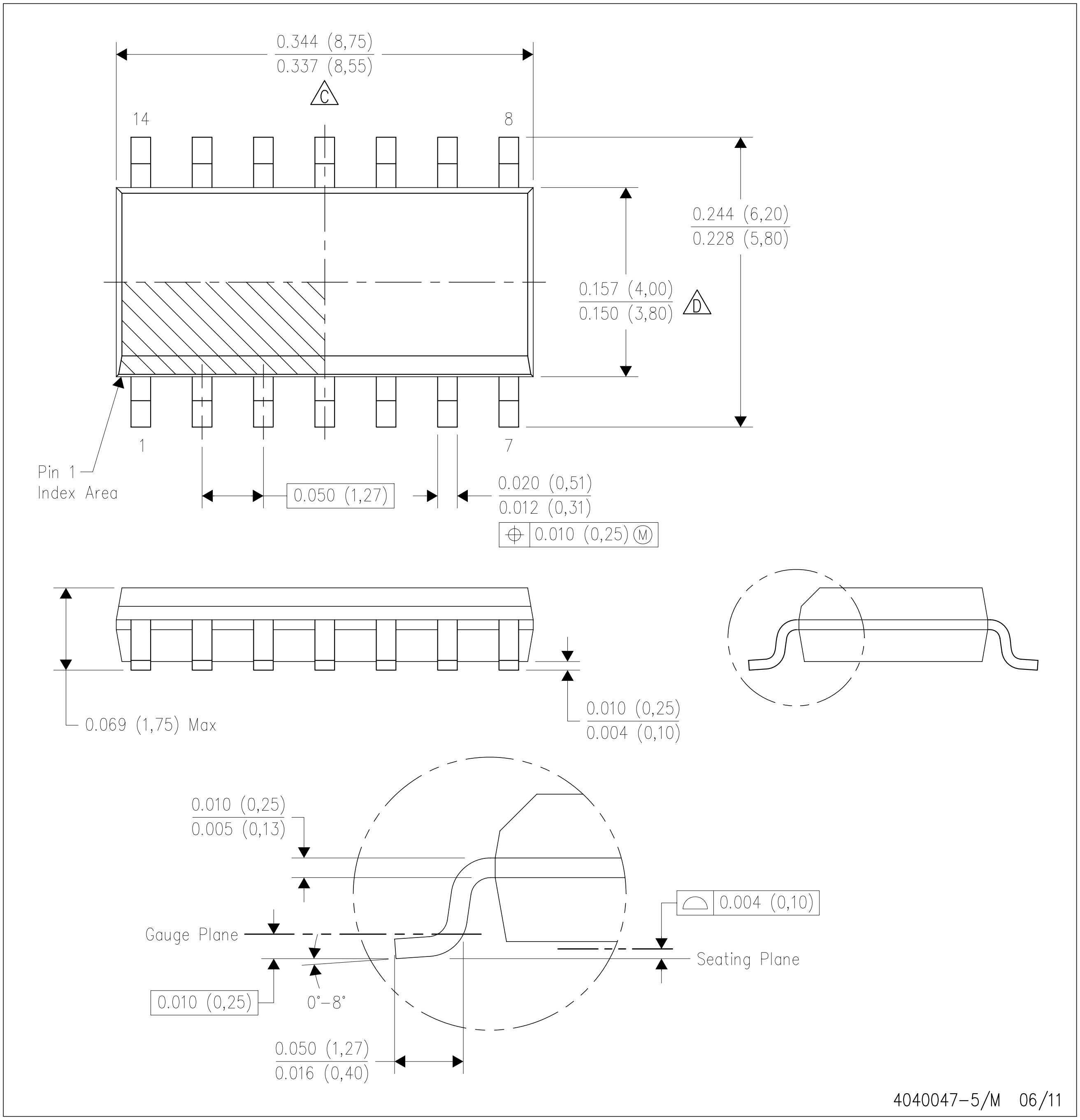
TUBE



*All dimensions are nominal

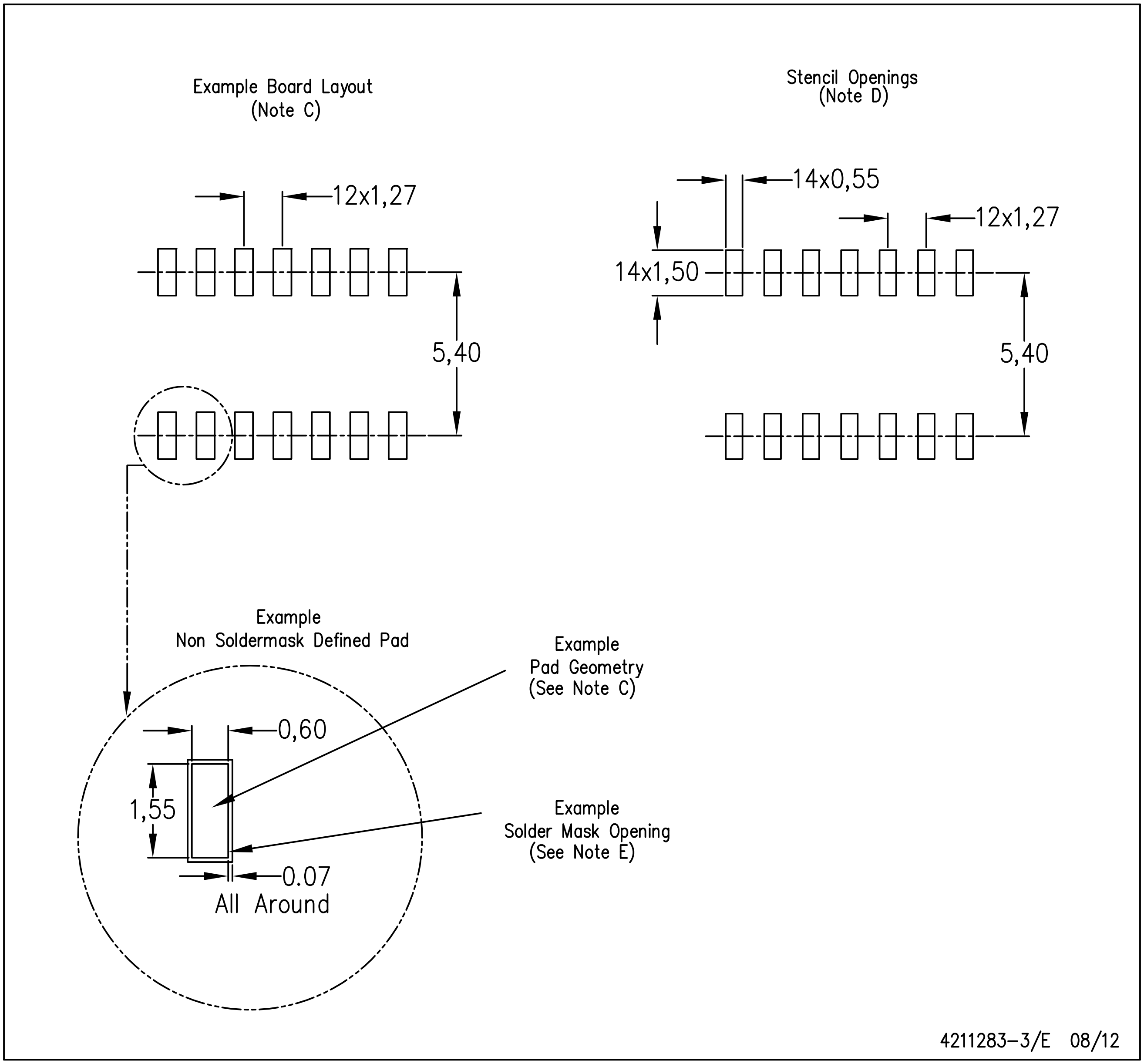
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD1792TDEP	D	SOIC	14	50	506.6	8	3940	4.32
V62/13620-01XE-T	D	SOIC	14	50	506.6	8	3940	4.32

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265