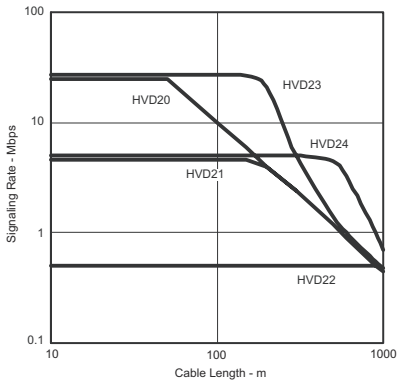
SN65HVD2x 扩展共模 RS-485 收发器

1 特性

- 共模电压范围（-20V 至 25V），是 TIA/EIA-485 标准要求范围的两倍以上
- 接收器均衡技术可支持更长的电缆和更高的信号传输速率 (SN65HVD2[3,4])
- 减少最多 256 个节点的单位负载
- 总线 I/O 保护超过 16kV HBM
- 失效防护接收器适用于开路、短路和总线空闲情况
- 低待机电源电流：1μA（最大值）
- 大于 100mV 的接收器迟滞

2 应用

- 长电缆解决方案
  - 工厂自动化
  - 安全网络
  - 构建 HVAC
- 严苛的电气环境
  - 电力逆变器
  - 工业驱动器
  - 航电设备



SN65HVD2x 应用范围

3 说明

SN65HVD2x 系列收发器提供的性能远超过典型的 RS-485 器件。除了满足 TIA/EIA-485-A 标准的所有要求外，SN65HVD2x 系列可在扩展的共模电压范围内运行，具有高 ESD 保护、宽接收器迟滞和失效防护模式运行等特性。此系列器件适用于长线缆网络以及对于普通收发器而言环境过于恶劣的其他应用。

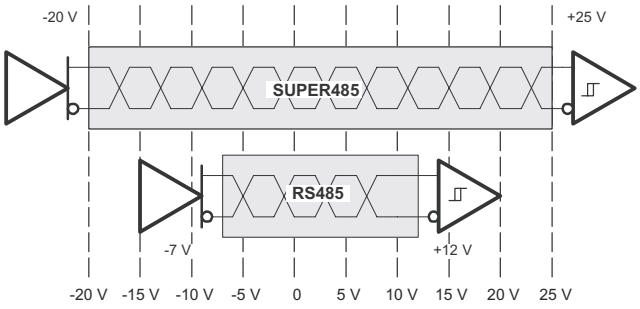
这些器件旨在通过多点双绞线电缆进行双向数据传输。示例应用包括数字电机控制器、远程传感器和终端、工业过程控制、安检站和环境控制系统。

这些器件将三态差分驱动器与差分接收器相结合，共同由单个 5V 电源供电。驱动器差分输出和接收器差分输入在内部连接，构成一个为总线提供最小负载的差分总线端口。该端口具有扩展的共模电压范围，使得这些器件适用于长线缆上的多点应用。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
SN65HVD2x	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



SN65HVD2x 器件在更宽的共模电压范围内运行

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (November 2016) to Revision G (August 2022) — **Page**

- Deleted the Available Options table 4
- Changed the D (SOIC) values in the *Thermal Information* 8

Changes from Revision E (May 2010) to Revision F (November 2016) — **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 删除了 *订购信息* 表；请参阅数据表末尾的 POA 1
- Added maximum temperature value (150°C) to the Storage temperate, T_{stg} parameter 6

Changes from Revision D (April 2005) to Revision E (May 2010) — **Page**

- Replaced the Dissipation Rating table with the *Thermal Information* table 8
- Changed I_O - Added test condition and values per device number (*Driver Electrical Characteristics* table) 8
- Changed the Thermal Characteristics table to *Power Dissipation* table 11
- Added the TEST MODE DRIVER DISABLE section 22

Changes from Revision C (September 2003) to Revision D (April 2005) — **Page**

- Added Receiver output current, I_O to the *Absolute Maximum Ratings* table 6

Changes from Revision B (June 2003) to Revision C (September 2003) — **Page**

- Added the *Thermal Information* table 8
- Added the Theory of Operation section 19
- Added the *Noise Considerations for Equalized Receivers* section 24

Changes from Revision A (March 2003) to Revision B (June 2003) **Page**

- Added V_{IK} Typical Value of 0.75 V (*Driver Electrical Characteristics* table)....8
- Deleted $V_{IT(F+)}$ – VCM = – 20 V to 25 V Minimum value (*Receiver Electrical Characteristics table*)....9
- Added the *Receiver Equalization Characteristics* table....10
- Added 图 8-6, 图 8-7, and 图 8-8 to the *Typical Characteristics* 12
- Changed A Input circuit in the *Equivalent Input and Output Schematic Diagrams* 23
- Changed the Integrated Receiver Equalization Using the SN65HVD23 section....25

Changes from Revision * (December 2002) to Revision A (March 2003) **Page**

- Changed t_{PZH}, t_{PHZ}, t_{PZL}, and t_{PLZ} - From a maximum value of 120 to include typical and maximum values for each entry (*Receiver Switching Characteristics* table)....10
- Changed t_{PZH}, t_{PHZ}, t_{PZL}, and t_{PLZ} - From a maximum value of 120 to include typical and maximum values for each entry (*Receiver Switching Characteristics* table)....10

5 说明（续）

SN65HVD20 器件可为由多达 64 个节点组成的互连网络提供高信号传输速率（高达 25Mbps）。

SN65HVD21 器件可在中等数据速率（高达 5Mbps）下连接多达 256 个节点。通过控制驱动器输出压摆率，可提供可靠开关，实现整形转换，减少高频噪声发射。

SN65HVD22 器件具有受控的驱动器输出压摆率，可在发射敏感型应用中实现低辐射噪声，并通过长残桩提高信号质量。在高达 500kbps 的信号传输速率下，可连接多达 256 个 SN65HVD22 节点。

SN65HVD23 器件采用接收器均衡技术，可改善差分总线应用的抖动性能，在长达 160 米的电缆长度下，数据速率高达 25Mbps。

SN65HVD24 器件采用接收器均衡技术，可改善差分总线应用的抖动性能，在长达 1000 米的电缆长度下，数据速率为 1Mbps 至 10Mbps。

接收器包括一个失效防护电路，此电路可在输入信号丢失后的 250 微秒内提供一个高电平输出。信号丢失的较常见原因是电缆断开连接、线路短路或总线上没有任何发送器运行。此功能防止在这些故障状况下将噪声作为有效数据进行接收，可用于“线或”式总线信号传输。

SN65HVD2x 器件的额定工作温度范围为 –40°C 至 85°C。

6 Device Comparison

表 6-1. Product Selection Guide

PART NUMBERS	CABLE LENGTH AND SIGNALING RATE(1)	NODES	MARKING
SN65HVD20	Up to 50 m at 25 Mbps	Up to 64	D: VP20, P: 65HVD20
SN65HVD21	Up to 150 m at 5 Mbps (with slew rate limit)	Up to 256	D: VP21, P: 65HVD21
SN65HVD22	Up to1200 m at 500 kbps (with slew rate limit)	Up to 256	D: VP22, P: 65HVD22
SN65HVD23	Up to 160 m at 25 Mbps (with receiver equalization)	Up to 64	D: VP23, P: 65HVD23
SN65HVD24	Up to 500 m at 3 Mbps (with receiver equalization)	Up to 256	D: VP24, P: 65HVD24

(1) Distance and signaling rate predictions based upon Belden 3105A cable and 15% eye pattern jitter.

7 Pin Configuration and Functions

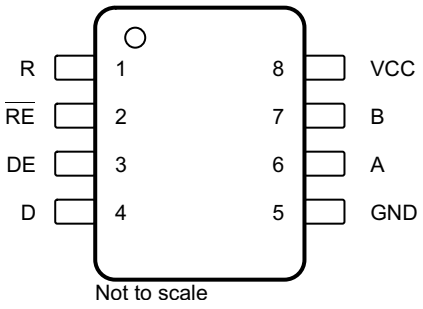


图 7-1. D or P Package, 8-Pin SOIC or PDIP (Top View)

表 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input and output	Driver output or receiver input (complementary to B)
B	7	Bus input and output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
VCC	8	Supply	4.5-V to 5.5-V supply

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage(2)			–0.5	7	V
Voltage at any bus I/O terminal			–27	27	V
Voltage input, transient pulse	A, B	(through 100 Ω, see 图 9-16)	–60	60	V
Voltage input	D, DE, $\overline{RE}$		–0.5	V_{CC} + 0.5	V
Receiver output current			–10	10	mA
Continuous total power dissipation			See *Power Dissipation Ratings*		
Junction temperature, T_J				150	°C
Storage temperature, T_{stg}				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 5, 6, and 7	±5000	V
			Pins 5, 6, and 7	±16000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	
		Machine Model (MM) (3)		±200	

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(2) Tested in accordance with JEDEC Standard 22, Test Method C101.
(3) Tested in accordance with JEDEC Standard 22, Test Method A115-A

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
	Voltage at any bus I/O terminal	A, B	–20		25	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{ID}	Differential input voltage	A with respect to B	–25		25	V
	Output current	Driver	–110		110	mA
		Receiver	–8		8	

8.3 Recommended Operating Conditions (continued)

				MIN	NOM	MAX	UNIT
I_{CC}	Supply current	Driver enabled (DE at V_{CC}), Receiver enabled (RE at 0 V), No load, V_I = 0 V or V_{CC}	SN65HVD20		6	9	mA
			SN65HVD21		8	12	
			SN65HVD22		6	9	
			SN65HVD23		7	11	
			SN65HVD24		10	14	
		Driver enabled (DE at V_{CC}), Receiver disabled (RE at V_{CC}), No load, V_I = 0 V or V_{CC}	SN65HVD20		5	8	
			SN65HVD21		7	11	
			SN65HVD22		5	8	
			SN65HVD23		5	9	
			SN65HVD24		8	12	
		Driver disabled (DE at 0 V), Receiver enabled (RE at 0 V), No load	SN65HVD20		4	7	
			SN65HVD21		5	8	
			SN65HVD22		4	7	
			SN65HVD23		4.5	9	
			SN65HVD24		5.5	10	
		Driver disabled (DE at 0 V), Receiver disabled (RE at V_{CC}) D open	All SN65HVD2x			1	µA
T_A	Operating free-air temperature(1)			–40		85	°C
T_J	Junction temperature			–40		130	°C

(1) Maximum free-air temperature operation is allowed as long as the device recommended junction temperature is not exceeded.

8.4 Thermal Information

THERMAL METRIC(1)		SN65HVD2x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.7	52.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49.9	57.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.7	38.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.0	19.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	31.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA		–1.5	0.75		V
V_O	Open-circuit output voltage	A or B, No load		0		V_{CC}	V
$\lvert V_{OD(SS)}\rvert$	Steady-state differential output voltage	No load (open circuit)		3.3	4.2	V_{CC}	V
		R_L = 54 Ω, See 图 9-1		1.8	2.5		
		With common-mode loading, See 图 9-2		1.8			
$\Delta\lvert V_{OD(SS)}\rvert$	Change in steady-state differential output voltage between logic states	See 图 9-1 and 图 9-3		–0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 9-1		2.1	2.5	2.9	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage, $V_{OC(H)} - V_{OC(L)}$	See 图 9-1 and 图 9-4		–0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage, $V_{OC(MAX)} - V_{OC(MIN)}$	R_L = 54 Ω, C_L = 50 pF, See 图 9-1 and 图 9-4		0.35			V
$V_{OD(RING)}$	Differential output voltage over and under shoot	R_L = 54 Ω, C_L = 50 pF, See 图 9-5				10%	
I_I	Input current	D, DE		–100		100	µA
I_O	Output current with power off. High impedance state output current.	V_O = –7 V to 12 V, Other input = 0 V	SN65HVD2[0,3]	–400		500	µA
			SN65HVD2[1,2,4]	–100		125	
		V_O = –20 V to 25 V, Other input = 0 V	SN65HVD2[0,3]	–800		1000	
			SN65HVD2[1,2,4]	–200		250	
I_{OS}	Short-circuit output current	V_O = –20 V to 25 V, See 图 9-9		–250		250	mA
C_{OD}	Differential output capacitance					20	pF

(1) All typical values are at V_{CC} = 5 V and 25°C.

8.6 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going differential input voltage threshold	See 图 9-10	V_O = 2.4 V, I_O = –8 mA		60	200	mV
$V_{IT(-)}$	Negative-going differential input voltage threshold		V_O = 0.4 V, I_O = 8 mA	–200	–60		
V_{HYS}	Hysteresis voltage (V_{IT+} – V_{IT-})			100	130		mV
$V_{IT(F+)}$	Positive-going differential input failsafe voltage threshold	See 图 9-15	VCM = –7 V to 12 V	40	120	200	mV
			VCM = –20 V to 25 V		120	250	
$V_{IT(F-)}$	Negative-going differential input failsafe voltage threshold	See 图 9-15	VCM = –7 V to 12 V	–200	–120	–40	mV
			VCM = –20 V to 25 V	–250	–120		
V_{IK}	Input clamp voltage	I_I = –18 mA		–1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See 图 9-11		4			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, See 图 9-11				0.4	V
$I_{I(BUS)}$	Bus input current (power on or power off)	V_I = –7 to 12 V, Other input = 0 V	SN65HVD2[0,3]	–400		500	μA
			SN65HVD2[1,2,4]	–100		125	
		V_I = –20 to 25 V, Other input = 0 V	SN65HVD2[0,3]	–800		1000	
			SN65HVD2[1,2,4]	–200		250	
I_I	Input current	$\overline{RE}$		–100		100	μA
R_I	Input resistance	SN65HVD2[0,3]		24			kΩ
		SN65HVD2[1,2,4]		96			
C_{ID}	Differential input capacitance	V_{ID} = 0.5 + 0.4 sine (2π × 1.5 × 10^6t)			20		pF

(1) All typical values are at V_{CC} = 5 V and 25°C.

8.7 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Differential output propagation delay, low-to-high and high-to-low	R_L = 54 Ω, C_L = 50 pF, See 图 9-3	SN65HVD2[0,3]	6	10	20	ns
			SN65HVD2[1,4]	20	32	60	
			SN65HVD22	160	280	500	
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, See 图 9-3	SN65HVD2[0,3]	2	6	12	ns
			SN65HVD2[1,4]	20	40	60	
			SN65HVD22	175	400	600	
t_{PZH}, t_{PHZ}	Propagation delay time, high-impedance-to-high-level output and high-level output-to-high-impedance	$\overline{RE}$ at 0 V, See 图 9-6	SN65HVD2[0,3]			40	ns
			SN65HVD2[1,4]			100	
			SN65HVD22			300	
t_{PZL}, t_{PLZ}	Propagation delay time, high-impedance-to-high-level output and high-level output-to-high-impedance	$\overline{RE}$ at 0 V, See 图 9-7	SN65HVD2[0,3]			40	ns
			SN65HVD2[1,4]			100	
			SN65HVD22			300	
$t_{d(standby)}$	Time from an active differential output to standby	$\overline{RE}$ at V_{CC}, See 图 9-8				2	μs
$t_{d(wake)}$	Wake-up time from standby to an active differential output					8	μs
$t_{sk(p)}$	Pulse skew | t_{PLH} – t_{PHL} |	SN65HVD2[0,3]				2	ns
		SN65HVD2[1,4]				6	
		SN65HVD22				50	

(1) All typical values are at V_{CC} = 5 V and 25°C

8.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time, low-to-high level output and high-to low level output	See 图 9-11	SN65HVD2[0,3]		16	35	ns
			SN65HVD2[1,2,4]		25	50	
t_r t_f	Receiver output rise time Receiver output fall time	See 图 9-11			2	4	ns
t_{PZH}	Receiver output enable time to high level and disable time from high level	See 图 9-12			90	120	ns
t_{PHZ}					16	35	
t_{PZL}	Receiver output enable time to low level and disable time from low level	See 图 9-13			90	120	ns
t_{PLZ}					16	35	
$t_{r(standby)}$	Time from an active receiver output to standby	See 图 9-14, DE at 0 V				2	µs
$t_{r(wake)}$	Wake-up time from standby to an active receiver output	See 图 9-14, DE at 0 V				8	µs
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$					5	ns
$t_{p(set)}$	Delay time, bus fail to failsafe set	See 图 9-15, pulse rate = 1 kHz			250	350	µs
$t_{p(reset)}$	Delay time, bus recovery to failsafe reset	See 图 9-15, pulse rate = 1 kHz			50		ns

8.9 Receiver Equalization Characteristics

over recommended operating conditions (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS				TYP	UNIT
$t_{j(pp)}$	Peak-to-peak eye-pattern jitter	Peudo-random NRZ code with a bit pattern length of $2^{16} - 1$, Beldon 3105A cable, See 图 10-2	25 Mbps	0 m	SN65HVD23	2	ns
				100 m	SN65HVD20	6	ns
					SN65HVD23	3	
				150 m	SN65HVD20	15	ns
					SN65HVD23	4	
				200 m	SN65HVD20	27	ns
					SN65HVD23	8	
			10 Mbps	200 m	SN65HVD20	22	ns
					SN65HVD23	8	
				250 m	SN65HVD20	34	ns
					SN65HVD23	15	
				300 m	SN65HVD20	49	ns
					SN65HVD23	27	
			5 Mbps	500 m	SN65HVD21	128	ns
					SN65HVD24	18	
			3 Mbps	500 m	SN65HVD20	93	ns
					SN65HVD21	103	
					SN65HVD23	90	
					SN65HVD24	16	
			1 Mbps	1000 m	SN65HVD21	216	ns
					SN65HVD24	62	

(1) The SN65HVD20 and SN65HVD21 do not have receiver equalization, but are specified for comparison.
(2) All typical values are at V_{CC} = 5 V, and temperature = 25°C.

8.10 Power Dissipation

PARAMETERS		TEST CONDITIONS			VALUE	UNIT
P_D	Device power dissipation	Typical	V_{CC} = 5 V, T_J = 25°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	SN65HVD20: 25 Mbps	295	mW
				SN65HVD21: 5 Mbps	260	
				SN65HVD22: 500 kbps	233	
				SN65HVD23: 25 Mbps	302	
				SN65HVD24: 5 Mbps	267	
		Worst case	V_{CC} = 5.5 V, T_J = 125°C, R_L = 54 Ω, C_L = 50 pF, C_L = 15 pF (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	SN65HVD20: 25 Mbps	408	mW
				SN65HVD21: 5 Mbps	342	
				SN65HVD22: 500 kbps	300	
				SN65HVD23: 25 Mbps	417	
				SN65HVD24: 5 Mbps	352	
T_{SD}	Thermal shut down junction temperature				170	°C

8.11 Typical Characteristics

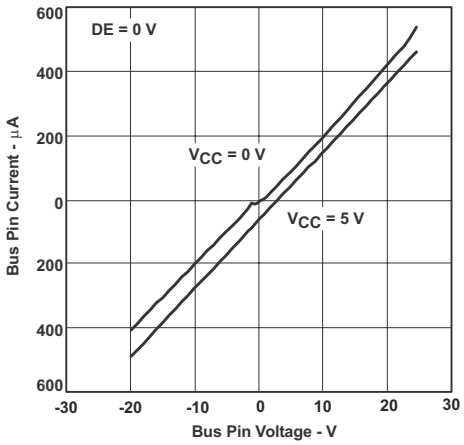


图 8-1. SN65HVD2[0,3] Bus Pin Current vs Bus Pin Voltage

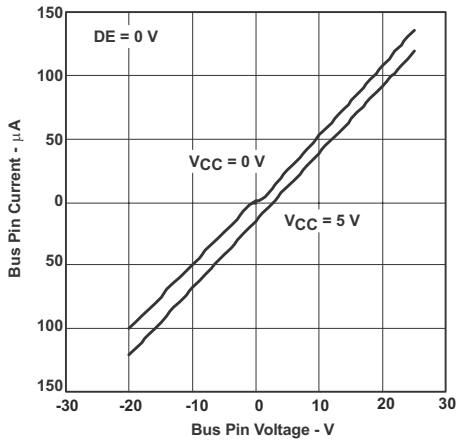


图 8-2. SN65HVD2[1,2,4] Bus Pin Current vs Bus Pin Voltage

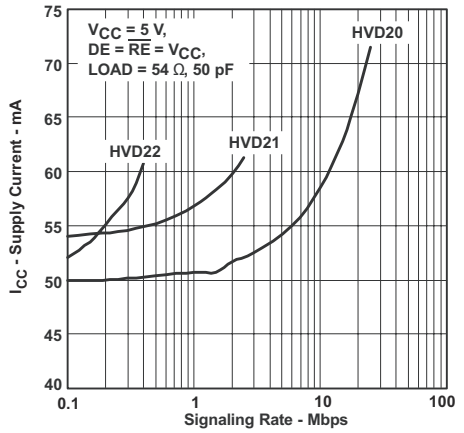


图 8-3. Supply Current vs Signaling Rate

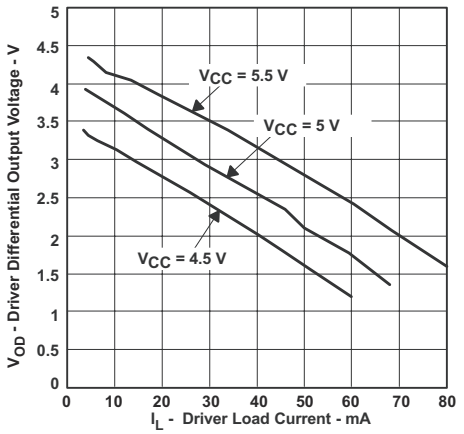


图 8-4. Driver Differential Output Voltage vs Driver Load Current

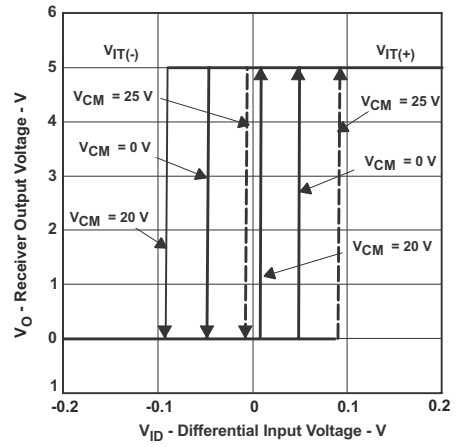


图 8-5. Receiver Output Voltage vs Differential Input Voltage

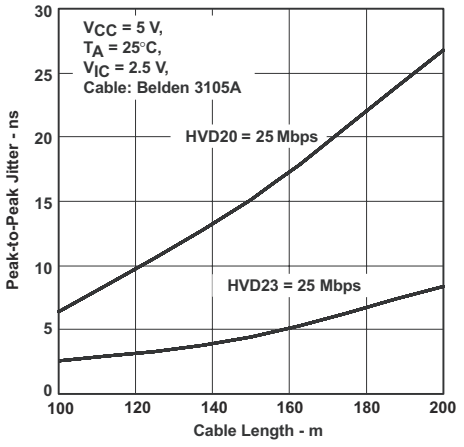


图 8-6. SN65HVD2[0,3] Peak-to-Peak Jitter vs Cable Length

8.11 Typical Characteristics (continued)

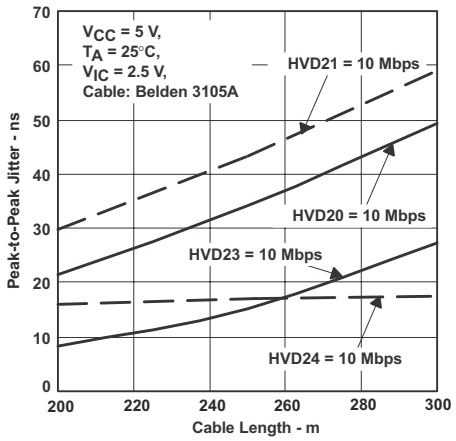


图 8-7. SN65HVD2[0,1,3,4] Peak-to-Peak Jitter vs Cable Length

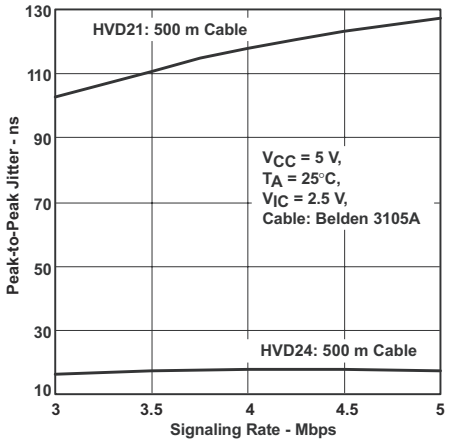


图 8-8. SN65HVD2[1,4] Peak-to-Peak Jitter vs Signaling Rate

9 Parameter Measurement Information

备注

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle, Z_O = 50 Ω (unless otherwise specified).

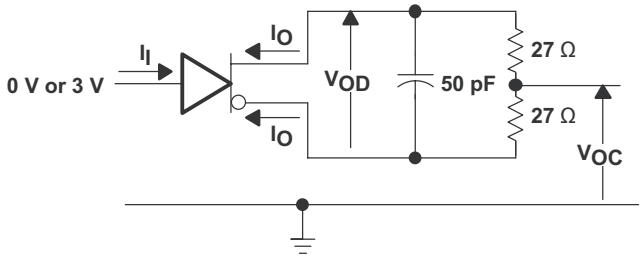


图 9-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

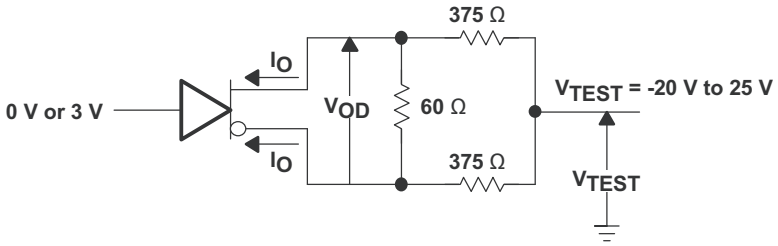


图 9-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

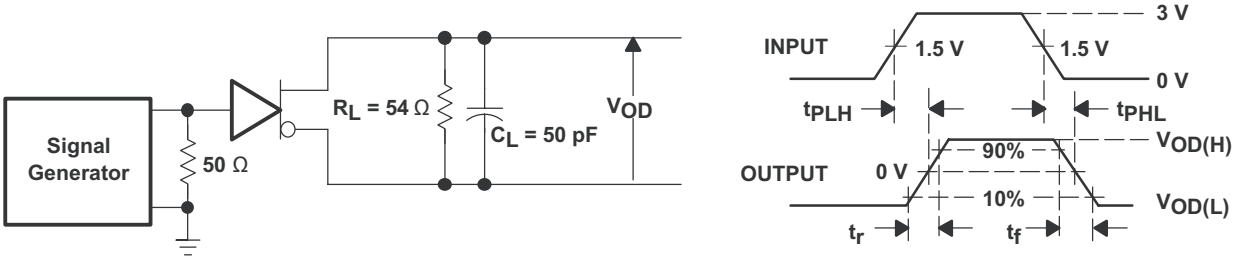


图 9-3. Driver Switching Test Circuit and Waveforms

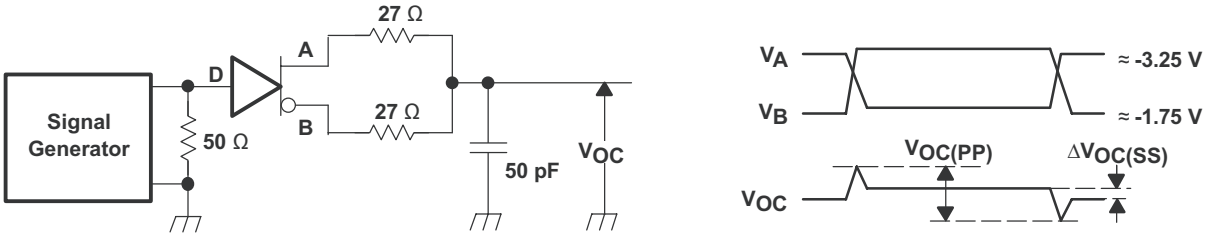
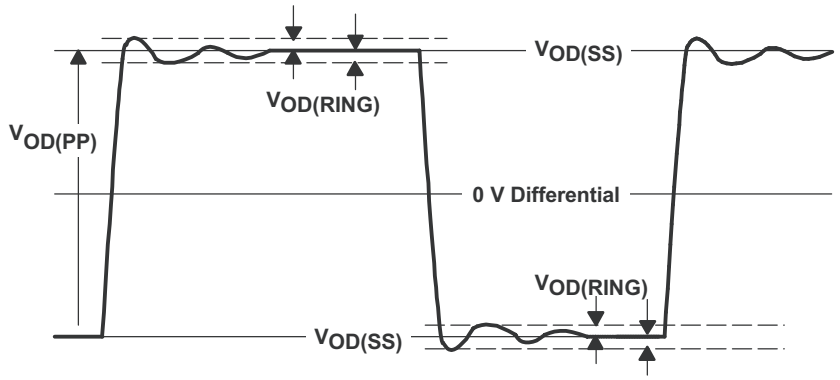


图 9-4. Driver V_{OC} Test Circuit and Waveforms



$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

图 9-5. $V_{OD(RING)}$ Waveform and Definitions

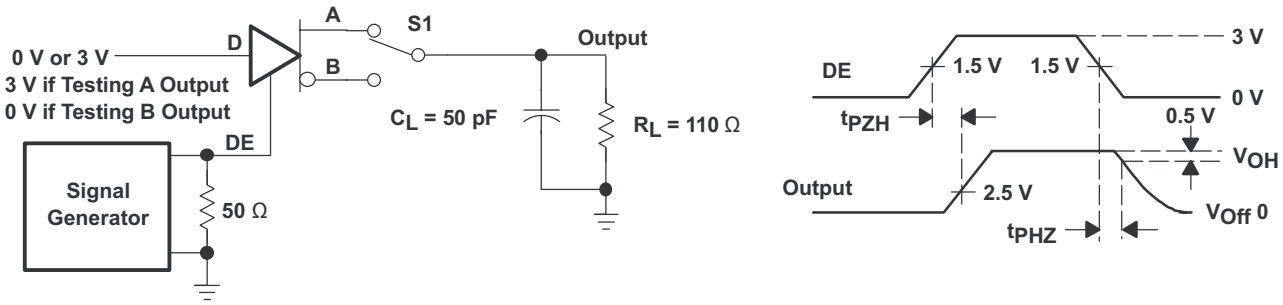


图 9-6. Driver Enable and Disable Test, High Output

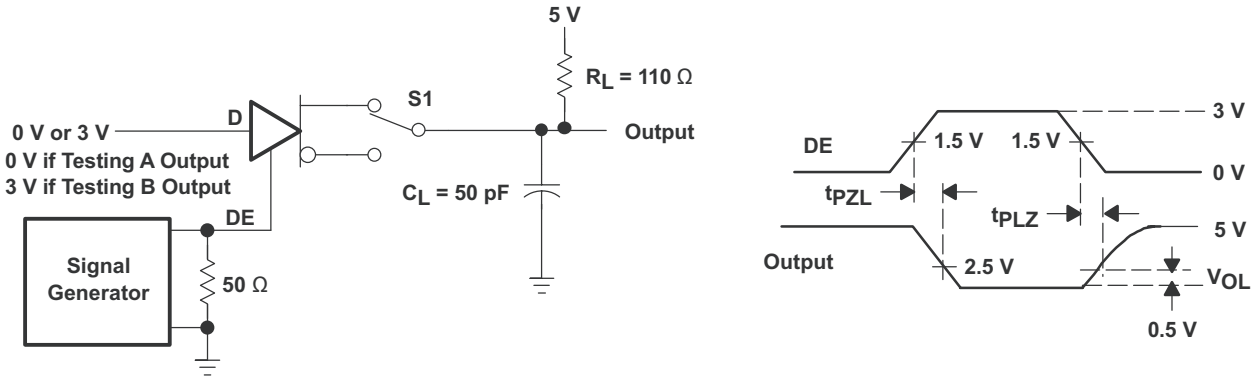


图 9-7. Driver Enable and Disable Test, Low Output

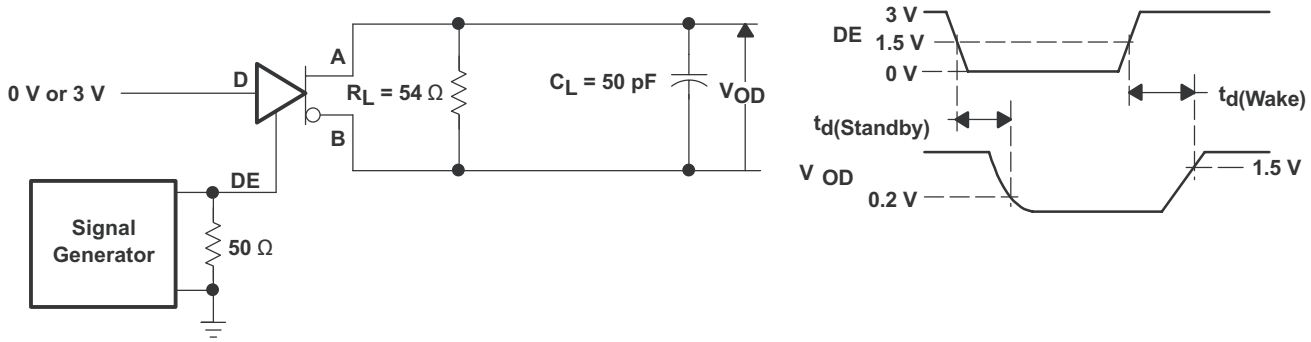


图 9-8. Driver Standby and Wake Test Circuit and Waveforms

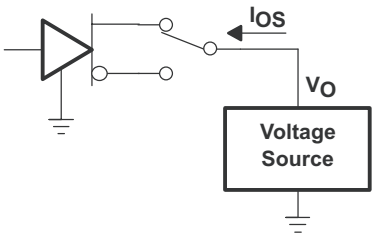


图 9-9. Driver Short-Circuit Test

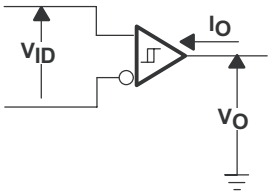


图 9-10. Receiver DC Parameter Definitions

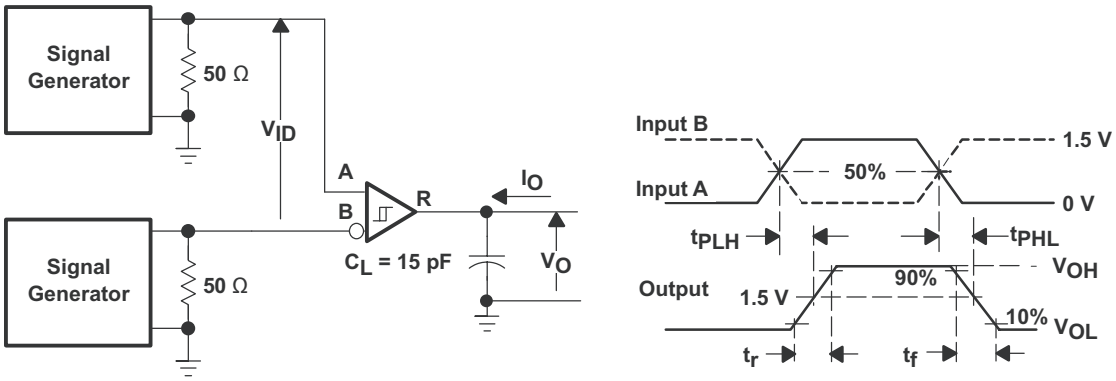


图 9-11. Receiver Switching Test Circuit and Waveforms

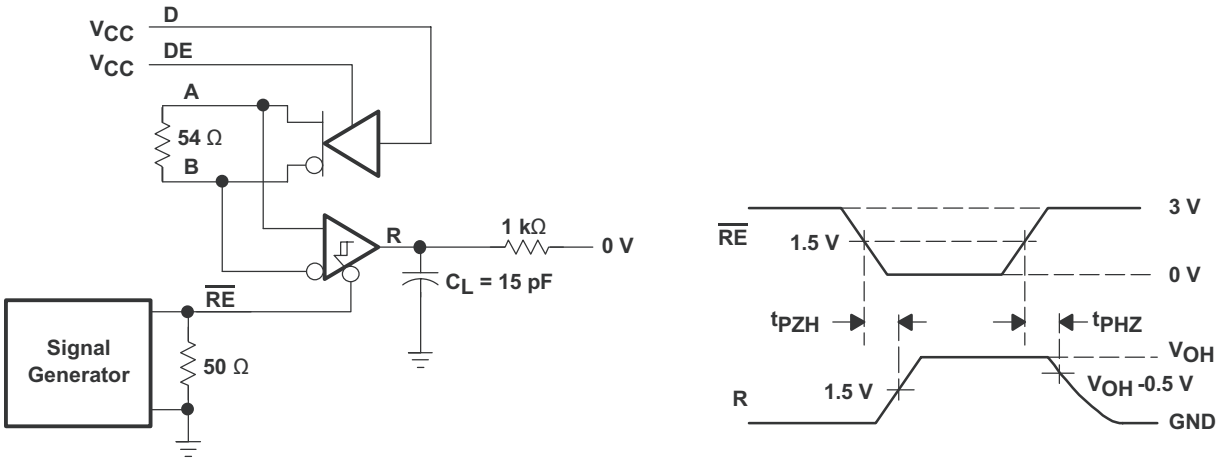


图 9-12. Receiver Enable Test Circuit and Waveforms, Data Output High

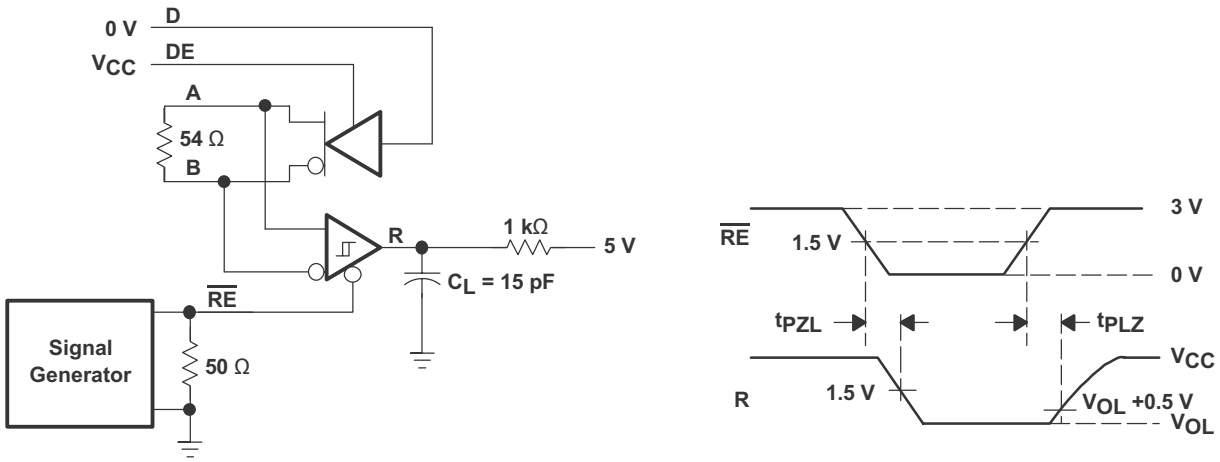


图 9-13. Receiver Enable Test Circuit and Waveforms, Data Output Low

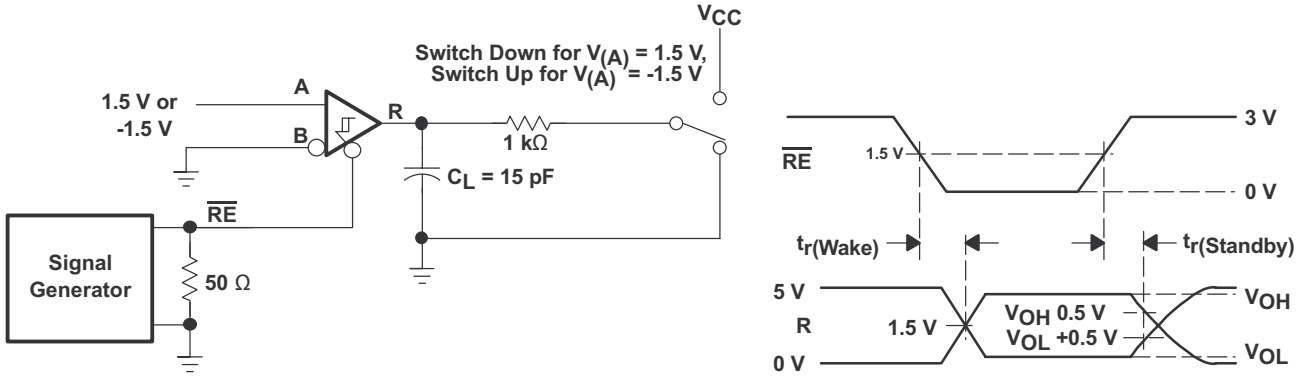


图 9-14. Receiver Standby and Wake Test Circuit and Waveforms

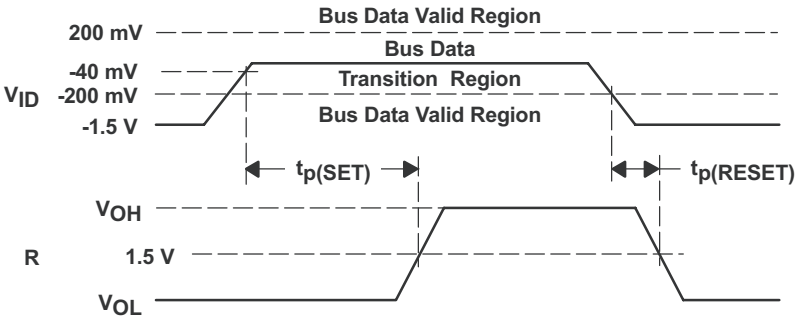


图 9-15. Receiver Active Failsafe Definitions and Waveforms

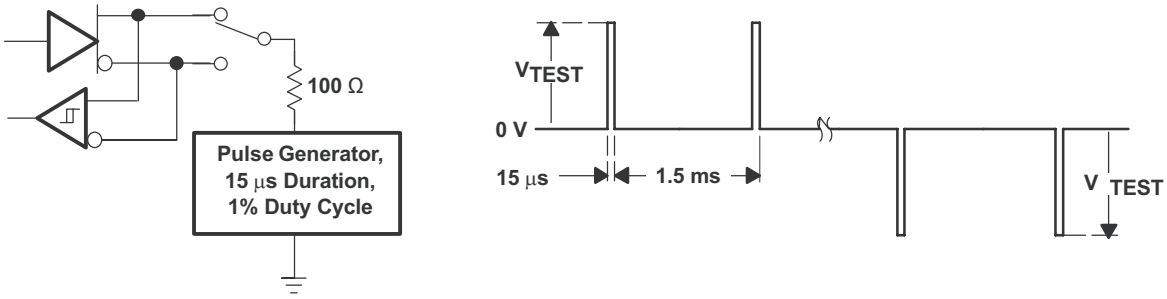


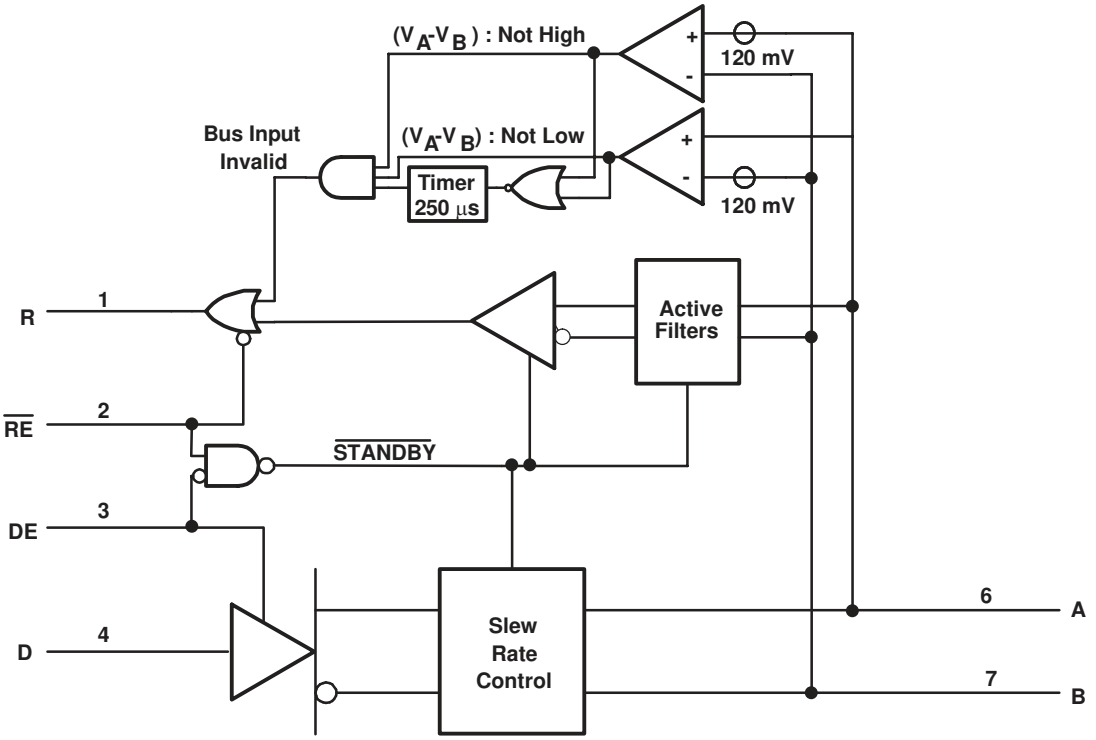
图 9-16. Test Circuit and Waveforms, Transient Overvoltage Test

10 Detailed Description

10.1 Overview

The SN65HVD2x family of devices are RS-485 compliant half-duplex transceivers designed for communication rates up to 500 kbps (SN65HVD22), 3 Mbps (SN65HVD24), 5 Mbps (SN65HVD21), or 25 Mpbs (SN65HVD20 and SN65HVD23). The devices feature extended common-mode range support, which provides immunity to larger ground potential differences that can occur between nodes that communicate over longer distances. The SN65HVD23 and the SN65HVD24 devices feature receiver equalization, which reduces the amount of data-dependent jitter that is introduced by the high-frequency losses associated with long cables.

10.2 Functional Block Diagram



10.3 Feature Description

The SN65HVD2x family of devices integrates a differential receiver and differential driver with additional features for improved performance in electrically-noisy, long-cable, or other fault-intolerant applications.

The receiver hysteresis (typically 130 mV) is much larger than found in typical RS-485 transceivers. This helps reject spurious noise signals which would otherwise cause false changes in the receiver output state.

Slew rate limiting on the driver outputs (SN65HVD2[1,2,4]) reduces the high-frequency content of signal edges. This decreases reflections from bus discontinuities, and allows longer stub lengths between nodes and the main bus line. Designers must consider the maximum signaling rate and cable length required for a specific application, and choose the transceiver best matching those requirements.

When DE is low, the differential driver is disabled, and the A and B outputs are in high-impedance states. When DE is high, the differential driver is enabled, and drives the A and B outputs according to the state of the D inputs.

When $\overline{RE}$ is high, the differential receiver output buffer is disabled, and the R output is in a high-impedance state. When $\overline{RE}$ is low, the differential receiver is enabled, and the R output reflects the state of the differential bus inputs on the A and B pins.

If both the driver and receiver are disabled, (DE low and $\overline{RE}$ high) then all nonessential circuitry, including auxiliary functions such as failsafe and receiver equalization is placed in a low-power standby state. This reduces power consumption to less than 5 µW. When either enable input is asserted, the circuitry again becomes active.

In addition to the primary differential receiver, these devices incorporate a set of comparators and logic to implement an active receiver failsafe feature. These components determine whether the differential bus signal is valid. Whenever the differential signal is close to zero volts (neither high nor low), a timer initiates, If the differential input remains within the transition range for more than 250 µs, the timer expires and set the receiver output to the high state. If a valid bus input (high or low) is received at any time, the receiver output reflects the valid bus state, and the timer is reset.

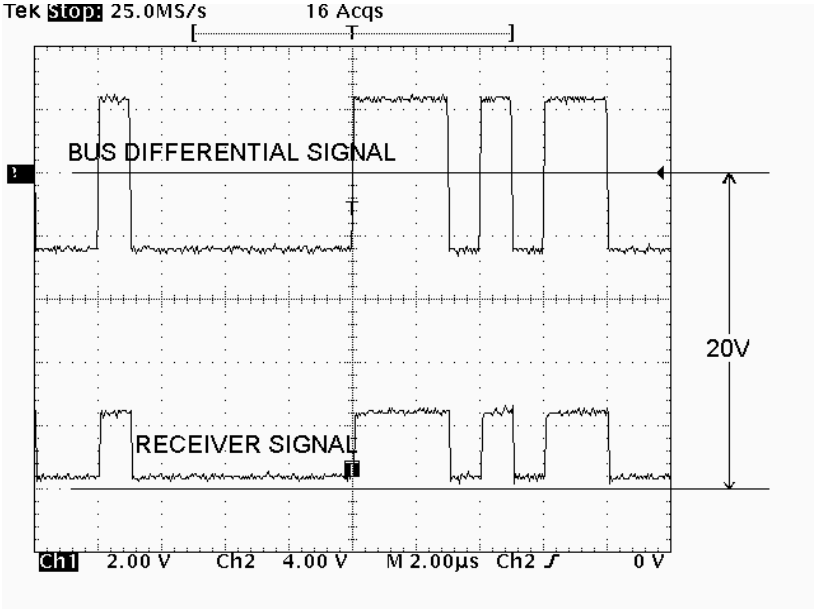


图 10-1. SN65HVD22 Receiver Operation With 20-V Offset on Input Signal

$$H(s) = k_0\left[(1-k_1)+\frac{k_1p_1}{(s+p_1)}\right]\left[(1-k_2)+\frac{k_2p_2}{(s+p_2)}\right]\left[(1-k_3)+\frac{k_3p_3}{(s+p_3)}\right]$$

k0 (DC loss)	p1 (MHz)	k1	p2 (MHz)	k2	p3 (MHz)	k3
Similar to 160m of Belden 3105A	0.95	0.25	0.3	3.5	0.5	15	1
Similar to 250m of Belden 3105A	0.9	0.25	0.4	3.5	0.7	12	1
Similar to 500m of Belden 3105A	0.8	0.25	0.6	2.2	1	8	1
Similar to 1000m of Belden 3105A	0.6	0.3	1	3	1	6	1

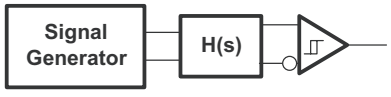


图 10-2. Cable Attenuation Model for Jitter Measurements

10.4 Device Functional Modes

The driver and receiver behavior for different input conditions are shown in 表 10-1 and 表 10-2, respectively.

表 10-1. Driver Function Table(1)

DEVICE	INPUT	ENABLE	OUTPUTS	
	D	DE	A	B
SN65HVD2[0,1,2]	H	H	H	L
	L	H	L	H
	X	L	Z	Z
	X	OPEN	Z	Z
	OPEN	H	H	L
SN65HVD2[3,4]	H	H	H	L
	L	H	L	H
	X	L	Z	Z
	X	OPEN	Z	Z
	OPEN	H	L	H

(1) Legend: H = high level, L = low level, X = don’t care, Z = high impedance (off), ? = indeterminate

表 10-2. Receiver Function Table(1)

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
0.2 V ≤ V_{ID}	L	H
–0.2 V < V_{ID} < 0.2 V	L	H(2)
V_{ID} ≤ –0.2 V	L	L
X	H	Z
X	OPEN	Z
Open circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = high level, L = low level, Z = high impedance (off)
(2) If the differential input V_{ID} remains within the transition range for more than 250 µs, the integrated failsafe circuitry detects a bus fault, and set the receiver output to a high state. See 图 9-15.

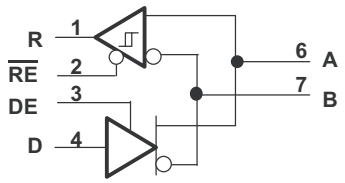


图 10-3. Logic Diagram

10.4.1 Test Mode Driver Disable

If the input signal to the D pin is such that:

1. the signal has signaling rate above 4 Mbps (for the SN65HVD21 and SN65HVD24),
2. the signal has signaling rate above 6 Mbps (for the SN65HVD20 and SN65HVD23),
3. the signal has average amplitude from 1.2 V to 1.6 V (1.4 V ± 200 mV), or
4. the average signal amplitude remains in this range for 100 µs or longer,

then the driver may activate a test-mode during which the driver outputs are temporarily disabled. This can cause loss of transmission of data during the period that the device is in the test-mode. The driver is re-enabled and resumes normal operation whenever the above conditions are not true. The device is not damaged by this test mode.

Although rare, there are combinations of specific voltage levels and input data patterns within the operating conditions of the SN65HVD2x family which may lead to a temporary state where the driver outputs are disabled for a period of time.

Observations:

1. The conditions for inadvertently entering the test mode are dependent on the levels, duration, and duty cycle of the logic signal input to the D pin. Operating input levels are specified as greater than 2 V for a logic HIGH input, and less than 0.8 V for a logic LOW input. Therefore, a valid steady-state logic input does not cause the device to activate the test mode
2. Only input signals with frequency content above 2 MHz (4 Mbps) have a possibility of activating the test mode. Therefore, this issue should not affect the normal operation of the SN65HVD22 (500 kbps).
3. For operating signaling rates of 4 Mbps (or above), the conditions stated above must remain true over a period of: 4 Mbps ×100 µs = 400 bits. Therefore, a normal short message does not inadvertently activate the test model.
4. One example of an input signal which may cause the test mode to activate is a clock signal with frequency 3 MHz and 50% duty cycle (symmetric HIGH and LOW half-cycles) with logic HIGH levels of 2.4 V and logic LOW levels of 0.4 V. This signal applied to the D pin as a driver input would meet the criteria listed above, and may cause the test-mode to activate, which would disable the driver. This example situation may occur if the clock signal is generated from a microcontroller or logic chip with a 2.7-V supply.

10.4.2 Equivalent Input and Output Schematic Diagrams

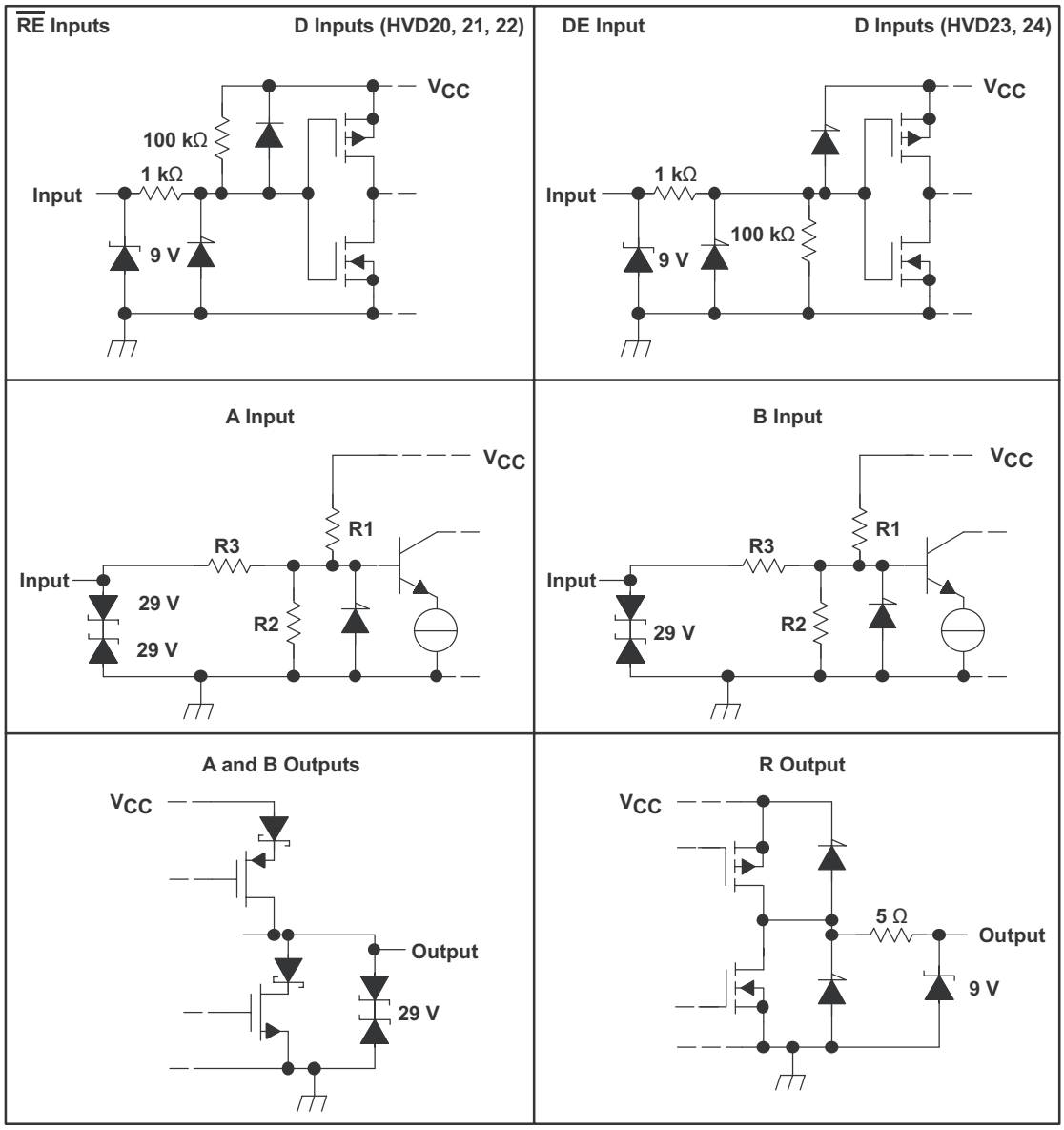


图 10-4. Equivalent Input and Output Schematic Diagrams

表 10-3. Input and Output Resistor Values

DEVICE	R1, R2	R3
SN65HVD2[0,3]	9 kΩ	45 kΩ
SN65HVD2[1,2,4]	36 kΩ	180 kΩ

11 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

11.1 Application Information

The SN65HVD2x devices are half-duplex RS-485 transceivers that can be used for bidirectional, multipoint communication at various data rates over differential transmission lines. These devices support a wide common-mode range, allowing for robust communication even in the presence of voltage differences between the reference potentials of different nodes on a network.

11.2 Typical Application

图 11-1 shows a typical RS-485 application. Transceivers of different nodes are connected to one another over a shared bus. Twisted-pair cabling with a controlled differential impedance is used, and termination resistances are placed at the two ends of the cable to match the transmission line impedance and minimize signal reflections.

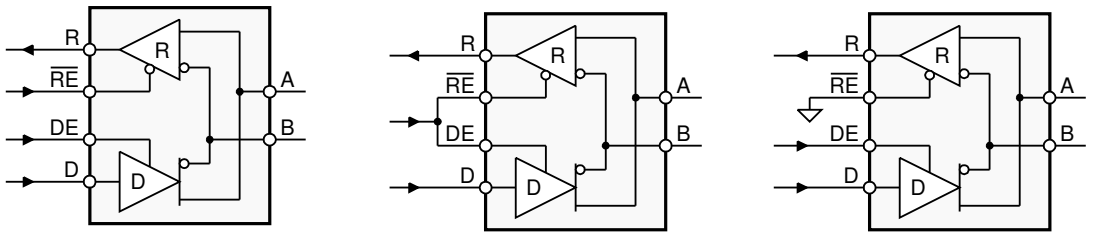


图 11-1. Half-Duplex Transceiver Configurations

11.2.1 Design Requirements

As the distances between nodes in an RS-485 network become greater and greater, it becomes more of a challenge to ensure reliable communication. The increased distance often means that the reference (ground) potentials has more of a difference between nodes. These ground potential differences give rise to differences in the common-mode voltages seen by the various transceivers on the bus. Standard RS-485 transceivers are typically specified to operate over a common-mode voltage from –7 V to 12 V, which may be insufficient for larger distances. The SN65HVD2x family of devices extends this range to –20 V to 25 V, allowing for greater communication distances between nodes.

Increased cable lengths can lead to increased jitter, especially in links operating at high data rates. This increased jitter is due to the attenuation of the cable, which tends to increase with frequency. Having unequal loss between higher and lower frequencies causes the RS-485 signal to distort, adding some timing deviation (jitter) to the edge crossings of the RS-485 data. If the jitter amplitude exceeds the jitter tolerance of the receiving MCU or UART, then bit errors are likely to result in the link. However, jitter can be reduced for a given link through the use of receiver equalization.

11.2.2 Detailed Design Procedure

11.2.2.1 Noise Considerations for Equalized Receivers

The simplest way of overcoming the effects of cable losses is to increase the sensitivity of the receiver. If the maximum attenuation of frequencies of interest is 20 dB, increasing the receiver gain by a factor of ten compensates for the cable. However, this means that signal and noise are amplified. Therefore, the receiver with higher gain is more sensitive to noise and it is important to minimize differential noise coupling to the equalized receiver.

Differential noise is crated when conducted or radiated noise energy generates more voltage on one line of the differential pair than the other. For this to occur from conducted or electric far-field noise, the impedance to ground of the lines must differ.

For noise frequency out to 50 MHz, the input traces can be treated as a lumped capacitance if the receiver is approximately 10 inches or less from the connector. Therefore, matching impedance of the lines is accomplished by matching the lumped capacitance of each.

The primary factors that affect the capacitance of a trace are in length, thickness, width, dielectric material, distance from the signal return path, stray capacitance, and proximity to other conductors. It is difficult to match each of the variables for each line of the differential pair exactly, but a reasonable effort to do so keeps the lines balanced and less susceptible to differential noise coupling.

Another source of differential noise is from near-field coupling. In this situation, an assumption of equal noise-source impedance cannot be made as in the far-field. Familiarly known as crosstalk, more energy from a nearby signal is coupled to one line of the differential pair. Minimization of this differential noise is accomplished by keeping the signal pair close together and physical separation from high-voltage, high-current, or high-frequency signals.

In summary, follow these guidelines in board layout for keeping differential noise to a minimum.

- Keep the differential input traces short.
- Match the length, physical dimensions, and routing of each line of the pair.
- Keep the lines close together.
- Match components connected to each line.
- Separate the inputs from high-voltage, high-frequency, or high-current signals.

11.2.3 Application Curves

图 11-2 illustrates the benefits of integrated receiver equalization as implemented in the SN65HVD23 transceiver. In this test setup, a differential signal generator applied a signal voltage at one end of the cable, which was Belden 3105A twisted-pair shielded cable. The test signal was a pseudo-random bit stream (PRBS) of nonreturn-to-zero (NRZ) data. Channel 1 (top) shows the eye-pattern of the differential voltage at the receiver inputs (after the cable attenuation). Channel 2 (bottom) shows the output of the receiver.

图 11-3 illustrates the benefits of integrated receiver equalization as implemented in the SN65HVD24 transceiver. In this test setup, a differential signal generator applied a signal voltage at one end of the cable, which was Belden 3105A twisted-pair shielded cable. The test signal was a pseudo-random bit stream (PRBS) of nonreturn-to-zero (NRZ) data. Channel 1 (top) shows the eye-pattern of the bit stream. Channel 2 (middle) shows the eye-pattern of the differential voltage at the receiver inputs (after the cable attenuation). Channel 3 (bottom) shows the output of the receiver.

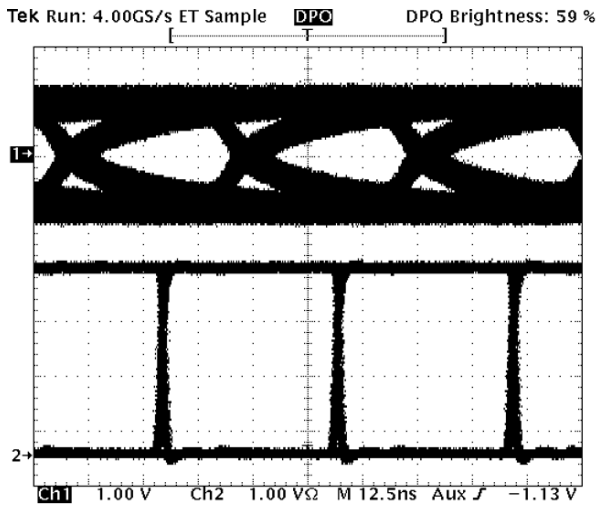


图 11-2. SN65HVD23 Receiver Performance at 25 Mbps Over 150 Meter Cable

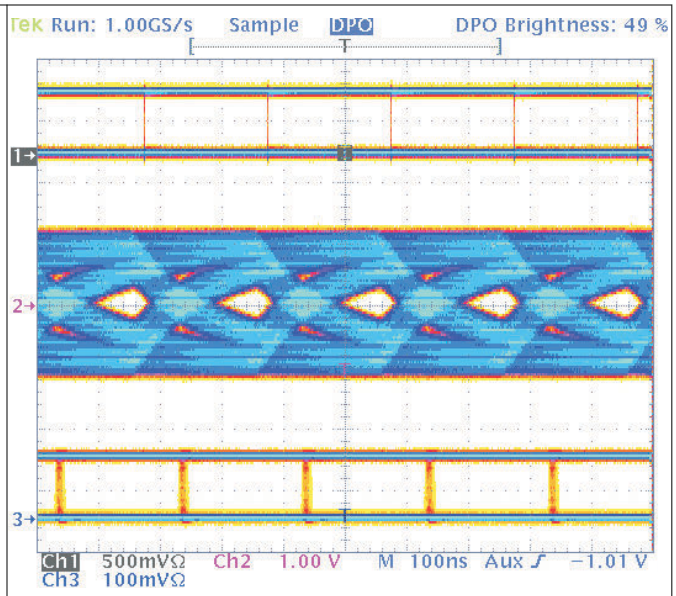


图 11-3. SN65HVD24 Receiver Performance at 5 Mbps Over 500 Meter Cable

12 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor placed as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

13 Layout

13.1 Layout Guidelines

In addition to the guidelines on differential trace matching given in 节 11.2.2, the layout guidelines below must be followed:

- Route power and ground nets as planes rather than traces, and keep their widths as large as possible to minimize resistance and inductance while maximizing parasitic capacitance.
- If external components (like transient voltage suppression diodes) are used for transient protection, place them close to the connector port and within the path of the signal lines. Make sure component capacitances are small enough not to impact the RS-485 signaling at the chosen data rate.
- Small-valued series pulse-proof resistances can be used to provide additional immunity to transients. This is needed to limit input currents if the clamping voltages of external transient protection devices exceed the absolute maximum ratings of the transceiver. These resistances must be less than 10 Ω so that the RS-485 signal is not overly attenuated.

13.2 Layout Example

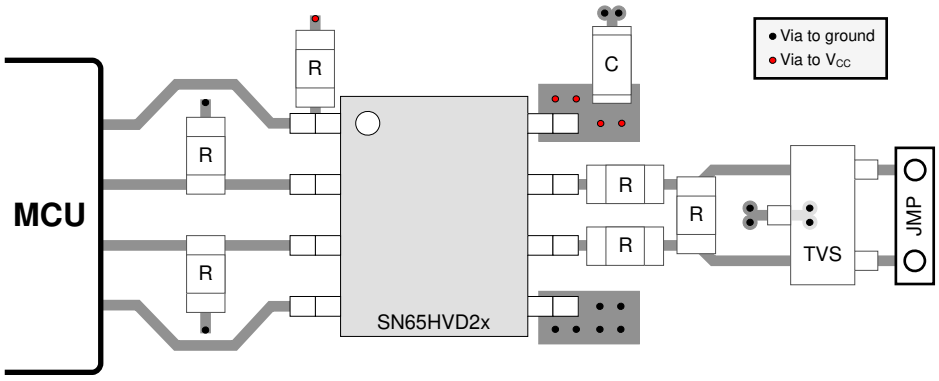


图 13-1. SN65HVD2x Layout Example

14 Device and Documentation Support

14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

14.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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14.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD20D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP20	
SN65HVD20DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP20	Samples
SN65HVD20P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65HVD20	Samples
SN65HVD21D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP21	
SN65HVD21DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP21	Samples
SN65HVD21P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65HVD21	Samples
SN65HVD22D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP22	
SN65HVD22DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP22	Samples
SN65HVD22DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP22	Samples
SN65HVD22P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65HVD22	Samples
SN65HVD23D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP23	
SN65HVD23DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP23	Samples
SN65HVD23P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65HVD23	Samples
SN65HVD24D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP24	
SN65HVD24DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP24	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

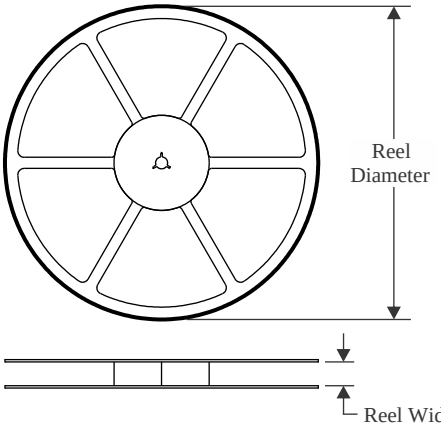
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

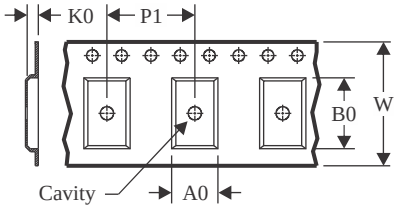
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

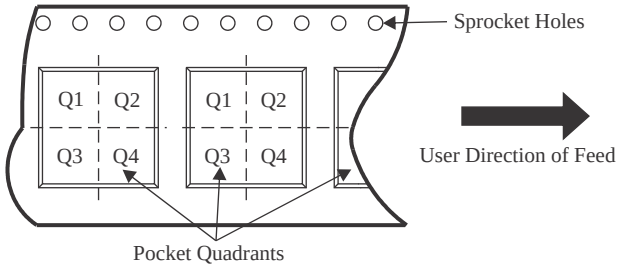


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

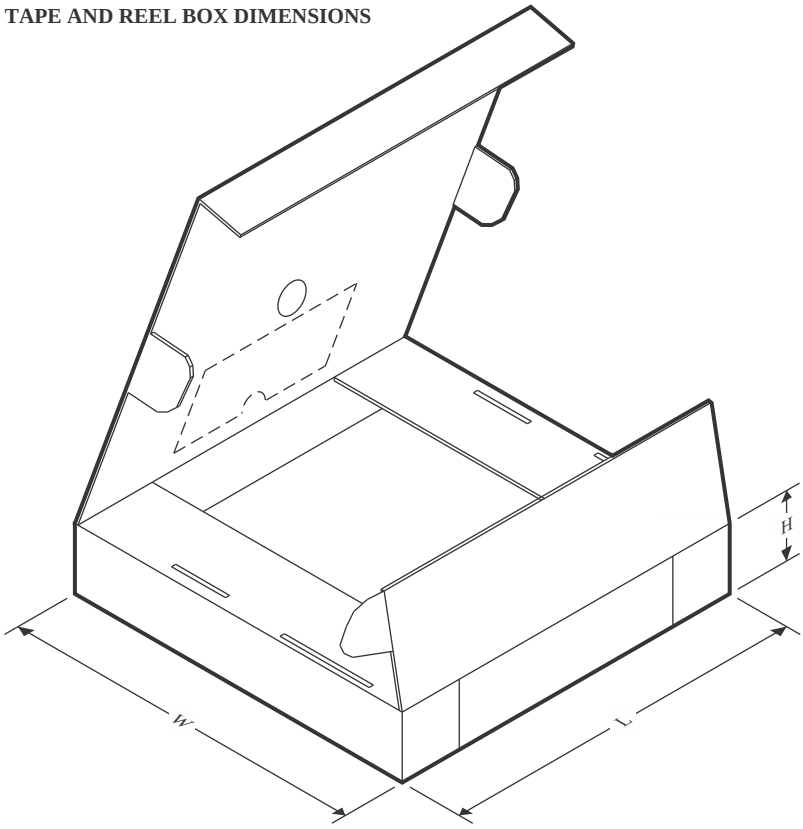
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD20DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD21DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD22DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD23DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD24DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

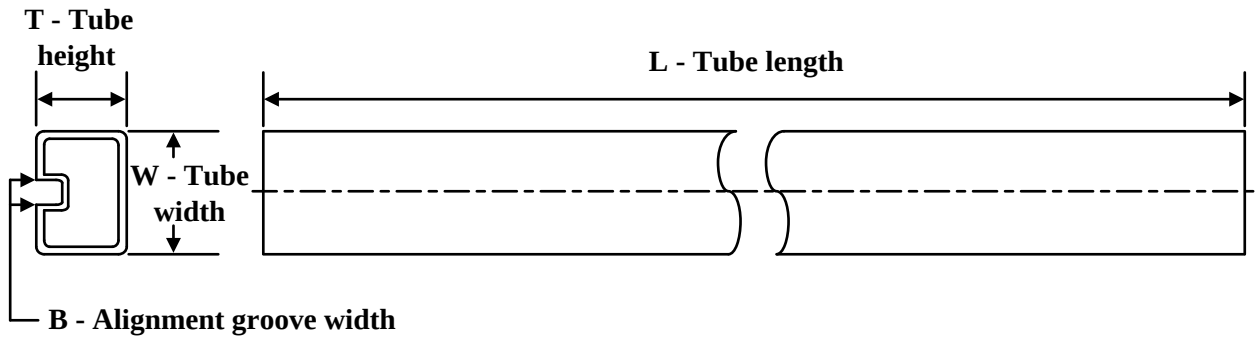
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

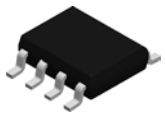
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD20DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD21DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD22DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD23DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD24DR	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD20P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD21P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD22P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD23P	P	PDIP	8	50	506	13.97	11230	4.32

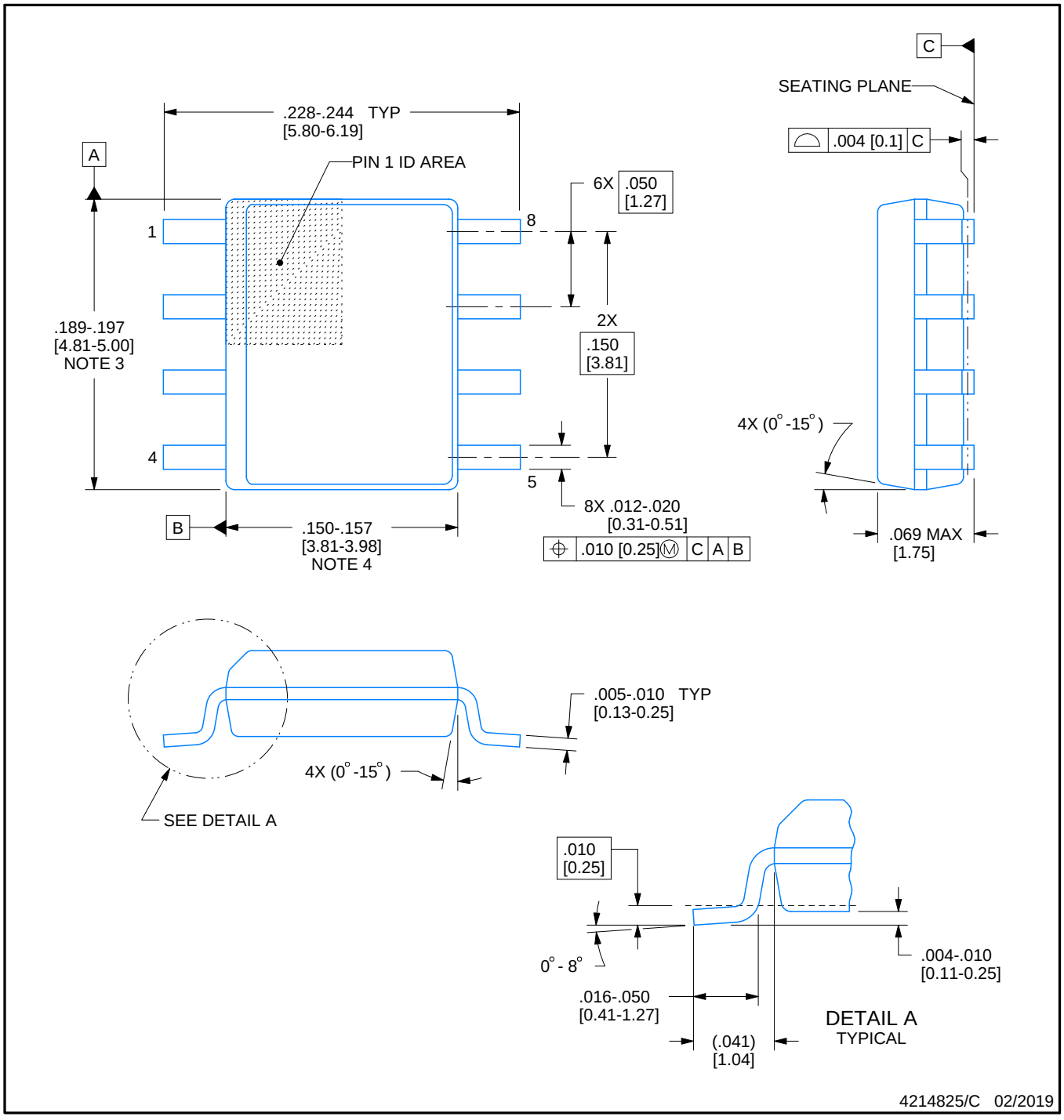


PACKAGE OUTLINE

D0008A

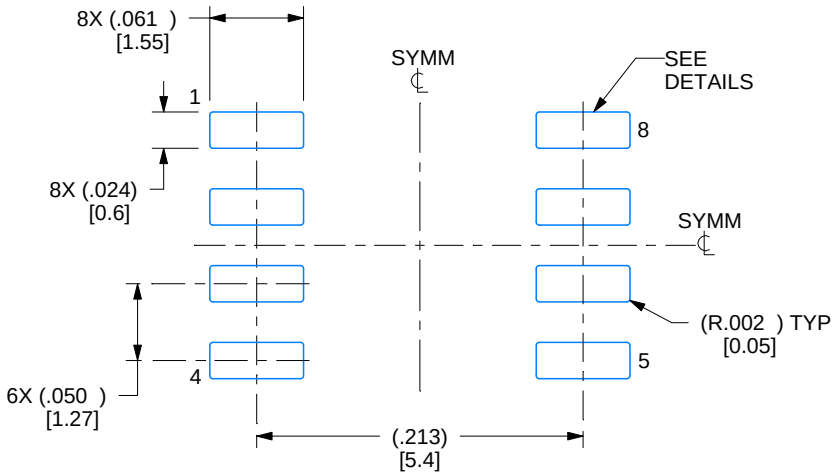
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

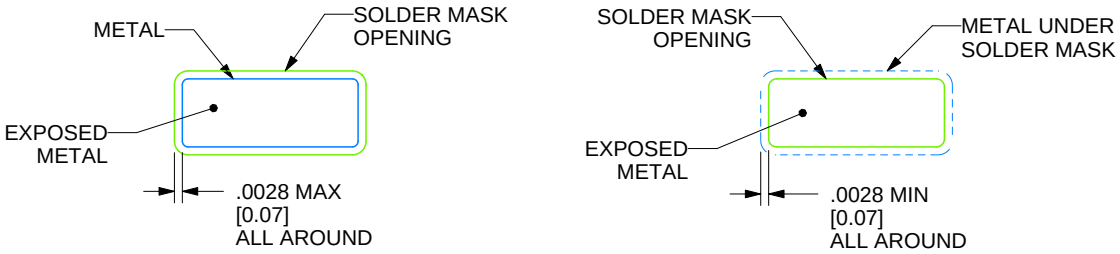


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

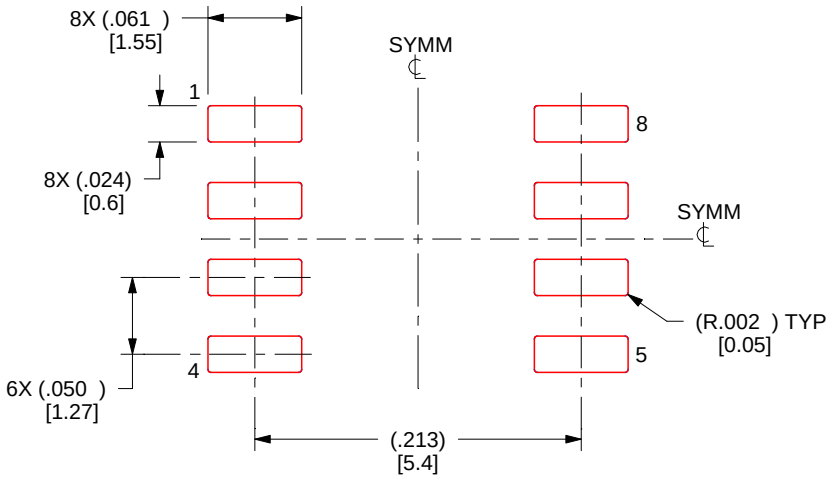
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



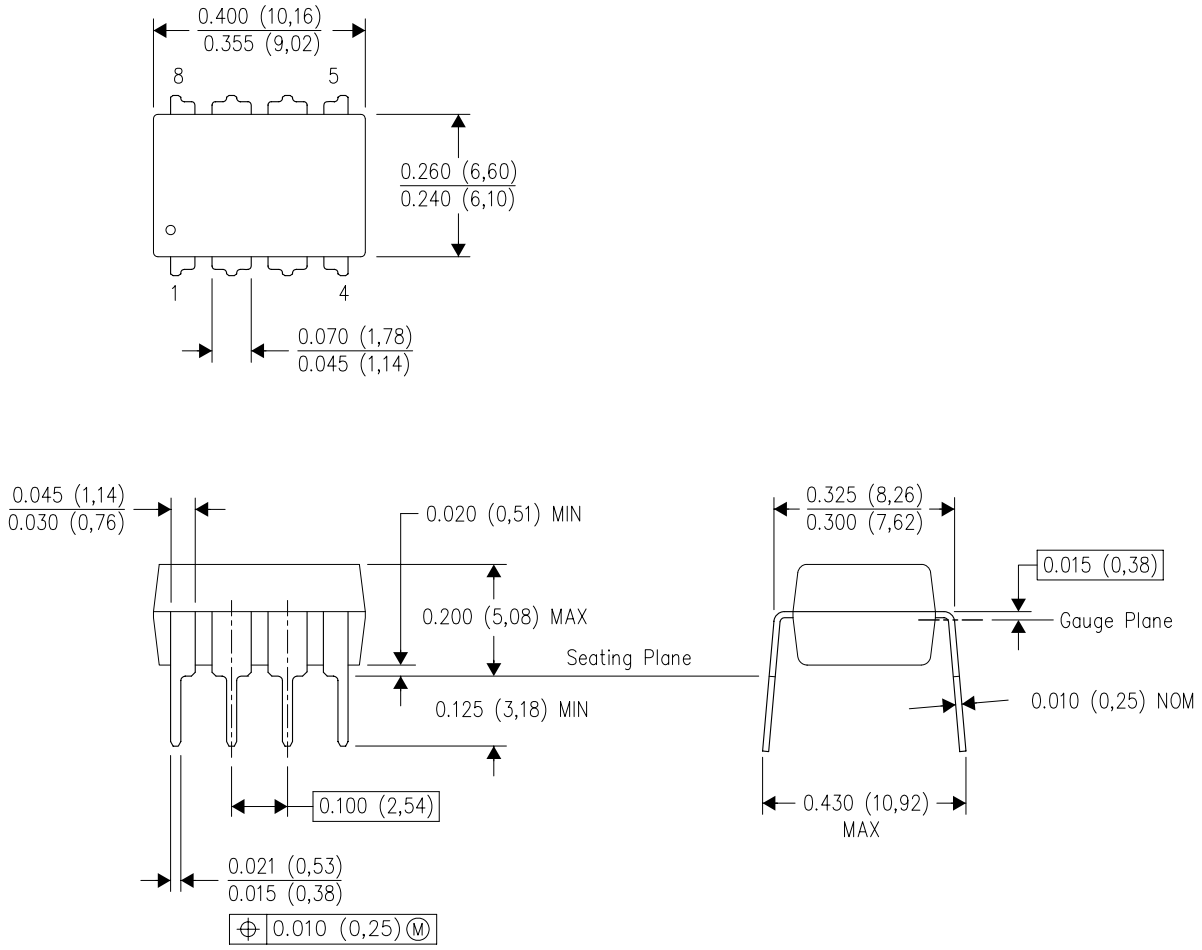
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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