

SN74LVC1G3157 单极双投模拟开关

1 特性

- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型 (A114-A)
 - 1000V 充电器件模型 (C101)
- 1.65V 至 5.5V V_{CC} 运行
- 可在 125°C 的温度下运行
- 指定的先断后合开关
- 轨到轨信号处理
- 室温下的典型工作频率为 340MHz
- 高速, 典型值为 0.5ns ($V_{CC} = 3V$, $C_L = 50pF$)
- 低导通电阻, 典型值 $\approx 6\Omega$ ($V_{CC} = 4.5V$)
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范的要求

2 应用

- 可穿戴设备和移动设备
- 便携式计算
- 物联网 (IoT)
- 音频信号路由
- 远程无线电单元
- 便携式医疗设备
- 监控
- 家庭自动化
- I2C/SPI/UART 总线多路复用
- 无线充电

3 说明

该单通道单极双投 (SPDT) 模拟开关的额定工作电压为 1.65V 至 5.5V V_{CC} 。

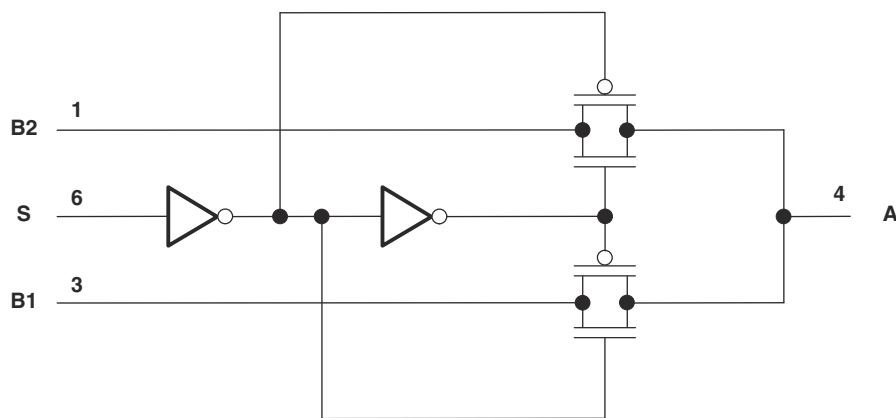
SN74LVC1G3157 器件可处理模拟信号和数字信号。SN74LVC1G3157 器件允许在任意方向传输振幅高达 V_{CC} (峰值) 的信号。

应用包括信号选通、斩波、调制或者解调 (modem), 以及针对模数和数模转换系统的信号复用。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
SN74LVC1G3157	SOT-23 (DBV) (6)	2.90mm × 1.60mm
	SC70 (DCK) (6)	2.00mm × 1.25mm
	SOT (DRL) (6)	1.60mm × 1.20mm
	SON (DRY) (6)	1.45mm × 1.00mm
	DSBGA (YZP) (6)	1.41mm × 0.91mm
	SON (DSF) (6)	1.00mm × 1.00mm
	X2SON (DTB) (6)	0.80mm × 1.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



简化版原理图



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4 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision L (May 2017) to Revision M (August 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 更新了 引脚配置和功能 部分	4
• 更新了 详细设计过程 部分中的公式	18

Changes from Revision K (January 2017) to Revision L (May 2017)	Page
• 删除了 特性 中的“用于模拟和数字应用”	1
• 删除了 特性 中的“高度线性”	1
• 将 说明 中的第一句从“该单极双投 (SPDT)...”更改为“该单通道单极双投 (SPDT)...”	1
• 向 器件信息 添加了 X2SON (DTB) 封装	1
• 向 引脚配置和功能 添加了 X2SON (DTB) 封装	4
• I/O 已更改为：I _{I/O} K (对于绝对最大额定值中的 I/O 端口二极管电流)	6
• 在 热性能信息 表中添加了 DTB (X2SON) 封装	7
• 更改了 模拟开关特性 表中的注释 1 和注释 2	9
• 删除了 模拟开关特性 表中的注释 3 “由设计指定”	9
• 从 开关特性 85°C 表中删除了注释 4 “根据设计确定”	10
• 从 开关特性 125°C 表中删除了注释 4 “根据设计确定”	10
• 更改了图 7-2，从 SW1 = V _{IL} 更新为 SW1 = V _{IH} ，从 SW2 = V _{IH} 更新为：SW2 = V _{IL}	11
• 更改了图 7-5	11
• 在图 7-6 中的 B1 上添加了一个串联 50 Ω 电阻器	11
• 更改了图 7-7	11

Changes from Revision J (June 2016) to Revision K (January 2017)	Page
• 向 应用 部分添加了新的应用	1
• 在 建议运行条件 中为 BGA 以及所有其他封装添加了自然通风工作温度范围 T _A	7
• 在 电气特性 表中添加了 125°C 数据	8
• 在标题中添加了 85°C，以便与新的 125°C 开关特性 部分进行区分	10

- 添加了 125°C 开关特性 部分和数据。 10

Changes from Revision I (June 2015) to Revision J (June 2016) Page

- 删除了特性中的 200V 机器模型 (A115-A)..... 1
- 将特性从“室温下的典型工作频率为 300MHz”更改为“室温下的典型工作频率为 340MHz” 1
- 更新了器件信息表..... 1
- 更新了所有封装的引脚排列图..... 4
- 在绝对最大额定值中添加了贮存温度、 T_{stg} 和结温 T_J 的温度范围..... 6
- 将电气特性表中 I_{off} 和 I_{IN} 的 MAX 值更新为 ± 1 至 ± 0.1 8
- 添加了接收文档更新通知 部分..... 20

Changes from Revision H (May 2012) to Revision I (June 2015) Page

- 添加了器件信息表、引脚配置和功能 部分、ESD 等级表、特性说明 部分、器件功能模式 部分、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分..... 1
- 更新了特性 1

Changes from Revision G (September 2011) to Revision H (May 2012) Page

- 使用正确的引脚标签更改了 YZP。 4
- 新增了热性能信息表..... 7
- 已更改为正确的引脚标签“S” 8

5 引脚配置和功能

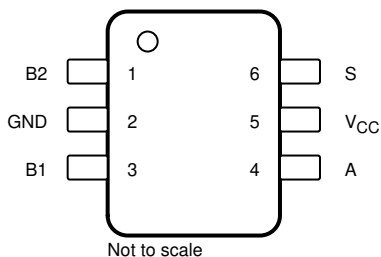


图 5-1. DBV 封装, 6 引脚 SOT-23 (顶视图)

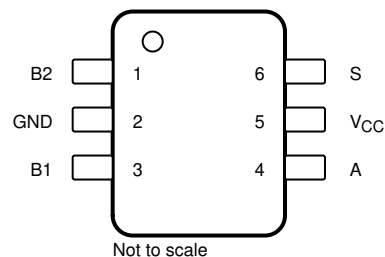


图 5-2. DCK 封装、6 引脚 SC70 (顶视图)

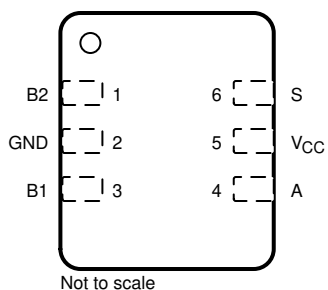


图 5-3. DRY 封装、6 引脚 SON (顶视图)

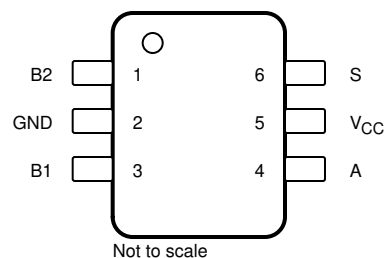


图 5-4. DRL 封装、6 引脚 SOT (顶视图)

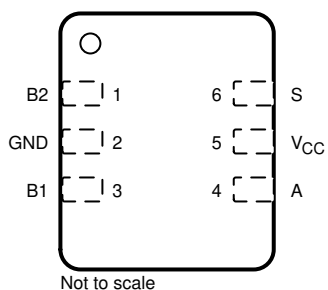


图 5-5. DSF 封装、6 引脚 SON (顶视图)

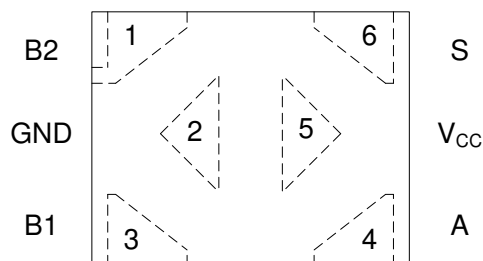


图 5-6. DTB 封装、6 引脚 X2SON (顶视图)

表 5-1. 引脚功能

引脚		类型 ⁽¹⁾	说明
名称	SOT-23、SC70、SON、X2SON 或 SOT		
B2	1	I/O	开关 I/O。将 S 设置为高电平以启用。
GND	2	P	接地
B1	3	I/O	开关 I/O。将 S 设置为低电平以启用。
A	4	I/O	普通端子
V _{CC}	5	P	电源
S	6	I	选择

(1) I = 输入 ; O = 输出 ; P = 电源

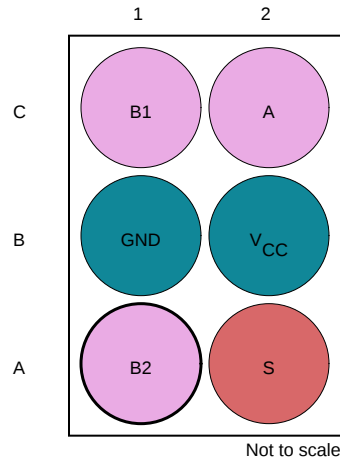


图 5-7. YZP 封装、6 引脚 DSBGA (底视图)

图例	
输入	输入或输出
电源	

表 5-2. 引脚功能

引脚		类型 ⁽¹⁾	说明
编号	名称		
A1	B2	I/O	开关 I/O。将 S 设置为高电平以启用。
A2	S	I	选择
B1	GND	P	接地
B2	V _{CC}	P	电源
C1	B1	I/O	开关 I/O。将 S 设置为低电平以启用。
C2	A	I/O	普通端子

(1) I = 输入 ; O = 输出 ; P = 电源

6 规格

6.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得 (除非另有说明) ⁽¹⁾

		最小值	最大值	单位
V_{CC}	电源电压 ⁽²⁾	-0.5	6.5	V
V_{IN}	控制输入电压 ^{(2) (3)}	-0.5	6.5	V
$V_{I/O}$	开关 I/O 电压 ^{(2) (3) (4) (5)}	-0.5	$V_{CC}+0.5$	V
I_{IK}	控制输入钳位电流	$V_{IN} < 0$	-50	mA
$I_{I/OK}$	I/O 端口二极管电流	$V_{I/O} < 0$ 或 $V_{I/O} > V_{CC}$	± 50	mA
$I_{I/O}$	导通状态开关电流 ⁽⁶⁾	$V_{I/O} = 0$ 至 V_{CC}	± 128	mA
	通过 V_{CC} 或 GND 的持续电流		± 100	mA
T_J	结温		150	°C
T_{stg}	存储温度	-65	150	°C

- (1) 应力超出绝对最大额定值下列出的值可能会对器件造成损坏。这些仅为压力额定值，并不表示器件在这些条件下以及在建议运行条件以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
- (2) 除非另有说明，否则所有电压均以接地为基准。
- (3) 如果遵守输入和输出钳位电流额定值，则可能会超过输入和输出负电压额定值。
- (4) 该值被限制为最大 5.5V。
- (5) V_I 、 V_O 、 V_A 和 V_{Bn} 用于表示 $V_{I/O}$ 的特定条件。
- (6) I_I 、 I_O 、 I_A 和 I_{Bn} 用于表示 $I_{I/O}$ 的特定条件。

6.2 ESD 等级

		值	单位
$V_{(ESD)}$	静电放电		
	人体放电模型 (HBM), 符合 ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
充电器件模型 (CDM), 符合 JEDEC 规范 JESD22-C101 ⁽²⁾	± 1000		

- (1) JEDEC 文档 JEP155 指出: 500V HBM 能够在标准 ESD 控制流程下安全生产。
- (2) JEDEC 文件 JEP157 指出: 250V CDM 可实现在标准 ESD 控制流程下安全生产。

6.3 建议运行条件

在自然通风条件下的工作温度范围内测得 (除非另有说明) (1)

		最小值	最大值	单位	
V _{CC}	电源电压	1.65	5.5	V	
V _{I/O}	开关输入或输出电压	0	V _{CC}	V	
V _{IN}	控制输入电压	0	5.5	V	
V _{IH}	高电平输入电压, 控制输入	V _{CC} =1.65V 至 1.95V	V _{CC} × 0.75	V	
		V _{CC} = 2.3V 至 5.5V	V _{CC} × 0.7		
V _{IL}	低电平输入电压, 控制输入	V _{CC} =1.65V 至 1.95V	V _{CC} × 0.25	V	
		V _{CC} = 2.3V 至 5.5V	V _{CC} × 0.3		
Δt/Δv	输入转换上升或下降速率	V _{CC} =1.65V 至 1.95V	20	ns/V	
		V _{CC} =2.3V 至 2.7V	20		
		V _{CC} =3V 至 3.6V	10		
		V _{CC} = 4.5V 至 5.5V	10		
T _A	自然通风工作温度	BGA 封装 (YZP)	- 40	85	°C
		所有其他封装 (DBV、DCK、DRL、DRY、DSF)	-40	125	°C

(1) 器件所有的未使用输入必须被保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 [慢速或浮点 CMOS 输入的影响 \(SCBA004\)](#)。

6.4 热性能信息

热指标 ⁽¹⁾	SN74LVC1G3157						单位	
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	DTB (X2SON)	YZP (DSBGA)		
	6 引脚	6 引脚	6 引脚	6 引脚	6 引脚	6 引脚		
R _{θJA}	结至环境热阻	234.9	269.5	244.1	284.2	324.5	129.4	°C/W
R _{θJC(top)}	结至外壳 (顶部) 热阻	150.4	189.5	112.5	138.6	150.5	1.9	°C/W
R _{θJB}	结至电路板热阻	86.4	84.7	109.9	170.9	239.0	40.0	°C/W
ψ _{JT}	结至顶部特征参数	60.8	62.7	9.3	13.7	17.2	0.6	°C/W
ψ _{JB}	结至电路板特征参数	86.1	84.0	109.3	167.9	238.3	40.2	°C/W
R _{θJC(bot)}	结至外壳 (底部) 热阻	不适用	不适用	不适用	不适用	不适用	不适用	°C/W

(1) 有关新旧热指标的更多信息, 请参阅 [半导体和 IC 封装热指标](#) 应用报告。

6.5 电气特性

在推荐的自然通风条件下的工作温度范围 (除非另外注明)

参数	测试条件		V _{CC}	T _A = -40 至 85°C			T _A = -40 至 125°C			单位
				最小值	典型值 ⁽¹⁾	最大值	最小值	典型值 ⁽¹⁾	最大值	
r _{on} 导通状态开关电阻 ⁽²⁾	请参阅图 6-1 和图 7-1	V _I = 0V	I _O = 4 mA	1.65V	11	20	11	20	Ω	
		V _I = 1.65V	I _O = -4 mA		15	50	15	50		
		V _I = 0V	I _O = 8 mA	2.3V	8	12	8	12		
		V _I = 2.3V	I _O = -8 mA		11	30	11	30		
		V _I = 0V	I _O = 24 mA	3V	7	9	7	9		
		V _I = 3V	I _O = -24 mA		9	20	9	20		
		V _I = 0V	I _O = 30 mA	4.5V	6	7	6	7		
		V _I = 2.4V	I _O = -30 mA		7	12	7	12		
V _I = 4.5V	I _O = -30 mA	7	15		7	15				
r _{range} 信号范围内的导通状态开关电阻 ^{(2) (3)}	0 ≤ V _{Bn} ≤ V _{CC} (请参阅图 6-1 和图 7-1)	I _A = -4mA	1.65V	140	140	Ω				
		I _A = -8mA	2.3V	45	45					
		I _A = -24mA	3V	18	18					
		I _A = -30mA	4.5V	10	10					
Δ r _{on} 开关之间导通状态电阻的差异 ^{(2) (4) (5)}	请参阅图 7-1	V _{Bn} = 1.15V	I _A = -4mA	1.65V	0.5	0.5	Ω			
		V _{Bn} = 1.6V	I _A = -8mA	2.3V	0.1	0.3				
		V _{Bn} = 2.1V	I _A = -24mA	3V	0.1	0.3				
		V _{Bn} = 3.15V	I _A = -30mA	4.5V	0.1	0.2				
r _{on(flat)} 导通电阻稳定性 ^{(2) (4) (6)}	0 ≤ V _{Bn} ≤ V _{CC}	I _A = -4mA	1.65V	110	110	Ω				
		I _A = -8mA	2.3V	26	40					
		I _A = -24mA	3V	9	10					
		I _A = -30mA	4.5V	4	5					
I _{off} ⁽⁷⁾ 关断状态开关漏电流	0 ≤ V _I , V _O ≤ V _{CC} (请参阅图 7-2)	1.65V 至 5.5V	±1	±1	μA					
I _{S(on)} 导通状态开关漏电流	V _I = V _{CC} 或 GND, V _O = 开 (请参阅图 7-3)	5.5V	±1	±1	μA					
I _{IN} 控制输入电流	0 ≤ V _{IN} ≤ V _{CC}	0V 至 5.5V	±1	±1	μA					
I _{CC} 电源电流	S = V _{CC} 或 GND	5.5V	1	10	35	μA				
Δ I _{CC} 电源电流变化	S = V _{CC} - 0.6V	5.5V	500	500	μA					
C _i 控制输入电容	S	5V	2.7	2.7	pF					
C _{io(off)} 开关输入/输出电容	Bn	5V	5.2	5.2	pF					
C _{io(on)} 开关输入/输出电容	Bn	5V	17.3	17.3	pF					
	A		17.3	17.3						

(1) T_A = 25°C

(2) 在通过开关的指示电流下由 I/O 引脚之间的电压降测量。通态电阻由两个 (A 或 B) 端口上的较低电压决定。

(3) 由设计指定

(4) Δ r_{on} = r_{on(max)} - r_{on(min)}, 在相同的 V_{CC}、温度或电压电平下测得

(5) 此参数已表征, 但未经生产测试。

(6) 平坦度定义为在指定条件范围内导通状态电阻的最大值和最小值之间的差异。

(7) I_{off} 与 I_{S(off)} 相同 (关断状态开关漏电流) 。

6.6 模拟开关特性

$T_A = 25^\circ\text{C}$

参数	FROM (输入)	TO (输出)	测试条件	V_{CC}	典型值	单位
频率响应 ⁽¹⁾ (开关导通)	A 或 Bn	Bn 或 A	$R_L = 50\Omega$, f_{in} = 正弦波 (请参阅图 7-5)	1.65V	340	MHz
				2.3V	340	
				3V	340	
				4.5V	340	
串扰 ⁽²⁾ (开关间)	B1 或 B2	B2 或 B1	$R_L = 50\Omega$, $f_{in} = 10\text{MHz}$ (正弦波) (请参阅图 7-6)	1.65V	-54	dB
				2.3V	-54	
				3V	-54	
				4.5V	-54	
馈通衰减 ⁽²⁾ (开关关闭)	A 或 Bn	Bn 或 A	$C_L = 5\text{pF}$, $R_L = 50\Omega$, $f_{in} = 10\text{MHz}$ (正弦波) (请参阅图 7-7)	1.65V	-57	dB
				2.3V	-57	
				3V	-57	
				4.5V	-57	
电荷注入	S	A	$C_L = 0.1\text{nF}$, $R_L = 1\text{M}\Omega$ (请参阅图 7-8)	3.3V	3	pC
				5V	7	
总谐波失真	A 或 Bn	Bn 或 A	$V_I = 0.5\text{V}_{p-p}$, $R_L = 600\Omega$, $f_{in} = 600\text{Hz}$ 至 20kHz (正弦波) (请参阅图 7-9)	1.65V	0.1%	
				2.3V	0.025%	
				3V	0.015%	
				4.5V	0.01%	

- (1) 将 f_{in} 设置为 0dBm 并提供 0.4V 的偏压。增大 f_{in} 频率，直到增益低于插入损耗 3dB。
 (2) 将 f_{in} 设置为 0dBm 并提供 0.4V 的偏压。

6.7 开关特性 85°C

$T_A = -40$ 至 $+85^\circ\text{C}$ (请参阅图 7-4 和图 7-10)

参数	FROM (输入)	TO (输出)	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		$V_{CC} = 5\text{V} \pm 0.5\text{V}$		单位
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
$t_{pd}^{(1)}$	A 或 Bn	Bn 或 A	2		1.2		0.8		0.3		ns
$t_{en}^{(2)}$	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
$t_{dis}^{(3)}$			3	13	2	7.5	1.5	5.3	0.8	3.8	
t_{B-M}			0.5		0.5		0.5		0.5		ns

(1) t_{pd} 为 t_{PLH} 或 t_{PHL} 的较低者。当由一个理想电压源 (零输出阻抗) 驱动时, 传播延迟是使用开关导通状态电阻典型值和额定负载电容计算得出的 RC 时间常数。

(2) t_{en} 为 t_{PZL} 或 t_{PZH} 的较低者。

(3) t_{dis} 为 t_{PLZ} 或 t_{PHZ} 的较低者。

6.8 开关特性 125°C

$T_A = -40$ 至 $+125^\circ\text{C}$ (请参阅图 7-4 和图 7-10)

参数	FROM (输入)	TO (输出)	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		$V_{CC} = 5\text{V} \pm 0.5\text{V}$		单位
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
$t_{pd}^{(1)}$	A 或 Bn	Bn 或 A	2		1.2		0.8		0.5		ns
$t_{en}^{(2)}$	S	Bn	1	24.5	1	14.5	2.5	8	1.7	6	ns
$t_{dis}^{(3)}$			2.5	13.5	2	8	1.5	5.5	0.8	4	
t_{B-M}			0.5		0.5		0.5		0.5		ns

6.9 典型特性

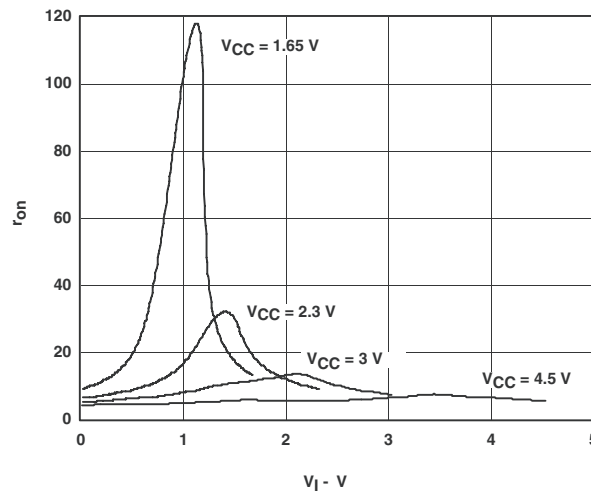


图 6-1. 典型 r_{on} 与输入电压 (V_I) 之间的函数关系 ($V_I = 0$ 至 V_{CC})

7 参数测量信息

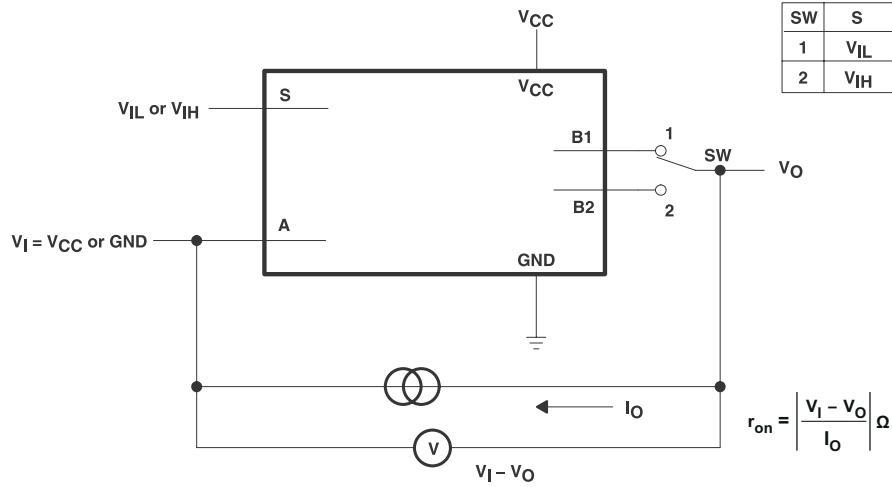


图 7-1. 导通电阻测试电路

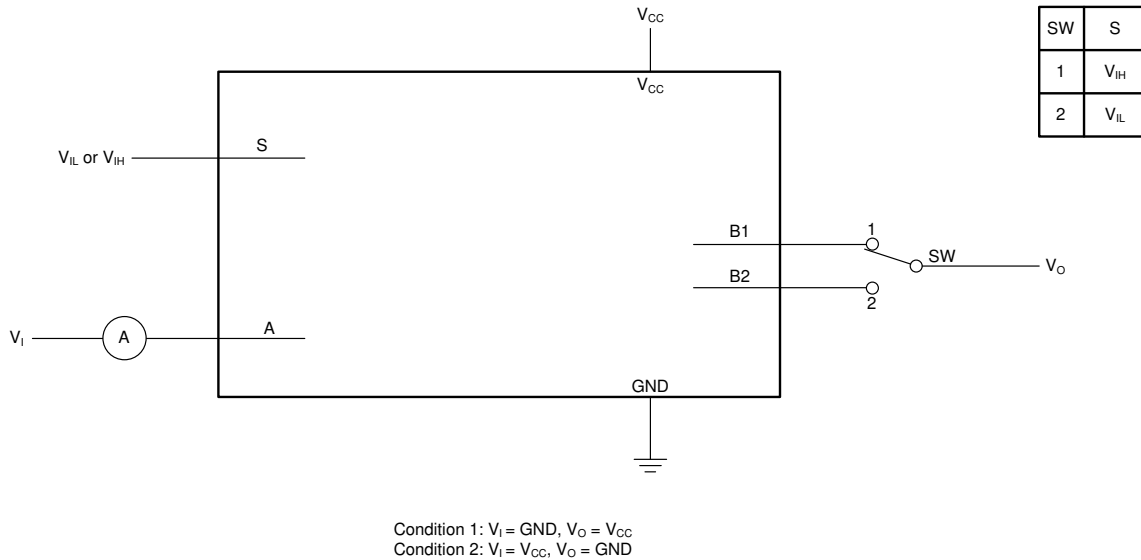


图 7-2. 关断状态开关漏电流测试电路

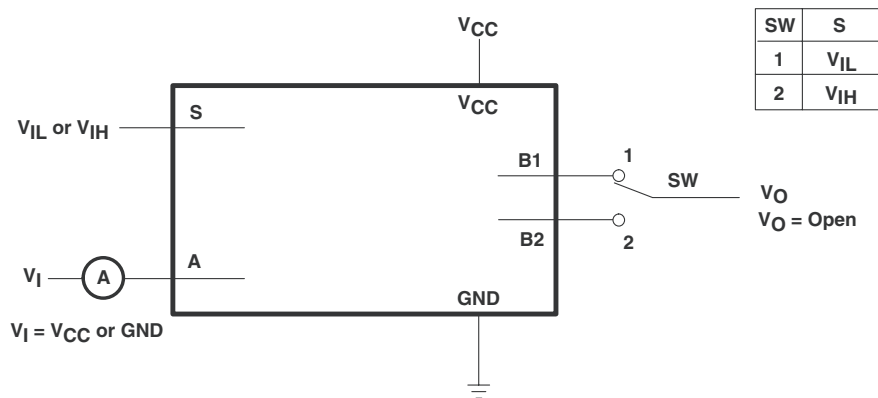
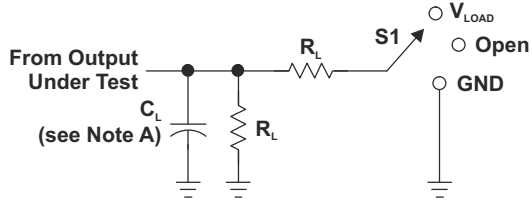


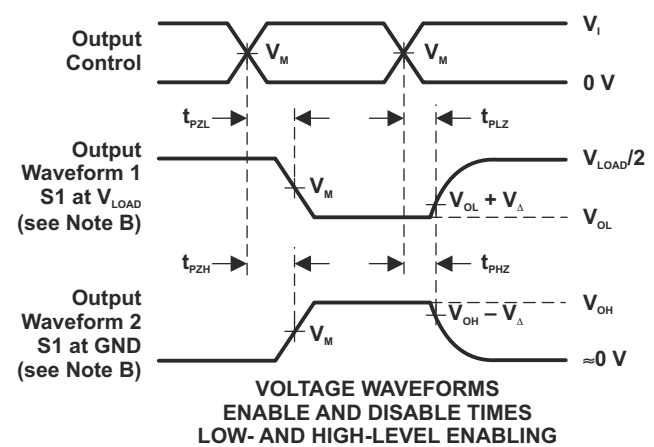
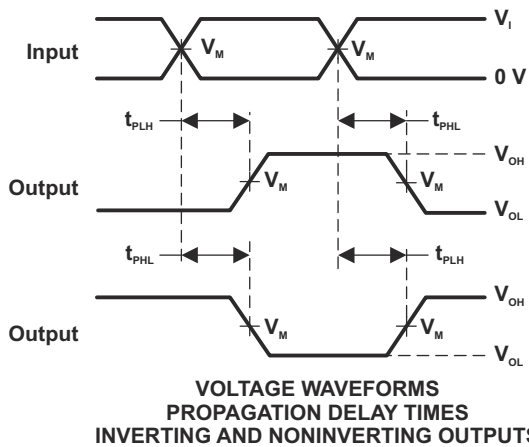
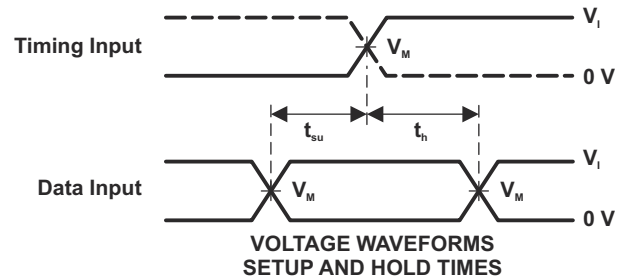
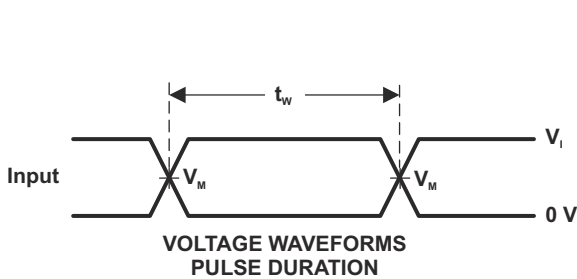
图 7-3. 导通状态开关漏电流测试电路



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_f/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

图 7-4. 负载电路和电压波形

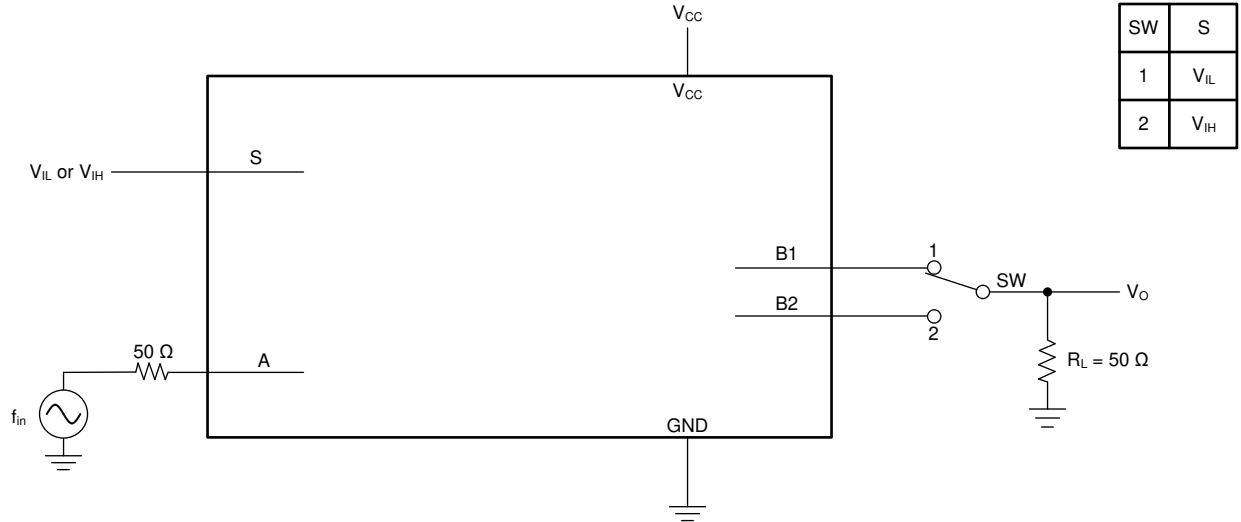


图 7-5. 频率响应 (开关导通)

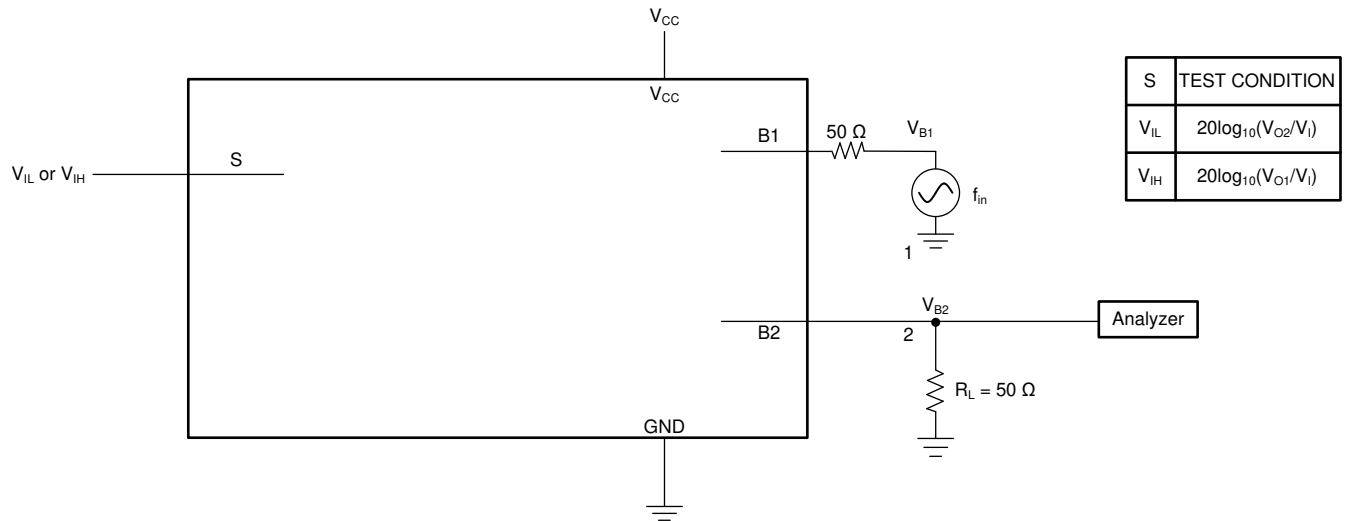


图 7-6. 串扰 (开关间)

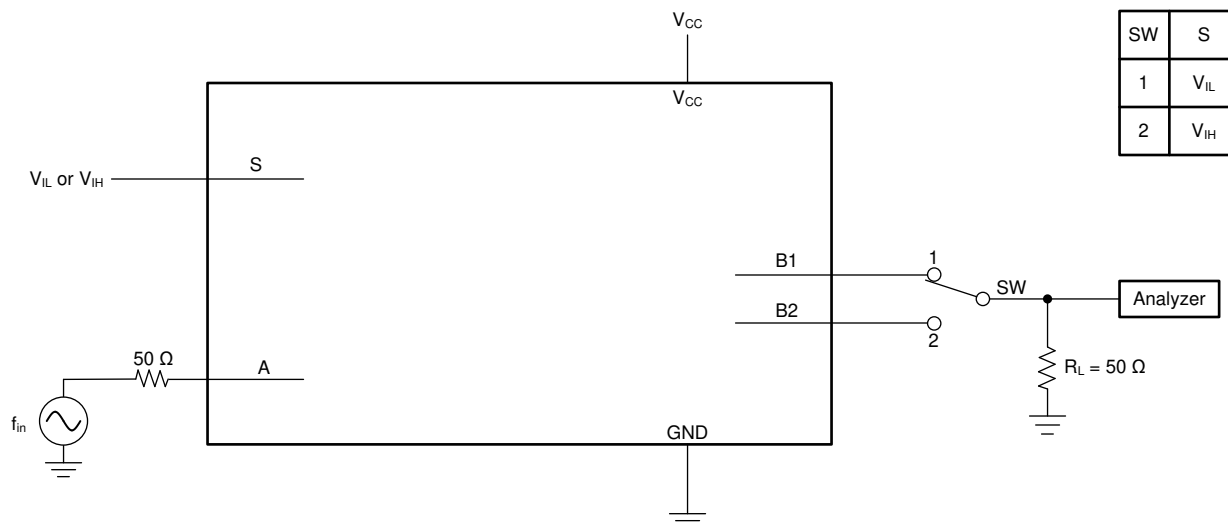


图 7-7. 馈通

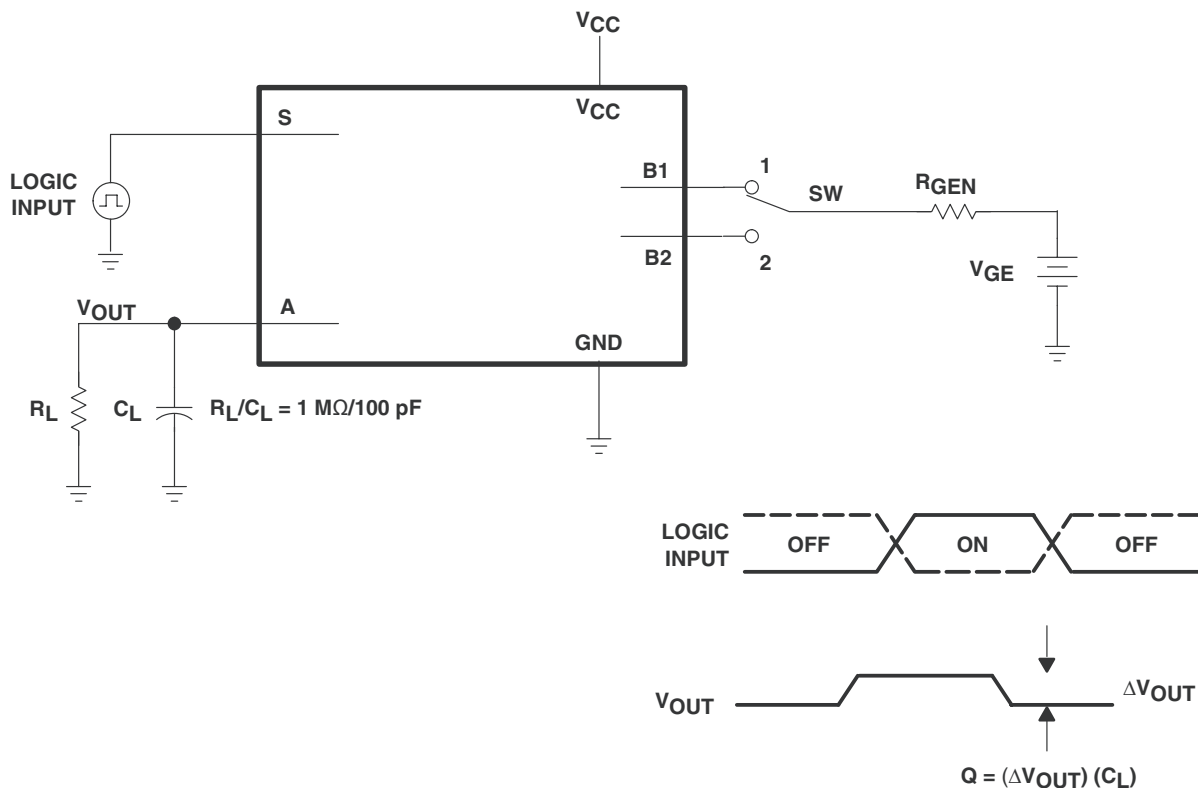


图 7-8. 电荷注入测试

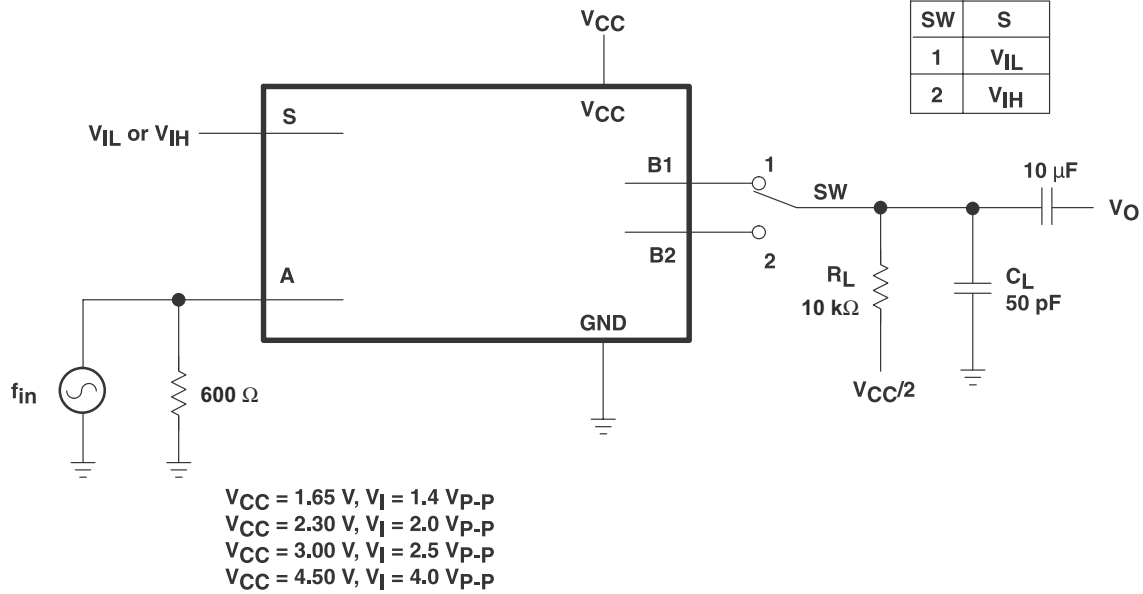


图 7-9. 总谐波失真

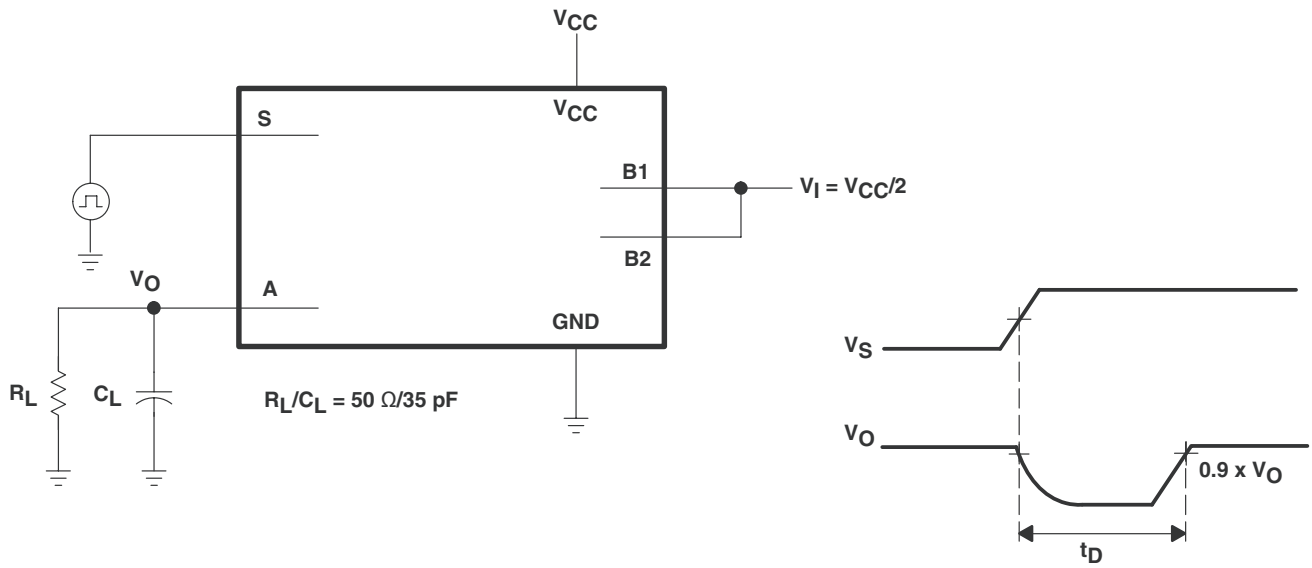


图 7-10. 先断后合内部时序

8 详细说明

8.1 概述

SN74LVC1G3157 器件是一种单极双投 (SPDT) 模拟开关, 设计工作电压范围为 1.65V 至 5.5V V_{CC} 。SN74LVC1G3157 器件可处理模拟信号和数字信号。该器件允许在任意方向传输振幅高达 V_{CC} (峰值) 的信号。

8.2 功能框图

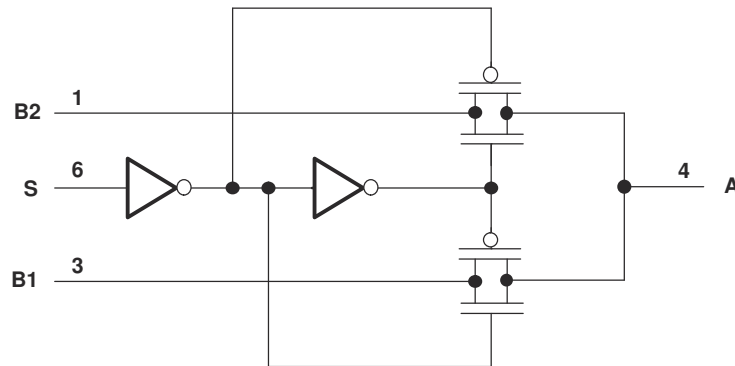


图 8-1. 逻辑图 (正逻辑)

8.3 特性说明

由 1.65V 至 5.5V 电源供电允许该器件在由不同逻辑电平组成的许多不同系统中运行, 从而实现轨到轨信号切换。根据控制输入激活 B1 通道或 B2 通道。如果控制输入为低电平, 则选择 B1 通道。如果控制输入为高电平, 则选择 B2 通道。

8.4 器件功能模式

表 8-1 列出了选择其中一个控制输入时的导通通道。

表 8-1. 功能表

控制输入	导通通道
L	B1
H	B2

9 应用和实现

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 应用信息

SN74LVC1G3157 SPDT 模拟开关足够灵活，可用于各种电路，例如模拟音频路由、加电监视器、内存共享等。有关应用的详细信息，请参阅 [SN74LVC1G3157](#) 和 [SN74LVC2G53 SPDT 模拟开关](#)。

9.2 典型应用

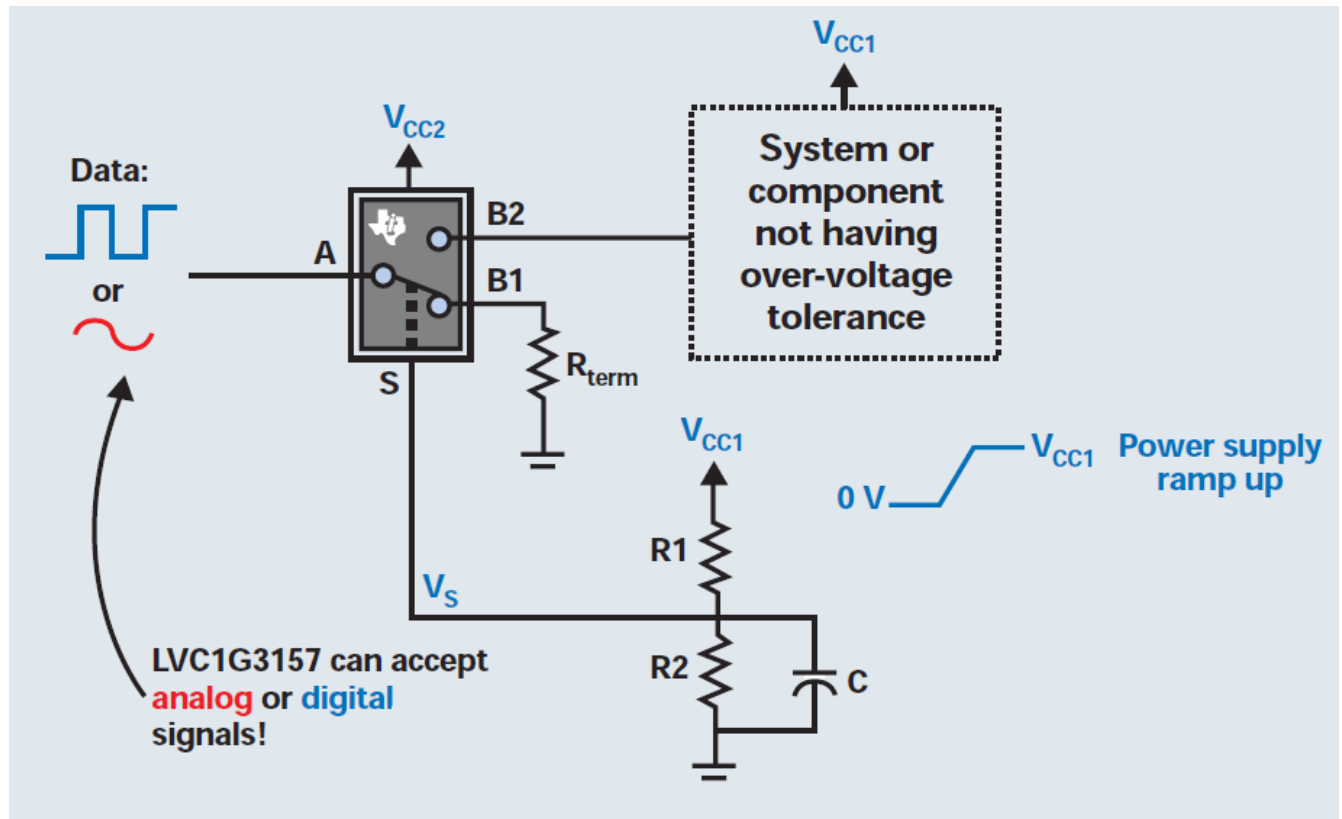


图 9-1. 典型应用原理图

9.2.1 设计要求

输入可以是模拟输入或数字输入，但 TI 建议在施加任何信号之前等待 V_{CC} 上升到 [节 6.3](#) 中的电平。应根据信号类型和规格使用适当的终端电阻器。选择引脚不应悬空；上拉或下拉时使用可由 GPIO 过驱动的电容器。

9.2.2 详细设计过程

使用此电路创意，系统设计人员可以确保组件或子系统电源在允许信号施加到其输入之前斜升。这对于没有过压耐受输入的集成电路很有用。基本思路是在 VCC1 电源轨上使用电阻分压器，该分压器正在斜升。电阻分压器的 RC 时间常数进一步延迟了 SPDT 总线开关选择引脚上的电压斜坡。通过仔细选择 R1、R2 和 C 的值，可以确保 VCC1 在从 A 到 B2 的路径建立之前达到其标称值，从而防止在器件/系统上电之前 I/O 上出现信号通电。为了确保实现所需的极低延迟，设计人员应使用方程式 1 来计算从接地转换 (0V) 到电源电压 (VCC1/2) 一半所需的时间。

$$\text{Set} \left(\frac{R2}{R1 + R2} \times V_{CC1} > V_{IH} \right) \text{ of the select pin} \quad (1)$$

选择 Rs 和 C 以获得所需的延迟。

当 V_S 变为高电平时，信号将被传递。

9.2.3 应用曲线

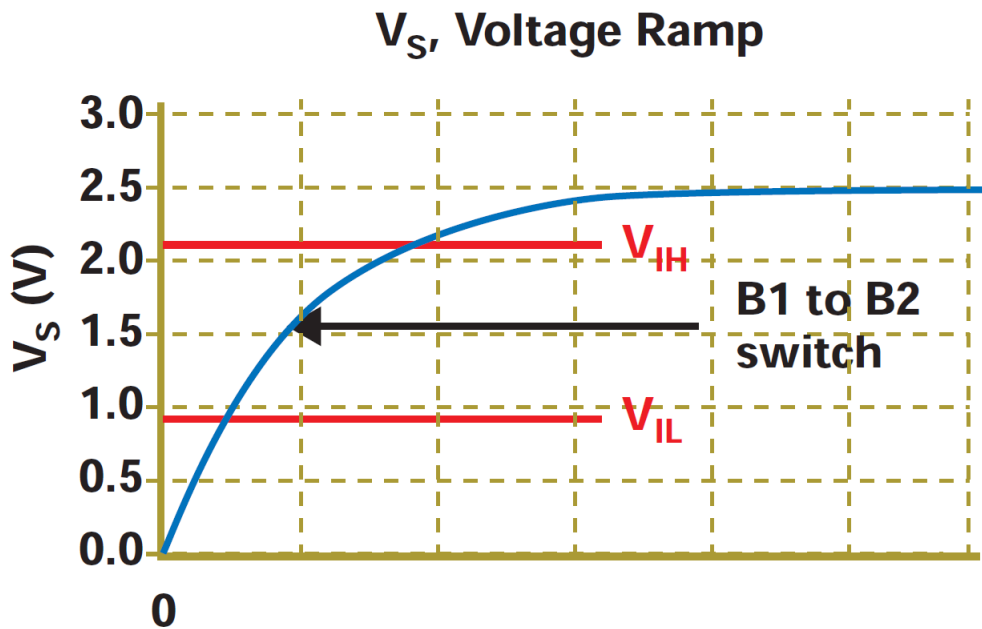


图 9-2. V_S 电压斜坡

10 电源相关建议

大多数系统有一个常见的 3.3V 或 5V 电源轨，可为该器件的 V_{CC} 引脚供电。如果这不可用，则可以使用开关模式电源 (SMPS) 或线性压差稳压器 (LDO) 从另一个电压轨为该器件供电。

11 布局

11.1 布局指南

TI 建议使信号线路尽可能短。TI 还建议在信号线长度大于 1 英寸时采用微带线或带状线技术。根据应用的要求，这些布线的特征阻抗必须设计为 $50\ \Omega$ 或 $75\ \Omega$ 。不要将此器件放置在离高压开关元件太近的地方，因为它们可能会干扰器件。

11.2 布局示例

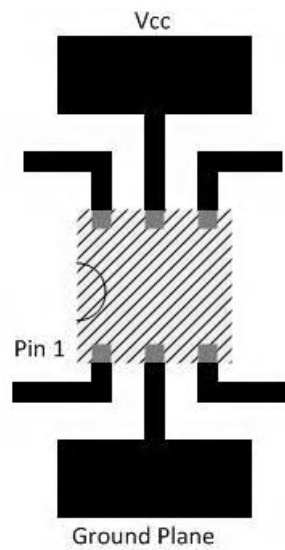


图 11-1. 推荐布局示例

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI), [慢速或浮点 CMOS 输入的影响](#)
- 德州仪器 (TI), [SN74LVC1G3157 和 SN74LVC2G53 SPDT 模拟开关](#)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

12.4 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1G3157DBVRE4	LIFEBUY	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CC5F, CC5R)	
74LVC1G3157DBVRG4	LIFEBUY	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CC5F, CC5R)	
74LVC1G3157DCKRE4	LIFEBUY	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)	
74LVC1G3157DCKRG4	LIFEBUY	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)	
74LVC1G3157DRYRG4	LIFEBUY	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5	
SN74LVC1G3157DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S	Samples
SN74LVC1G3157DCK3	LIFEBUY	SC70	DCK	6	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	C5Z	
SN74LVC1G3157DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)	Samples
SN74LVC1G3157DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)	Samples
SN74LVC1G3157DRY2	LIFEBUY	SON	DRY	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C5	
SN74LVC1G3157DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DTBR	ACTIVE	X2SON	DTB	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X	Samples
SN74LVC1G3157YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G3157 :

- Automotive : [SN74LVC1G3157-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G3157DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G3157DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G3157DRY2	SON	DRY	6	5000	180.0	8.4	1.65	1.2	0.7	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G3157DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	180.0	9.5	0.94	1.13	0.41	2.0	8.0	Q2
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G3157DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G3157DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DRY2	SON	DRY	6	5000	202.0	201.0	28.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	189.0	185.0	36.0
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

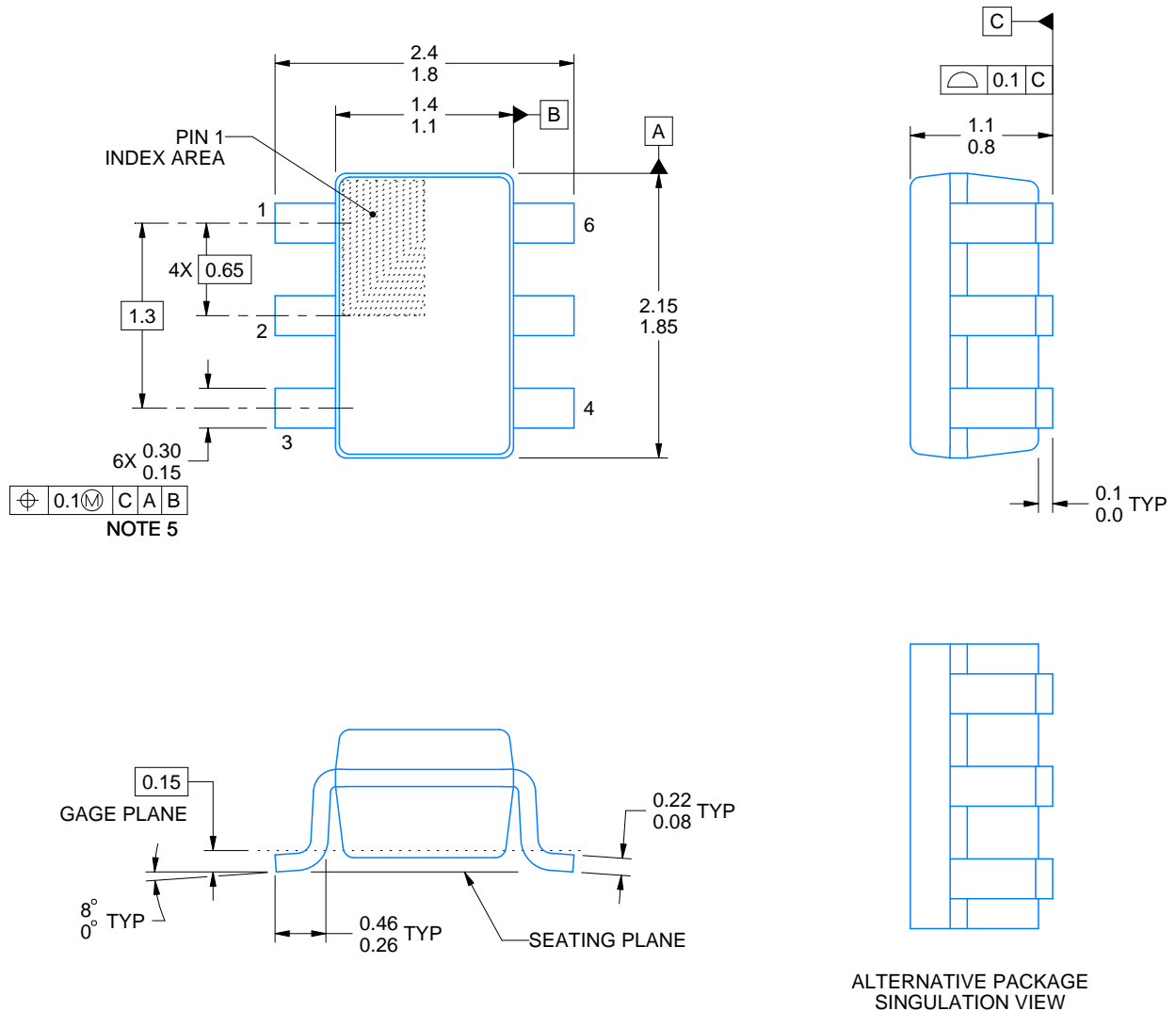
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

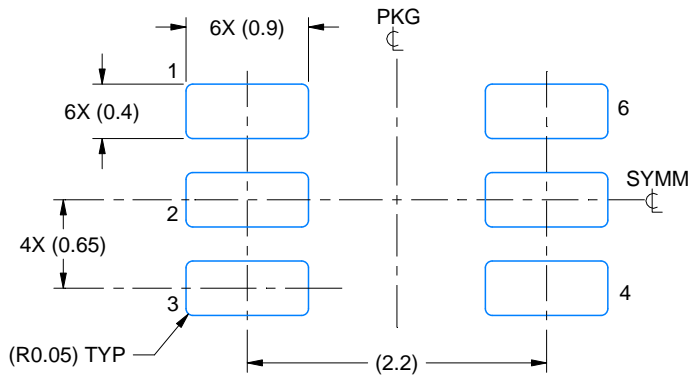
SMALL OUTLINE TRANSISTOR



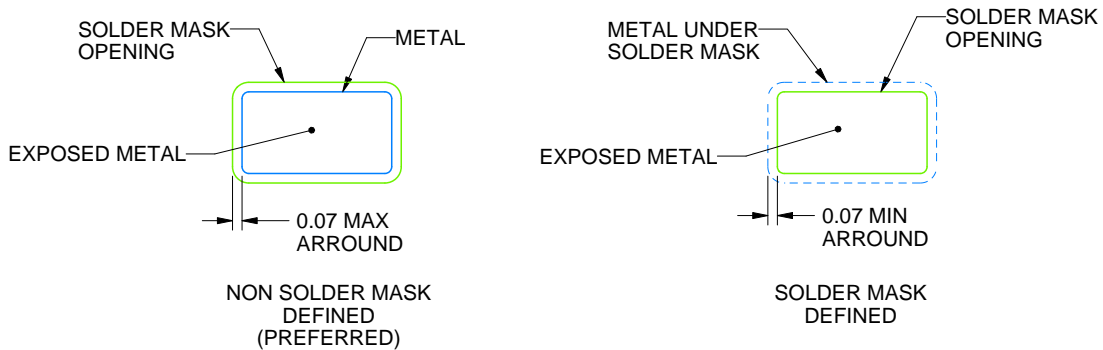
4214835/B 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/B 04/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



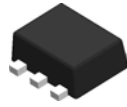
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/B 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

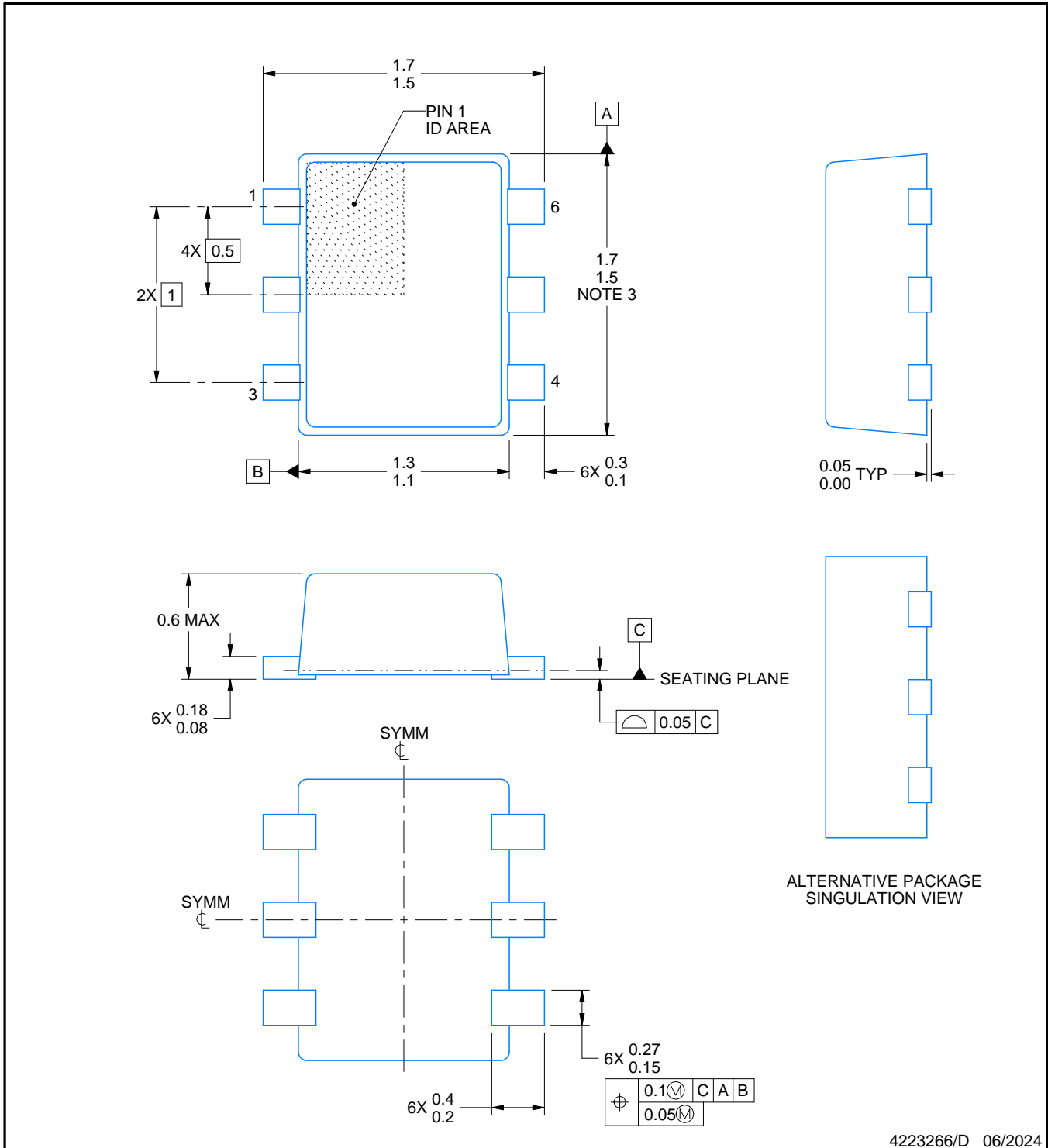
DRL0006A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/D 06/2024

NOTES:

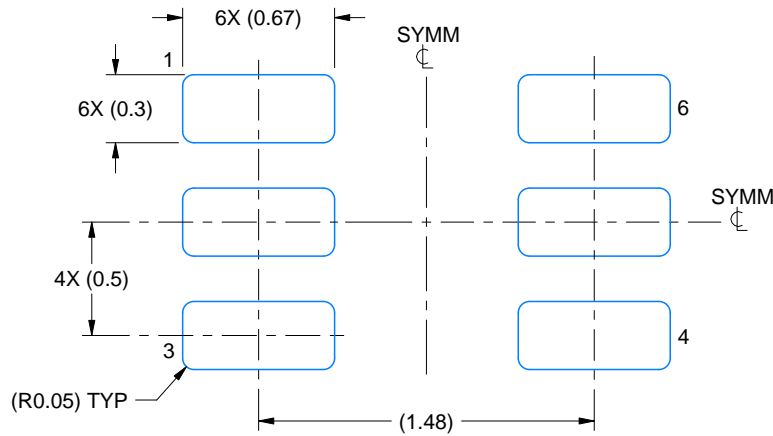
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

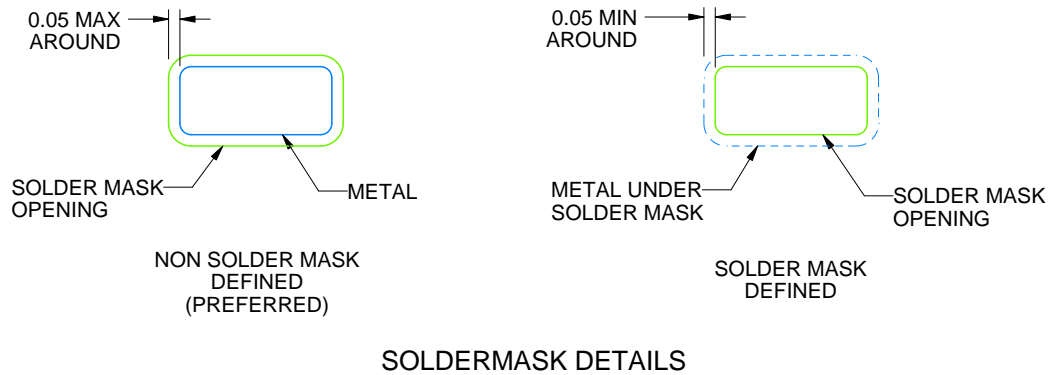
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/D 06/2024

NOTES: (continued)

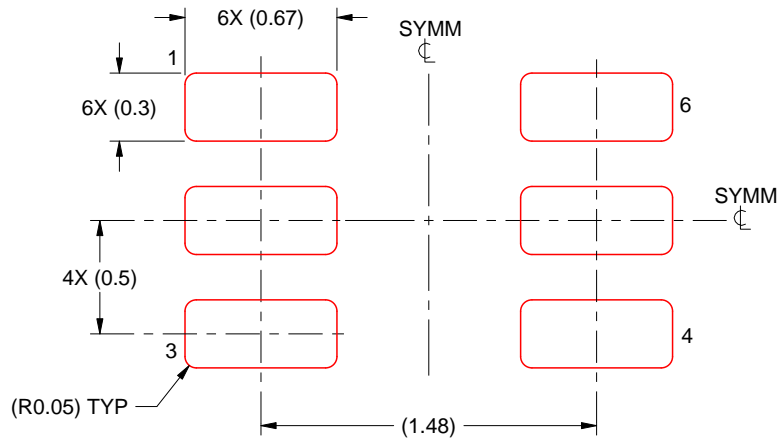
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/D 06/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



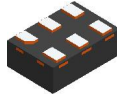
SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

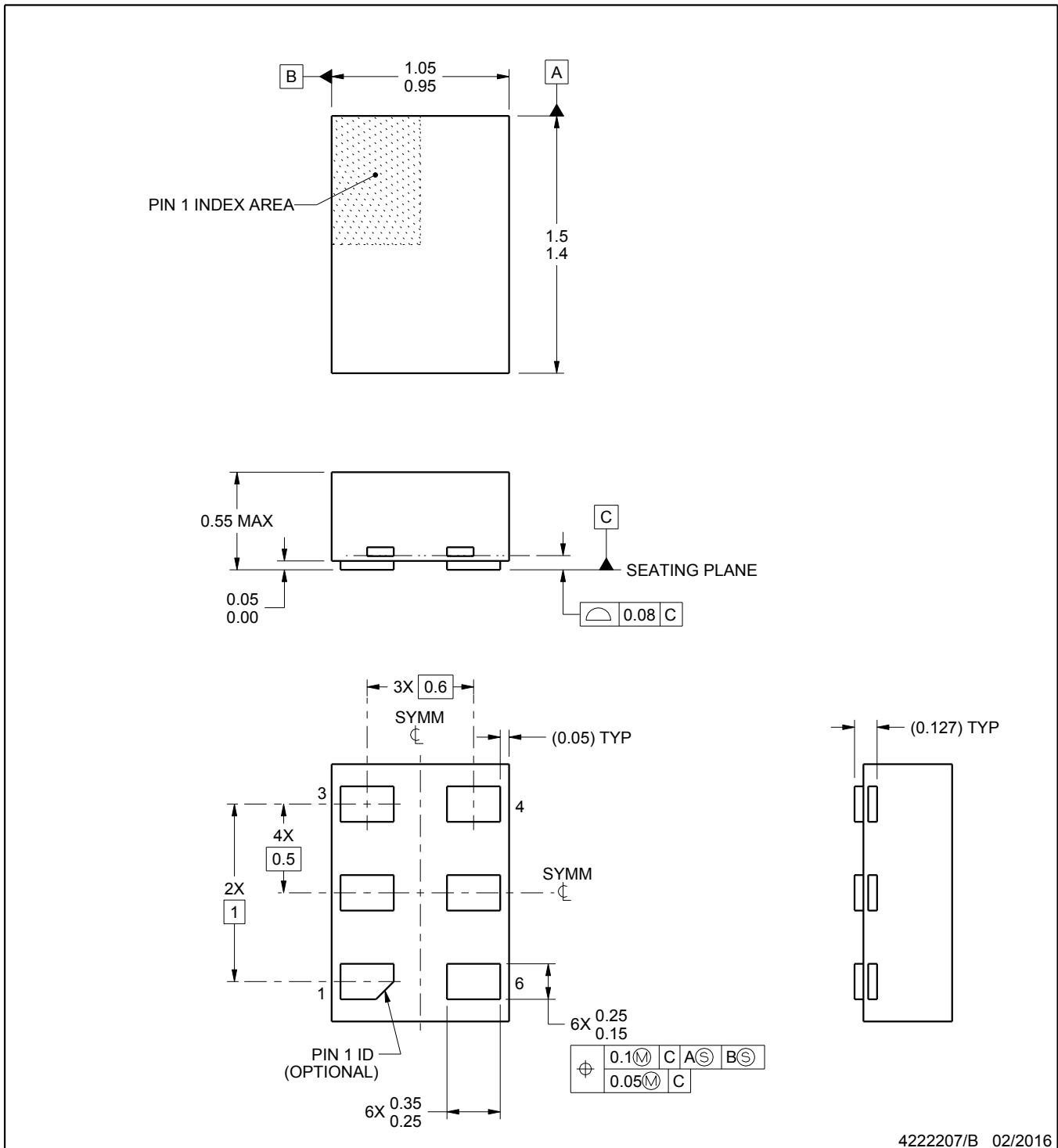
DRY0006B



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

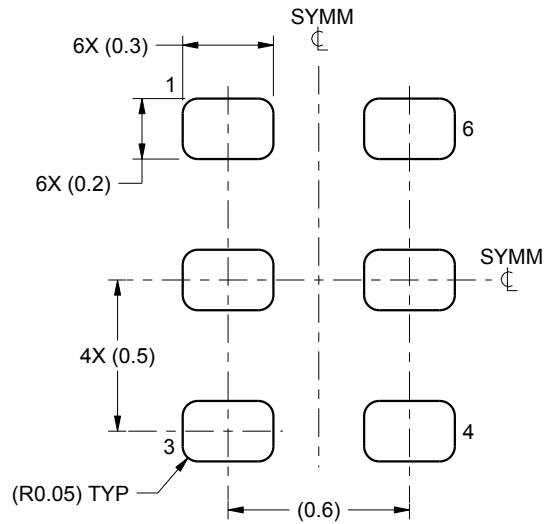
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

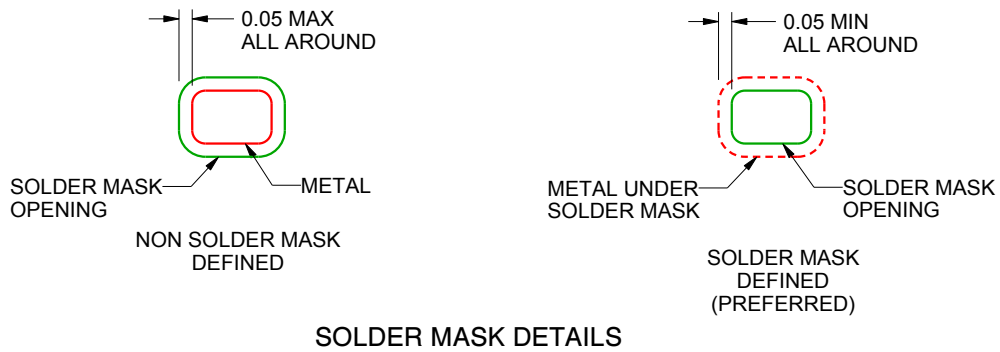
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

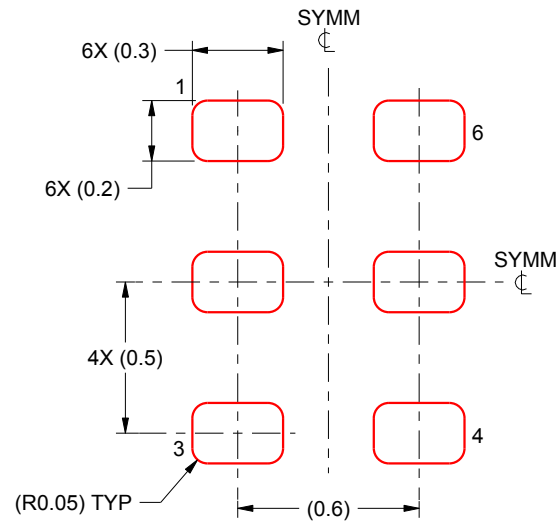
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

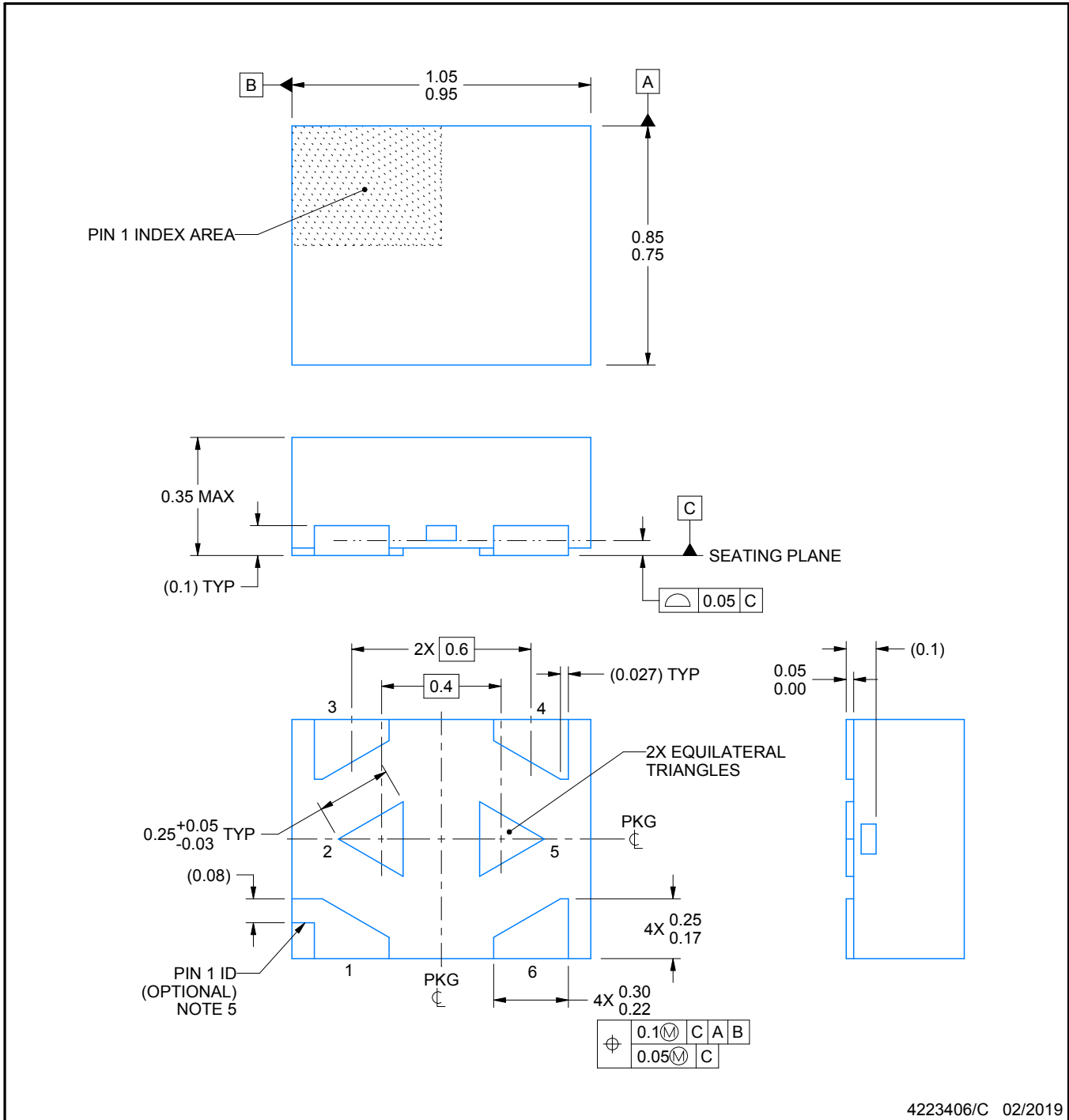
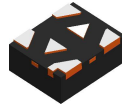


SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



NOTES:

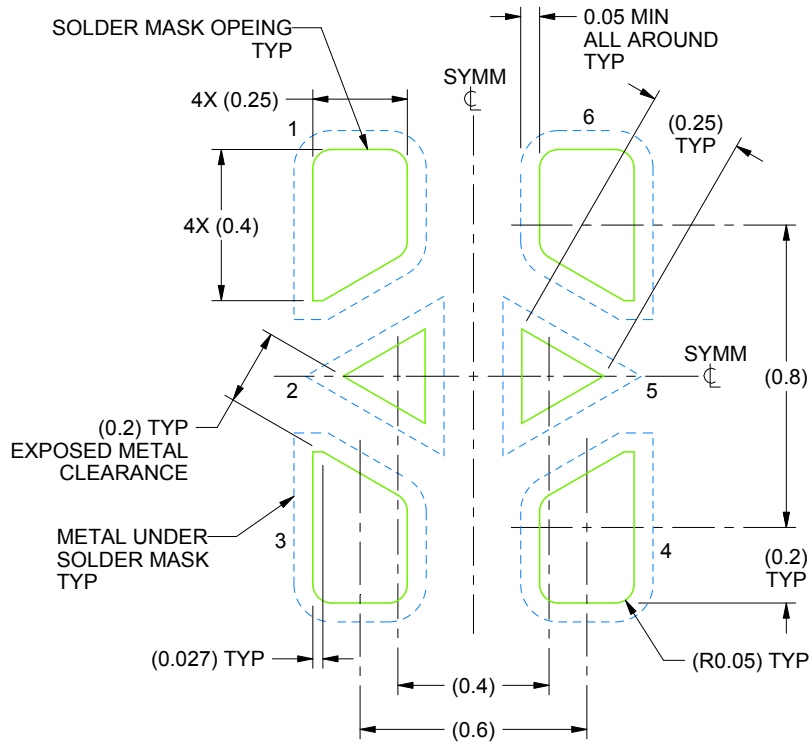
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

EXAMPLE BOARD LAYOUT

DTB0006A

X2SON - 0.35 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

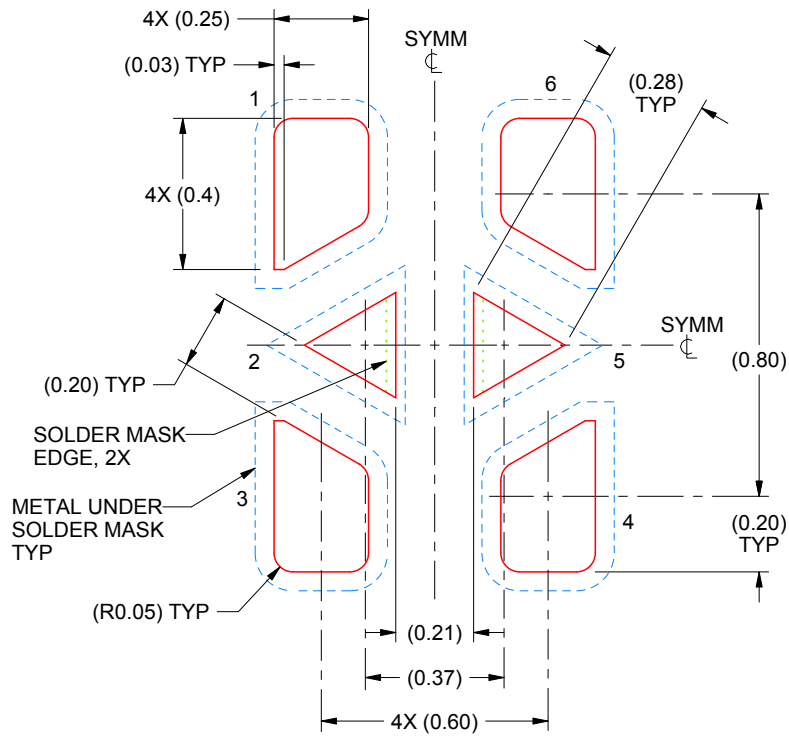
6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DTB0006A

X2SON - 0.35 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

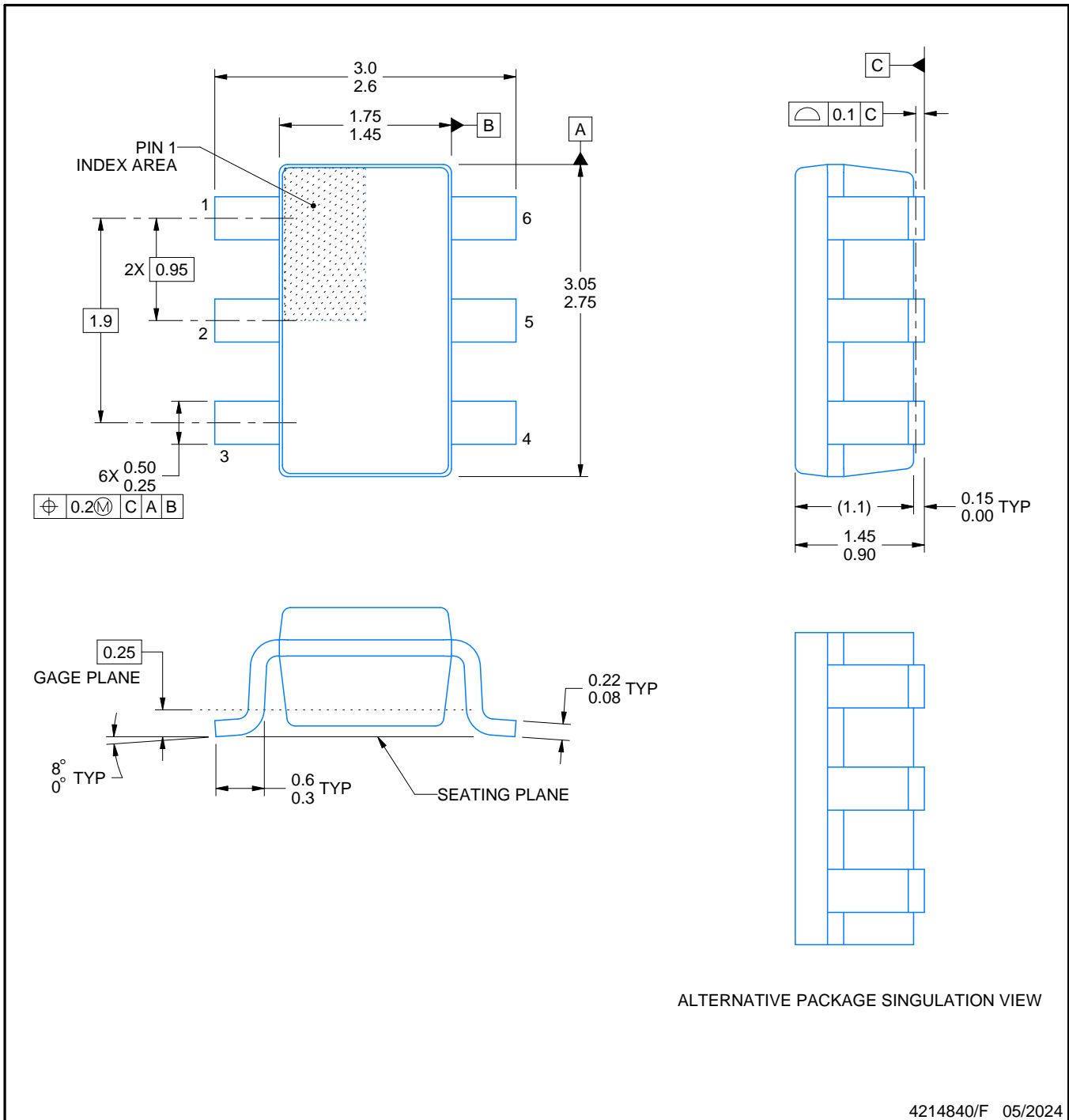
DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/F 05/2024

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
- Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

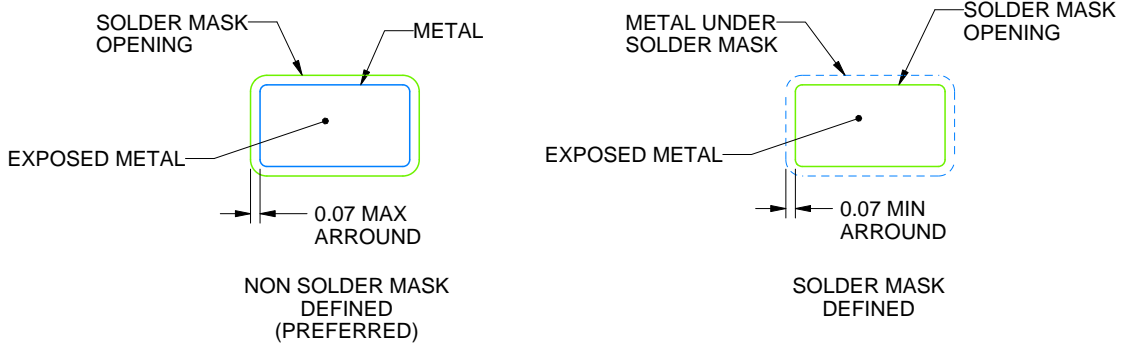
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

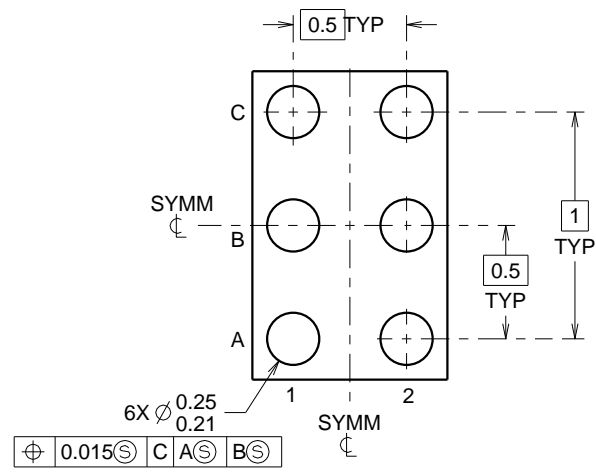
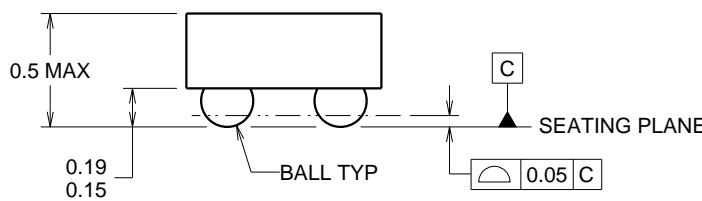
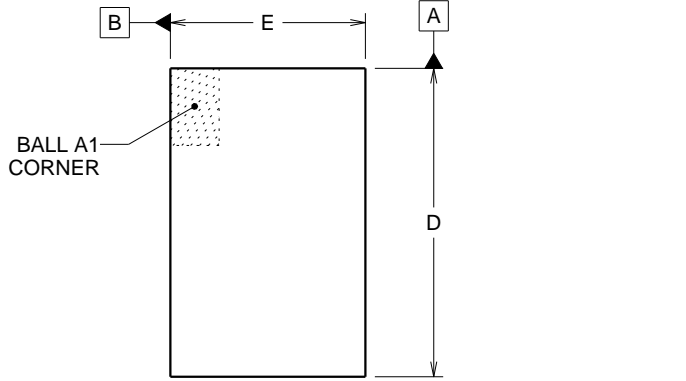
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.357 mm
 E: Max = 0.918 mm, Min = 0.857 mm

4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

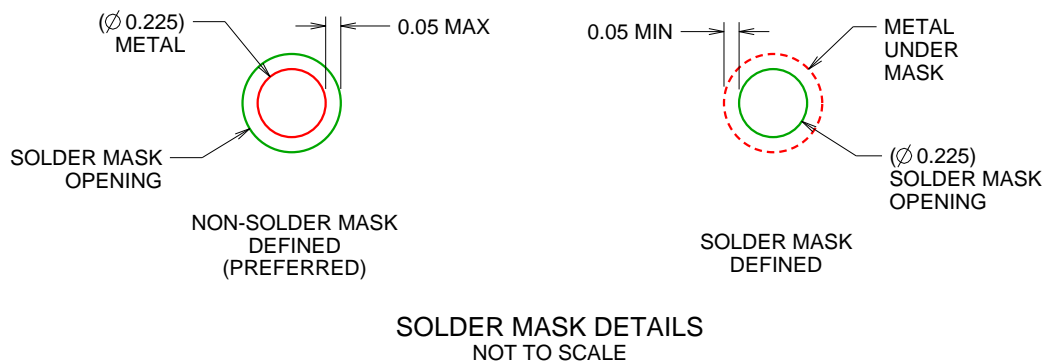
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



4219524/A 06/2014

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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