SN75172 四路差分线路驱动器

1 特性

- 符合或超出 ANSI 标准 EIA/TIA-422-B、RS-485 和 ITU 建议 V.11 的要求
- 适用于嘈杂环境中长总线上的多点传输
- 三态输出
- 共模输出电压范围：-7V 至 12V
- 高电平有效和低电平有效使能
- 热关断保护
- 正负电流限制
- 由 5V 单电源供电
- 与 AM26LS31 在逻辑上可以互换

2 应用

- 化学和气体传感器
- 现场变送器：温度传感器和压力传感器
- 电机控制：无刷直流和有刷直流
- 采用 Modbus 的温度传感器和控制器

3 说明

SN75172 是一款具有三态输出的单片四路差分线路接收器，符合 ANSI 标准 EIA/TIA-422-B、RS-485 和 ITU 建议 V.11 的要求。该器件经优化，能够以高达 4 兆波特的速率实现平衡多点总线传输。每个驱动器都具有较宽的正负共模输出电压范围，因此适用于嘈杂环境中的合用线应用。

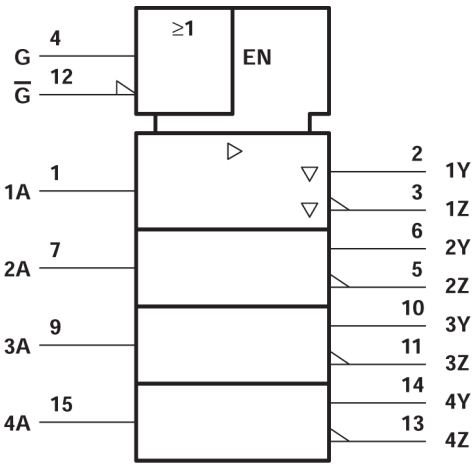
SN75172 可提供正负电流限制和热关断功能，避免传输总线出现线路故障状况。在结温约为 150°C 时关断。该器件在与 SN75173 或 SN75175 四路差分线路接收器配合使用时性能更高。

SN75172 的工作温度范围是 0°C 至 70°C。

封装信息

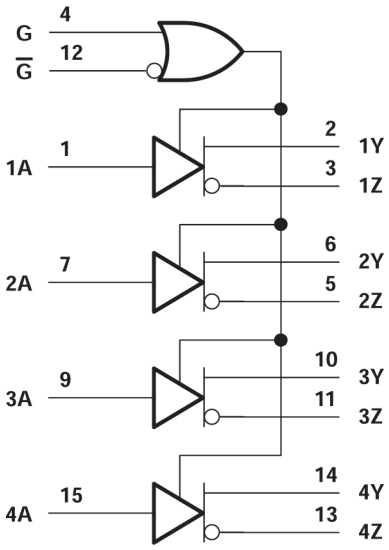
器件型号	封装(1)	封装尺寸(2)
SN75172	N（PDIP，16）	19.3mm x 9.4mm
	DW（SOIC，20）	12.8mm x 10.3mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



A. 所示引脚编号适用于 N 封装。

逻辑符号 [1]



逻辑图（正逻辑）

[1] 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

Table of Contents

4 Pin Configuration and Functions

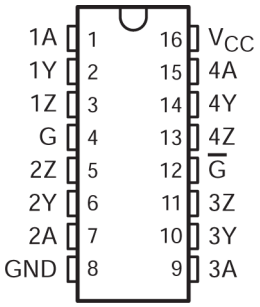
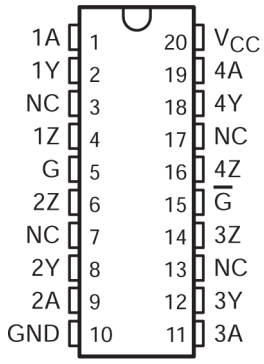


图 4-1. N Package (Top View)



NC – No internal connection

图 4-2. DW Package (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage, see (2)	-0.3	7	V
V_{BUS}	Voltage range at any bus terminal	–10	15	V
V_I	Input voltage	-0.3	5.5	V
P_D	Continuous total dissipation	See Dissipation Rating Table		
T_A	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	–65	150	°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

5.2 Dissipation Ratings

PACKAGE	$T_A \leqslant 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125mW	9mW/°C	720mW
N	1150mW	9.2mW/°C	736mW

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}	-7		12	V
High-level output current, I_{OH}			–60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

5.4 Thermal Information

THERMAL METRIC[1]		N (PDIP)	DW	UNIT
		16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = ±18mA					±1.5	V
V_O	Output voltage	I_O = 0			0		6	V
V_{OH}	High-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OH} = ±33mA		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OH} = 33mA		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0			1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See 图 6-1		1/2 V_{OD1} or 2[2]			V
		R_I = 54 Ω,	See 图 6-1		1.5	1.5	5	V
V_{OD3}	Differential output voltage	See [5]			1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage[3]						±0.2	V
V_{OC}	Common-mode output voltage[4]	R_L = 54 Ω or 100 Ω		See 图 6-1	-1		3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage[3]						±0.2	V
I_O	Output current with power off	V_{CC} = 0	V_O = ±7V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = ±7V to 12V					±100	µA
I_{IH}	High-level input current	V_I = 1.7V					20	µA
I_{IL}	Low-level input current	V_I = 0.5V					±360	µA
I_{OS}	Short-circuit output current	V_O = ±7V					±180	mA
		V_O = V_{CC}					180	
		V_O = 12V					500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			38	60	mA
			Outputs disabled			18	40	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with a 100Ω load is either 1/2 V_{OD1} or 2V, whichever is greater.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5) See 图 6-3 of EIA Standard RS-485.

表 5-1. Symbol Equivalents

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100Ω)	V_t (R_L = 54Ω)
$\|V_{OD2}\|$		V_t (Test Termination Measurement(5))
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|,\|I_{sb}\|$	
I_O	$\|I_{xa}\|,\|I_{xb}\|$	I_{ia},I_{ib}

5.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54Ω,	See 图 6-2		45	65	ns
$t_{t(OD)}$	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110Ω,	See 图 6-3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110Ω,	See 图 6-4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110Ω,	See 图 6-3		78	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110Ω,	See 图 6-4		18	30	ns

5.7 Typical Characteristics

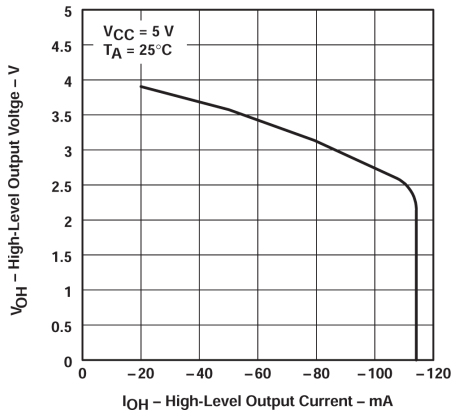


图 5-1. High-level Output Voltage vs High-level Output Current

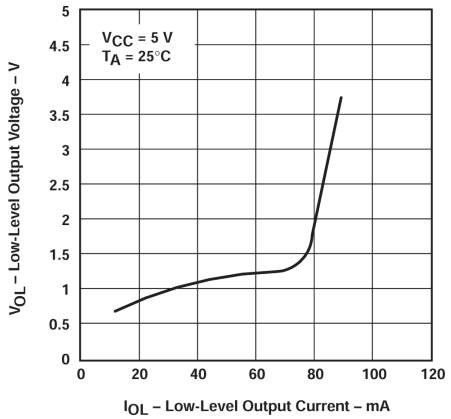


图 5-2. Low-level Output Voltage vs Low-level Output Current

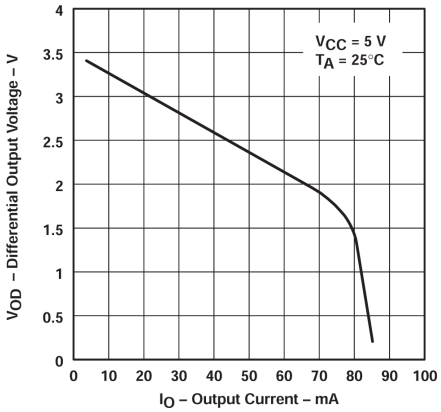


图 5-3. Differential Output Voltage vs Output Current

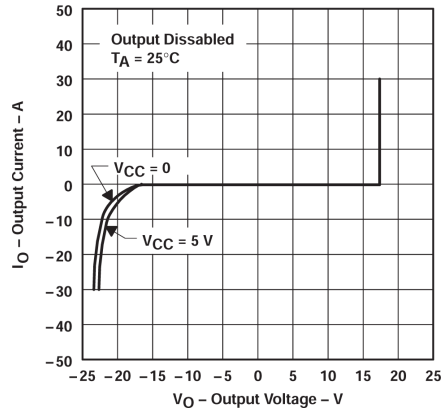


图 5-4. Output Current vs Output Voltage

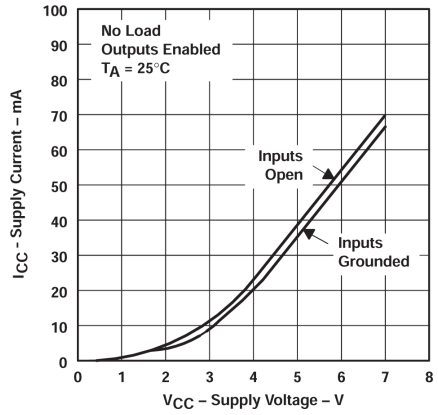


图 5-5. Supply Current vs Supply Voltage

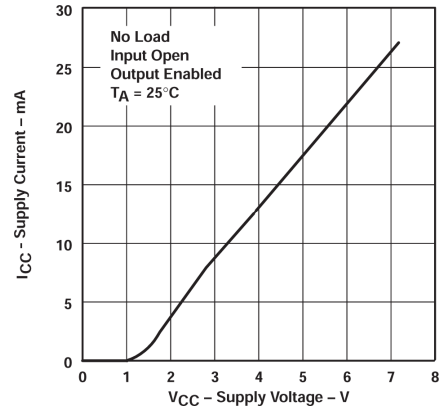


图 5-6. Supply Current vs Supply Voltage

6 Parameter Measurement Information

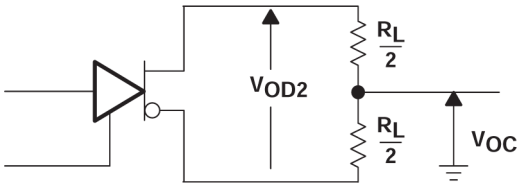
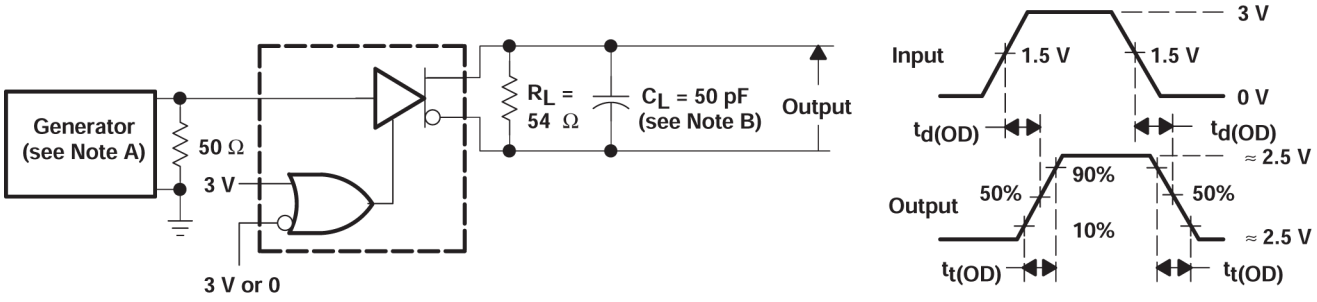


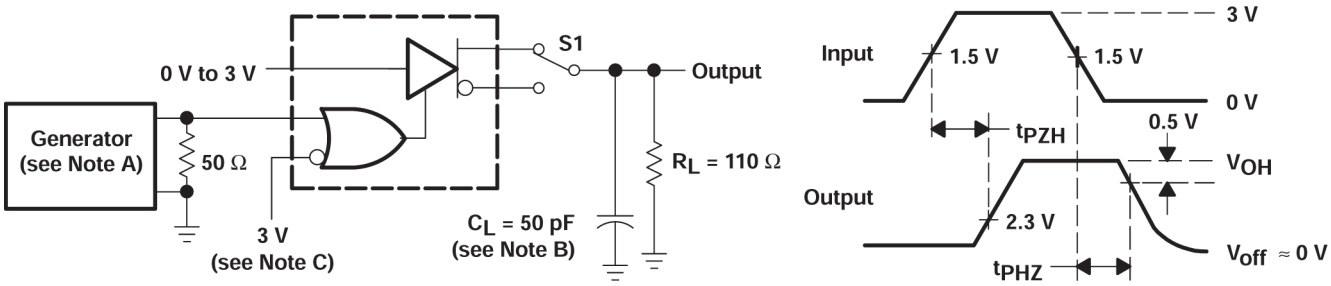
图 6-1. Differential and Common-Mode Output Voltages



A. The input pulse is supplied by a generator having the following characteristics: $t_r \leqslant 10$ns, $t_f \leqslant 10$ns, PRR $\leqslant$ 1MHz, duty cycle = 50%, $Z_O = 50\Omega$.

B. C_L includes probe and stray capacitance.

图 6-2. Differential-Output Test Circuit and Voltage Waveforms

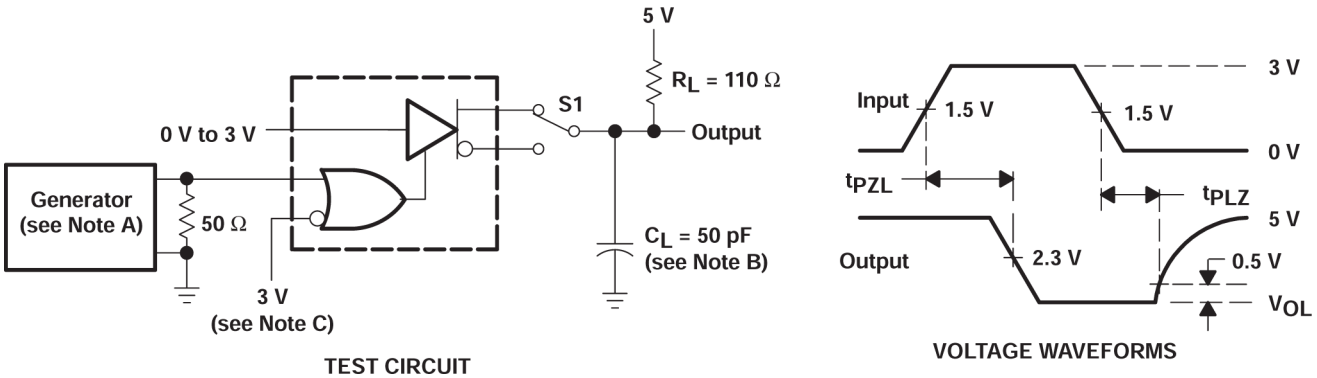


A. A. The input pulse is supplied by a generator having the following characteristics: PRR $\leqslant$ 1MHz, duty cycle = 50%, $t_r \leqslant$ 10ns, $t_f \leqslant$ 10ns, $Z_O = 50\Omega$.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

图 6-3. Test Circuit and Voltage Waveforms



A. A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1MHz, duty cycle = 50%, t_r ⩽ 5ns, t_f ⩽ 5ns, Z_O = 50Ω.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

图 6-4. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

Function Table (Each Driver)

INPUT A(1)	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

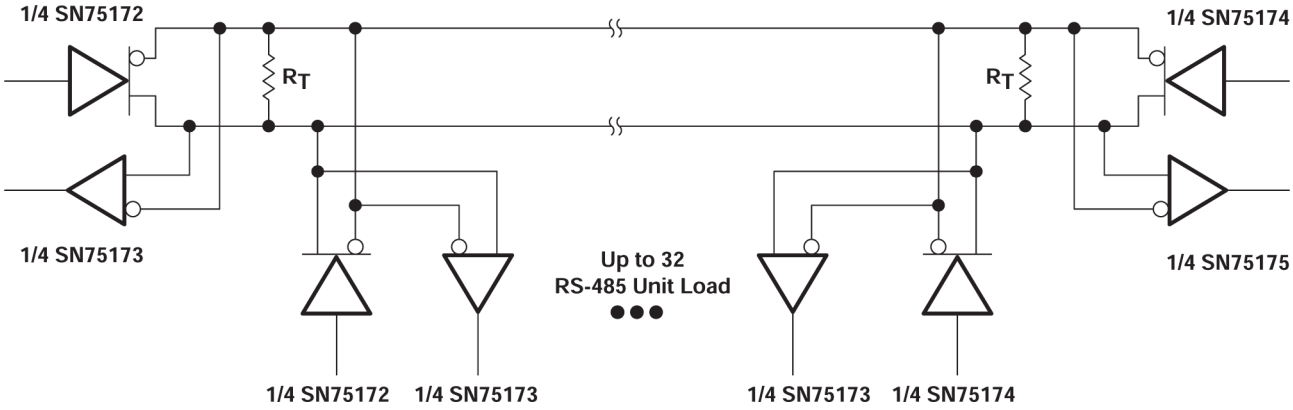
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information



A. The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (May 1995) to Revision C (April 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1
• Added the *Thermal Information* table	5
• Changed Note A in 图 6-2 and 图 6-3	8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75172DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	SN75172	
SN75172DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172	Samples
SN75172N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75172N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

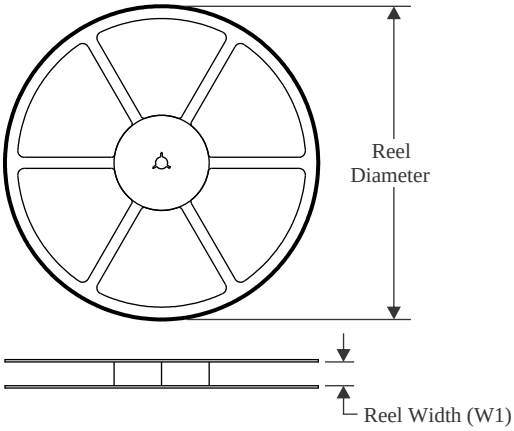
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

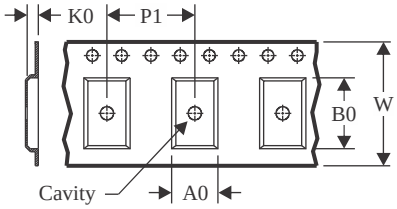
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

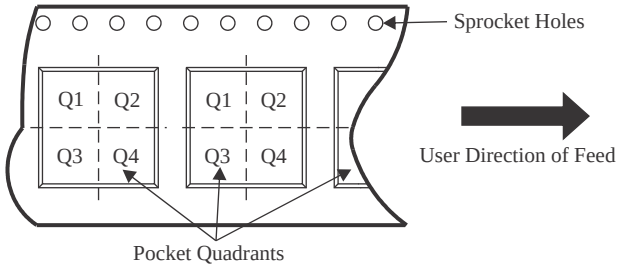


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

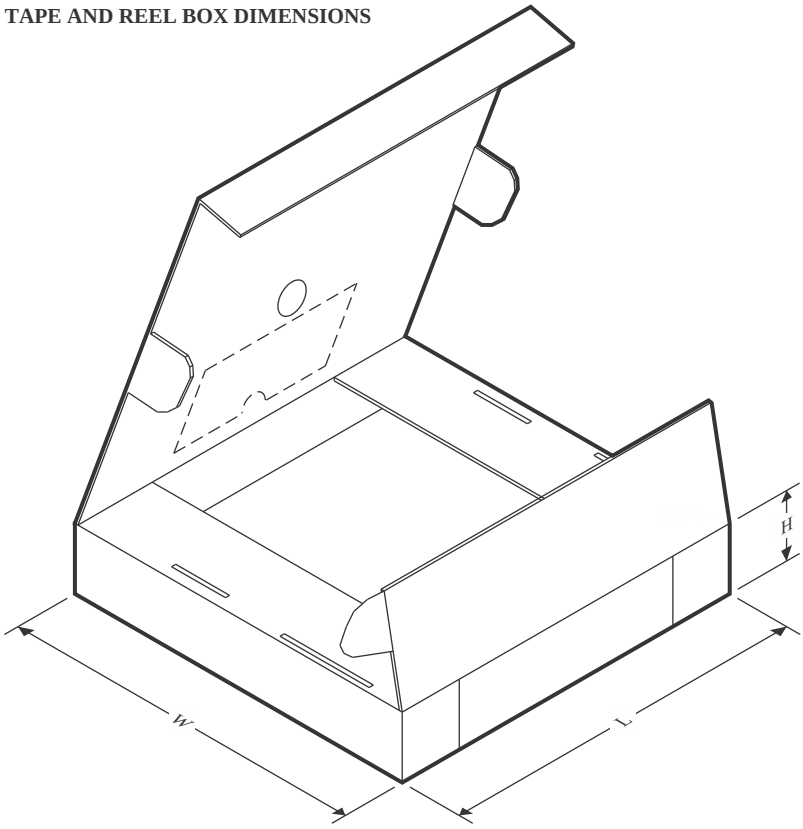
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

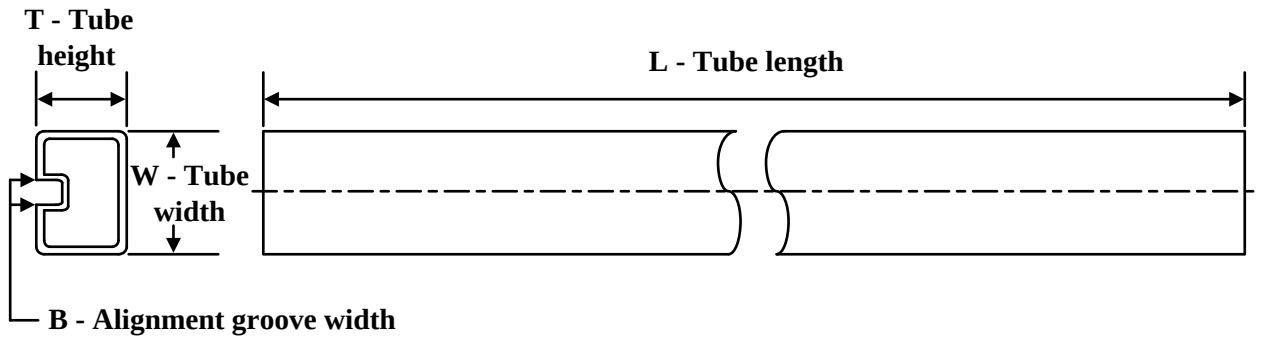
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75172DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



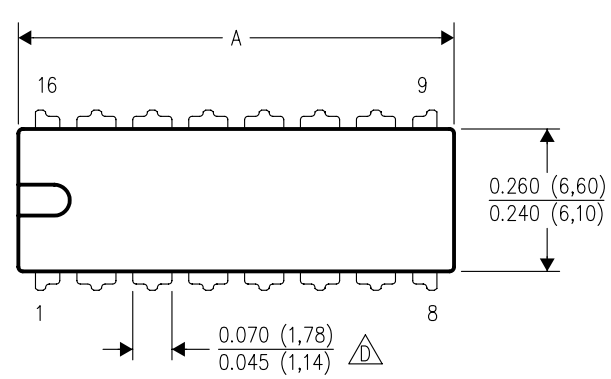
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75172DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75172DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75172N	N	PDIP	16	25	506	13.97	11230	4.32

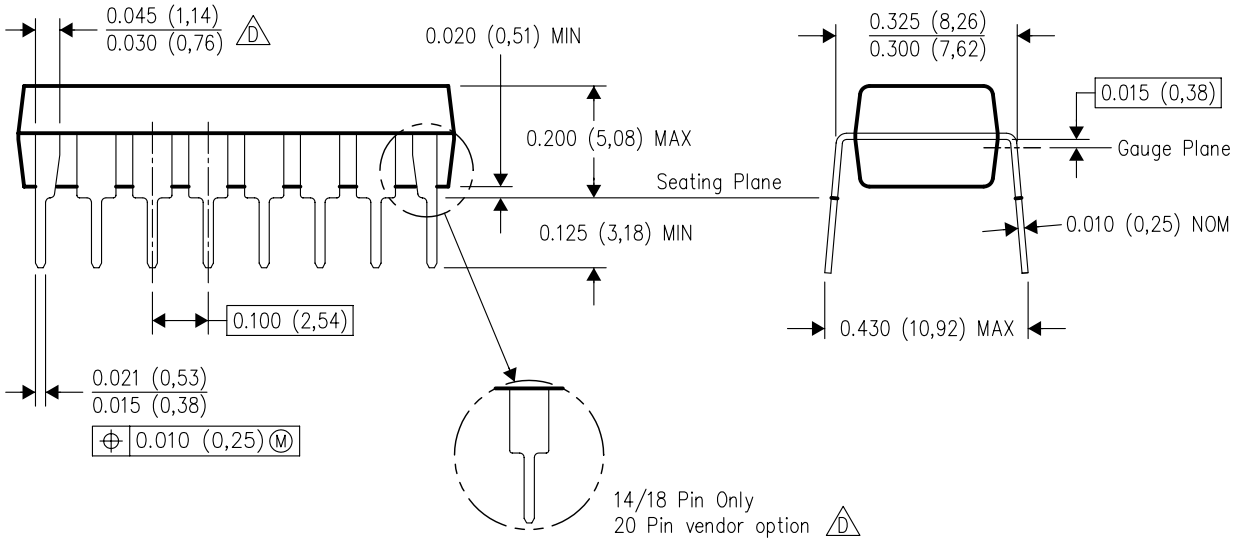
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

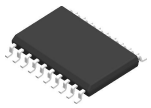


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

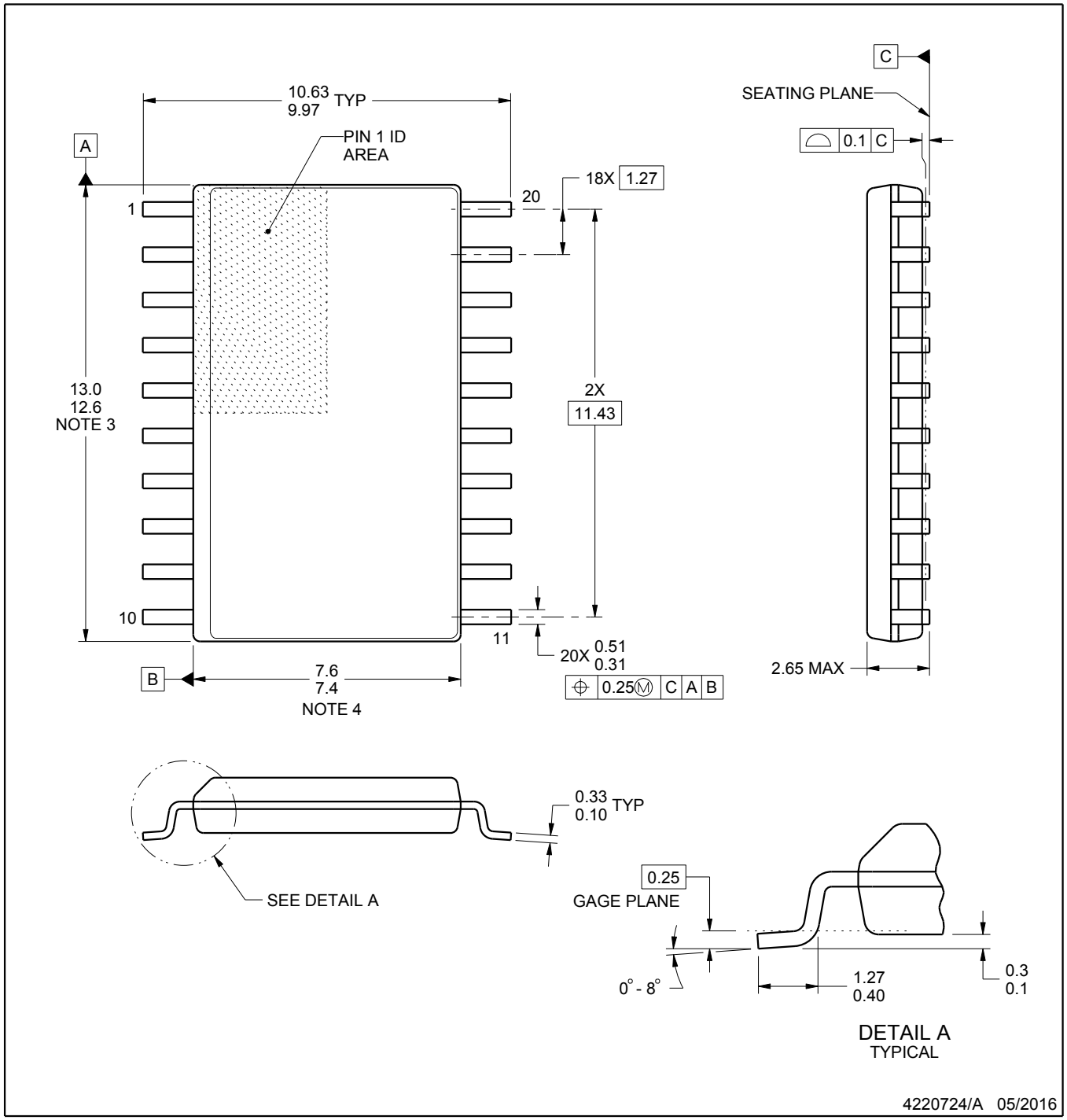


PACKAGE OUTLINE

DW0020A

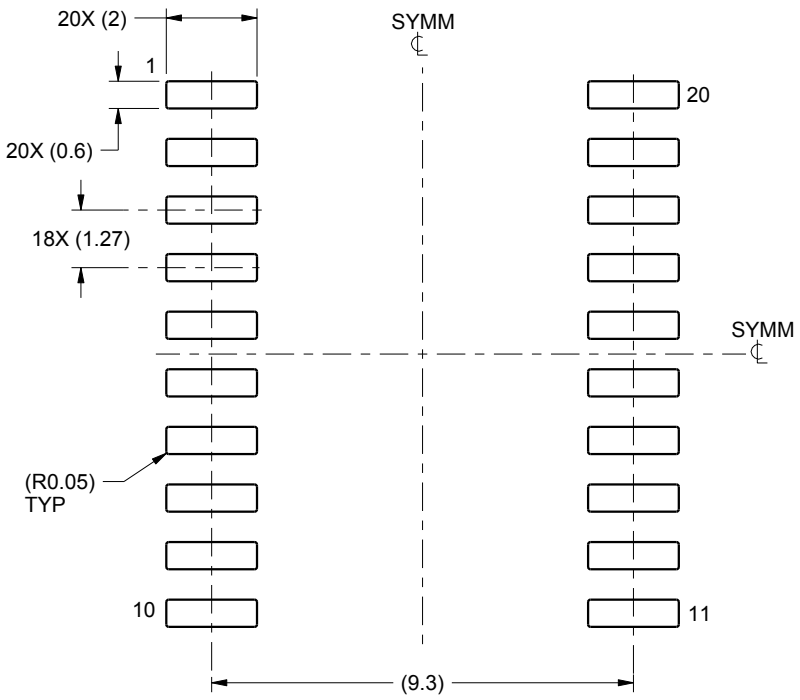
SOIC - 2.65 mm max height

SOIC

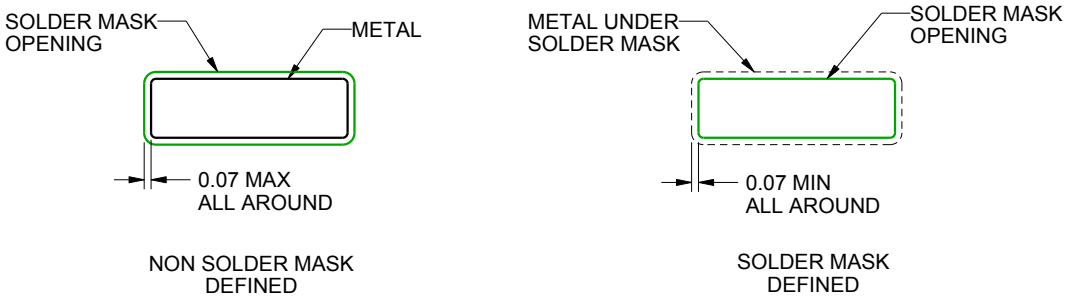


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

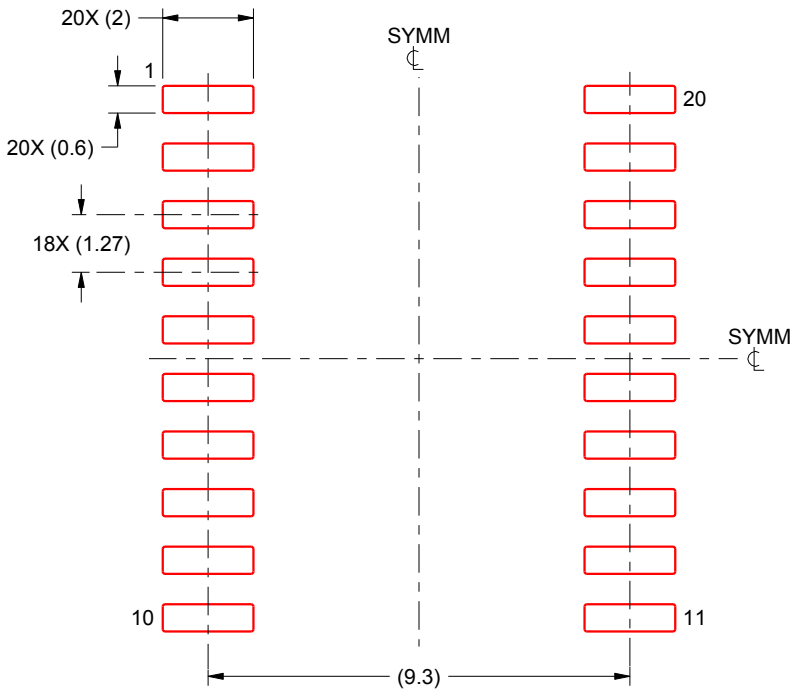


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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