

SNx5175 四路差分线路接收器

1 特性

- 符合或超出 ANSI 标准 EIA/TIA-422-B、RS-423-B 和 RS-485 的要求
- 符合 ITU 建议 V.10、V.11、X.26 和 X.27 的要求
- 适用于嘈杂环境中长总线上的多点总线传输
- 三态输出
- 共模输入电压范围：-12V 至 12V
- 输入灵敏度： $\pm 200\text{mV}$
- 输入迟滞：50mV (典型值)
- 高输入阻抗：12k Ω (最小值)
- 由 5V 单电源供电
- 低功耗要求
- MC3486 的插入式替代产品

2 应用

- 电机驱动器
- 工厂自动化和控制

3 说明

SN65175 和 SN75175 是具有三态输出的单片四路差分线路接收器。这些器件符合 ANSI 标准 EIA/TIA-422-B、RS-423-B 和 RS-485 以及数项 ITU 建议的要求。这些标准适用于速率高达 10 兆位/秒的平衡多点总线传输。两对接收器中的每一对都具有一个共用的高电平有效使能端。

这些接收器具有高输入阻抗、用于提高抗噪性的输入迟滞、以及在 $\pm 12\text{V}$ 共模输入电压范围内 $\pm 200\text{mV}$ 的输入灵敏度。SN65175 和 SN75175 与 SN75172 或 SN75174 四路差分线路驱动器配合使用时，可实现卓越性能。

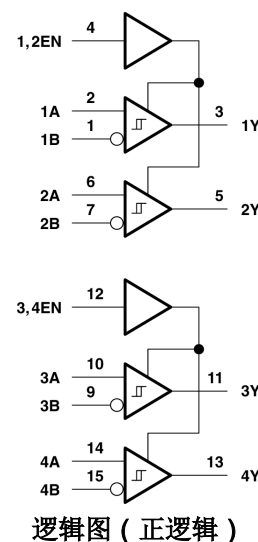
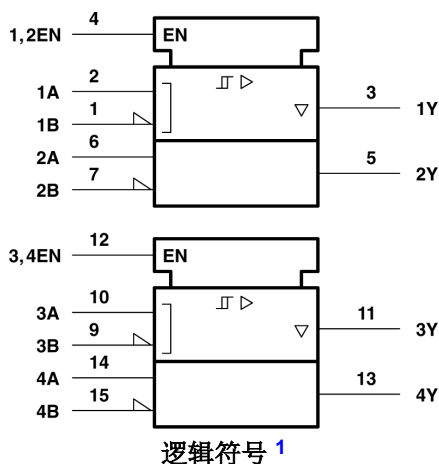
SN65175 的额定工作温度范围为 -40°C 至 85°C 。SN75175 的额定工作温度范围为 0°C 至 70°C 。

封装信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ |
|---------|-------------------|---------------------|
| SN65175 | D (SOIC, 16) | 9.9mm × 6mm |
| SN75175 | N (PDIP, 16) | 19.3mm × 9.4mm |
| | D (SOIC, 16) | 9.9mm × 6mm |
| | NS (SOP, 16) | 10.2mm × 7.8mm |

(1) 有关所有详细信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



¹ 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。



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4 Pin Configuration and Functions

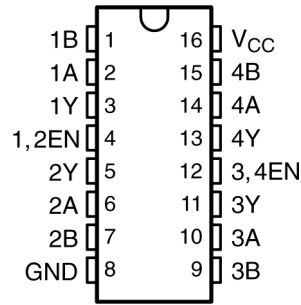


图 4-1. D, N, or NS Package (Top View)

表 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------|-----|---------------------|---|
| NAME | NO. | | |
| 1B | 1 | I | Channel 1 Differential Receiver Inverting Input |
| 1A | 2 | I | Channel 1 Differential Receiver Non-Inverting Input |
| 1Y | 3 | O | Channel 1 Single Ended Output |
| 1,2EN | 4 | I | Active High Enable for Channels 1 and 2 |
| 2Y | 5 | O | Channel 2 Single Ended Output |
| 2A | 6 | I | Channel 2 Differential Receiver Non-Inverting Input |
| 2B | 7 | I | Channel 2 Differential Receiver Inverting Input |
| GND | 8 | GND | Device GND |
| 3B | 9 | I | Channel 3 Differential Receiver Inverting Input |
| 3A | 10 | I | Channel 3 Differential Receiver Non-Inverting Input |
| 3Y | 11 | O | Channel 3 Single Ended Output |
| 3,4EN | 12 | I | Active High Enable for Channels 3 and 4 |
| 4Y | 13 | O | Channel 4 Single Ended Output |
| 4A | 14 | I | Channel 4 Differential Receiver Non-Inverting Input |
| 4B | 15 | I | Channel 4 Differential Receiver Inverting Input |
| V _{CC} | 16 | PWR | Device V _{CC} (4.75 V to 5.25 V) |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIX | MAX | UNIT | |
|------------------------------|--|-------------------------------------|-----|------|----|
| V_{CC} ⁽²⁾ | Supply voltage | | 7 | V | |
| V_I | Input voltage (A or B inputs) | | ±25 | V | |
| V_{ID} ⁽³⁾ | Differential input voltage | | ±25 | V | |
| $V_{I(EN)}$ | Enable input voltage | | 7 | V | |
| I_{OL} | Low-level output current | | 50 | mA | |
| Continuous total dissipation | | See <i>Dissipation Rating</i> table | | | |
| T_A | Operating free-air temperature range: | SN65175 | -40 | 85 | °C |
| | | SN75175 | 0 | 70 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260 | °C | |
| T_{stg} | Storage temperature range | -65 | 150 | °C | |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential input voltage, are with respect to network ground terminal.
- (3) Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|--|-----------------|---------------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW | 494 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |

5.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---------|------|-----|------|------|
| Supply voltage, V_{CC} | | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, V_{IC} | | | | ±12 | V |
| Differential input voltage, V_{ID} | | | | ±12 | V |
| High-level enable-input voltage, V_{IH} | | 2 | | | V |
| Low-level enable-input voltage, V_{IL} | | | | 0.8 | V |
| High-level output current, I_{OH} | | | | -400 | µA |
| Low-level output current, I_{OL} | | | | 16 | mA |
| Operating free-air temperature, T_A | SN65175 | -40 | | 85 | °C |
| | SN75175 | 0 | | 70 | |

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | D (SOIC) | N (PDIP) | NS (SOP) | UNIT |
|-------------------------------|--|----------|----------|----------|------|
| | | 16-PINS | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 84.6 | 60.6 | 88.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 43.5 | 48.1 | 46.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 43.2 | 40.6 | 50.7 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 10.4 | 27.5 | 13.5 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 42.8 | 40.3 | 50.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|---|---|--|---------------------|--------------------|-------------|---------------|
| V_{IT+} | Positive-going input threshold voltage | $V_O = 2.7\text{ V}$, | $I_O = -0.4\text{ mA}$ | | | 0.2 | V |
| V_{IT-} | Negative-going input threshold voltage | $V_O = 0.5\text{ V}$, | $I_O = 16\text{ mA}$ | -0.2 ⁽²⁾ | | | V |
| V_{hys} | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | See 图 5-1 | | | 50 | | mV |
| V_{IK} | Enable-input clamp voltage | $I_I = -18\text{ mA}$ | | | | -1.5 | V |
| V_{OH} | High-level output voltage | $V_{ID} = 200\text{ mV}$, | $I_{OH} = -400\text{ }\mu\text{A}$, See 图 6-1 | 2.7 | | | V |
| V_{OL} | Low-level output voltage | $V_{ID} = -200\text{ mV}$, | See 图 6-1 $I_{OL} = 8\text{ mA}$ $I_{OL} = 16\text{ mA}$ | | | 0.45 0.5 | V |
| I_{OZ} | High-impedance-state output current | $V_O = 0.4\text{ V to }2.4\text{ V}$ | | | | ± 20 | μA |
| I_I | Line input current | Other input at 0 V, See ⁽⁴⁾ | $V_I = 12\text{ V}$ $V_I = -7\text{ V}$ | | | 1 -0.8 | mA |
| I_{IH} | High-level enable-input current | $V_{IH} = 2.7\text{ V}$ | | | | 20 | μA |
| I_{IL} | Low-level enable-input current | $V_{IL} = 0.4\text{ V}$ | | | | -100 | μA |
| r_i | Input resistance | | | 12 | | | k Ω |
| I_{OS} | Short-circuit output current ⁽³⁾ | | | -15 | | -85 | mA |
| I_{CC} | Supply current | Outputs disabled | | | | 70 | mA |

- (1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(4) Refer to ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485 for exact conditions.

5.6 Switching Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|---------------------------|-----|-----|-----|------|
| t_{PLH} | Propagation delay time, low- to high-level output | See 图 6-2 | | 22 | 35 | ns |
| t_{PHL} | Propagation delay time, high- to low-level output | | | 25 | 35 | ns |
| t_{PZH} | Output enable time to high level | See 图 6-3 | | 13 | 30 | ns |
| t_{PZL} | Output enable time to low level | | | 19 | 30 | ns |
| t_{PHZ} | Output disable time from high level | See 图 6-3 | | 26 | 35 | ns |
| t_{PLZ} | Output disable time from low level | | | 25 | 35 | ns |

5.7 Typical Characteristics

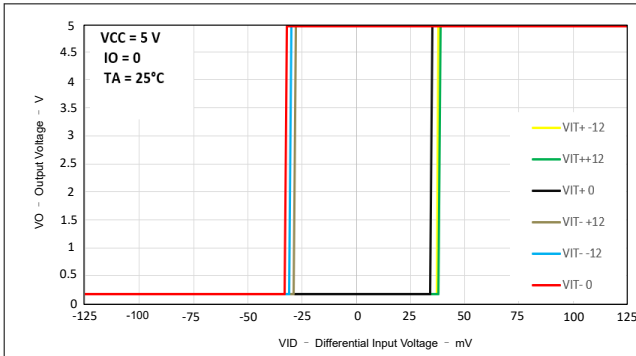


图 5-1. Output Voltage vs Differential Input Voltage

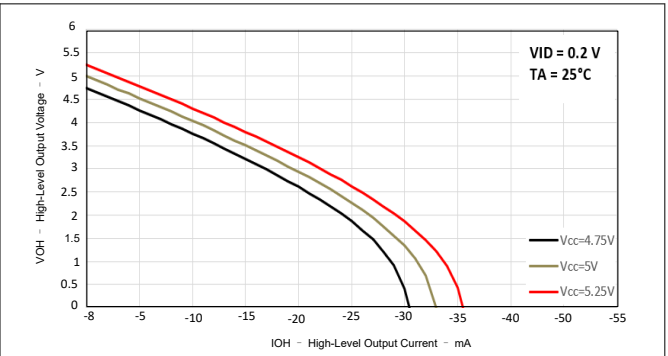


图 5-2. High-level Output Voltage vs High-level Output Current

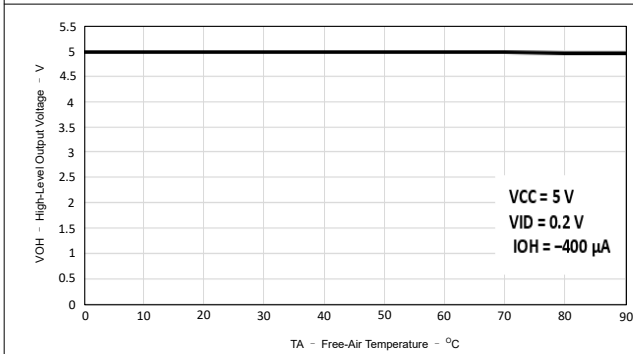


图 5-3. High-level Output Voltage vs Free-air Temperature 5

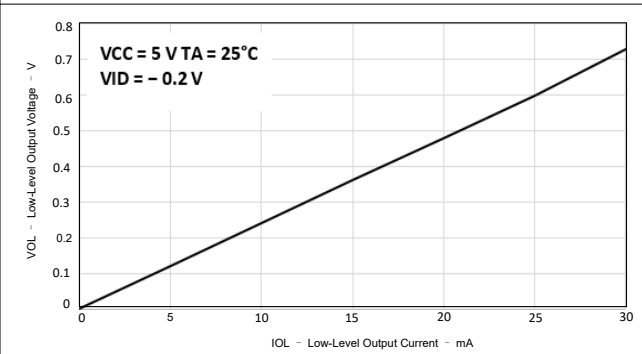


图 5-4. Low-level Output Voltage vs Low-level Output Current

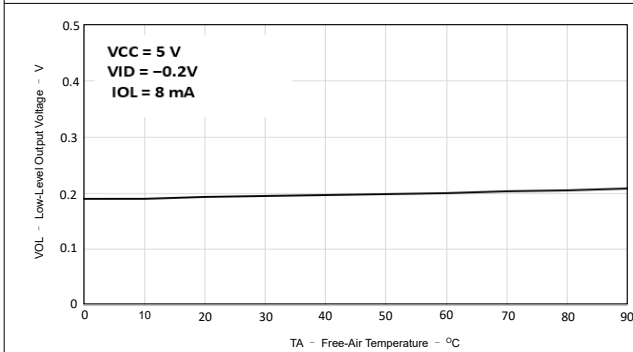


图 5-5. Low-level Output Voltage vs Free-air Temperature

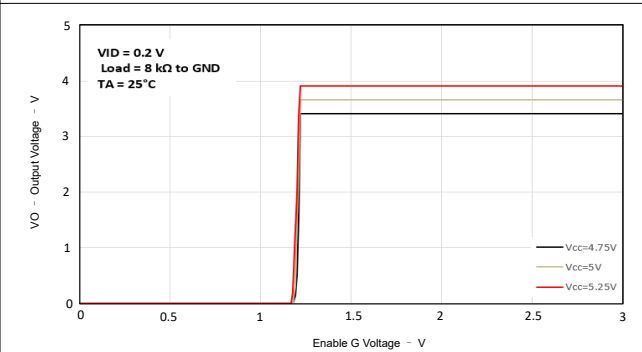
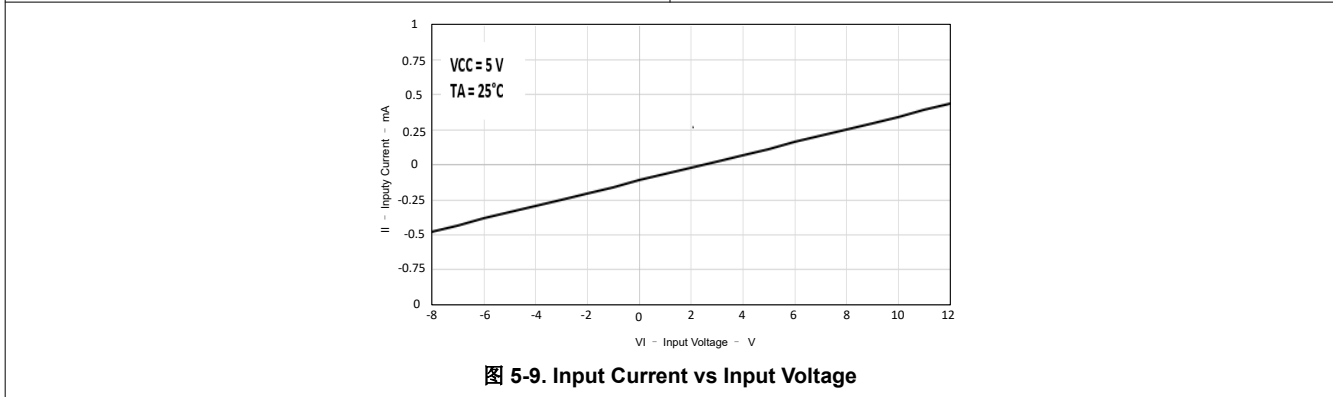
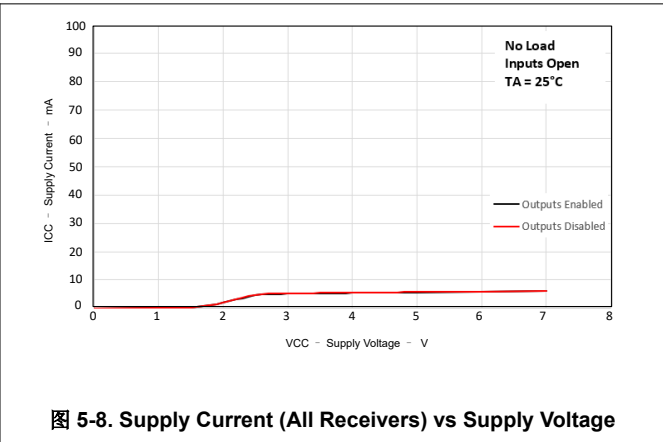
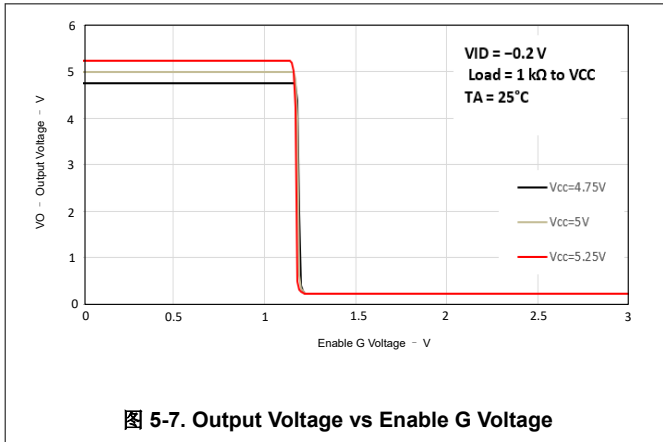


图 5-6. Output Voltage vs Enable G Voltage

5.7 Typical Characteristics (continued)



6 Parameter Measurement Information

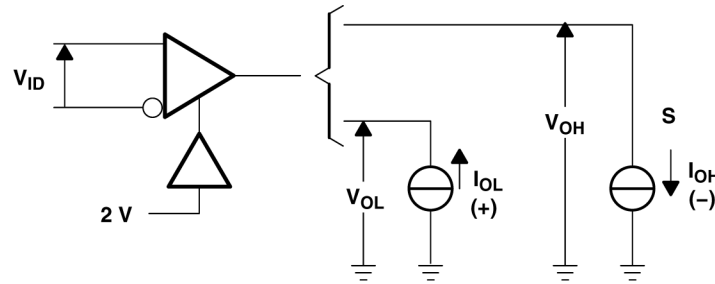
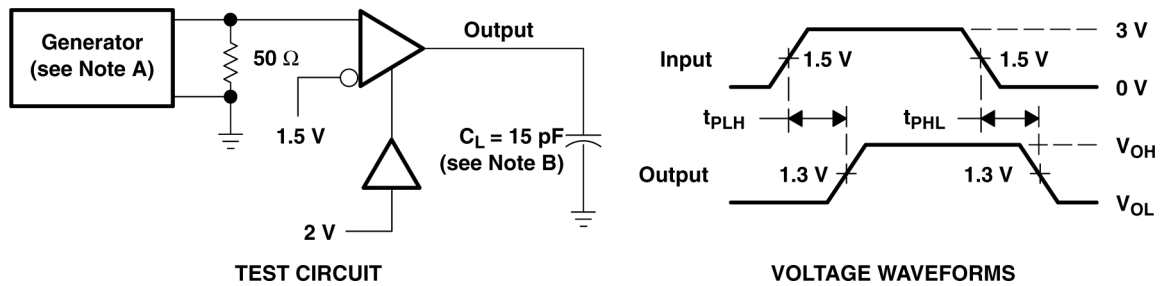


图 6-1. V_{OH} , V_{OL}

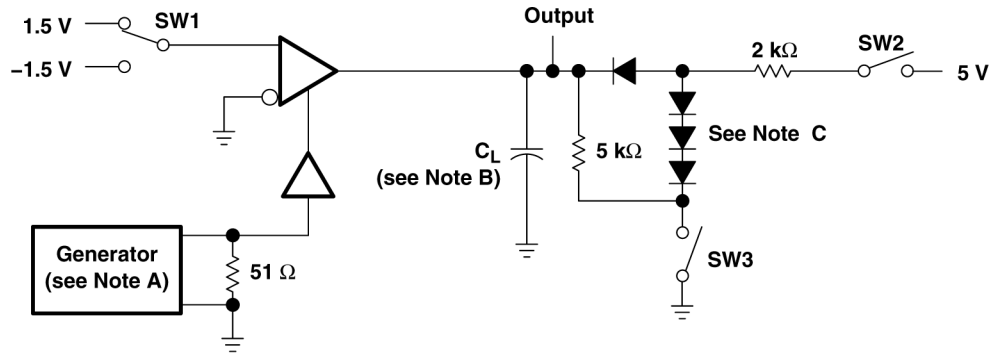


TEST CIRCUIT

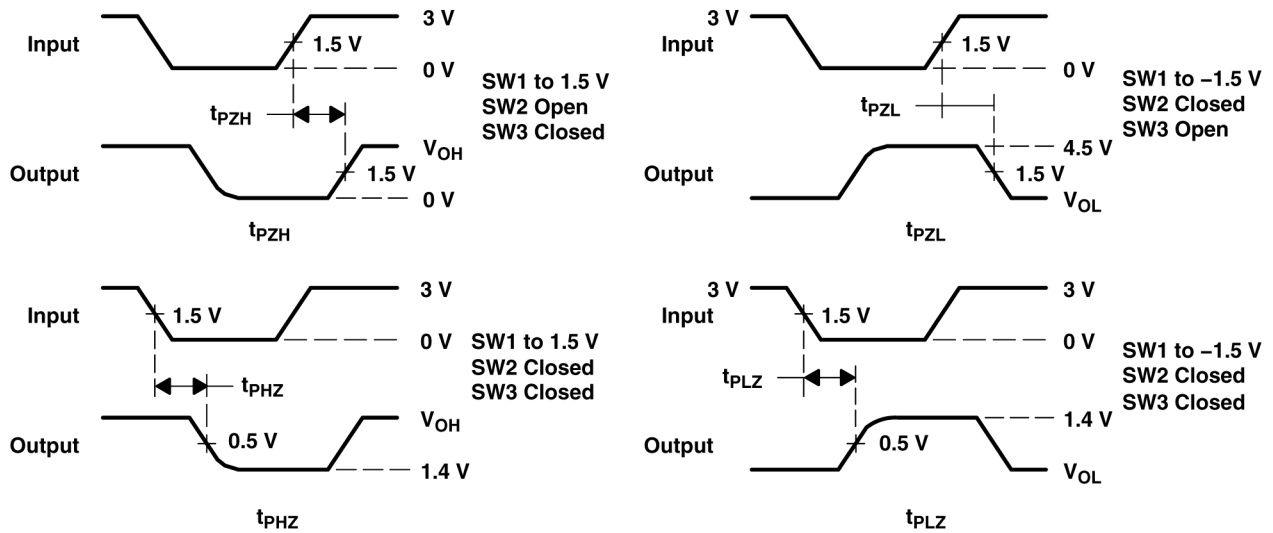
VOLTAGE WAVEFORMS

- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle = 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
- B. C_L includes probe and stray capacitance.

图 6-2. Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle = 50%, $t_f \leq 6$ ns, $t_r \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and stray capacitance.
- C. All diodes are 1N916 or equivalent.

图 6-3. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

| DIFFERENTIAL A - B ⁽¹⁾ | ENABLE | OUTPUT Y |
|---|--------|----------|
| $V_{ID} \geq 0.2 \text{ V}$ | H | H |
| $-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$ | H | ? |
| $V_{ID} \leq -0.2 \text{ V}$ | H | L |
| X | L | Z |
| Open circuit | H | ? |

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

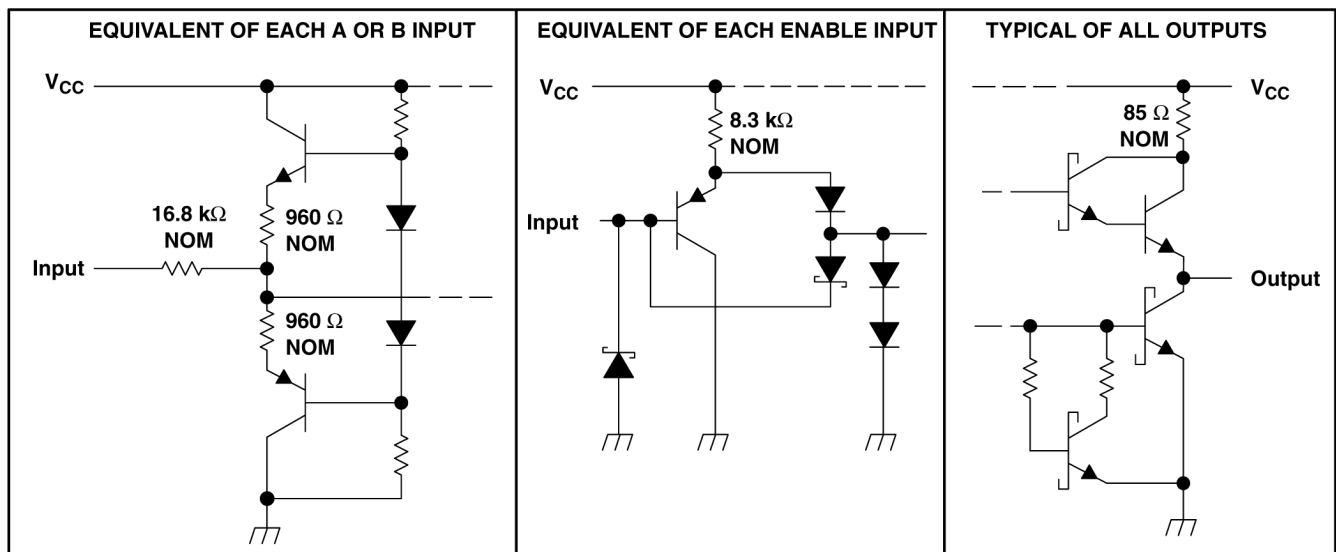


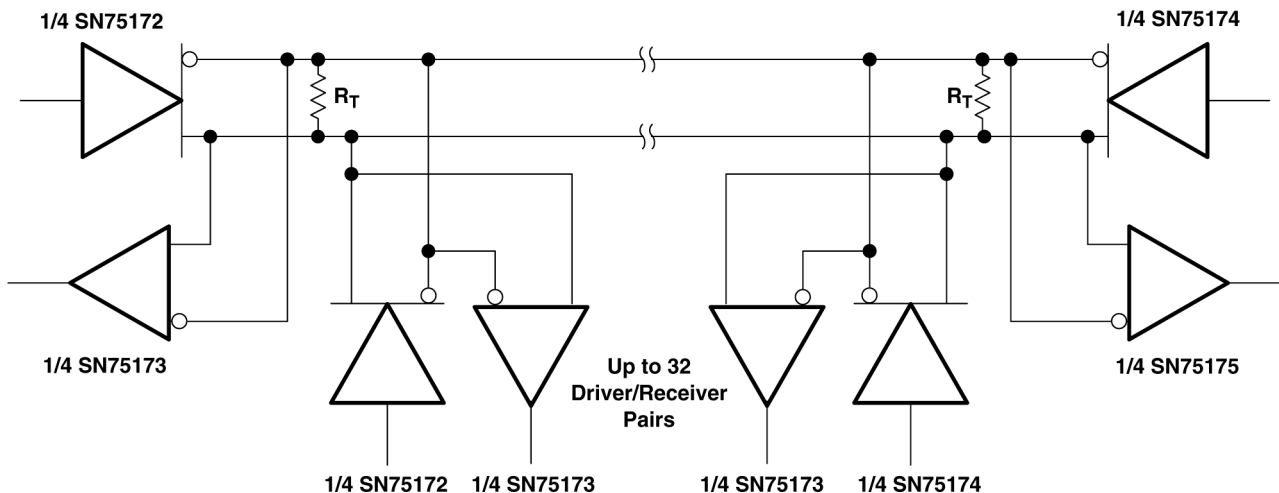
图 7-1. Schematics of Inputs and Outputs

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information



- A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision C (November 2006) to Revision D (October 2023) | Page |
|--|------|
| • 更改了整个文档中的表格、图和交叉参考的编号格式..... | 1 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN65175D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SN65175 | Samples |
| SN65175DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SN65175 | Samples |
| SN75175D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | 0 to 70 | SN75175 | |
| SN75175DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75175 | Samples |
| SN75175N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75175N | Samples |
| SN75175NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75175 | Samples |
| SN75175NSRG4 | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75175 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75175NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN75175NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65175DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN75175DR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| SN75175DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN75175NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN75175NSR | SO | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65175D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN75175N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES:

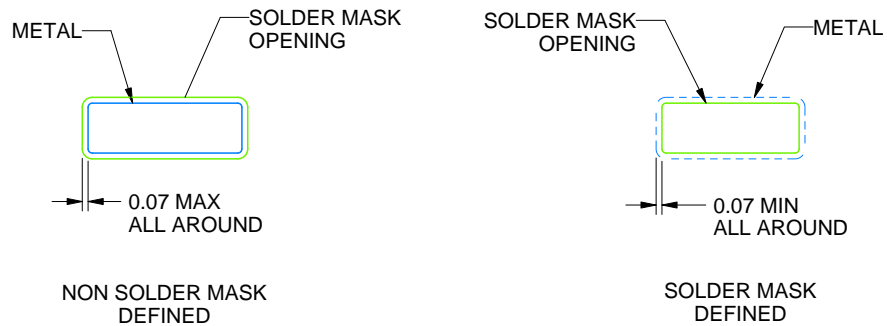
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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