TL081, TL081A, TL081B, TL081H
TL082, TL082A, TL082B, TL082H
TL084, TL084A, TL084B, TL084H
ZHCSMO4N – FEBRUARY 1977 – REVISED JUNE 2024

TL08xx FET 输入运算放大器

1 特性

- 高压摆率：20V/μs（TL08xH，典型值）
- 低失调电压：1mV（TL08xH，典型值）
- 低失调电压漂移：2μV/°C
- 低功耗：940μA/通道（TL08xH，典型值）
- 宽共模和差分
  电压范围
  - 共模输入电压范围
    包括 V_{CC+}
- 低输入偏置和失调电流
- 低噪声：
  f = 1kHz 时，V_n = 18nV/√Hz（典型值）
- 输出短路保护
- 低总计谐波失真：0.003%（典型值）
- 宽电源电压：
  ±2.25V 至 ±20V，4.5V 至 40V

2 应用

- 太阳能：串式和中央逆变器
- 电机驱动器：交流和伺服驱动控制及功率级模块
- 单相在线式 UPS
- 三相 UPS
- 专业音频混合器
- 电池测试设备

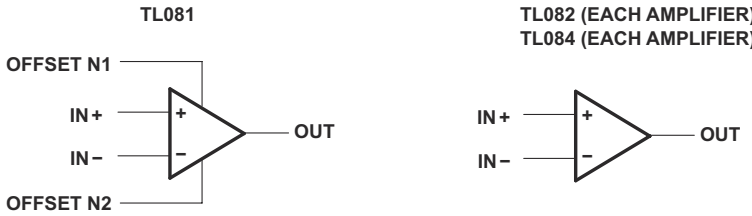
3 说明

TL08xH（TL081H、TL082H 和 TL084H）系列器件是业界通用的 TL08x（TL081、TL082 和 TL084）器件的下一代版本。这些器件为成本敏感型应用提供了卓越的价值，其特性包括低失调电压（1mV，典型值）、高压摆率 (20V/μs) 和正电源的共模输入。得益于高 ESD（1.5kV，HBM）、集成 EMI 和射频滤波器以及 –40°C 至 125°C 的完整运行温度范围，TL08xH 器件可用于要求严苛的应用。

器件信息

器件型号	封装(1)	本体尺寸（标称值）(2)
TL081x	P（PDIP，8）	9.59mm × 6.35mm
	DCK（SC70，5）	2mm × 1.25mm
	PS（SO，8）	6.2mm × 5.3mm
	D（SOIC，8）	4.9mm × 3.9mm
	DBV（SOT-23，5）	2.9mm × 1.6mm
TL082x	P（PDIP，8）	9.59mm × 6.35mm
	PS（SO，8）	6.2mm × 5.3mm
	D（SOIC，8）	4.9mm × 3.9mm
	DDF（SOT-23，8）	2.9mm × 1.6mm
	PW（TSSOP，8）	4.4mm × 3mm
TL082M	JG（CDIP，8）	9.6mm × 6.67mm
	FK（LCCC，20）	8.89mm × 8.89mm
TL084x	N（PDIP，14）	19.3mm × 6.35mm
	NS（SO，14）	10.3mm × 5.3mm
	D（SOIC，14）	8.65mm × 3.91mm
	DYY（SOT-23，14）	4.2mm × 2mm
	PW（TSSOP，14）	5mm × 4.4mm
TL084M	J（CDIP，14）	19.56mm × 6.67mm
	FK（LCCC，20）	8.89mm × 8.89mm

(1) 有关更多信息，请参阅节 11。
(2) 本体尺寸（长 x 宽）为标称值，不包括引脚。



逻辑符号

Table of Contents

4 Pin Configuration and Functions

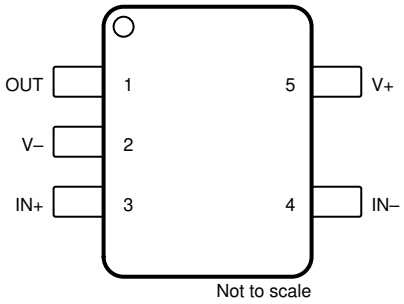


图 4-1. TL081H DBV Package, 5-Pin SOT-23 (Top View)

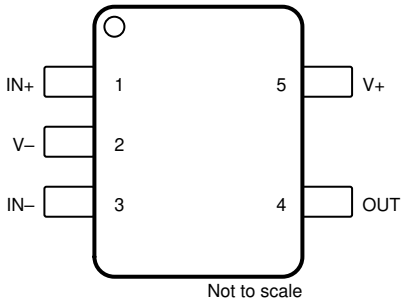
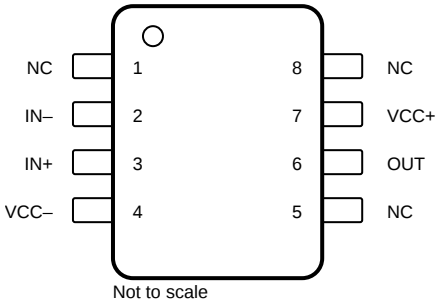


图 4-2. TL081H DCK Package, 5-Pin SC70 (Top View)



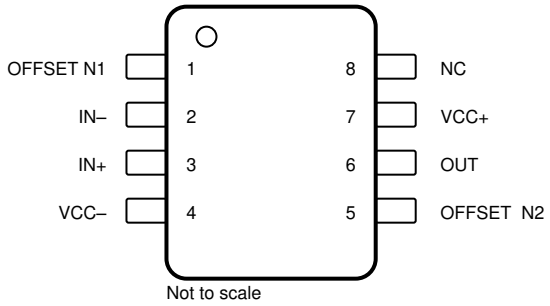
NC- no internal connection

图 4-3. TL081H D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions: TL081H

PIN				TYPE[1]	DESCRIPTION
NAME	DBV	DCK	D		
IN –	4	3	2	I	Inverting input
IN+	3	1	3	I	Noninverting input
NC	—	—	8	—	Do not connect
NC	—	—	1	—	Do not connect
NC	—	—	5	—	Do not connect
OUT	1	4	6	O	Output
VCC –	2	2	4	—	Power supply
VCC+	5	5	7	—	Power supply

(1) I = input, O = output



NC- no internal connection

图 4-4. TL081x D, P, and PS Package, 8-Pin SOIC, PDIP, and SO (Top View)

表 4-2. Pin Functions: TL081x

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN –	2	I	Inverting input
IN+	3	I	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC –	4	—	Power supply
VCC+	7	—	Power supply

(1) I = input, O = output

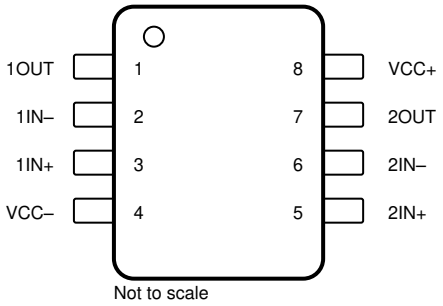
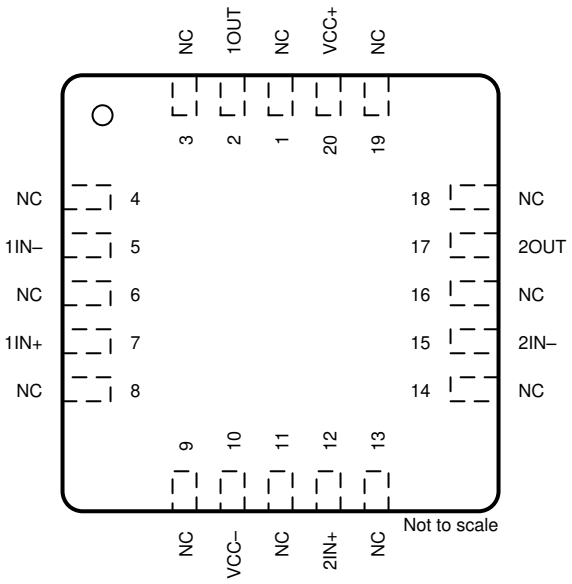


图 4-5. TL082x D, DDF, DGK, JG, P, PS, and PW Package, 8-Pin SOIC, SOT-23 (8), VSSOP, CDIP, PDIP, SO, and TSSOP (Top View)

表 4-3. Pin Functions: TL082x

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1IN –	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN –	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
VCC –	4	—	Power supply
VCC+	8	—	Power supply

(1) I = input, O = output



NC- no internal connection

图 4-6. TL082 FK Package, 20-Pin LCCC (Top View)

表 4-4. Pin Functions: TL082x

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1IN –	5	I	Inverting input
1IN+	7	I	Noninverting input
1OUT	2	O	Output
2IN –	15	I	Inverting input
2IN+	12	I	Noninverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC –	10	—	Power supply
VCC+	20	—	Power supply

(1) I = input, O = output

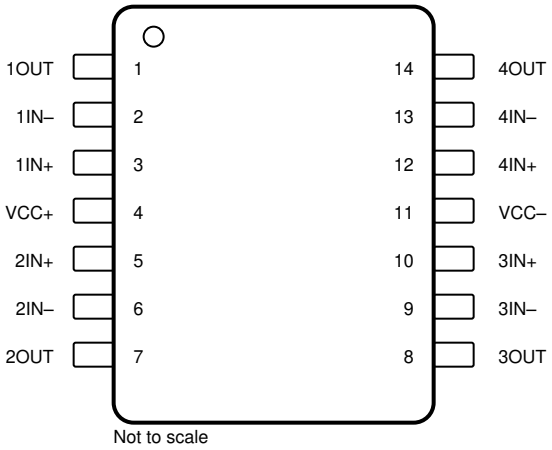
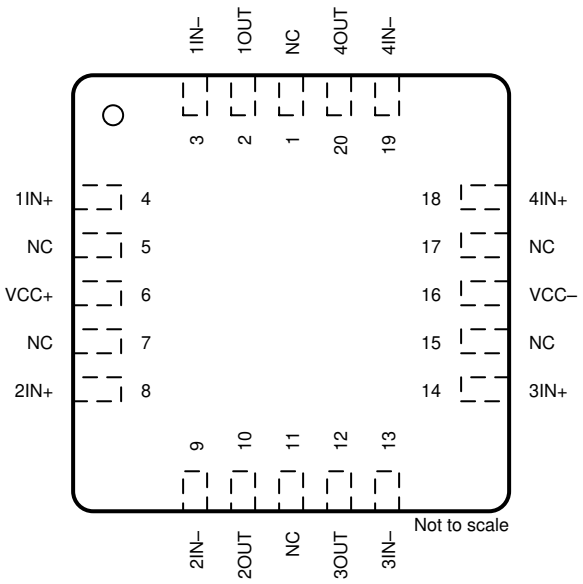


图 4-7. TL084x D, N, NS, PW, J, and DYY Package, 14-Pin SOIC, PDIP, SO, TSSOP, CDIP, and SOT-23 (14) (Top View)

表 4-5. Pin Functions: TL084x

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1IN –	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN –	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
3IN –	9	I	Inverting input
3IN+	10	I	Noninverting input
3OUT	8	O	Output
4IN –	13	I	Inverting input
4IN+	12	I	Noninverting input
4OUT	14	O	Output
V_{CC-}	11	—	Power supply
V_{CC+}	4	—	Power supply

(1) I = input, O = output



NC- no internal connection

图 4-8. TL084 FK Package, 20-Pin LCCC (Top View)

表 4-6. Pin Functions: TL084x

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1IN –	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN –	9	I	Inverting input
2IN+	8	I	Noninverting input
2OUT	10	O	Output
3IN –	13	I	Inverting input
3IN+	14	I	Noninverting input
3OUT	12	O	Output
4IN –	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC –	16	—	Power supply
VCC+	6	—	Power supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V –)		All NS and PS packages; All TL08xM devices	–0.3	36	V
		All other devices	0	42	V
Signal input pins	Common-mode voltage (3)	All NS and PS packages; All TL08xM devices	(V –) – 0.3	(V –) + 36	V
		All other devices	(V –) – 0.5	(V+) + 0.5	V
	Differential voltage (3)	All NS and PS packages; All TL08xM devices (4)	(V –) – 0.3	(V –) + 36	V
		All other devices		V_S + 0.2	V
	Current (3)	All NS and PS packages; All TL07xM devices		50	mA
		All other devices	–10	10	mA
Output short-circuit (2)			Continuous		
Operating ambient temperature, T_A			–55	150	°C
Junction temperature, T_J				150	°C
Case temperature for 60 seconds - FK package				260	°C
Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds				300	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10 mA or less.
(4) Differential voltage only limited by input voltage.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V –)	All NS and PS packages; All TL08xM devices(1)	10	30	V
		All other devices	4.5	40	V
V_I	Input voltage range	All NS and PS packages; All TL08xM devices	(V –) + 2	(V+) + 0.1	V
		All other devices	(V –) + 4	(V+) + 0.1	V
T_A	Specified temperature	TL08xM	–55	125	°C
		TL08xH	–40	125	°C
		TL08xI	–40	85	°C
		TL08xC	0	70	°C

(1) V+ and V – are not required to be of equal magnitude, provided that the total V_S (V+ – V –) is between 10V and 30V.

5.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TL081xx					UNIT
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	P (PDIP)	PS (SO)	
		8 PINS	5 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.8	217.5	212.2	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.6	113.1	111.1	–	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.3	63.8	79.4	–	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.8	34.8	51.8	–	–	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.5	63.5	79.0	–	–	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TL082xx								UNIT
		D (SOIC)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SO)	PW (TSSOP)	U (CFP)	
		8 PINS	8 PINS	20 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.8	181.5	–	–	85	95	200.3	169.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.2	112.5	5.61	15.05	–	–	89.4	62.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.4	98.2	–	–	–	–	131.0	176.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	36.8	17.2	–	–	–	–	22.2	48.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.6	97.6	–	–	–	–	129.3	144.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	N/A	5.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		TL084xx								UNIT
		D (SOIC)	DYY (SOT-23)	FK (TSSOP)	J (TSSOP)	N (TSSOP)	NS (TSSOP)	PW (TSSOP)	W (TSSOP)	
		14 PINS	14 PINS	20 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.2	153.2	–	–	80	76	–	128.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	88.7	5.61	14.5	–	–	14.5	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.2	65.4	–	–	–	–	–	127.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.8	9.5	–	–	–	–	–	29	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.8	65.0	–	–	–	–	–	106.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	–	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.7 Electrical Characteristics: TL08xH

For $V_S = (V_{CC+}) - (V_{CC-}) = 4.5V$ to 40V (±2.25V to ±20V) at $T_A = 25°C$, $R_L = 10k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±4	mV
			T_A = –40°C to 125°C			±5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±2		µV/℃
PSRR	Input offset voltage versus power supply	V_S = 5V to 40V, $V_{CM} = V_S / 2$	T_A = –40°C to 125°C		±1	±10	µV/V
	Channel separation	f = 0Hz			10		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±120	pA
			DCK and DBV packages		±1	±300	pA
			T_A = –40°C to 125°C (1)			±5	nA
I_{OS}	Input offset current				±0.5	±120	pA
			DCK and DBV packages		±0.5	±250	pA
			T_A = –40°C to 125°C (1)			±5	nA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	Input voltage noise density	f = 1kHz			37		$nV/\sqrt{Hz}$
		f = 10kHz			21		
i_N	Input current noise	f = 1kHz			80		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			$(V_{CC-}) + 1.5$		(V_{CC+})	V
CMRR	Common-mode rejection ratio	V_S = 40V, $(V_{CC-}) + 2.5V < V_{CM} < (V_{CC+}) - 1.5V$		100	105		dB
			T_A = –40°C to 125°C	95			dB
		V_S = 40V, $(V_{CC-}) + 2.5V < V_{CM} < (V_{CC+})$		90	105		dB
			T_A = –40°C to 125°C	80			dB
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 2		MΩ ||pF
Z_{ICM}	Common-mode				6 || 1		TΩ ||pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40V, $V_{CM} = V_S / 2$, $(V_{CC-}) + 0.3V < V_O < (V_{CC+}) - 0.3V$	T_A = –40°C to 125°C	118	125		dB
A_{OL}	Open-loop voltage gain	V_S = 40V, $V_{CM} = V_S / 2$, R_L = 2kΩ, $(V_{CC-}) + 1.2V < V_O < (V_{CC+}) - 1.2V$	T_A = –40°C to 125°C	115	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.25		MHz
SR	Slew rate	V_S = 40V, G = +1, C_L = 20pF			20		V/µs
t_S	Settling time	To 0.1%, V_S = 40V, V_{STEP} = 10V , G = +1, CL = 20pF			0.63		µs
		To 0.1%, V_S = 40V, V_{STEP} = 2V , G = +1, CL = 20pF			0.56		
		To 0.01%, V_S = 40V, V_{STEP} = 10V , G = +1, CL = 20pF			0.91		
		To 0.01%, V_S = 40V, V_{STEP} = 2V , G = +1, CL = 20pF			0.48		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20pF			56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	V_S = 40V, V_O = 6V_{RMS}, G = +1, f = 1kHz			0.00012		%

5.7 Electrical Characteristics: TL08xH（续）

For $V_S = (V_{CC+}) - (V_{CC-}) = 4.5V$ to 40V (±2.25V to ±20V) at $T_A = 25°C$, $R_L = 10k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\ UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
EMIRR	EMI rejection ratio	f = 1GHz			53		dB
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	V_S = 40V, R_L = 10kΩ		115	210	mV
			V_S = 40V, R_L = 2kΩ		520	965	
		Negative rail headroom	V_S = 40V, R_L = 10kΩ		105	215	
			V_S = 40V, R_L = 2kΩ		500	1030	
I_{SC}	Short-circuit current				±26		mA
C_{LOAD}	Capacitive load drive				300		pF
Z_O	Open-loop output impedance	f = 1MHz, I_O = 0 A			125		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			937.5	1125	μA
		I_O = 0 A, (TL081H)			960	1156	
		I_O = 0 A	T_A = –40°C to 125°C			1130	
		I_O = 0 A, (TL082H)				1143	
		I_O = 0 A, (TL071H)				1160	
	Turn-On Time	At T_A = 25°C, V_S = 40V, V_S ramp rate > 0.3V/μs			60		μs

(1) Max I_B and I_{os} data is specified based on characterization results.

5.8 Electrical Characteristics (DC): TL08xC, TL08xAC, TL08xBC, TL08xI, TL08xM

For $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15V$ at $T_A = 25°C$, unless otherwise noted

PARAMETER		TEST CONDITIONS(1) (2)			MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 50\ \Omega$	TL08xC			3	10	mV
				T_A = Full range			13	
			TL08xAC			3	6	
				T_A = Full range			7.5	
			TL08xBC			2	3	
				T_A = Full range			5	
			TL08xI			3	6	
				T_A = Full range			8	
			TL081M, TL082M			3	6	
				T_A = Full range			9	
			TL084M			3	9	
				T_A = Full range			15	
dV_{OS}/dT	Input offset voltage drift	$V_O = 0V$, $R_S = 50\ \Omega$	T_A = Full range			±18		μV/℃
I_{OS}	Input offset current	$V_O = 0V$	TL08xC			5	100	pA
				T_A = Full range			10	nA
			TL08xAC, TL08xBC, TL08xI			5	100	pA
				T_A = Full range			2	nA
			TL08xM			5	100	pA
				T_A = Full range			20	nA
I_B	Input bias current	$V_O = 0V$	TL08xC, TL08xAC, TL08xBC, TL08xI			65	200	pA
				T_A = Full range			7	nA
			TL081M, TL082M			65	200	pA
				T_A = Full range			50	nA
			TL084M			65	200	pA
				T_A = Full range			20	nA
V_{CM}	Common-mode voltage range				±11	–12 to 15		V
VOM	Maximum peak output voltage swing	$R_L = 10k\ \Omega$	T_A = Full range		±12	±13.5		V
		$R_L \geqslant 10k\ \Omega$			±12			
		$R_L \geqslant 2k\ \Omega$			±10			
A_{OL}	Open-loop voltage gain	$V_O = 0V$	TL08xC		25	200		V/mV
				T_A = Full range	15			
			TL08xAC, TL08xBC, TL08xI		50	200		
				T_A = Full range	25			
			TL08xM		35	200		
				T_A = Full range	15			
GBW	Gain-bandwidth product	All NS and PS packages; All TL08xM devices				3		MHz
		All other devices				5.25		
R_{ID}	Common-mode input resistance					1		TΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$, $V_O = 0V$, $R_S = 50\ \Omega$	TL08xC		70	100		dB
			TL08xAC, TL08xBC, TL08xI		75	100		
			TL08xM		80	86		
PSRR	Input offset voltage versus power supply	$V_S = \pm 9V$ to $\pm 18V$, $V_O = 0V$, $R_S = 50\ \Omega$	TL08xC		70	100		dB
			TL08xAC, TL08xBC, TL08xI		80	100		
			TL08xM		80	86		

5.8 Electrical Characteristics (DC): TL08xC, TL08xAC, TL08xBC, TL08xI, TL08xM（续）

For $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15V$ at $T_A = 25°C$, unless otherwise noted

PARAMETER		TEST CONDITIONS(1) (2)	MIN	TYP	MAX	UNIT
I_Q	Quiescent current per amplifier	V_O = 0V; no load		1.4	2.5	mA
	Channel separation	f = 0Hz		1		µV/V

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C for the TL07xC, TL07xAC, and TL07xBC; T_A = –40°C to 85°C for the TL07xI; and T_A = –55°C to 125°C for the TL07xM.

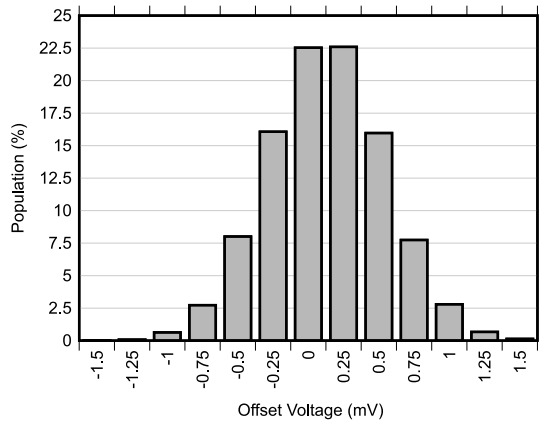
5.9 Electrical Characteristics (AC): TL08xC, TL08xAC, TL08xBC, TL08xI, TL08xM

For $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15V$ at $T_A = 25°C$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate	V_I = 10V, C_L = 100pF, R_L = 2kΩ	TL08xM	5	20		V/μs
			TL08xC, TL08xAC, TL08xBC, TL08xI	8	20		V/μs
t_S	Settling time	V_I = 20V, C_L = 100pF, R_L = 2kΩ			0.1		μs
					20%		
e_N	Input voltage noise density	All PS and NS packages; All TL08xM devices	R_S = 20 Ω, f = 1kHz		18		nV/√Hz
		All other devices	f = 1kHz		37		nV/√Hz
			f = 10kHz		21		
E_N	Input voltage noise	All PS and NS packages; All TL08xM devices	R_S = 20 Ω, f = 10Hz to 10kHz		4		μV_{RMS}
		All other devices	f = 0.1Hz to 10Hz		1.4		μV_{RMS}
i_N	Input current noise	R_S = 20 Ω, f = 1kHz			10		fA/√Hz
	Phase margin	TL08xC, TL08xAC, TL08xBC, TL08xI	G = +1, R_L = 10kΩ, C_L = 20pF		56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	All PS and NS packages; All TL08xM devices	V_O = $6V_{RMS}$, $R_L \geq$ 2kΩ, f = 1kHz, G = +1, $R_S \leq$ 1kΩ		0.003		%
		All other devices	V_S = 40V, V_O = $6V_{RMS}$, G = +1, f = 1kHz		0.00012		%
EMIRR	EMI rejection ratio	TL08xC, TL08xAC, TL08xBC, TL08xI	f = 1GHz		53		dB
Z_O	Open-loop output impedance	TL07xC, TL07xAC, TL07xBC, TL07xI	f = 1MHz, I_O = 0 A		125		Ω

5.10 Typical Characteristics: TL08xH

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)



T_A = 25°C

图 5-1. Offset Voltage Production Distribution

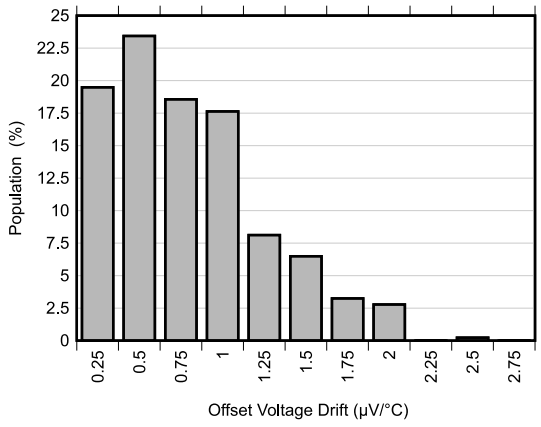
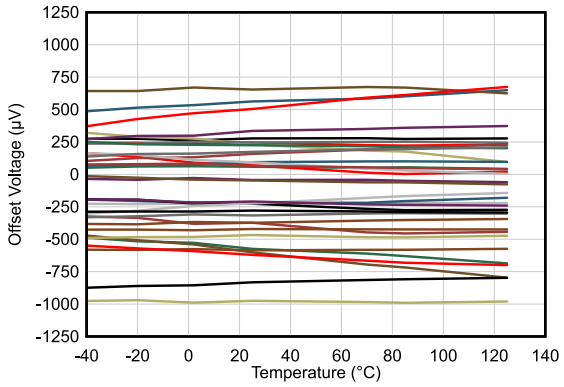
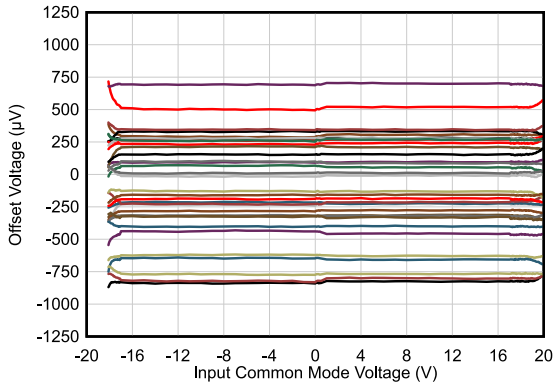


图 5-2. Offset Voltage Drift Distribution



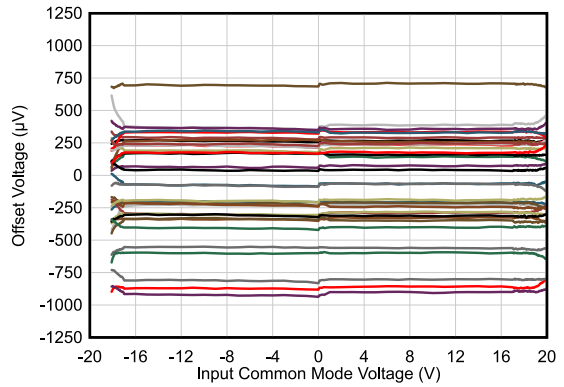
V_{CM} = V_S / 2

图 5-3. Offset Voltage vs Temperature



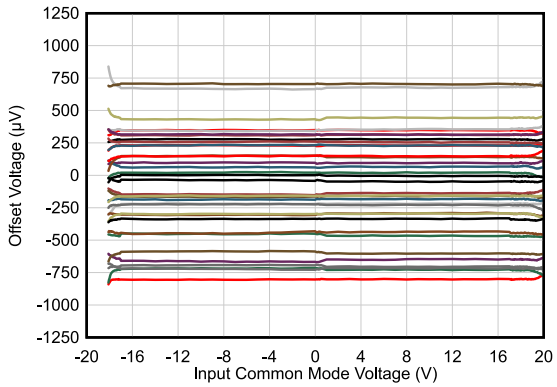
T_A = 25°C

图 5-4. Offset Voltage vs Common-Mode Voltage



T_A = 125°C

图 5-5. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

图 5-6. Offset Voltage vs Common-Mode Voltage

5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

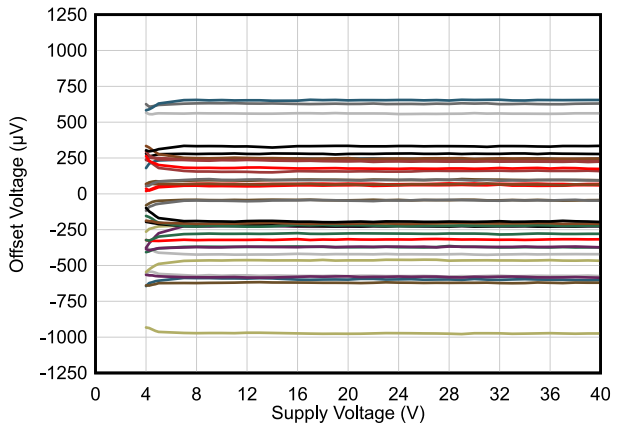


图 5-7. Offset Voltage vs Power Supply

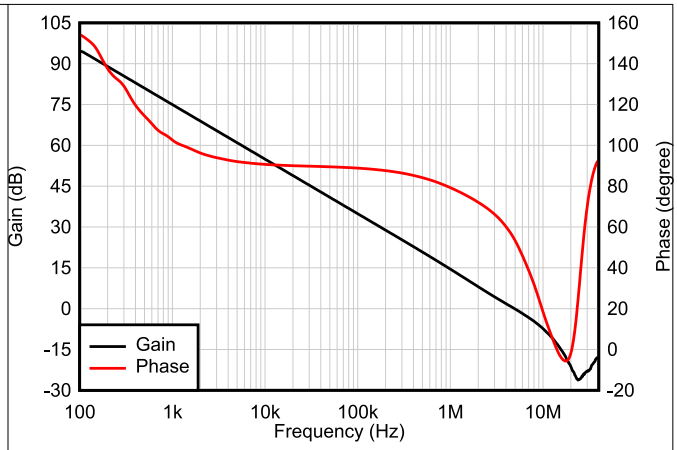


图 5-8. Open-Loop Gain and Phase vs Frequency

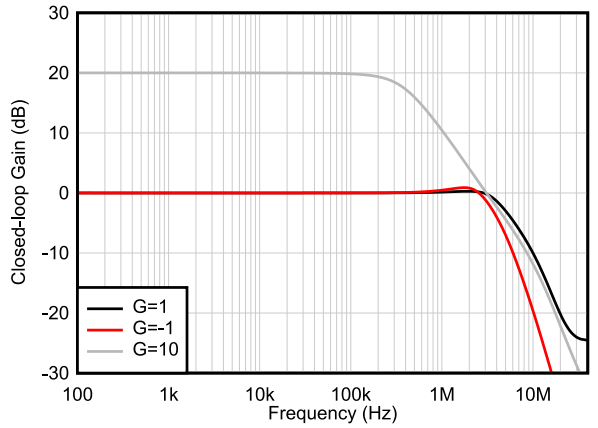


图 5-9. Closed-Loop Gain vs Frequency

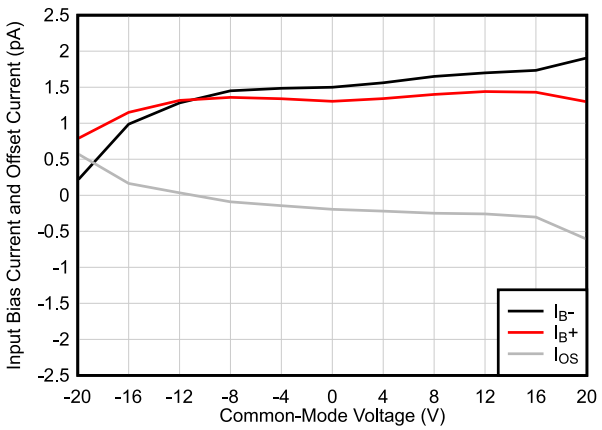


图 5-10. Input Bias Current vs Common-Mode Voltage

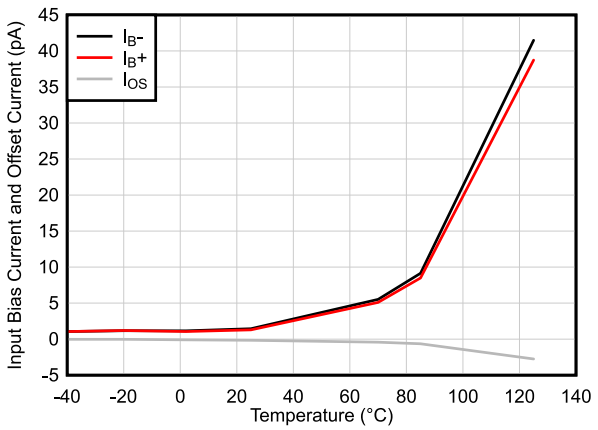


图 5-11. Input Bias Current vs Temperature

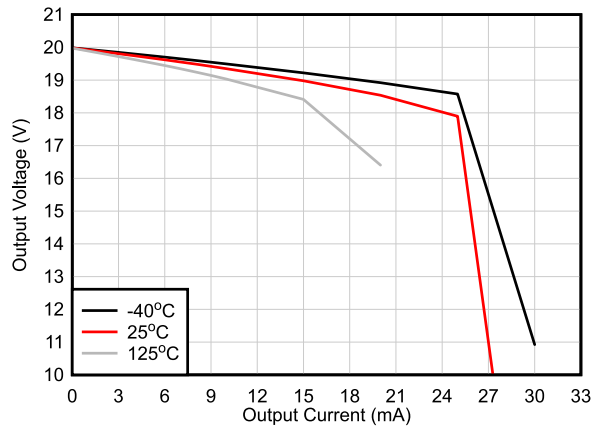


图 5-12. Output Voltage Swing vs Output Current (Sourcing)

5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

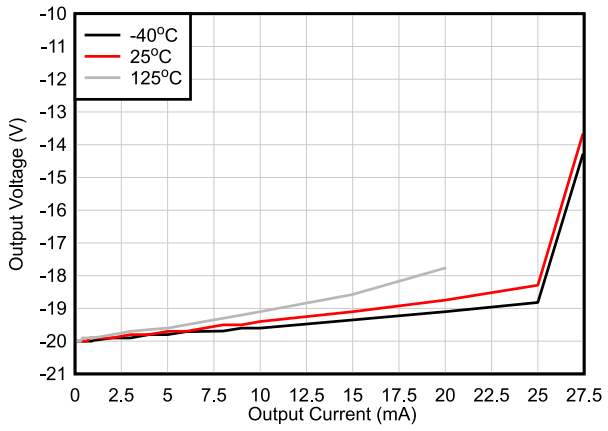


图 5-13. Output Voltage Swing vs Output Current (Sinking)

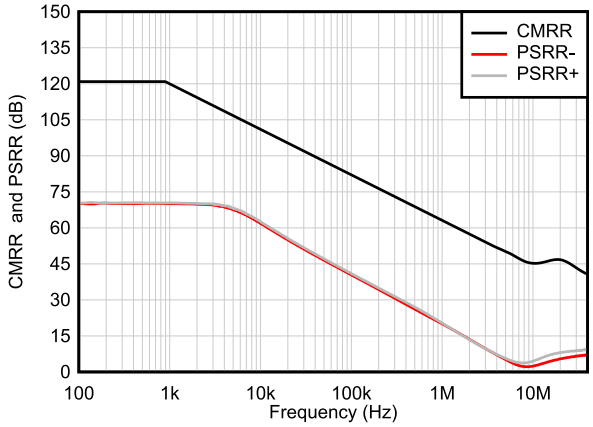


图 5-14. CMRR and PSRR vs Frequency

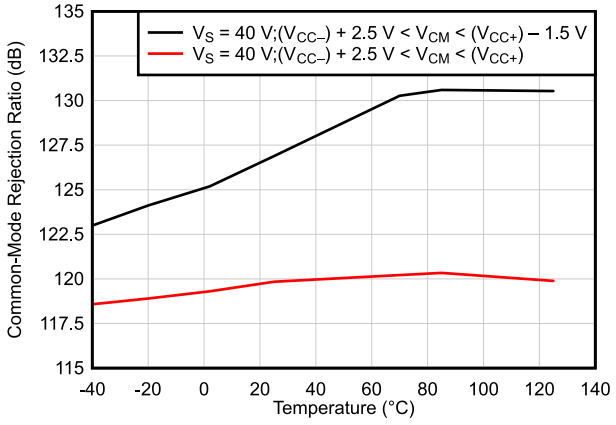


图 5-15. CMRR vs Temperature (dB)

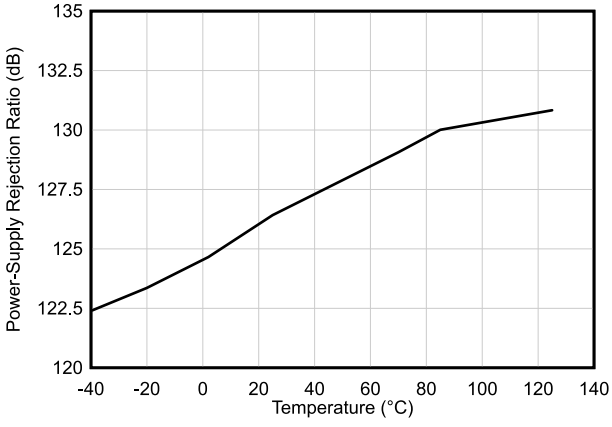


图 5-16. PSRR vs Temperature (dB)

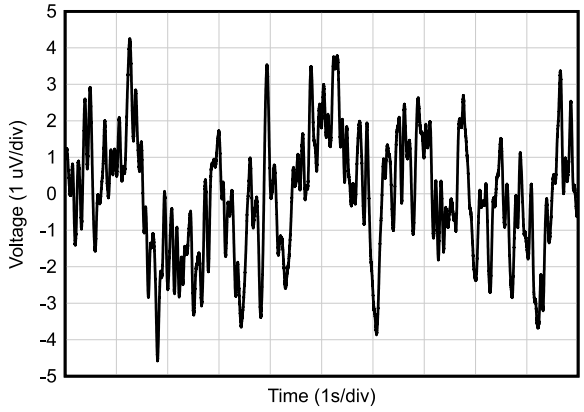


图 5-17. 0.1-Hz to 10-Hz Noise

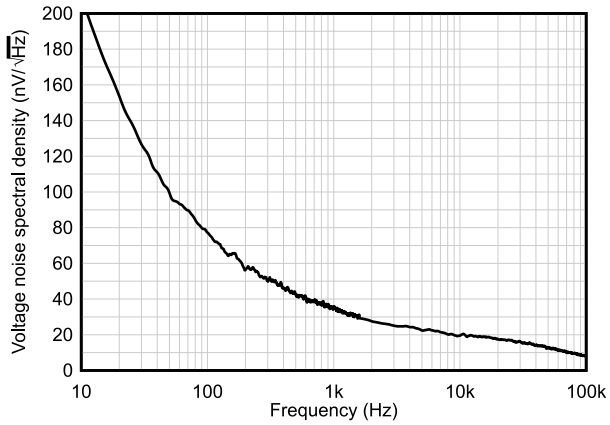
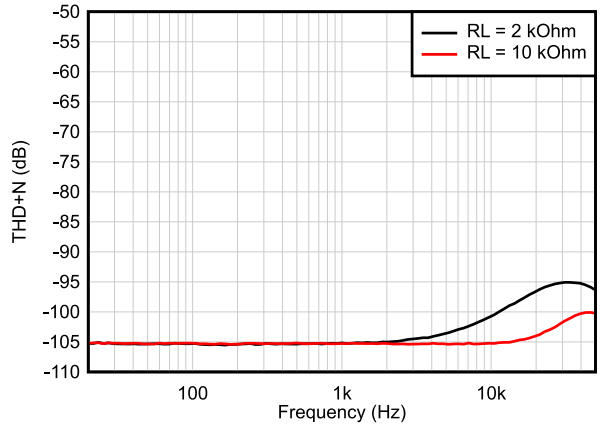


图 5-18. Input Voltage Noise Spectral Density vs Frequency

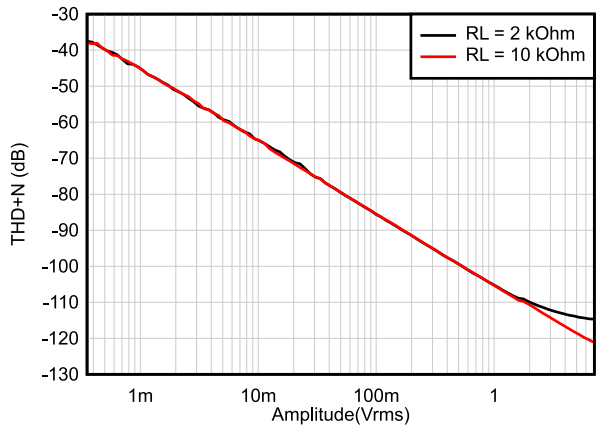
5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)



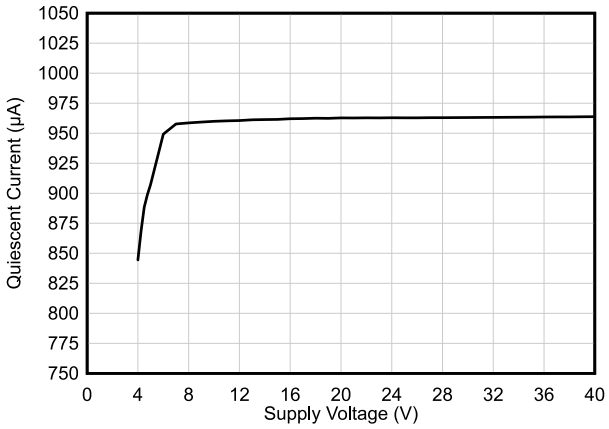
BW = 80kHz, V_{OUT} = 1V_{RMS}

图 5-19. THD+N Ratio vs Frequency



BW = 80kHz, f = 1kHz

图 5-20. THD+N vs Output Amplitude



V_{CM} = V_S / 2

图 5-21. Quiescent Current vs Supply Voltage

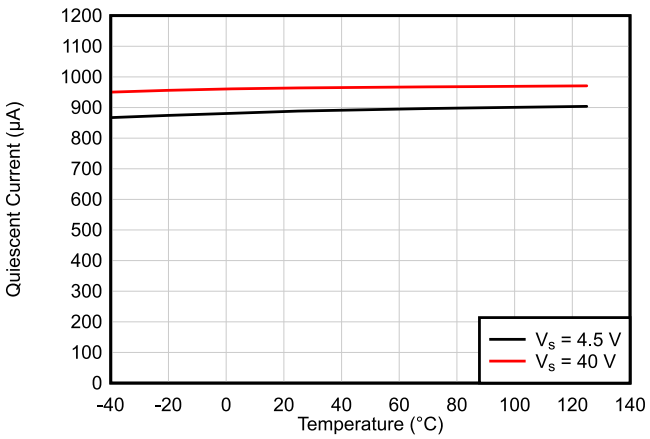


图 5-22. Quiescent Current vs Temperature

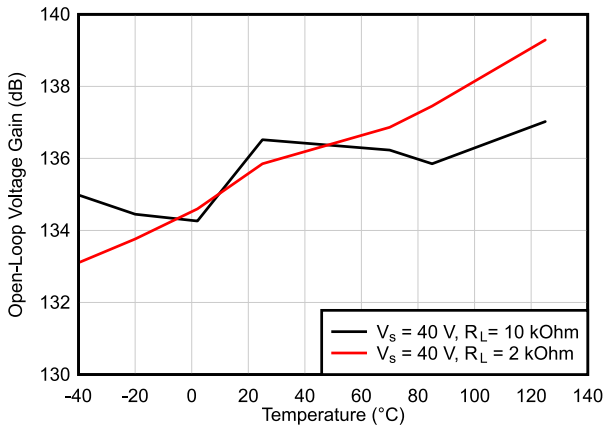


图 5-23. Open-Loop Voltage Gain vs Temperature (dB)

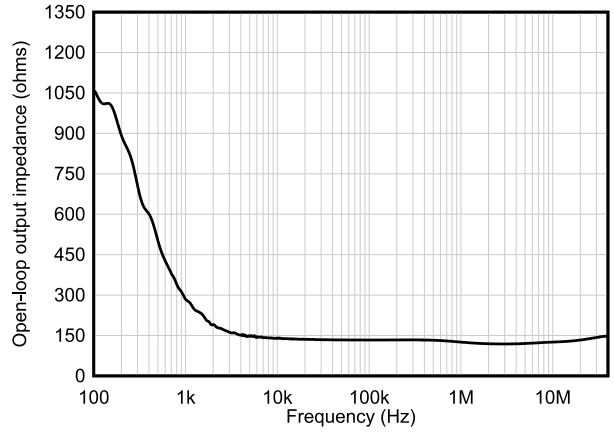
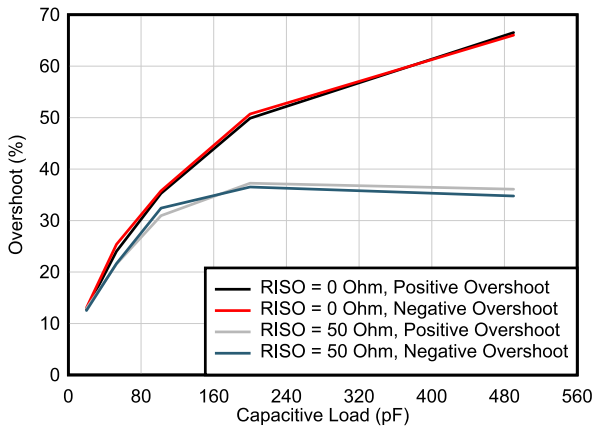


图 5-24. Open-Loop Output Impedance vs Frequency

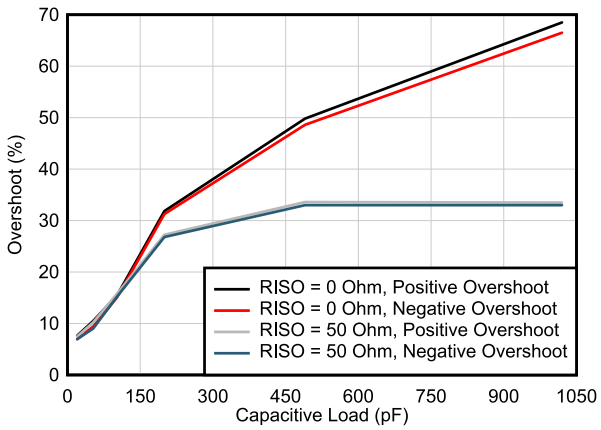
5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)



G = –1, 25-mV output step

图 5-25. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

图 5-26. Small-Signal Overshoot vs Capacitive Load

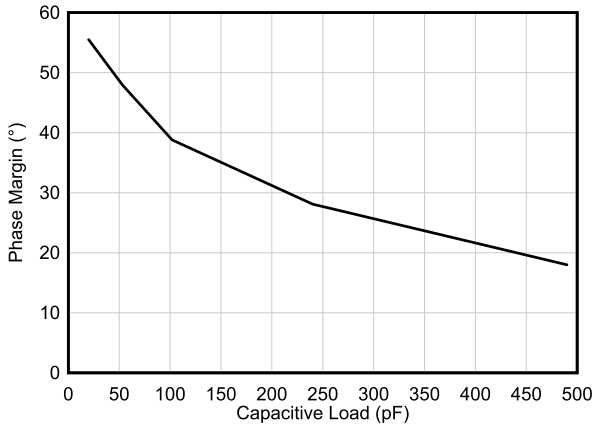
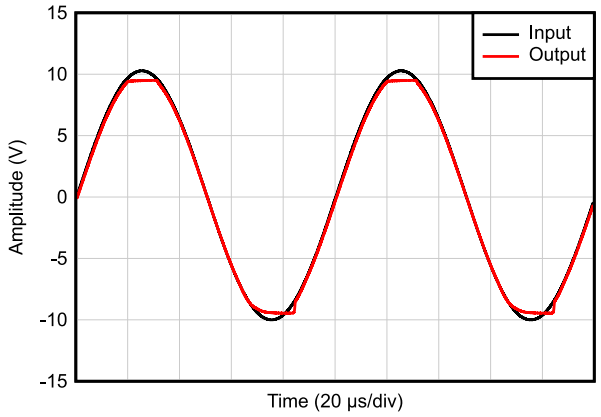
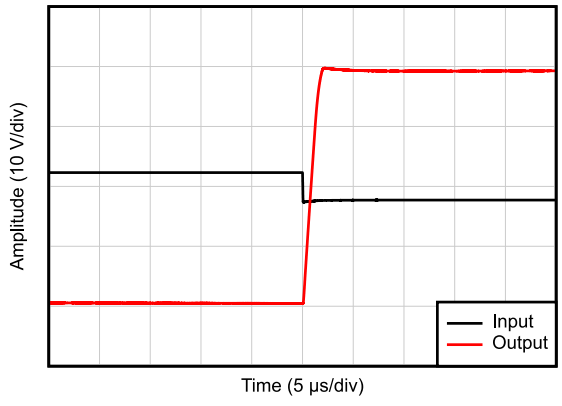


图 5-27. Phase Margin vs Capacitive Load



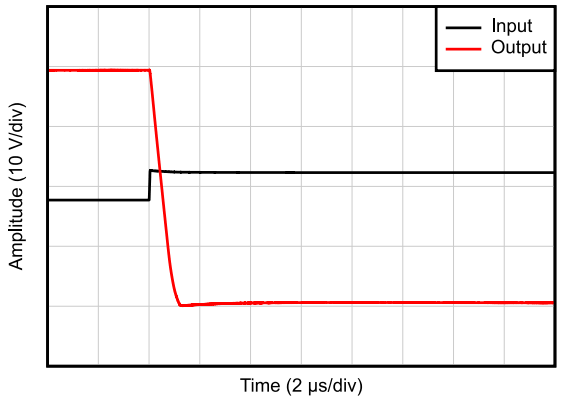
V_S = ±10V, V_{IN} = V_{OUT}

图 5-28. No Phase Reversal



G = –10

图 5-29. Positive Overload Recovery

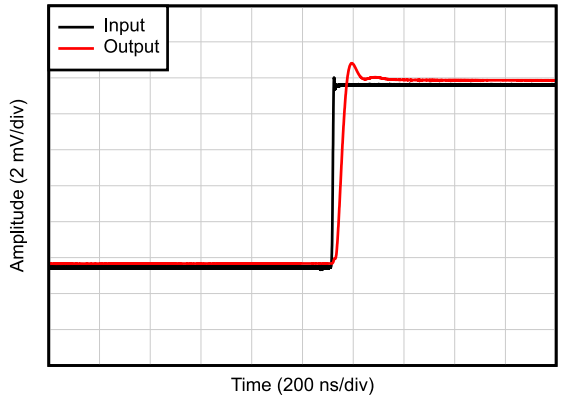


G = –10

图 5-30. Negative Overload Recovery

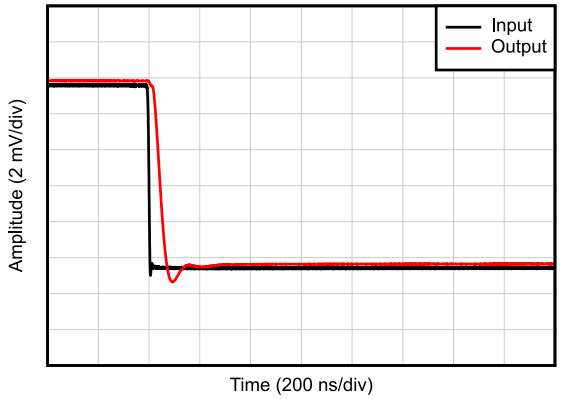
5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)



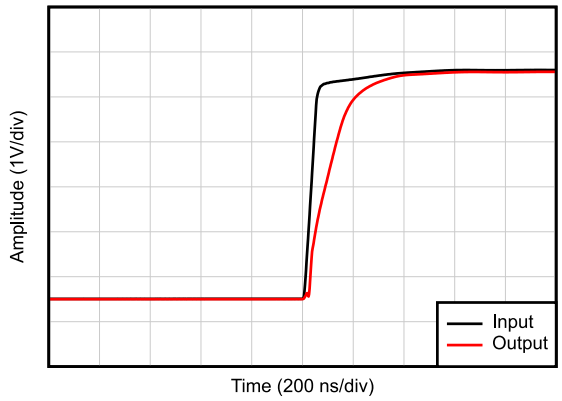
C_L = 20pF, G = 1, 10-mV step response

图 5-31. Small-Signal Step Response, Rising



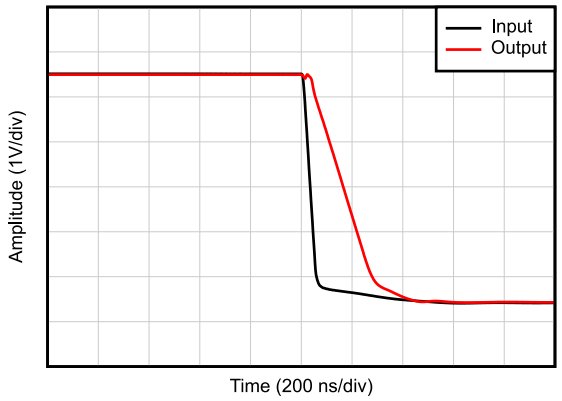
C_L = 20pF, G = 1, 10-mV step response

图 5-32. Small-Signal Step Response, Falling



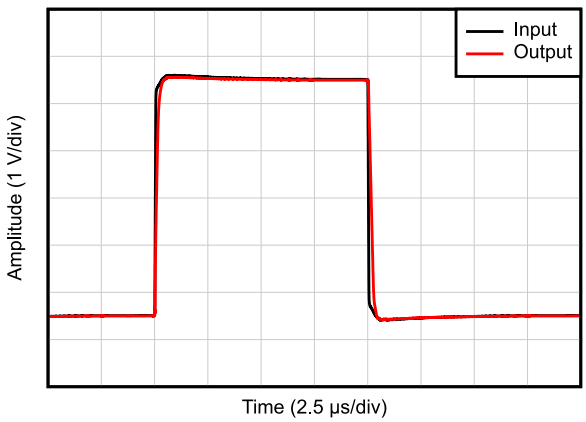
C_L = 20pF, G = 1

图 5-33. Large-Signal Step Response (Rising)



C_L = 20pF, G = 1

图 5-34. Large-Signal Step Response (Falling)



C_L = 20pF, G = 1

图 5-35. Large-Signal Step Response

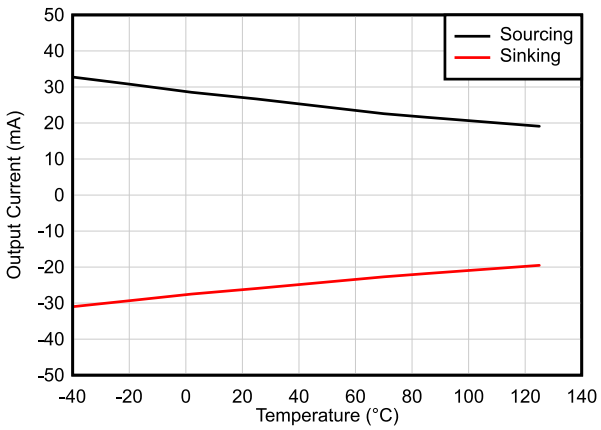


图 5-36. Short-Circuit Current vs Temperature

5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

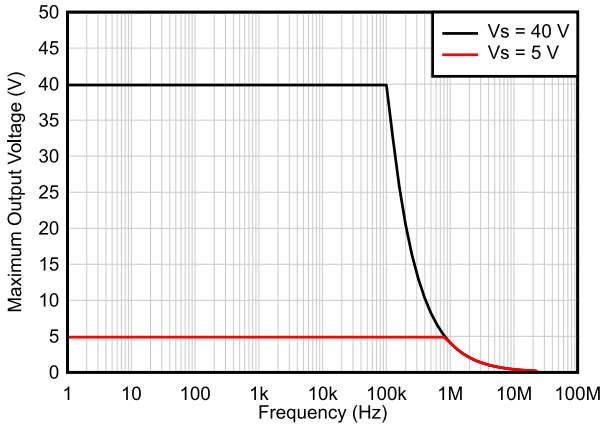


图 5-37. Maximum Output Voltage vs Frequency

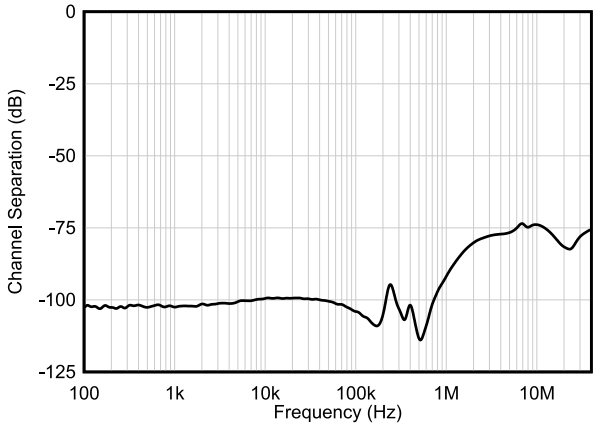


图 5-38. Channel Separation vs Frequency

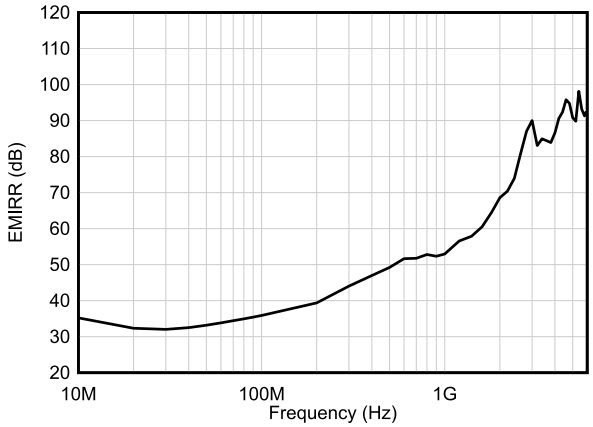


图 5-39. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Parameter Measurement Information

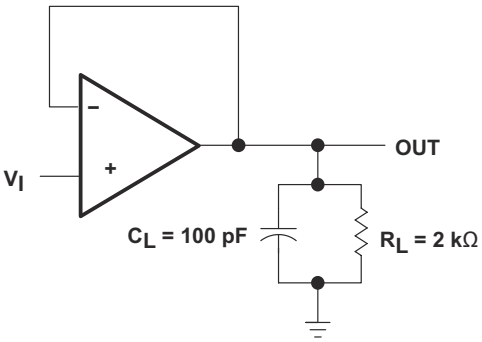


图 6-1. Test Figure 1

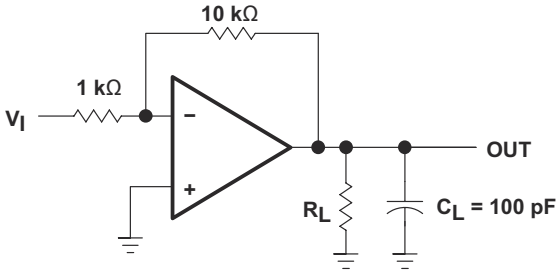


图 6-2. Test Figure 2

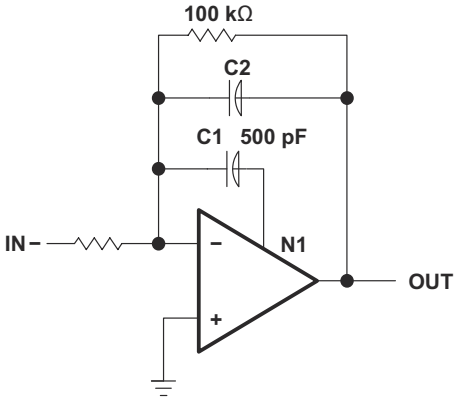


图 6-3. Test Figure 3

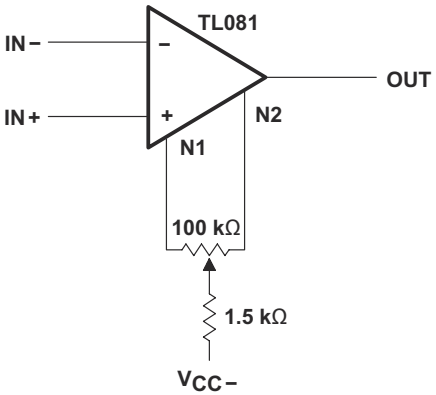


图 6-4. Test Figure 4

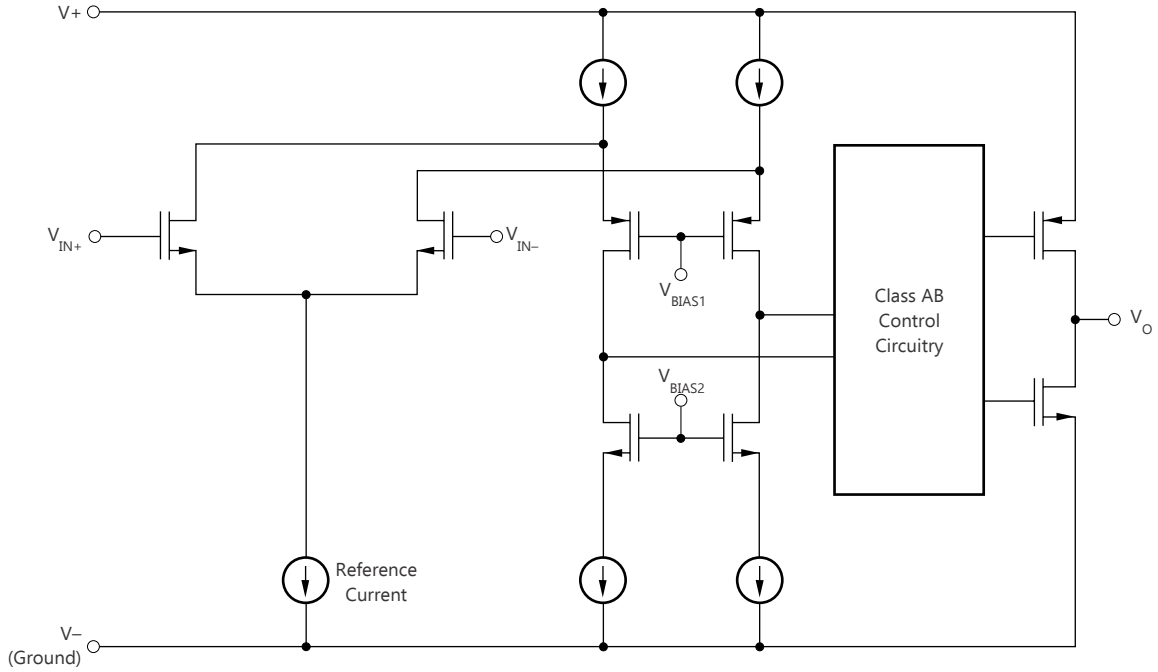
7 Detailed Description

7.1 Overview

The TL08xH family (TL081H, TL082H, and TL084H) is the next-generation family of the industry standard TL08x (TL081, TL082, and TL084) high-voltage general purpose amplifiers. These devices provide outstanding value for cost-sensitive applications requiring high slew rate with high voltage signals, such as motor drive and inverter systems.

A robust MUX-friendly input stage enhances flexibility in design, with common-mode voltage range extending to the positive rail as well as improved settling time in multi-channel applications. Low offset voltage (1mV, typ) and low offset voltage drift (2µV/°C) allows the TL08xH family to be used in rugged applications requiring precision current and voltage sensing. High voltage operation (up to 40V) and high slew rate (20V/µs) make the TL08xH family a premier choice for high-voltage applications with fast transients.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL08x devices will add little harmonic distortion when used in audio signal applications.

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 20V/ µ s slew rate.

7.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

8 Applications and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TL08x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

8.2 Typical Applications

8.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

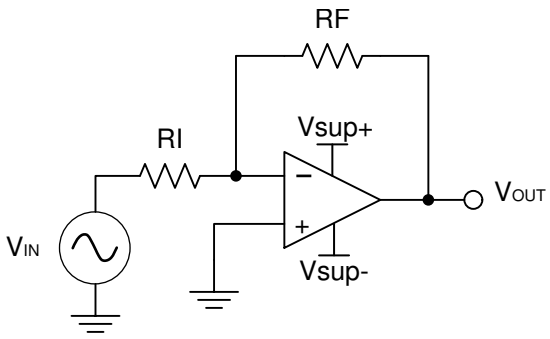


图 8-1. Schematic for Inverting Amplifier Application

8.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5V to ±1.8V. Setting the supply at ±12V is sufficient to accommodate this application.

8.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit will use currents in the milliamp range. This causes the part will not draw too much current. This example will choose 10kΩ for RI which means 36kΩ will be used for RF. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

8.2.1.3 Application Curve

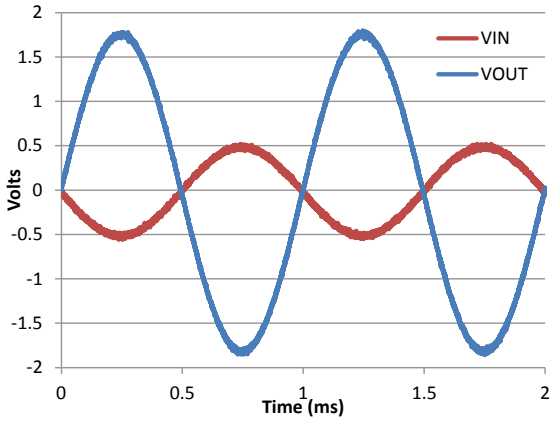


图 8-2. Input and Output Voltages of the Inverting Amplifier

8.3 System Examples

8.3.1 General Applications

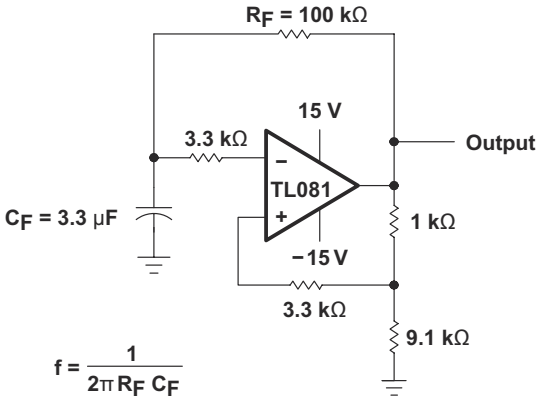


图 8-3. 0.5-Hz Square-Wave Oscillator

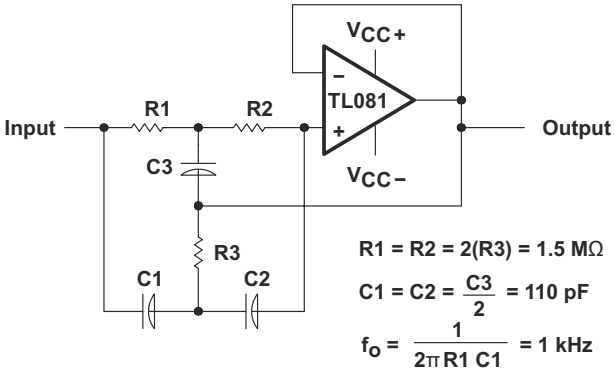


图 8-4. High-Q Notch Filter

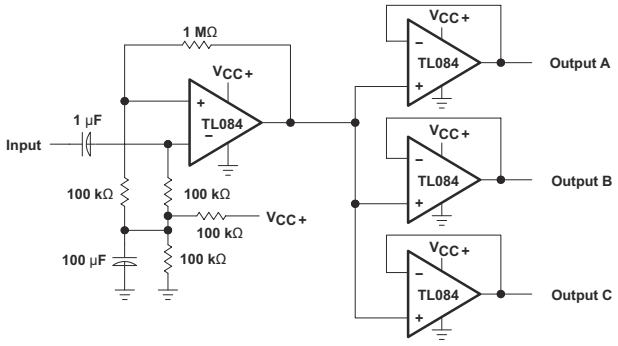
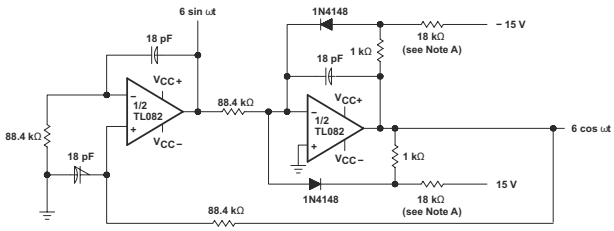


图 8-5. Audio-Distribution Amplifier



A. These resistor values may be adjusted for a symmetrical output.

图 8-6. 100-kHz Quadrature Oscillator

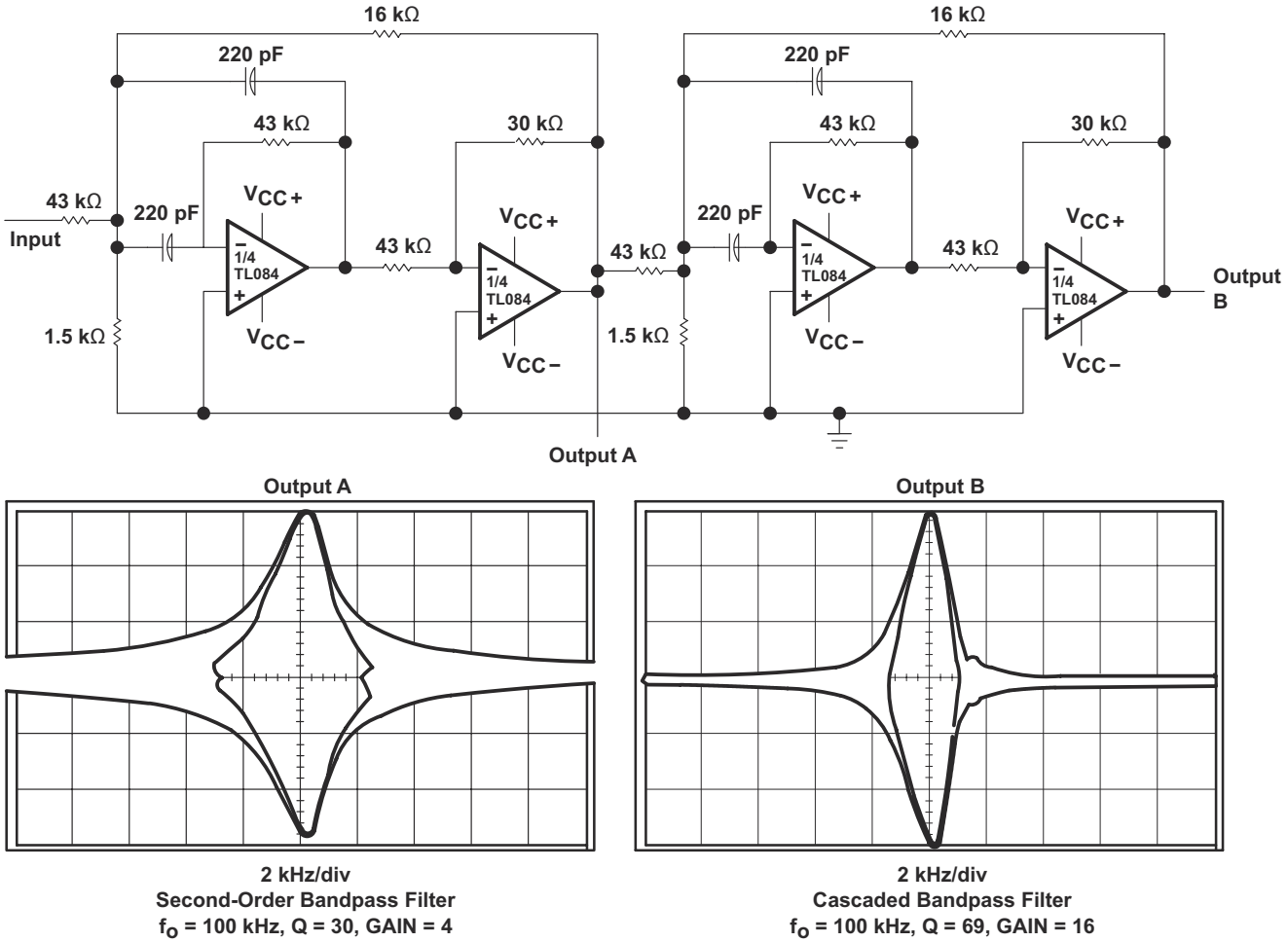


图 8-7. Positive-Feedback Bandpass Filter

8.4 Power Supply Recommendations

> 小心
>
> Supply voltages larger than 36V for a single-supply or outside the range of ±18V for a dual-supply can permanently damage the device (see 节 5.1).

Place 0.1 µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to 节 8.5.

8.5 Layout

8.5.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1 µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Ensure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in 节 8.5.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.5.2 Layout Examples

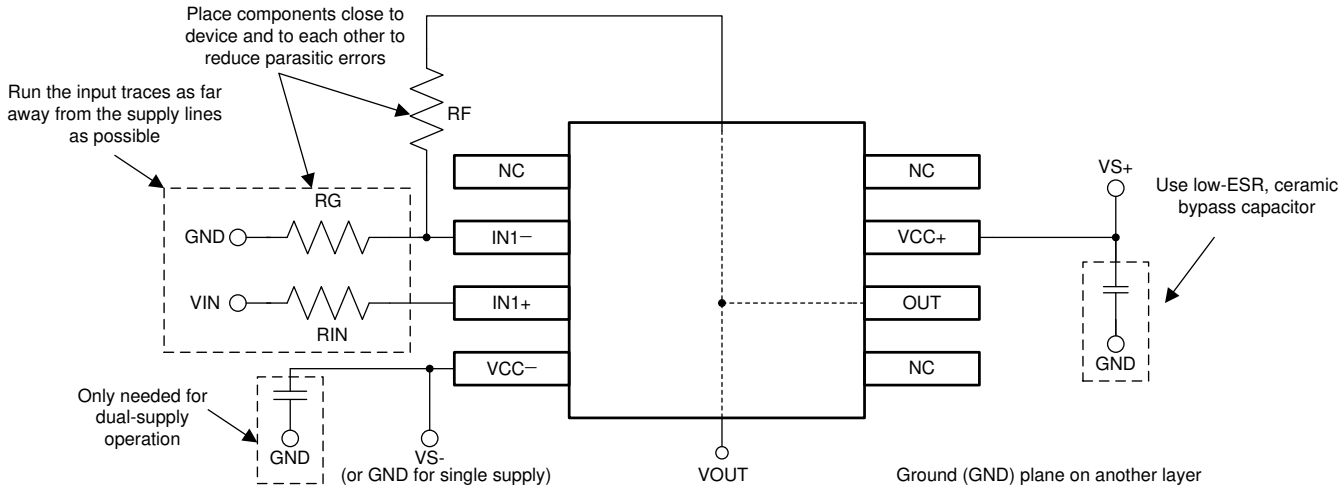


图 8-8. Operational Amplifier Board Layout for Noninverting Configuration

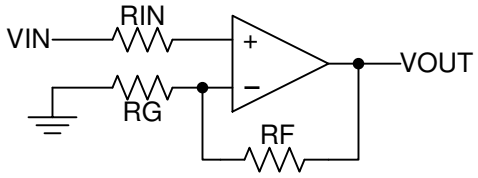


图 8-9. Operational Amplifier Schematic for Noninverting Configuration

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (December 2021) to Revision N (June 2024)	Page
• Changed Absolute Maximum Ratings, ESD Ratings, Recommended Operating Conditions, and Thermal Information sections by merging TL08xH and TL08xx specifications	9
• Changed Electrical Characteristics tables by merging TL08xC, TL08xAC, TL08xBC, TL08xI, and TL08xM specifications	14
• Increased gain bandwidth of all non-NS/non-PS packages and non-TL08xM devices from 3MHz to 5.25MHz	14
• Merged TL08xC, TL08xAC, TL08xBC, TL08xI, and TL08xM Switching Characteristics tables and renamed to Electrical Characteristics (AC)	16
• Changed input voltage noise density at 1kHz for all non-PS/non-NS packages and all non-TL08xM devices to 37nV/ √ Hz	16
• Changed THD+N for all non-PS/non-NS packages and all non-TL08xM devices to 0.00012%	16
• Updated *Functional Block Diagram* and *Feature Description* sections	25

Changes from Revision L (July 2021) to Revision M (December 2021)	Page
• Corrected DCK pinout diagram and table in *Pin Configurations and Functions* section	3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9851501Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	Samples
5962-9851501QPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
5962-9851503Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	Samples
5962-9851503QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	Samples
TL081ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	Samples
TL081BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	Samples
TL081CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples
TL081CPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70		Samples
TL081CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T081	Samples
TL081HIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T81V	Samples
TL081HIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1IP	Samples
TL081HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL081D	Samples
TL081IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL081IP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRE4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL082ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	Samples
TL082ACPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A	Samples
TL082BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082BCPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70		Samples
TL082CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRE4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL082CDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL082CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	Samples
TL082CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWRG4	ACTIVE	TSSOP	PW	8	2000	TBD	Call TI	Call TI	0 to 70		Samples
TL082HIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082F	Samples
TL082HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082D	Samples
TL082HIPWR	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082HPW	Samples
TL082IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDRE4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples
TL082IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082IPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	-40 to 85		Samples
TL082IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	Samples
TL082MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	Samples
TL082MJG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL082MJG	Samples
TL082MJGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
TL084ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL084ACN	Samples
TL084ACNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	Samples
TL084BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL084BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084BCNE4	ACTIVE	PDIP	N	14	25	TBD	Call TI	Call TI	0 to 70		Samples
TL084CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	Samples
TL084CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084HIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084HID	Samples
TL084HIDYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY	Samples
TL084HIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084PW	Samples
TL084IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084IDRE4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85		Samples
TL084IDRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85		Samples
TL084IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084MFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL084MFK	Samples
TL084MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	Samples
TL084MJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL084MJ	Samples
TL084MJB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503QCA TL084MJB	Samples
TL084QDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :

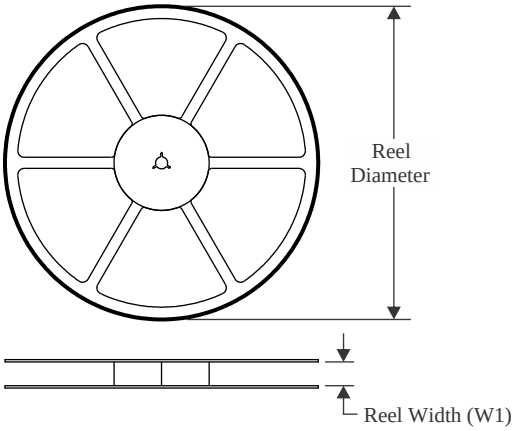
- Catalog : TL082, TL084
- Automotive : TL082-Q1, TL082-Q1
- Military : TL082M, TL084M

NOTE: Qualified Version Definitions:

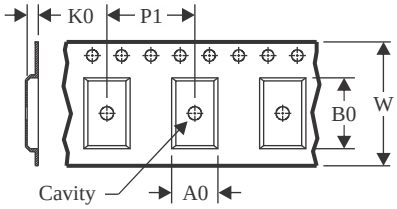
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

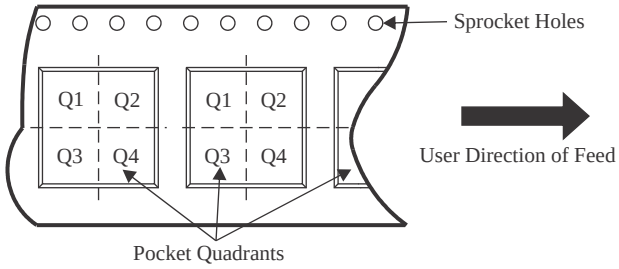


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

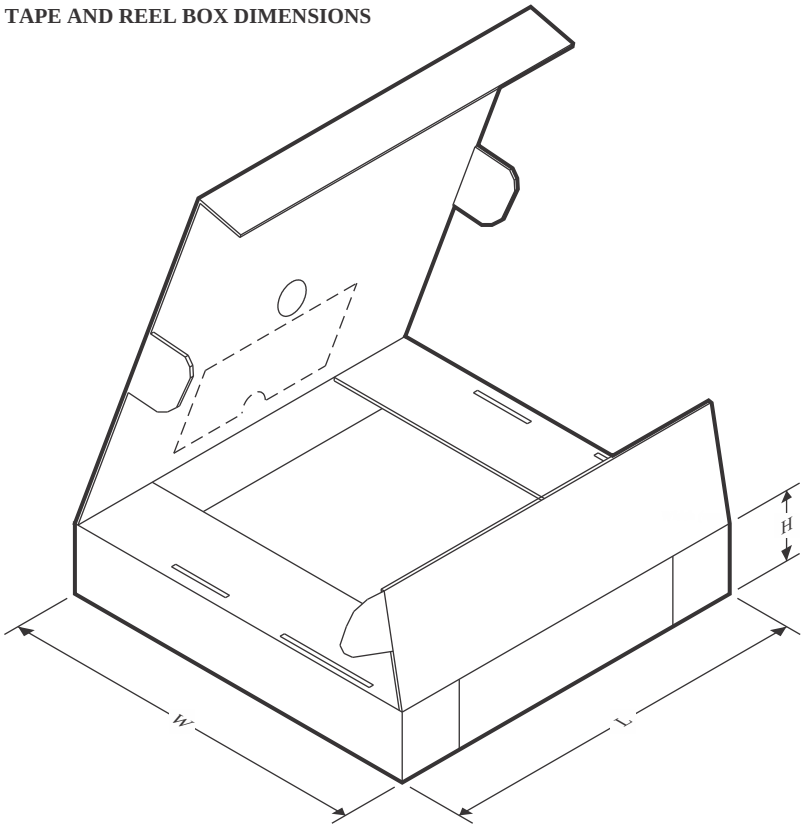


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL081HIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL081HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL081HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL082HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL084HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

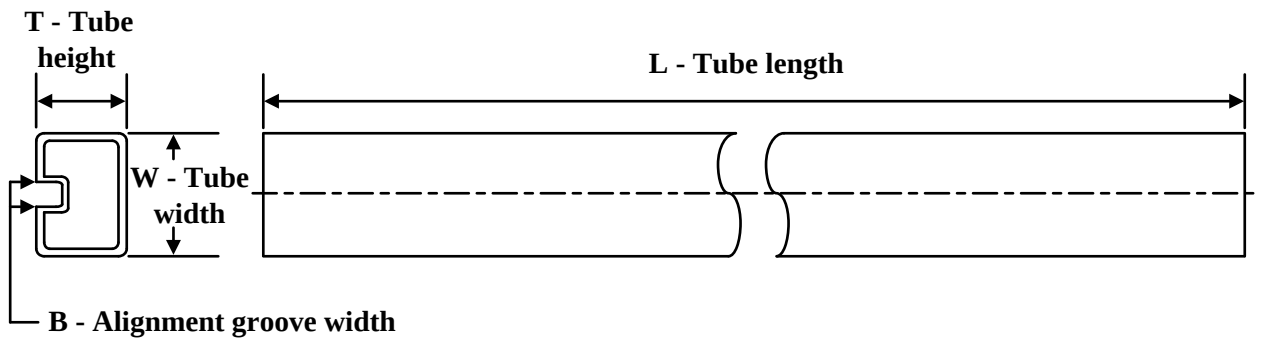


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL081BCDR	SOIC	D	8	2500	356.0	356.0	35.0
TL081BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL081HIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL081HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL081HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL081IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082ACPSR	SO	PS	8	2000	356.0	356.0	35.0
TL082BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082BCDR	SOIC	D	8	2500	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL082CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL082CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL082HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL082HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL082HIPWR	TSSOP	PW	8	3000	356.0	356.0	35.0
TL082IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL082IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL084ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084ACNSR	SO	NS	14	2000	356.0	356.0	35.0
TL084BCDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084CNSR	SO	NS	14	2000	356.0	356.0	35.0
TL084CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084HIDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL084HIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084IDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084IDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084QDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084QDRG4	SOIC	D	14	2500	350.0	350.0	43.0

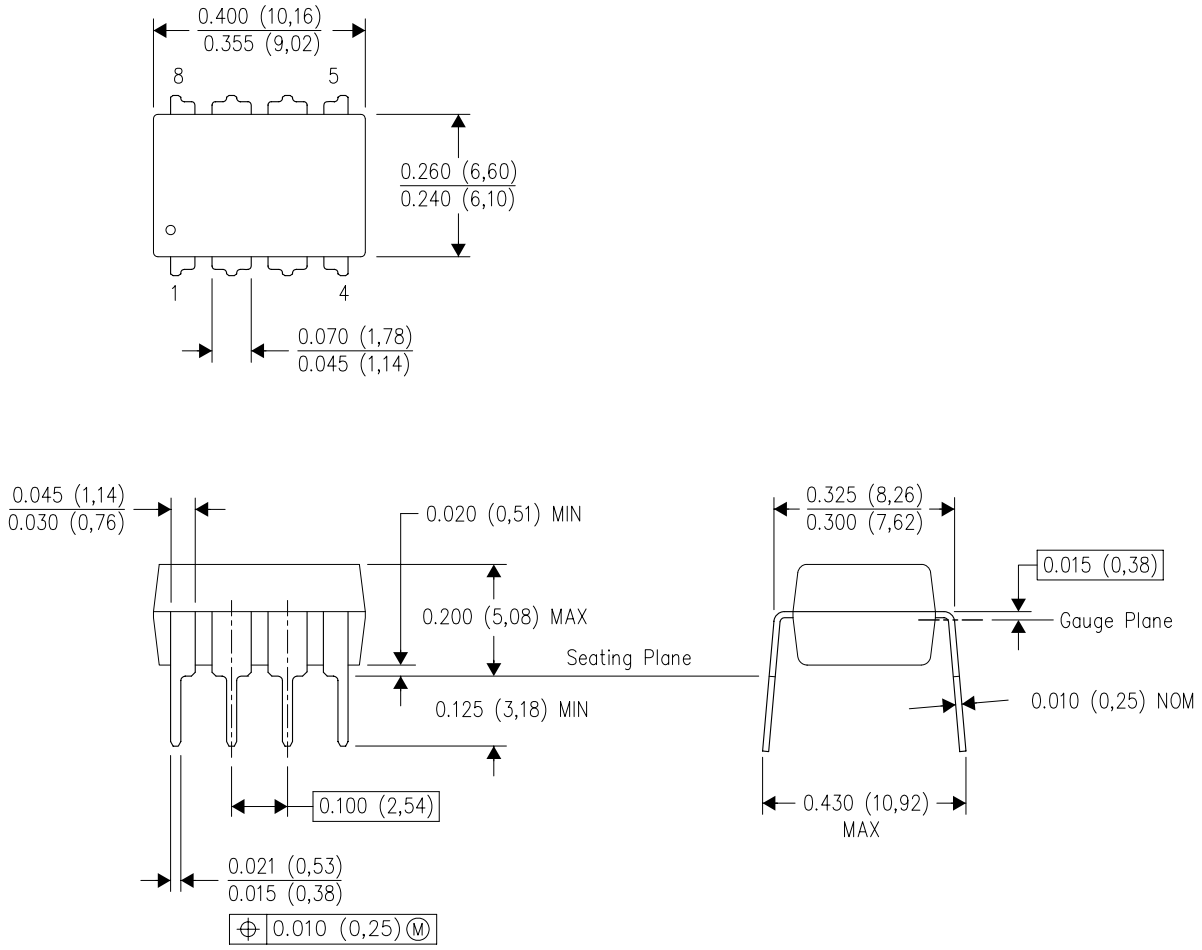
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9851501Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9851503Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL081ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL081BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL081CP	P	PDIP	8	50	506	13.97	11230	4.32
TL081IP	P	PDIP	8	50	506	13.97	11230	4.32
TL082ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL082BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL082CP	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP	P	PDIP	8	50	506	13.97	11230	4.32
TL082MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL084ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL084ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL084CN	N	PDIP	14	25	506	13.97	11230	4.32
TL084CN	N	PDIP	14	25	506	13.97	11230	4.32
TL084CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084IN	N	PDIP	14	25	506	13.97	11230	4.32
TL084IN	N	PDIP	14	25	506	13.97	11230	4.32
TL084IN	N	PDIP	14	25	506	13.97	11230	4.32
TL084INE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084INE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084INE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084MFK	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

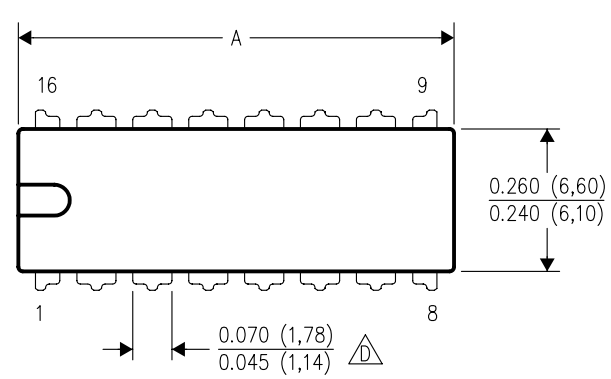


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

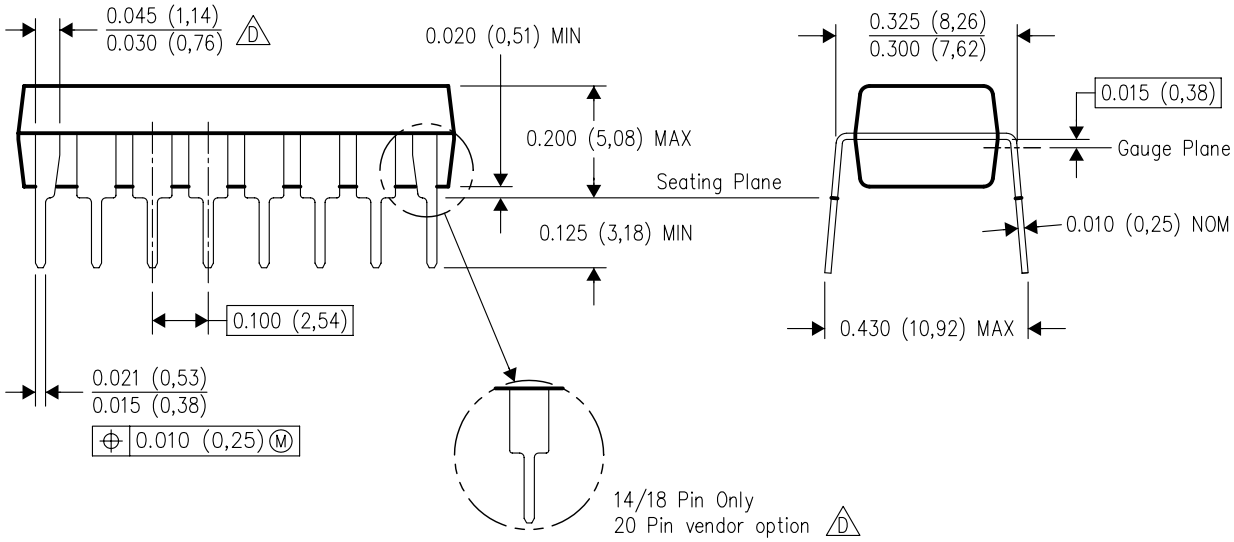
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

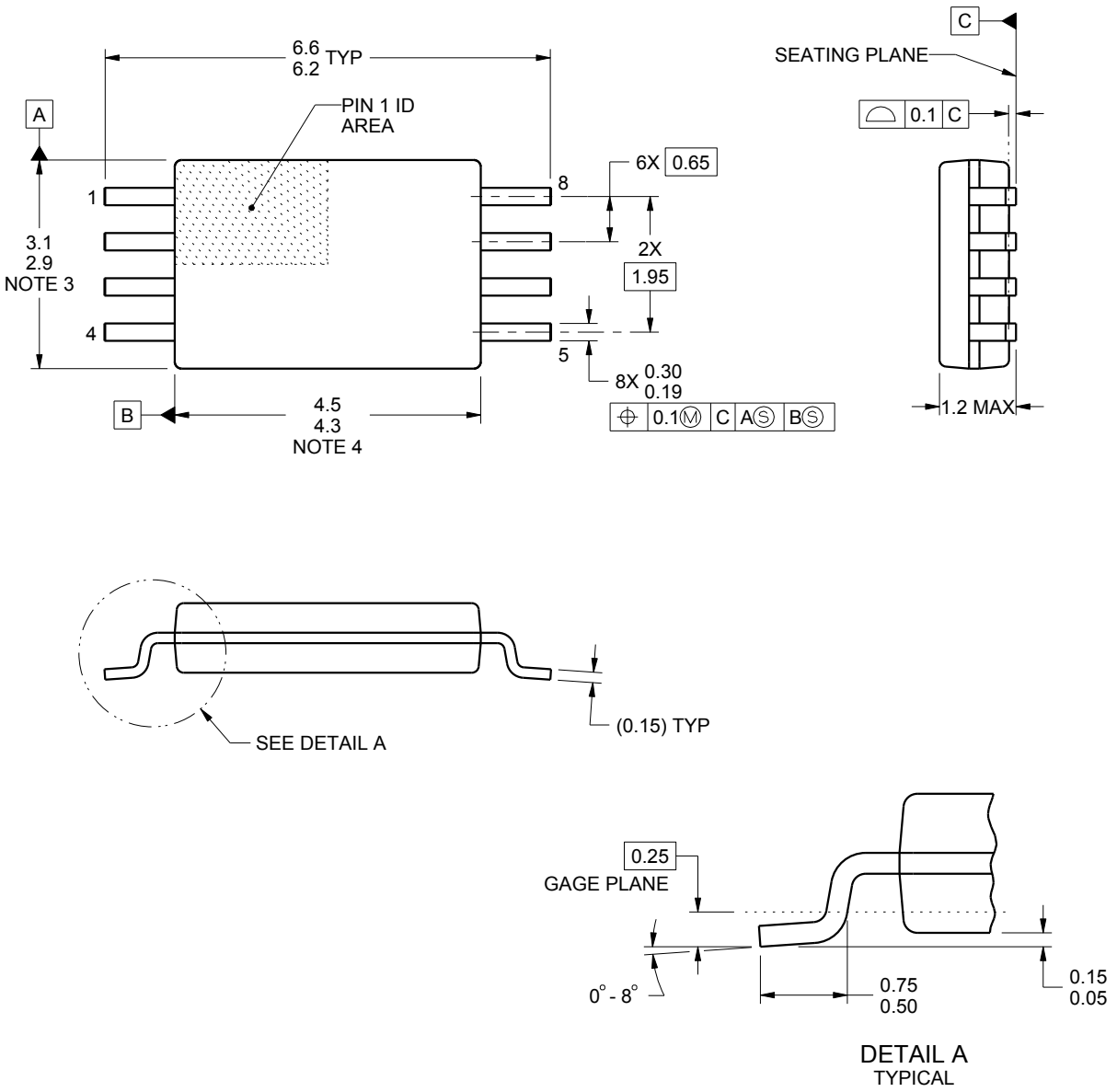
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0008A

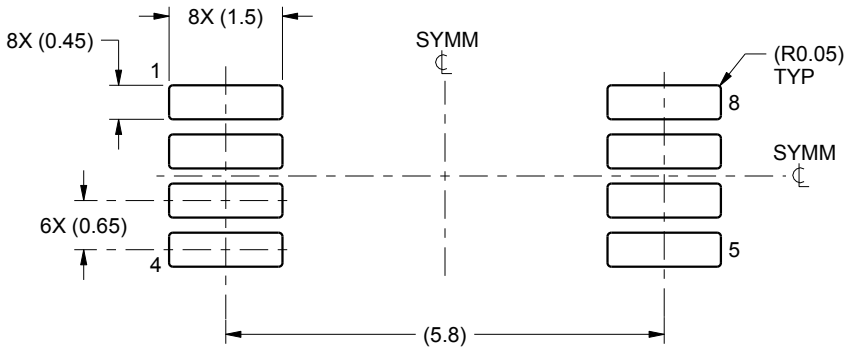
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

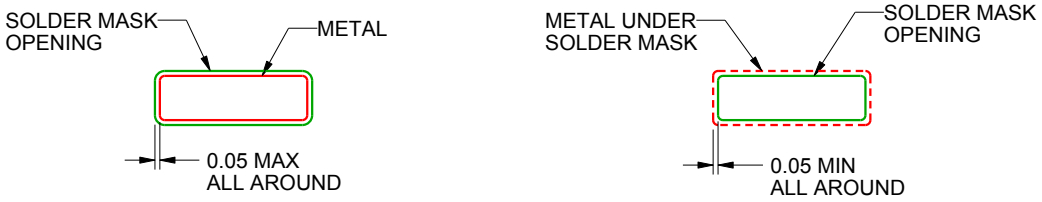


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

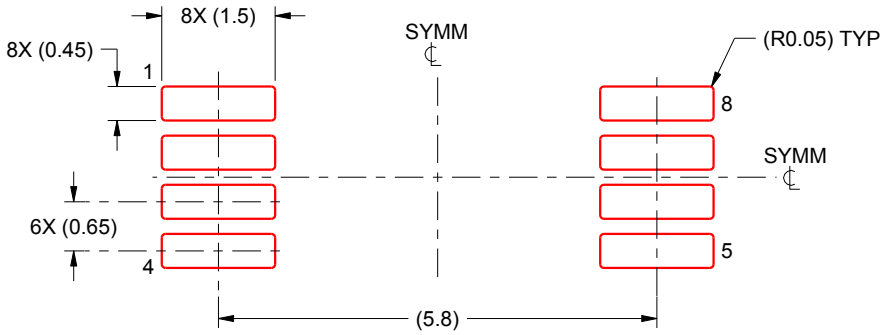


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

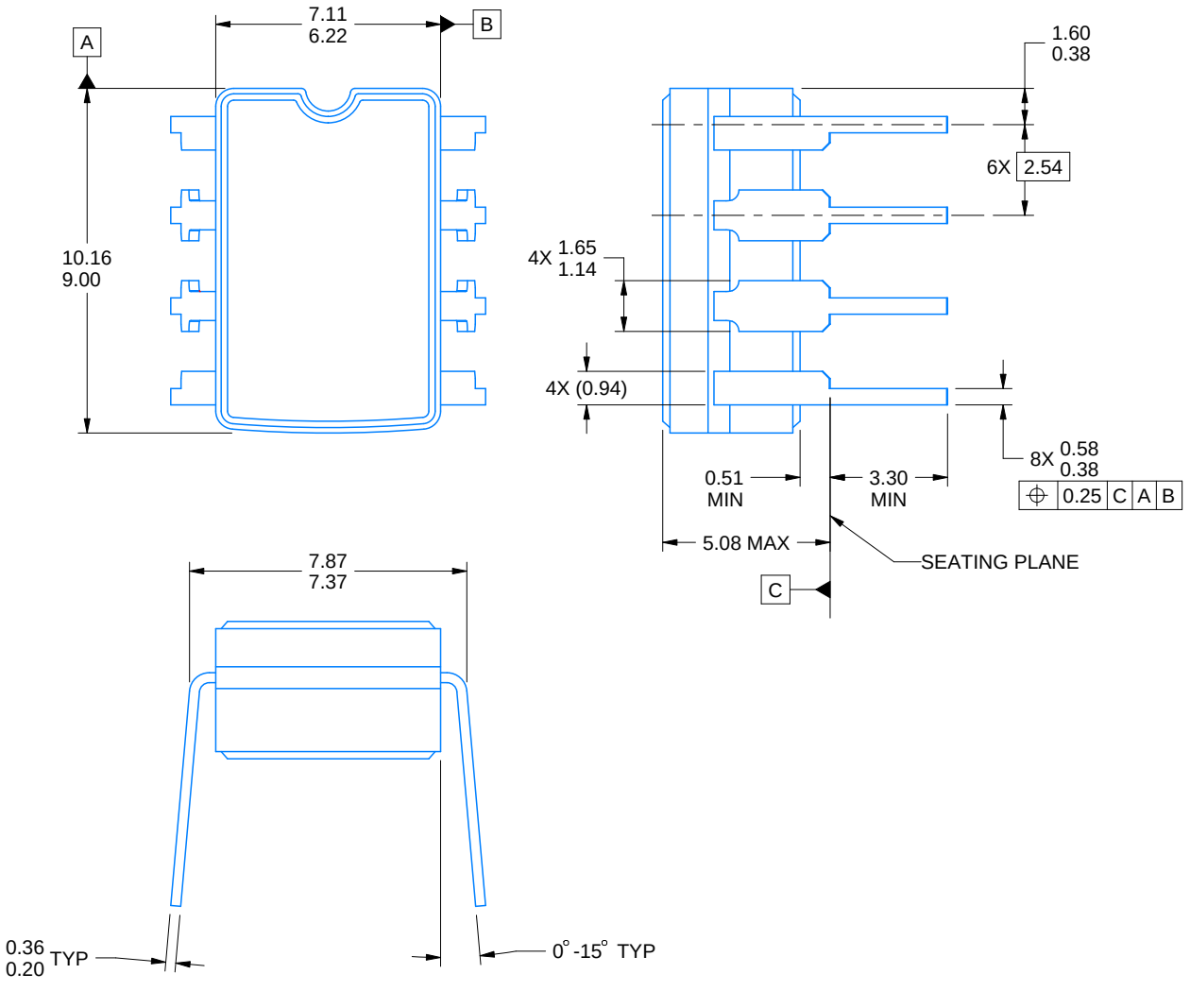
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

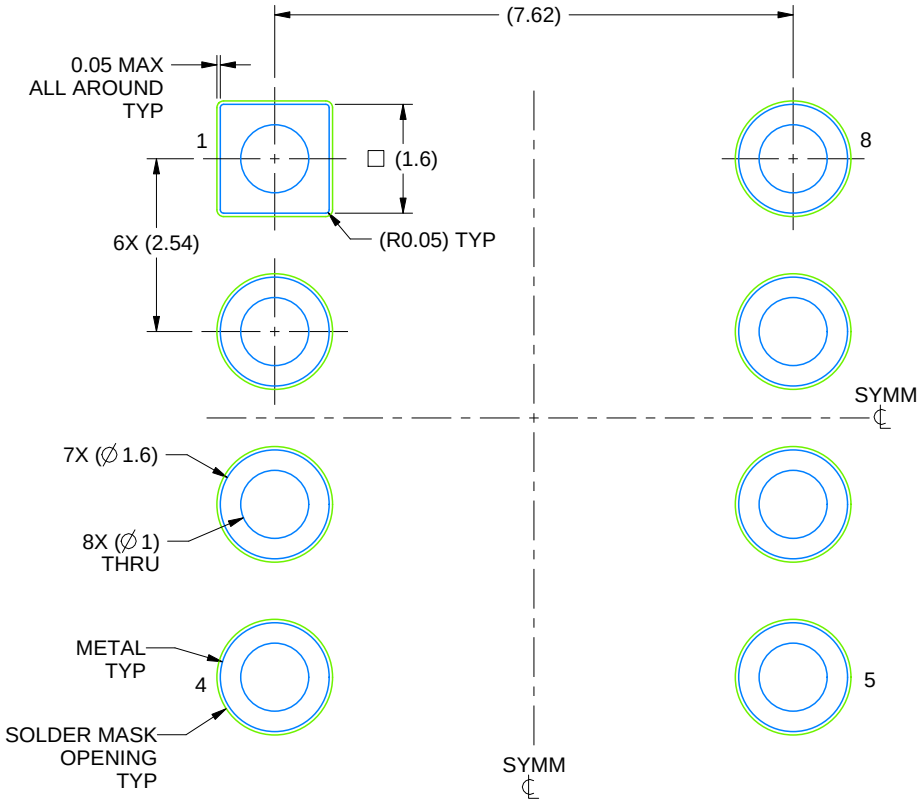
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

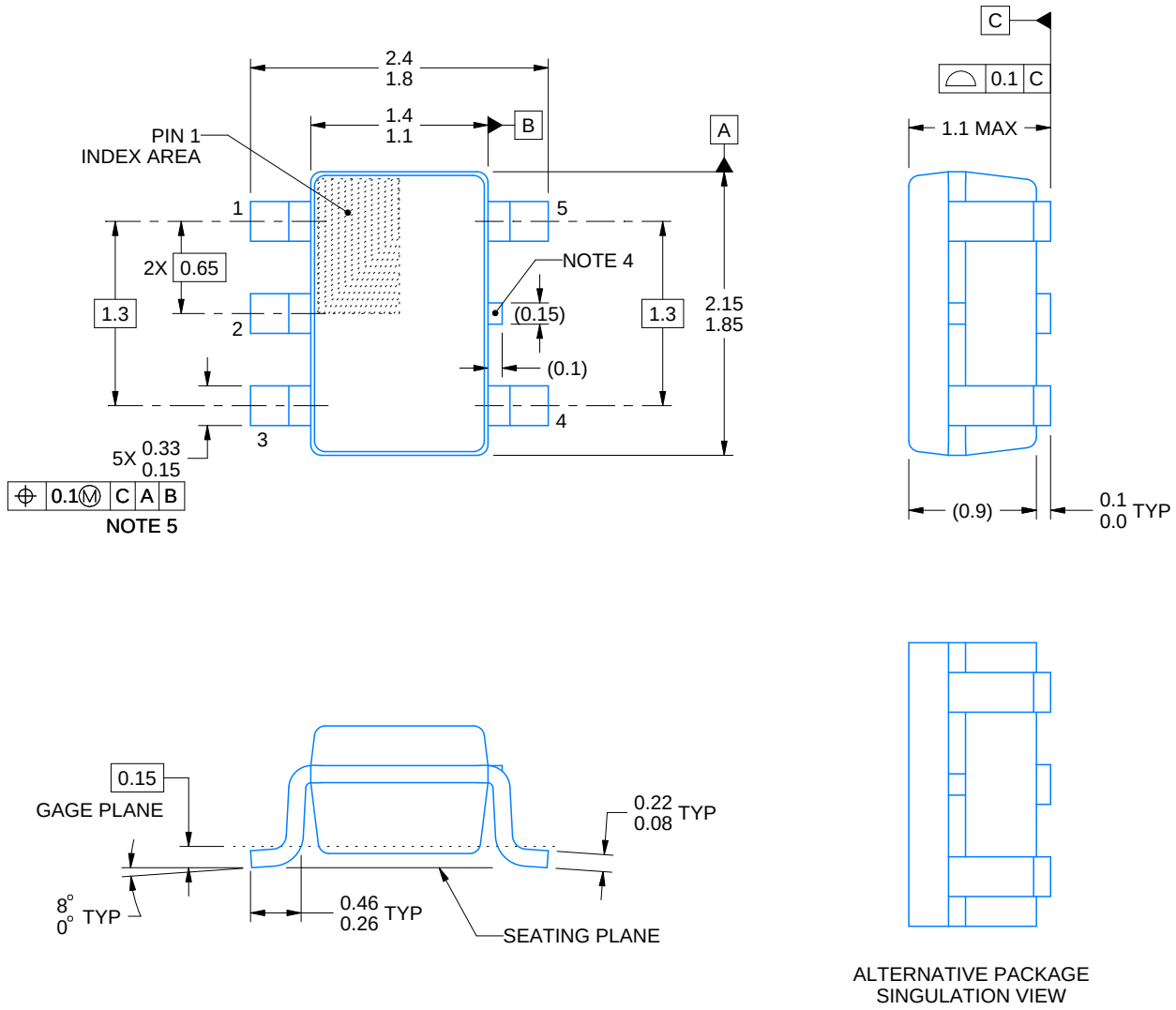
4230036/A 09/2023

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

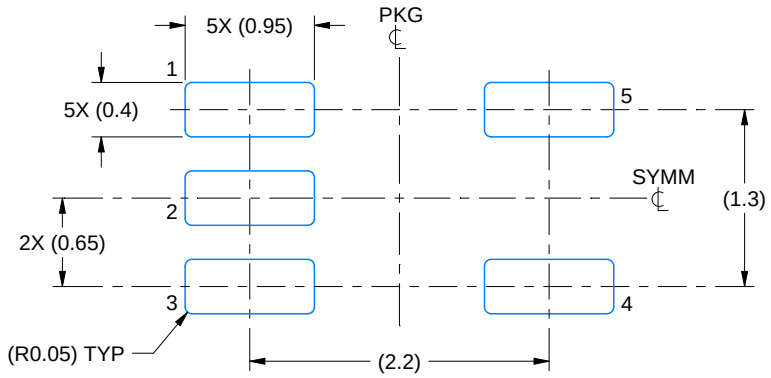
SMALL OUTLINE TRANSISTOR



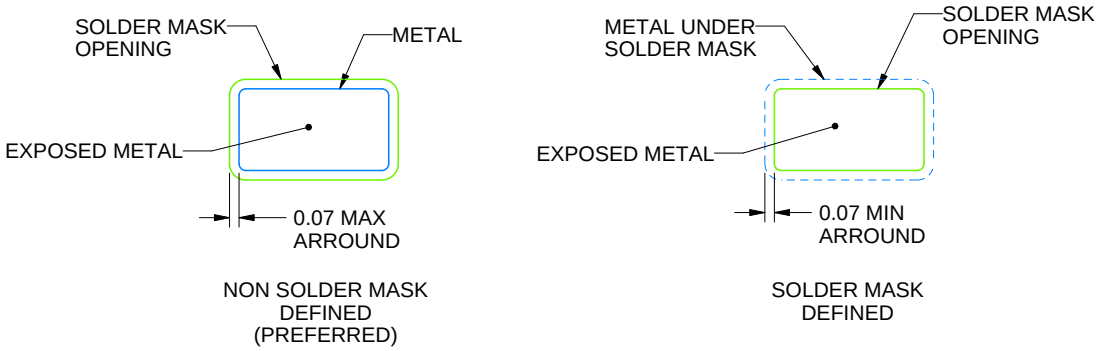
4214834/E 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

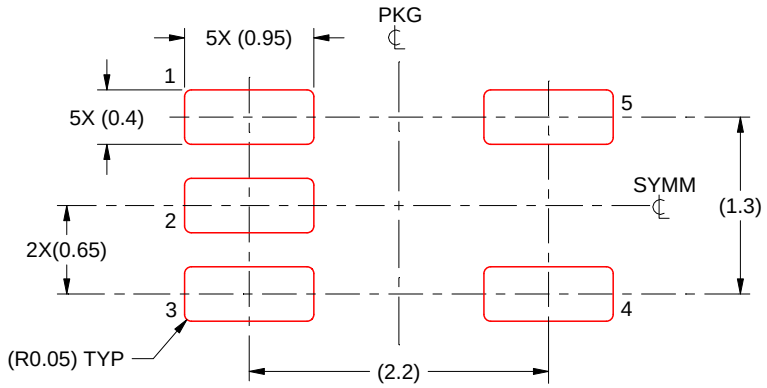


SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/E 06/2024

NOTES: (continued)

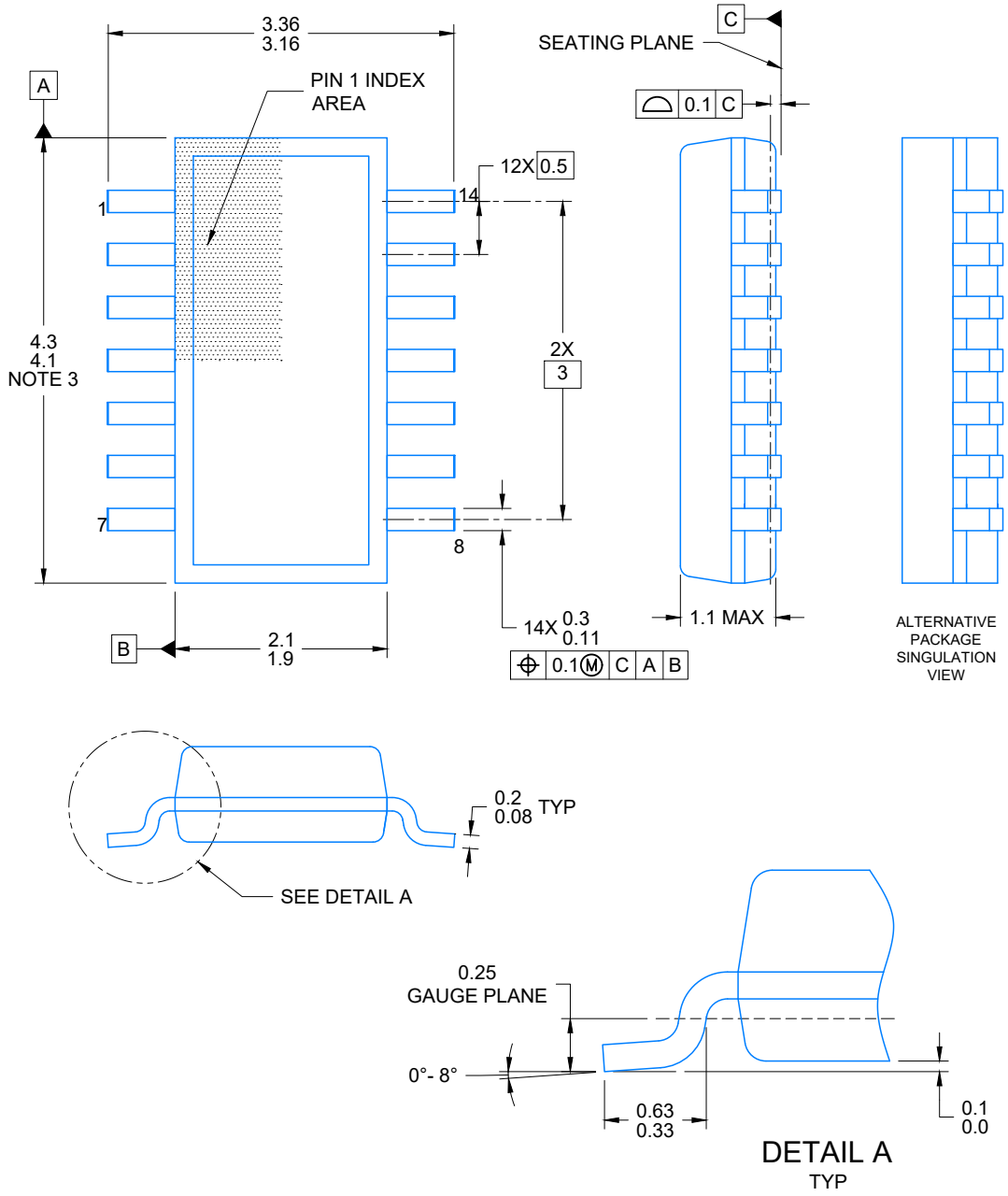
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

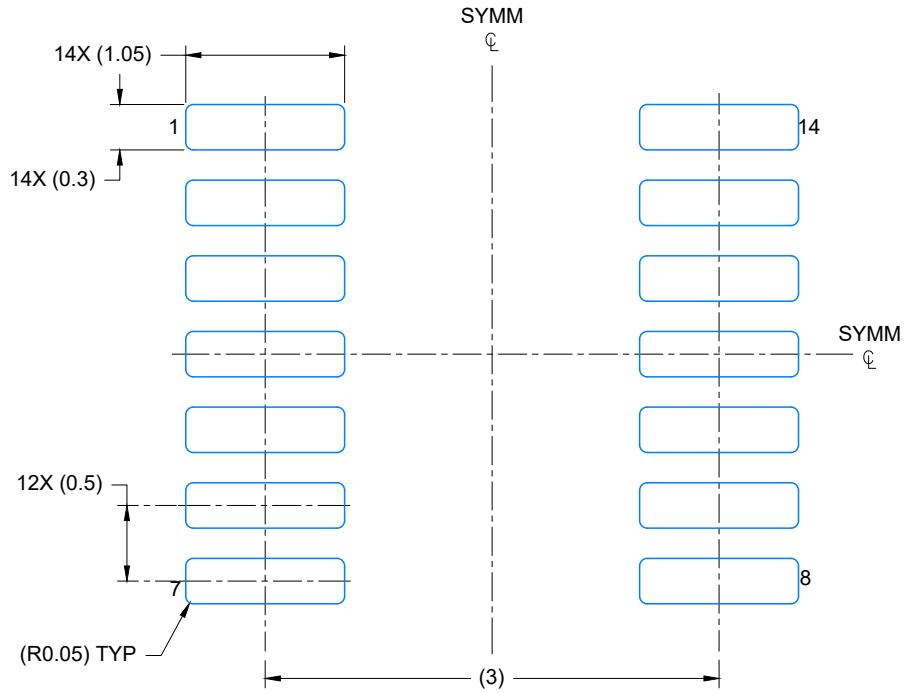
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

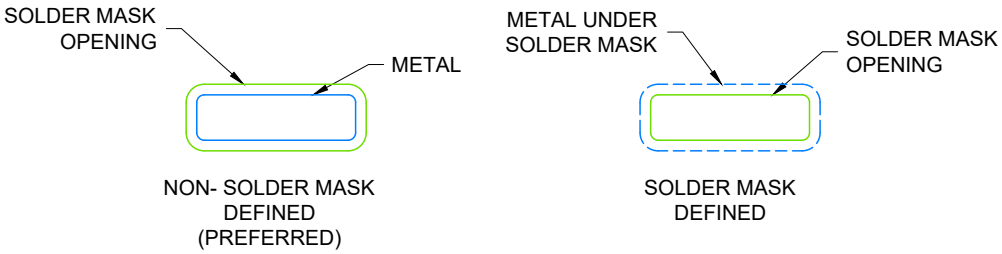


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

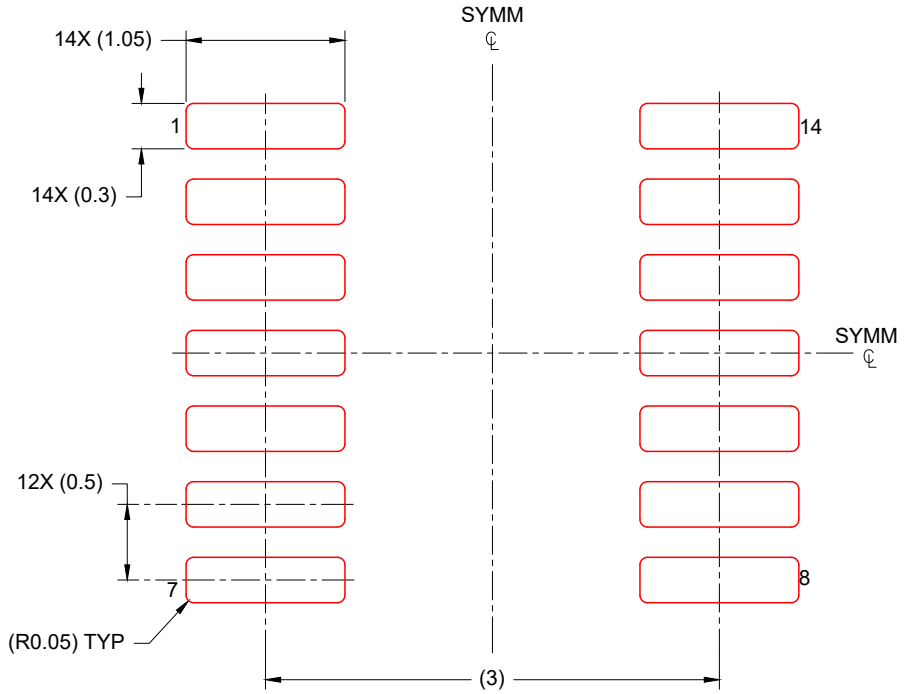


SOLDER MASK DETAILS

4224643/C 04/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/C 04/2024

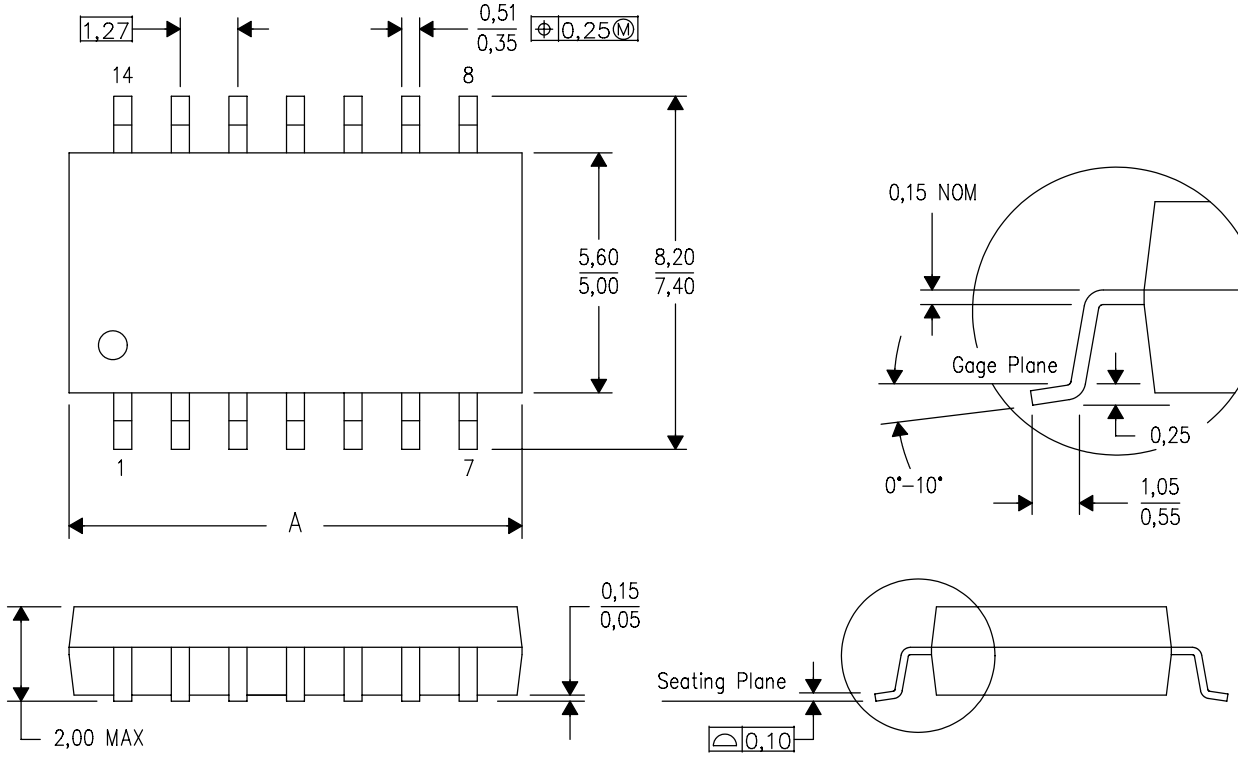
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

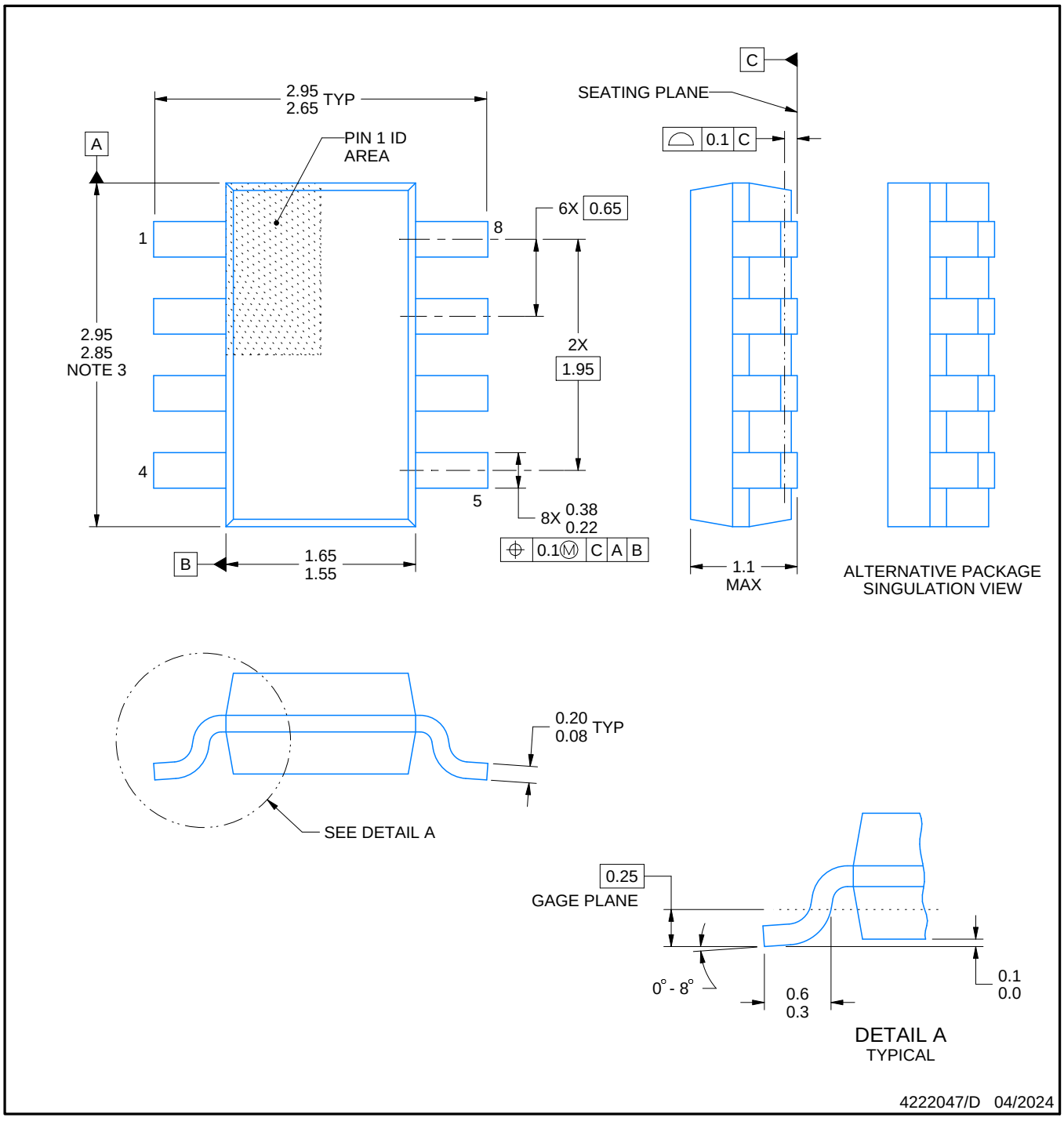
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

DDF0008A

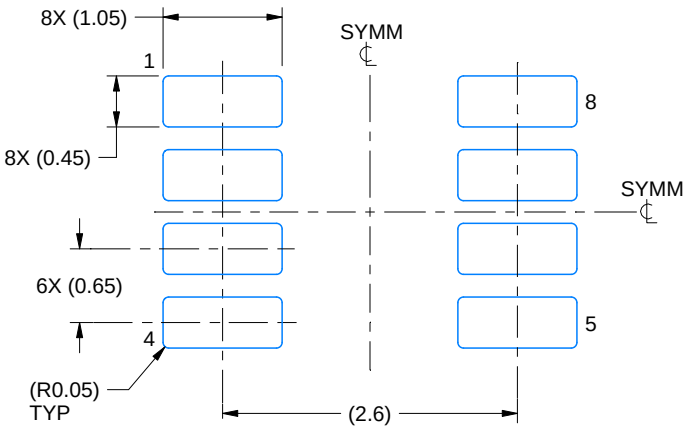
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

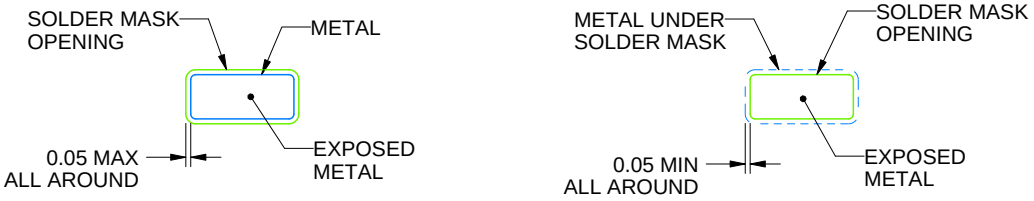


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

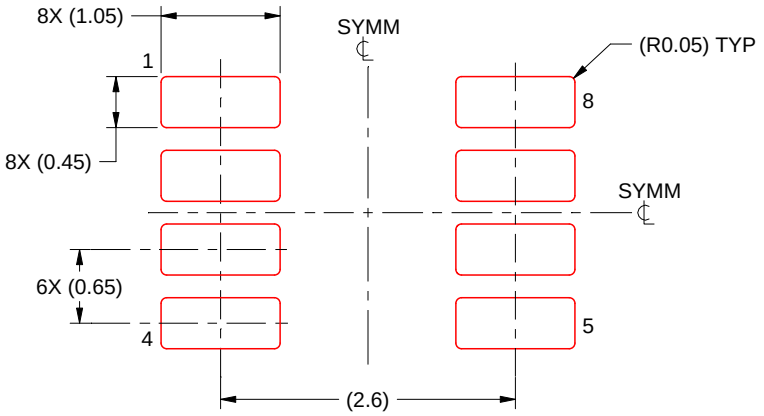


SOLDER MASK DETAILS

4222047/D 04/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/D 04/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

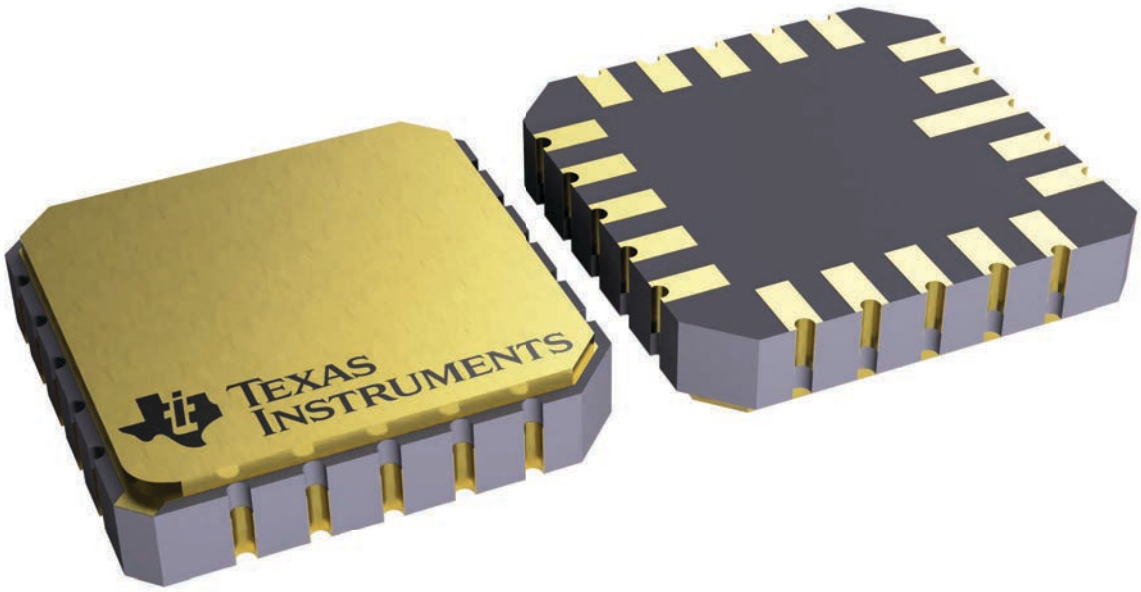
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

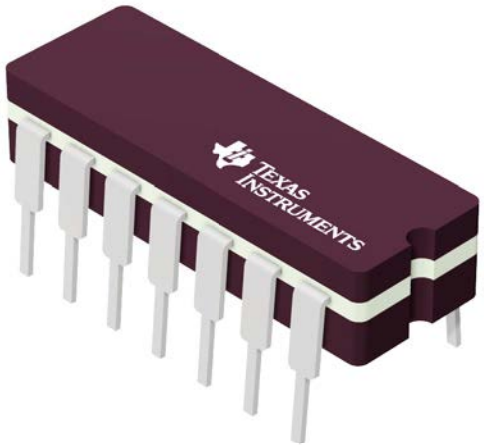


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

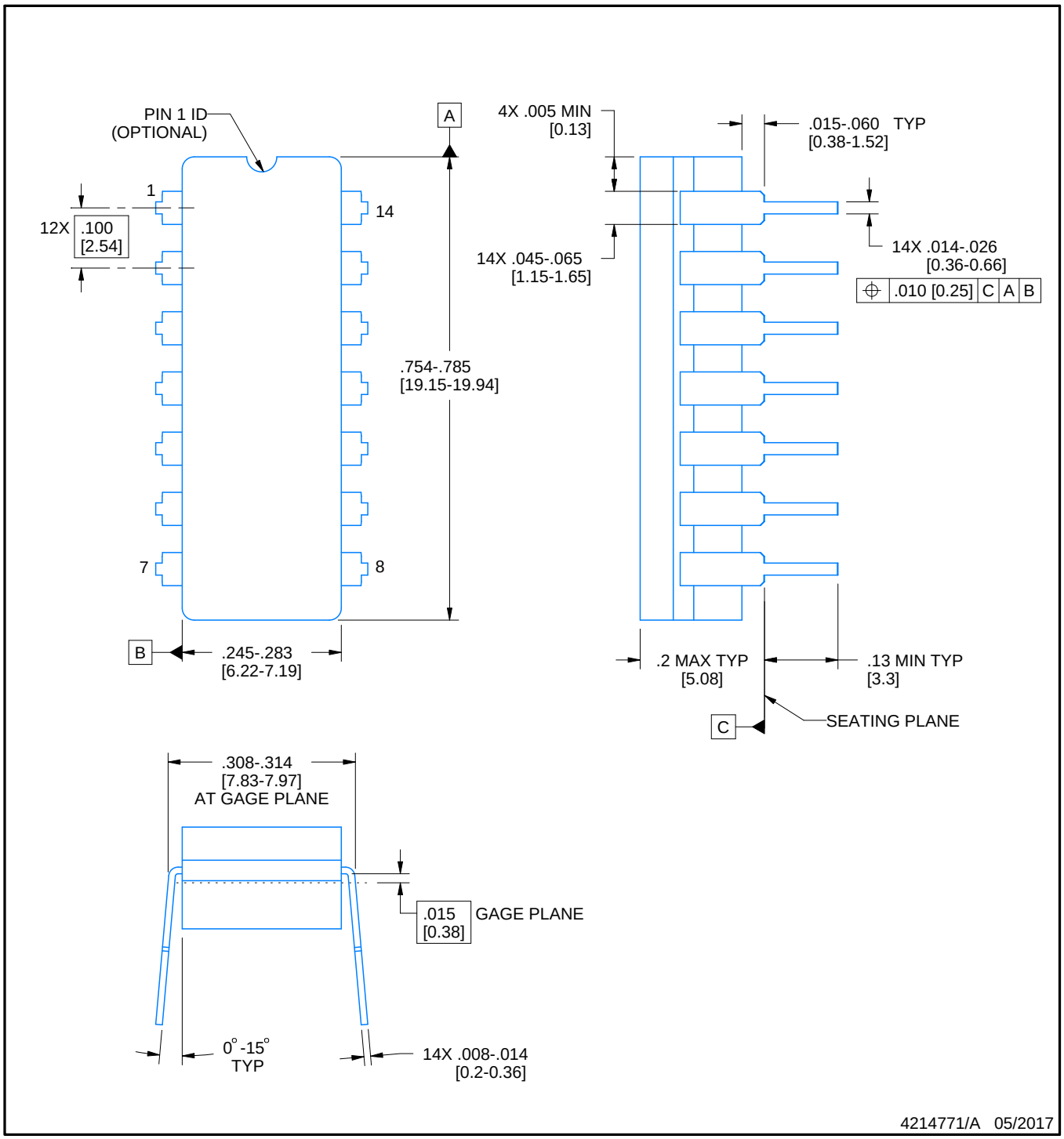
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

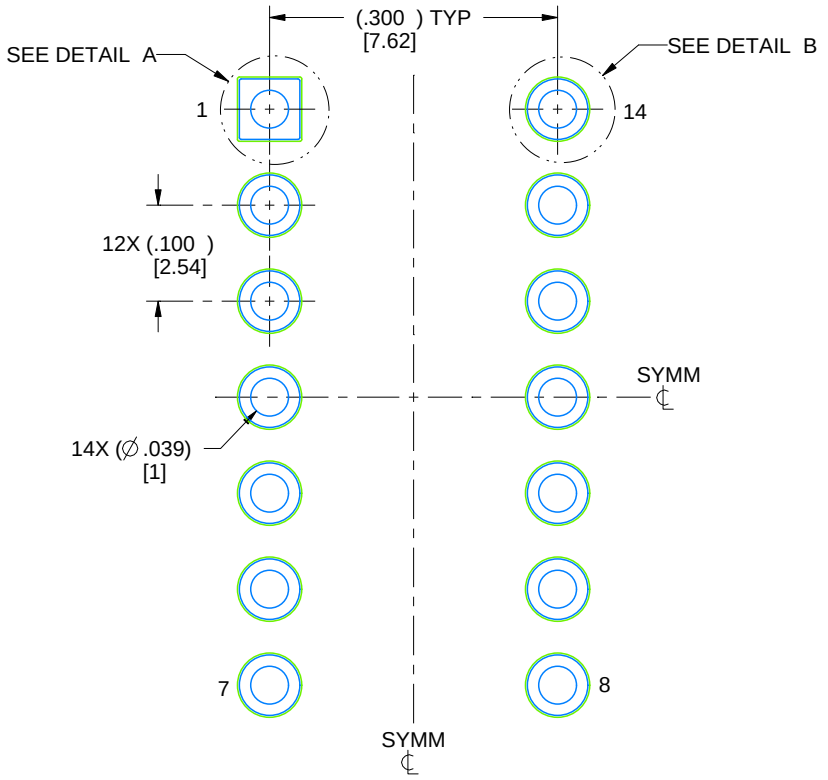
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

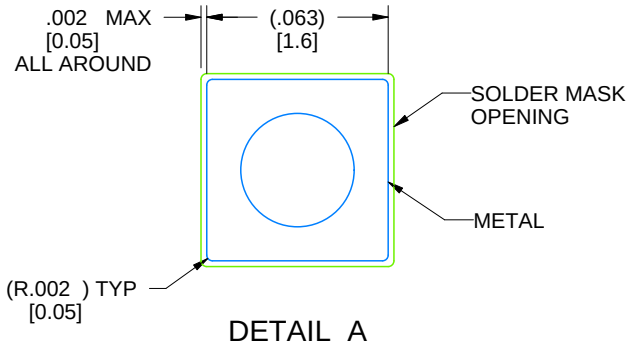
J0014A

CDIP - 5.08 mm max height

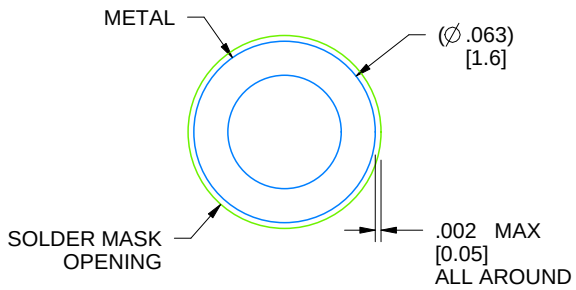
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

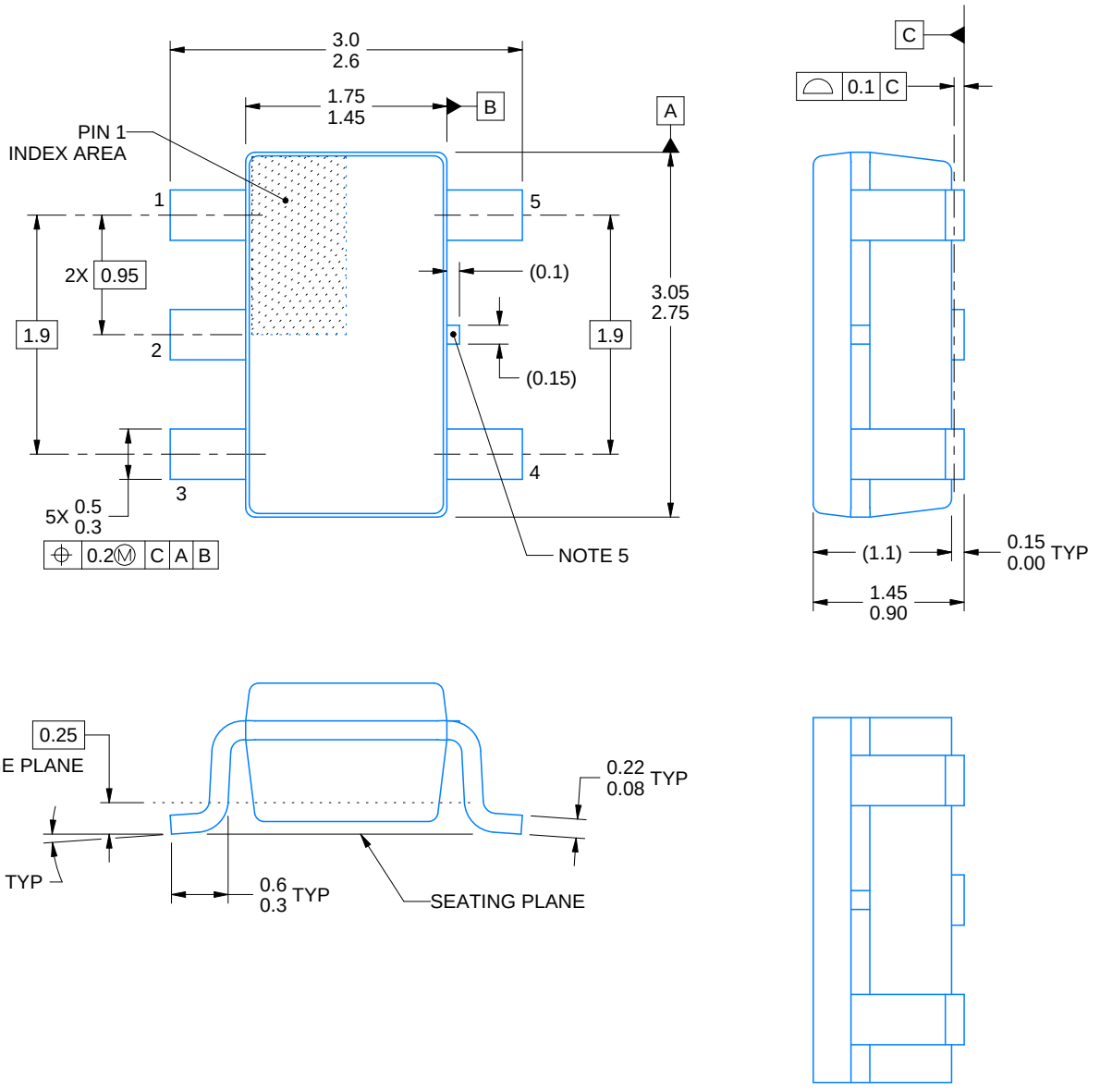
4214771/A 05/2017

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

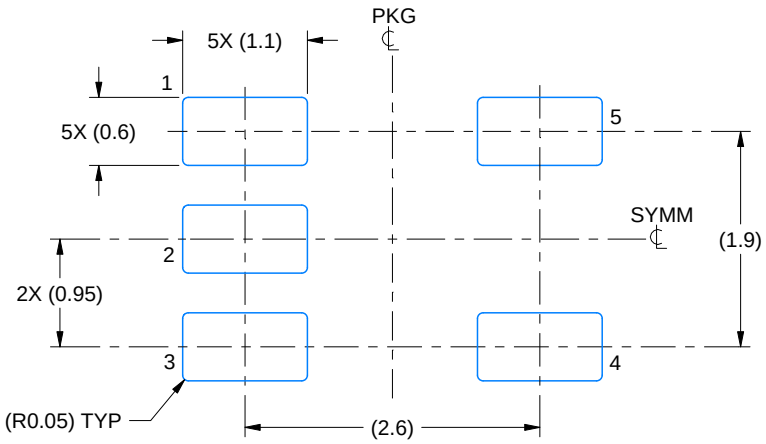


ALTERNATIVE PACKAGE SINGULATION VIEW

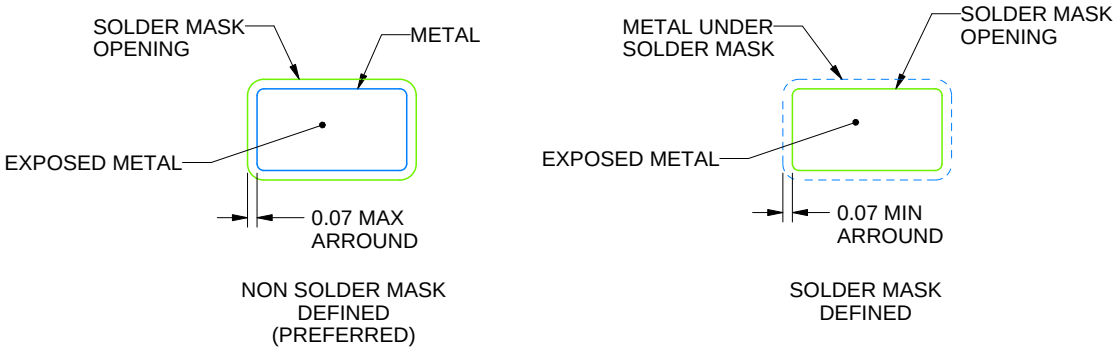
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

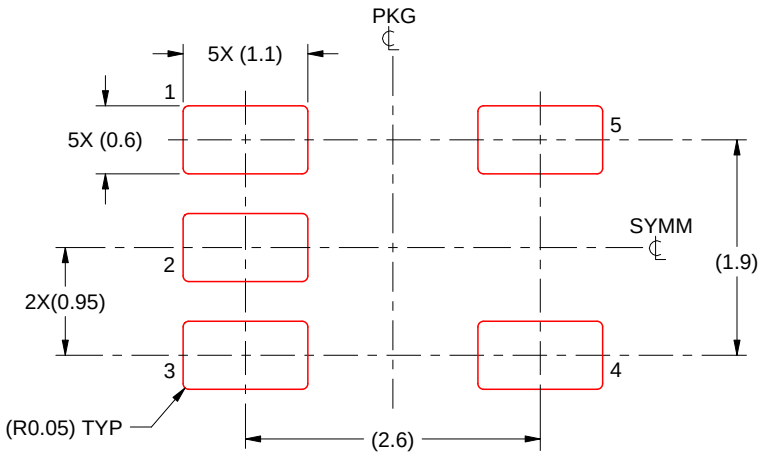


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



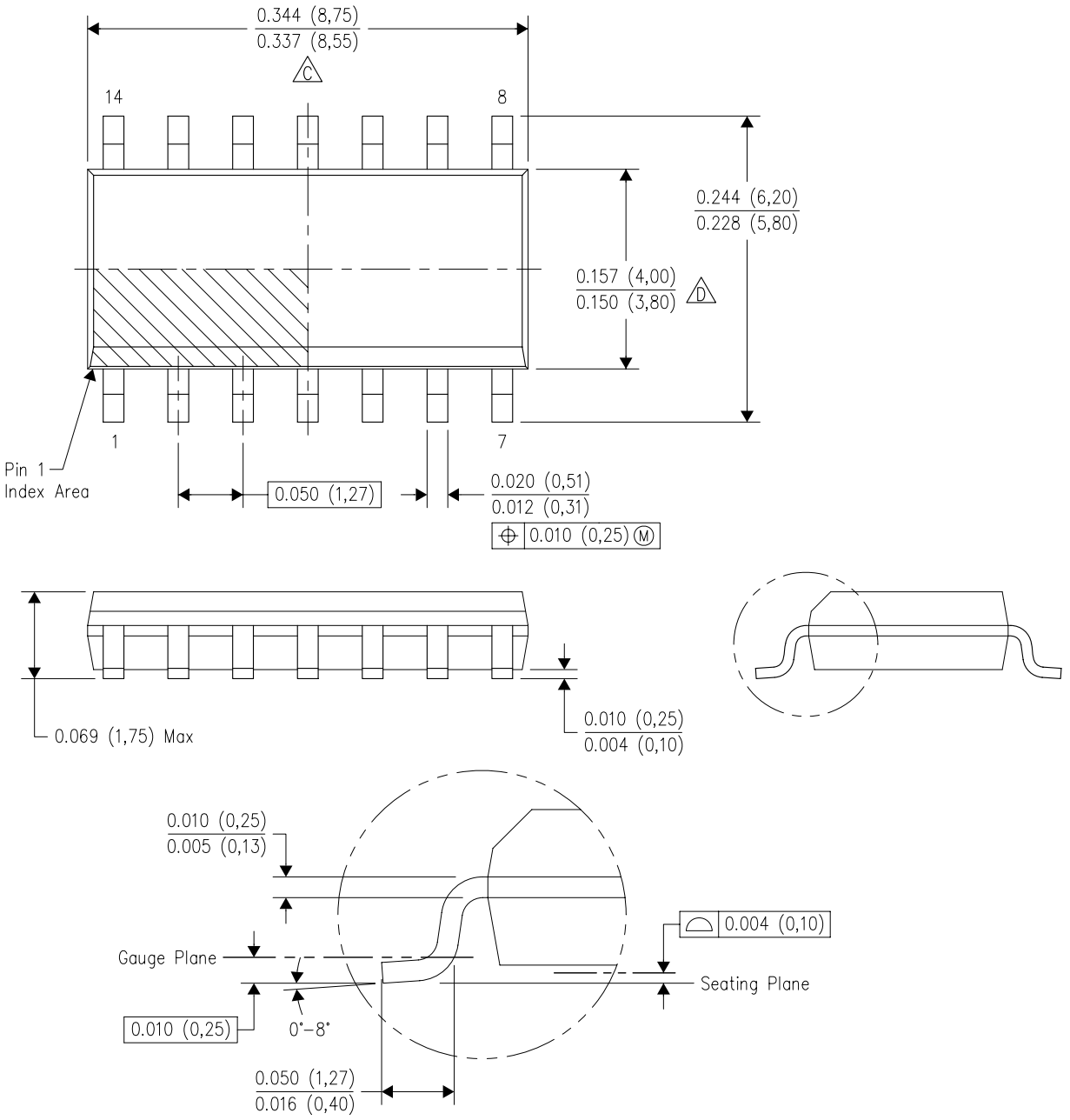
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

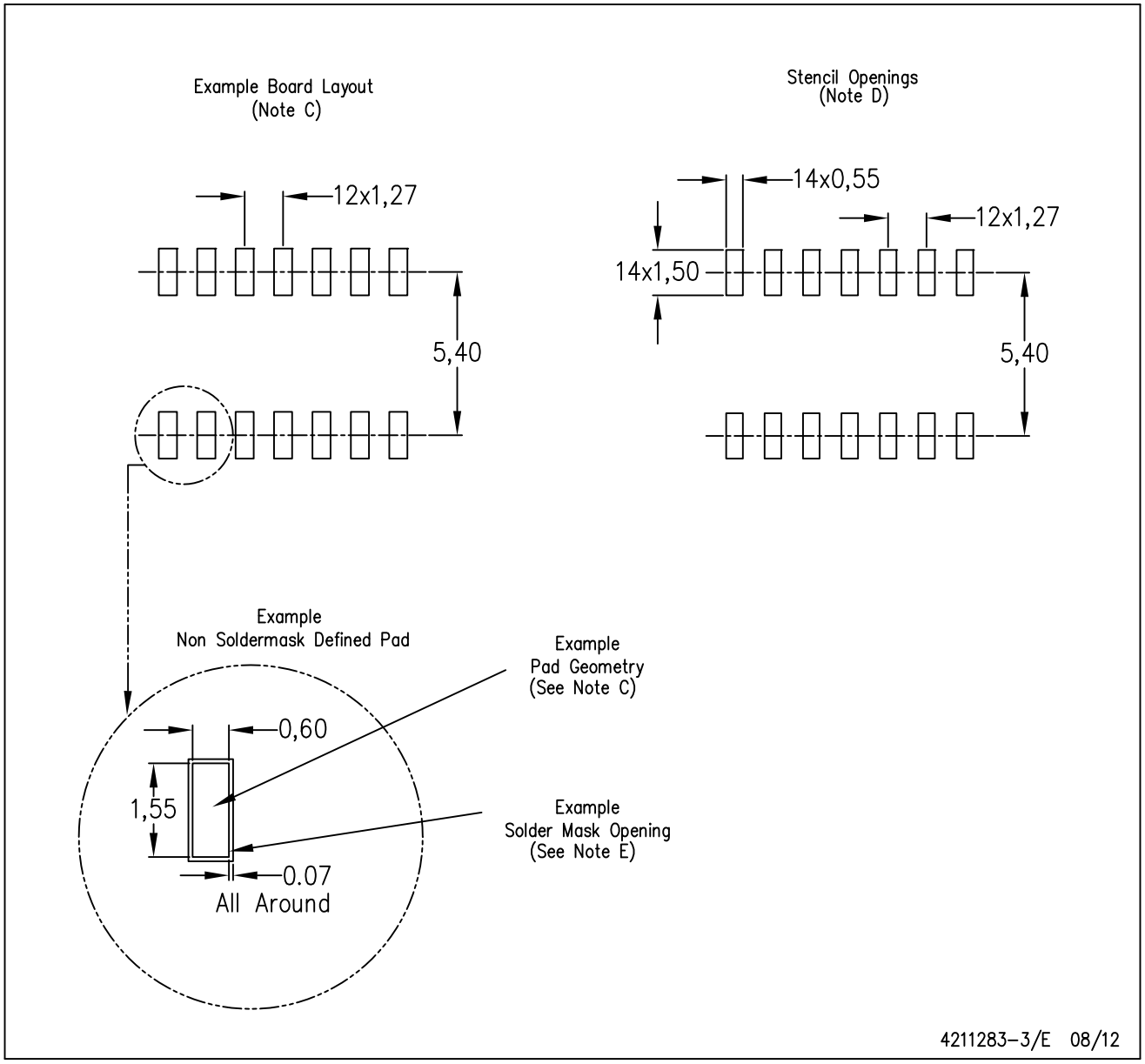
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

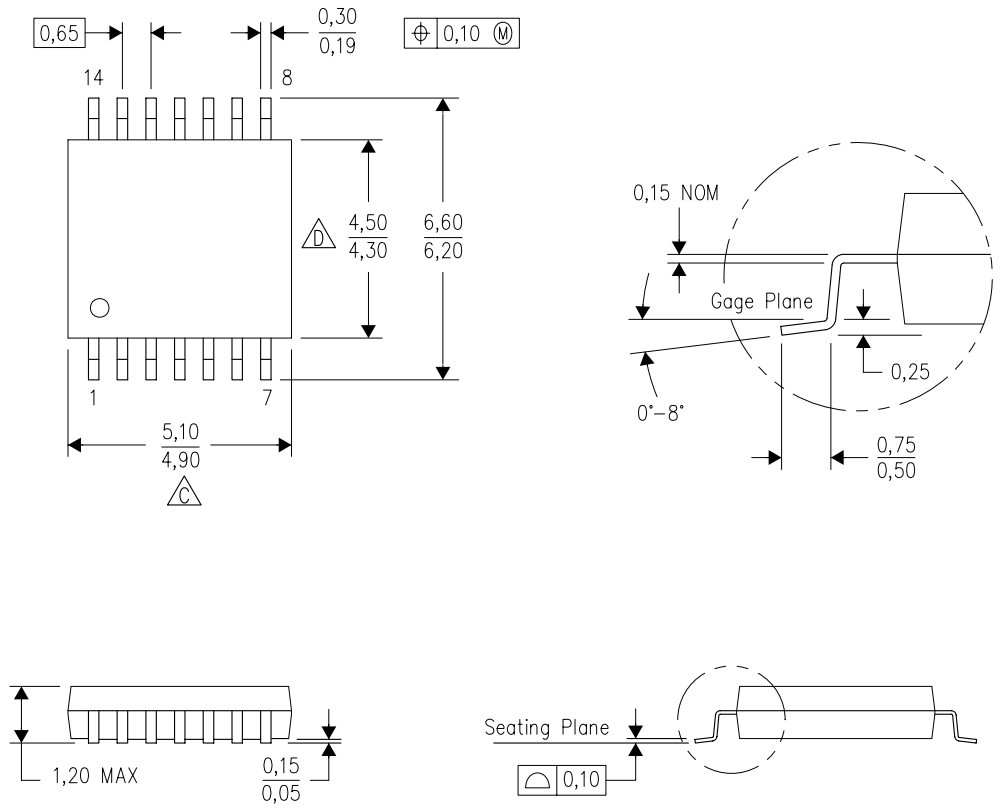
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



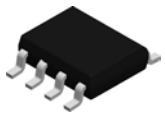
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

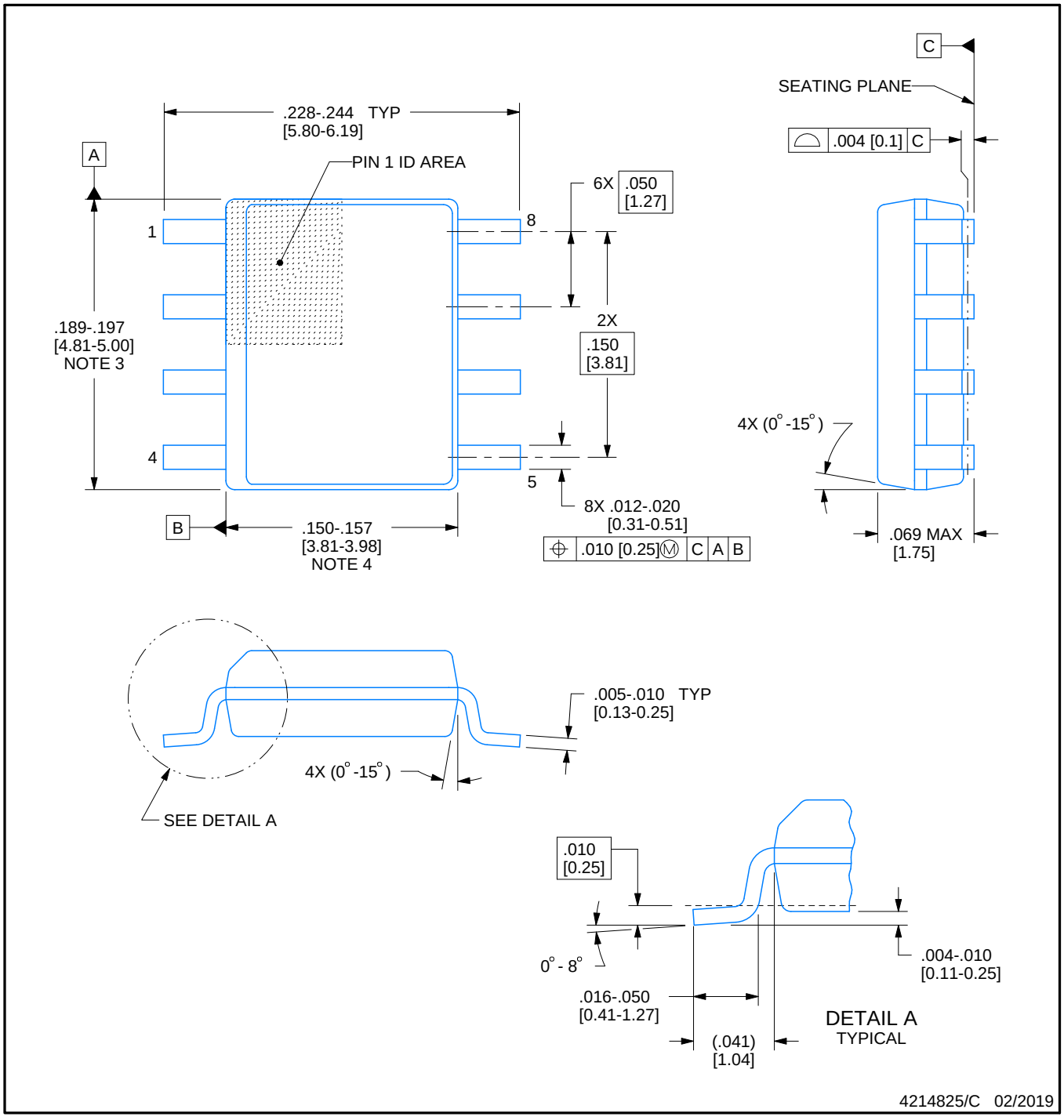


PACKAGE OUTLINE

D0008A

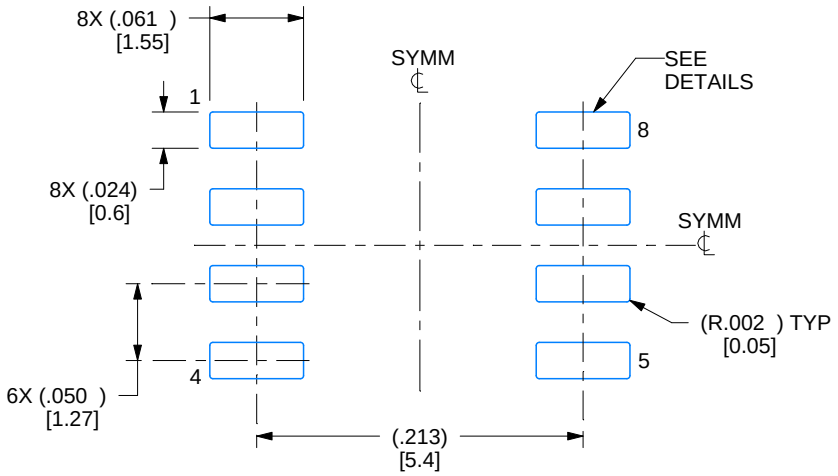
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

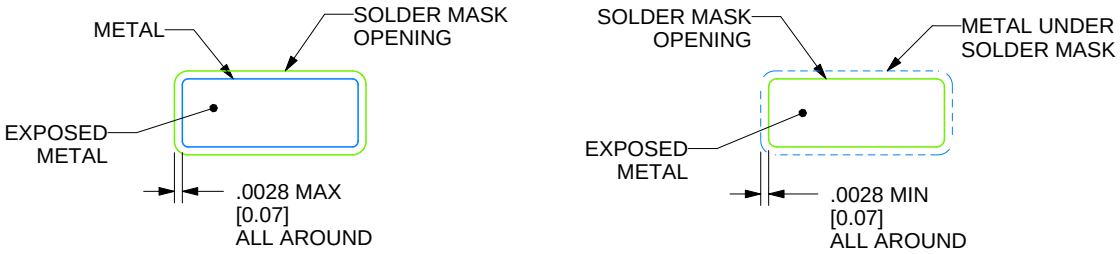


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

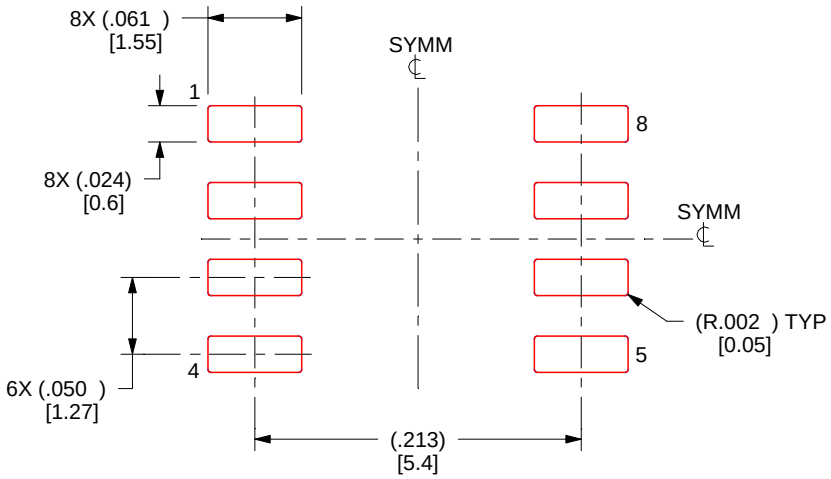
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

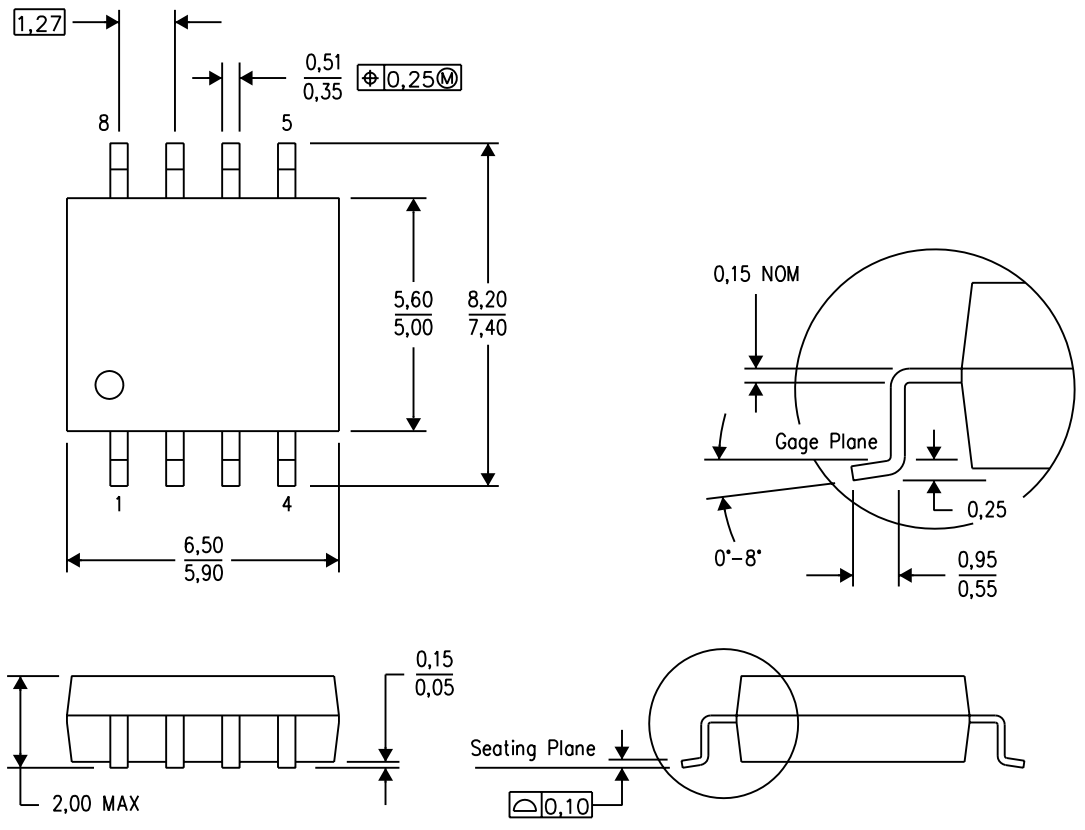
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

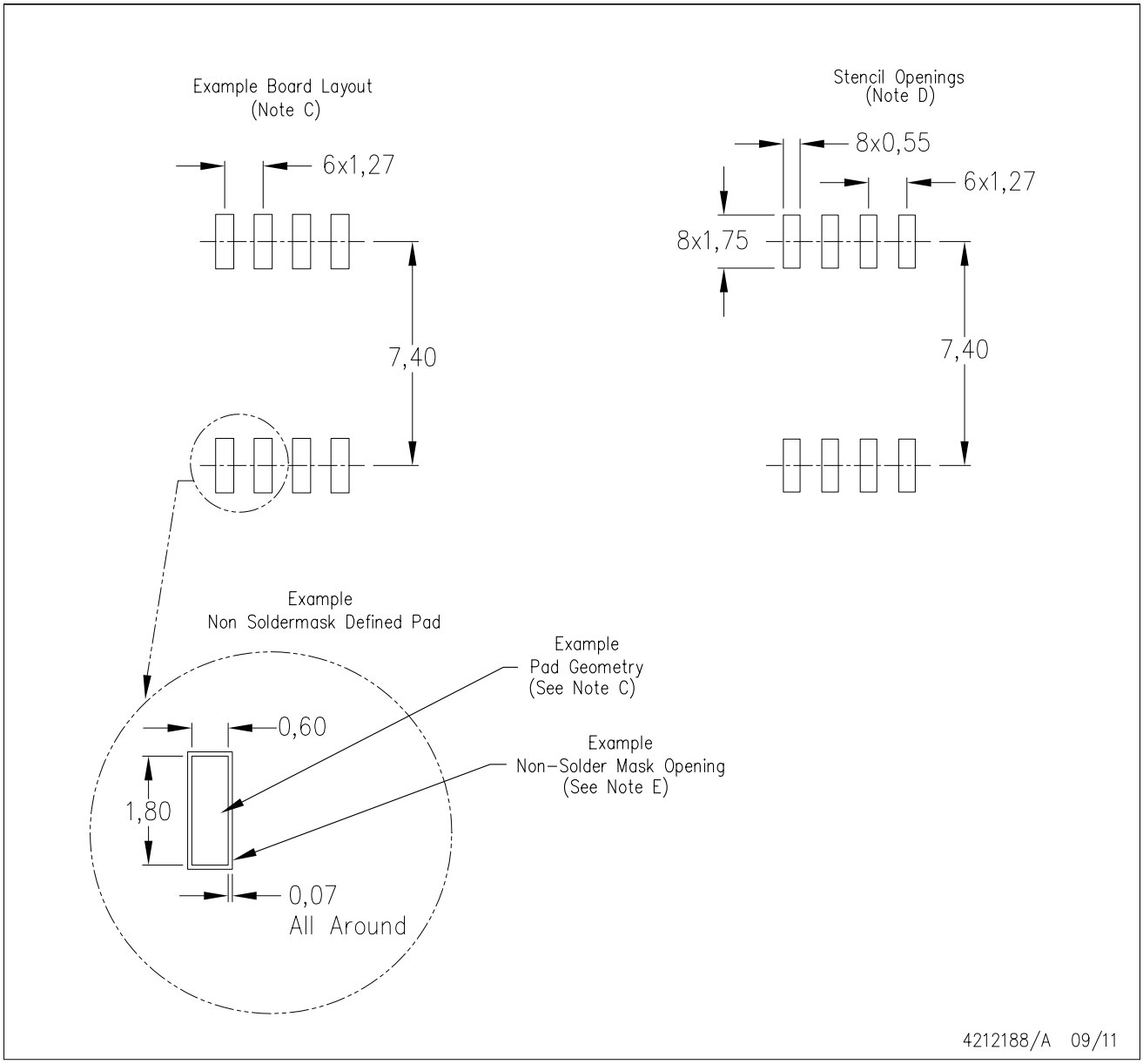
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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