具有使能功能的 TPS709 150mA、30V、1μA I_Q 稳压器

1 特性

- 超低 I_Q：1 μA
- 反向电流保护
- 低 $I_{关断}$：150nA
- 输入电压范围：2.7 V 至 30 V
- 支持 200mA 峰值输出
- 在工作温度范围内的精度为 2%
- 可提供固定输出电压：
  1.2 V 至 6.5 V
- 热关断保护和过流保护
- 封装：SOT-23-5、WSON-6

2 应用

- 烟雾和热量探测器
- 恒温器
- 运动检测器（PIR、uWave 等）
- 无线电动工具
- 电器电池组
- 电表
- 水表

3 说明

TPS709 系列线性稳压器是设计用于功耗敏感类应用的超低静态电流器件。一个精密带隙和误差放大器在温度范围内的精度为 2%。只有 1μA 的静态电流使得此器件成为由电池供电、要求非常小闲置状态功率耗散的常开系统的理想解决方案。为了增加安全性，这些器件还具有热关断、电流限制和反向电流保护功能。

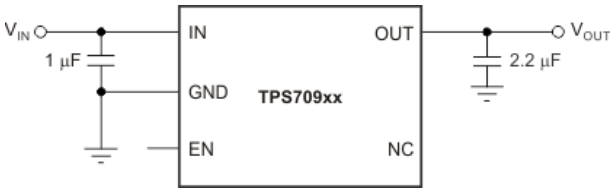
关断模式通过将 EN 引脚拉为低电平进行使能。该模式的关断电流低至 150nA（典型值）。

TPS709 系列采用 WSON-6 和 SOT-23-5 封装。

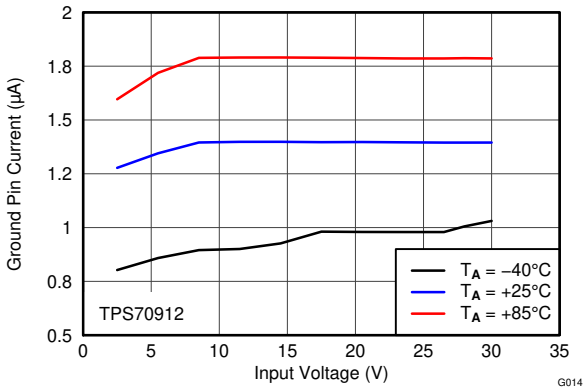
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS709	SOT-23 (5)	2.90mm × 1.60mm
	WSON (6)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。



典型应用电路



接地电流与 V_{IN} 和温度间的关系

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (November 2015) to Revision H (July 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 更改了*应用*部分 1
- Changed $V_{EN(HI)}$ row (changed parameter description and added test condition) in *Electrical Characteristics* table 5
- Added $V_{EN(LOW)}$ row to *Electrical Characteristics* table 5
- Added M3 suffix information to *Device Nomenclature* table 17

Changes from Revision F (December 2014) to Revision G (November 2015) — **Page**

- Added DBV package for TPS709A to *Pin Configurations and Functions* section 3
- Added DBV package for TPS709B to *Pin Configurations and Functions* section 3
- Added TPS709A and TPS709B to Pin Functions table 3
- Moved operating junction temperature from *Electrical Characteristics* to *Recommended Operating Conditions* 4

5 Pin Configuration and Functions

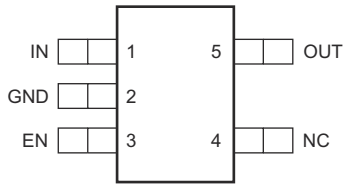


图 5-1. TPS709: DBV Package, 5-Pin SOT-23, Top View

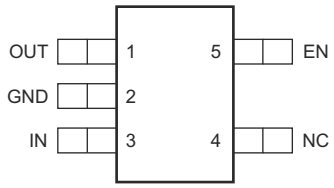


图 5-2. TPS709A: DBV Package, 5-Pin SOT-23, Top View

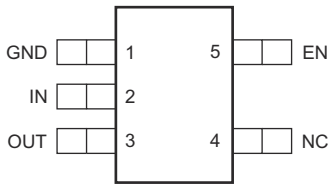


图 5-3. TPS709B: DBV Package, 5-Pin SOT-23, Top View

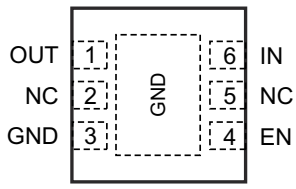


图 5-4. DRV Package, 6-Pin WSON, Top View

表 5-1. Pin Functions

PIN					I/O	DESCRIPTION
	DRV	DBV				
NAME	TPS709	TPS709	TPS709A	TPS709B		
EN	4	3	5	5	I	Enable pin. Drive this pin high to enable the device. Drive this pin low to put the device into low current shutdown. This pin can be left floating to enable the device. The maximum voltage must remain below 6.5 V.
GND	3	2	2	1	—	Ground
IN	6	1	3	2	I	Unregulated input to the device
NC	2, 5	4	4	4	—	No internal connection
OUT	1	5	1	3	O	Regulated output voltage. Connect a small 2.2-µF or greater ceramic capacitor from this pin to ground to assure stability.
Thermal pad		—	—	—	—	The thermal pad is electrically connected to the GND node. Connect this pad to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

specified at T_J = –40°C to 125°C (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	32	V
	V_{EN}	–0.3	7	
	V_{OUT}	–0.3	7	
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		30	V
V_{OUT}	Output voltage	1.2		6.5	V
V_{EN}	Enable voltage	0		6.5	V
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS709		UNIT
		DBV	DRV	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	212.1	73.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.5	97.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.5	42.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.86	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.7	42.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at ambient temperature (T_A) = –40°C to +85°C, V_{IN} = $V_{OUT(typ)}$ + 1 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = 2 V, and C_{IN} = C_{OUT} = 2.2-μF ceramic (unless otherwise noted); typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.7		30	V
V_{OUT}	Output voltage range		1.2		6.5	V
V_{OUT}	DC output accuracy	V_{OUT} < 3.3 V	–2%		2%	
		V_{OUT} ≥ 3.3 V	–1%		1%	
ΔV_{OUT}	Line regulation	($V_{OUT(nom)}$ + 1 V, 2.7 V) ≤ V_{IN} ≤ 30 V		3	10	mV
	Load regulation	V_{IN} = $V_{OUT(typ)}$ + 1.5 V or 3 V (whichever is greater), 100 μA ≤ I_{OUT} ≤ 150 mA		20	50	
V_{DO}	Dropout voltage(1) (3)	TPS70933, I_{OUT} = 50 mA		295	650	mV
		TPS70933, I_{OUT} = 150 mA		960	1400	
		TPS70950, I_{OUT} = 50 mA		245	500	
		TPS70950, I_{OUT} = 150 mA		690	1200	
		TPS70965, I_{OUT} = 50 mA		180	500	
		TPS70965, I_{OUT} = 150 mA		460	1000	
$I_{(CL)}$	Output current limit(4)	V_{OUT} = 0.9 × $V_{OUT(nom)}$	200	320	500	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA, V_{OUT} ≤ 3.3 V		1.3	2.05	μA
		I_{OUT} = 0 mA, V_{OUT} > 3.3 V		1.4	2.25	
		I_{OUT} = 150 mA		350		
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 2.7 V		150		nA
PSRR	Power-supply rejection ratio	f = 10 Hz		80		dB
		f = 100 Hz		62		
		f = 1 kHz		52		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 10 mA, V_{IN} = 2.7 V, V_{OUT} = 1.2 V		190		μV_{RMS}
t_{STR}	Start-up time(2)	$V_{OUT(nom)}$ ≤ 3.3 V		200	600	μs
		$V_{OUT(nom)}$ > 3.3 V		500	1500	
$V_{EN(HI)}$	Enable pin high-level input voltage	Device enabled	0.9			V
$V_{EN(LOW)}$	Enable pin low-level input voltage	Device disabled	0		0.4	V
I_{EN}	EN pin current	EN = 1.0 V, V_{IN} = 5.5 V		300		nA
$I_{(REV)}$	Reverse current (flowing out of IN pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		10		nA
	Reverse current (flowing into OUT pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		100		
t_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		158		°C
		Reset, temperature decreasing		140		

(1) V_{DO} is measured with V_{IN} = 0.98 × $V_{OUT(nom)}$.
(2) Start-up time = time from EN assertion to 0.95 × $V_{OUT(nom)}$ and load = 47 Ω.
(3) Dropout is only valid when V_{OUT} ≥ 2.8 V because of the minimum input voltage limits.
(4) Measured with V_{IN} = V_{OUT} + 3 V for V_{OUT} ≤ 2.5 V. Measured with V_{IN} = V_{OUT} + 2.5 V for V_{OUT} > 2.5 V.

6.6 Typical Characteristics

over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

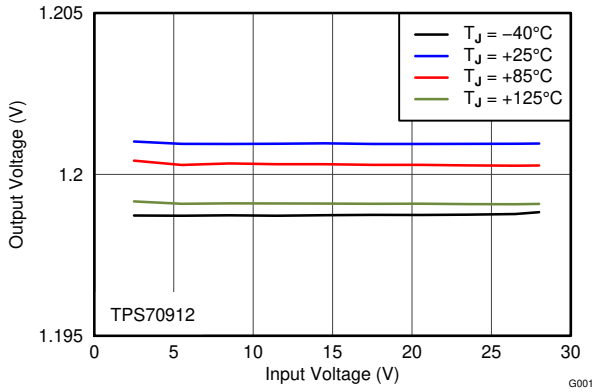


图 6-1. 1.2-V Line Regulation vs V_{IN} and Temperature

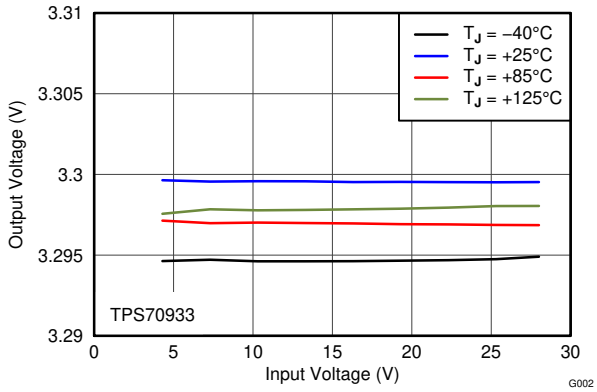


图 6-2. 3.3-V Line Regulation vs V_{IN} and Temperature

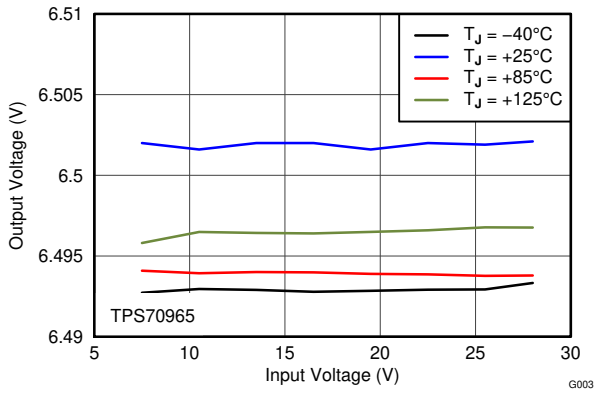


图 6-3. 6.5-V Line Regulation vs V_{IN} and Temperature

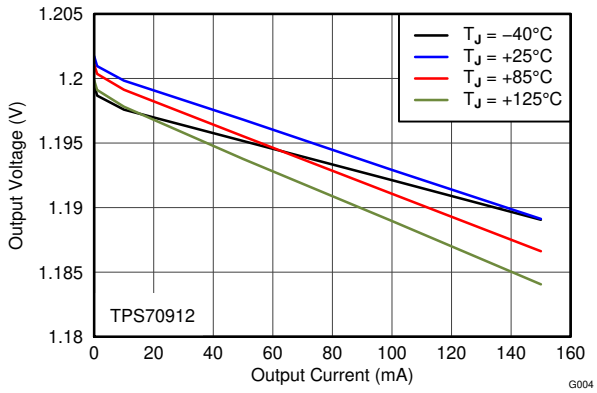


图 6-4. 1.2-V Load Regulation vs I_{OUT} and Temperature

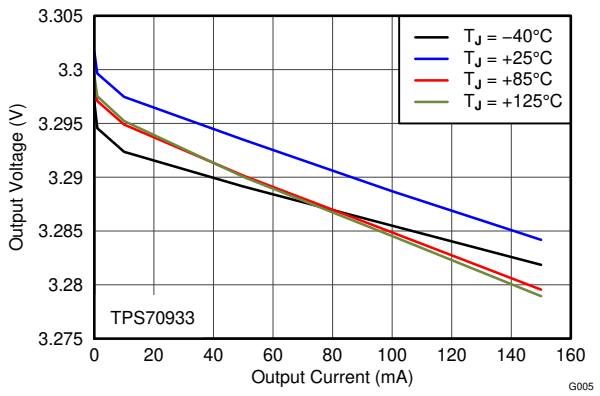


图 6-5. 3.3-V Load Regulation vs I_{OUT} and Temperature

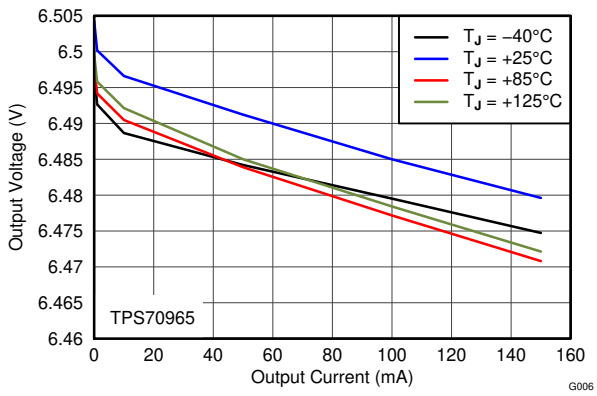


图 6-6. 6.5-V Load Regulation vs I_{OUT} and Temperature

6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

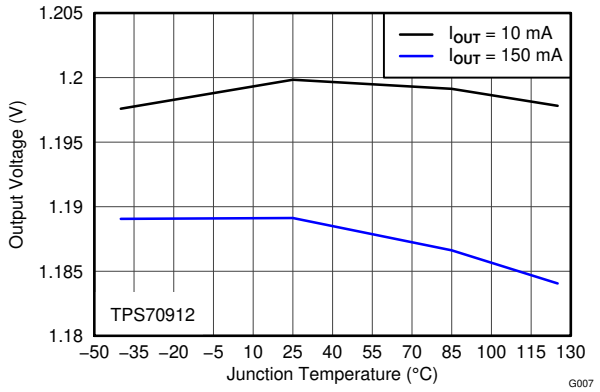


图 6-7. V_{OUT} vs Temperature

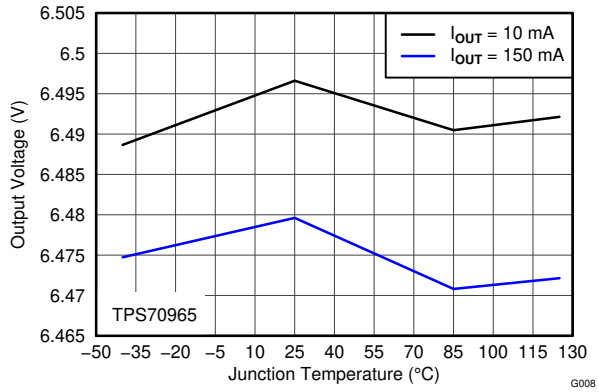


图 6-8. V_{OUT} vs Temperature

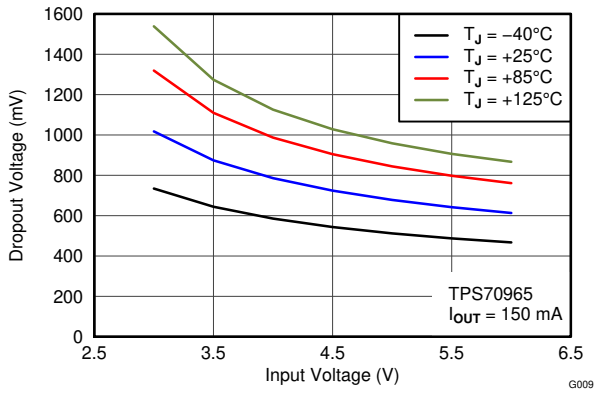


图 6-9. Dropout Voltage vs V_{IN} and Temperature

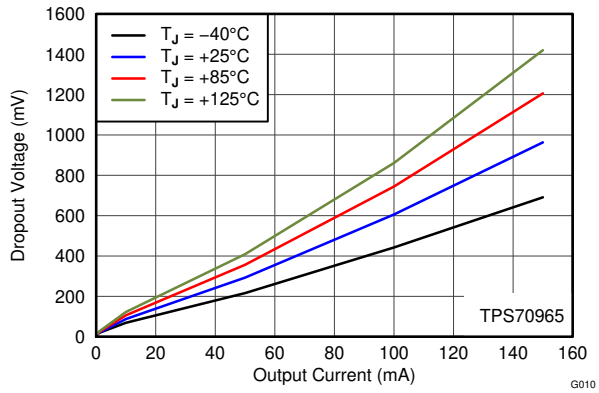


图 6-10. Dropout Voltage vs I_{OUT} and Temperature

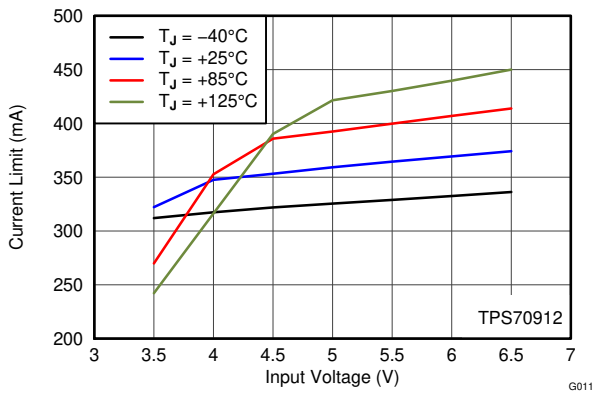


图 6-11. 1.2-V Current Limit vs V_{IN} and Temperature

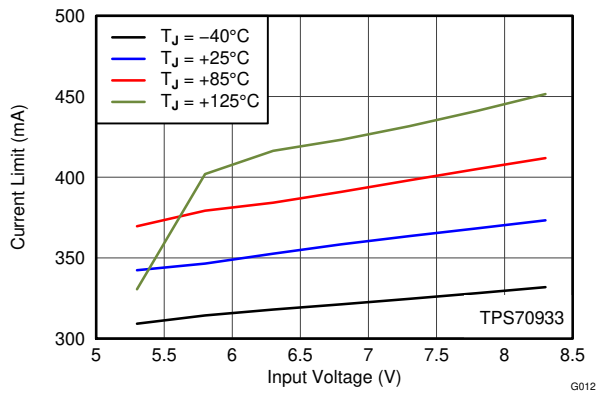


图 6-12. 3.3-V Current Limit vs V_{IN} and Temperature

6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

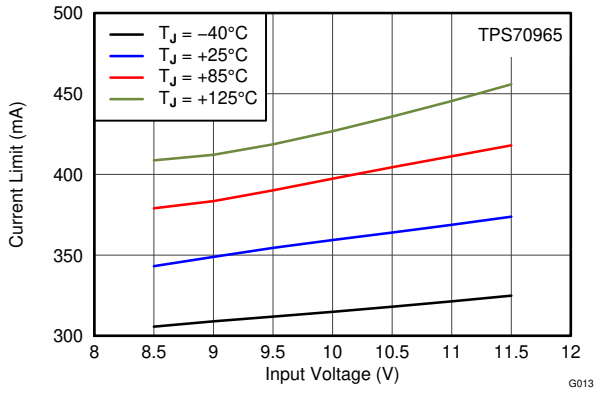


图 6-13. 6.5-V Current Limit vs V_{IN} and Temperature

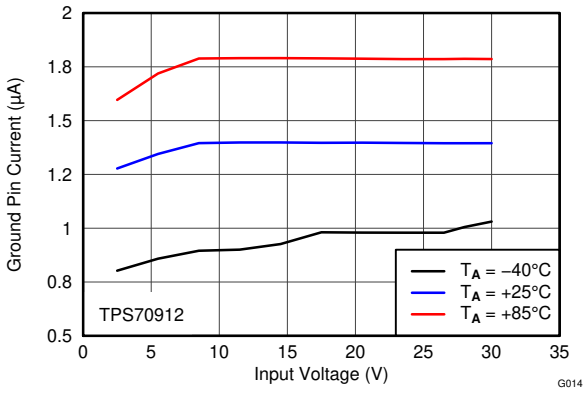


图 6-14. GND Current vs V_{IN} and Temperature

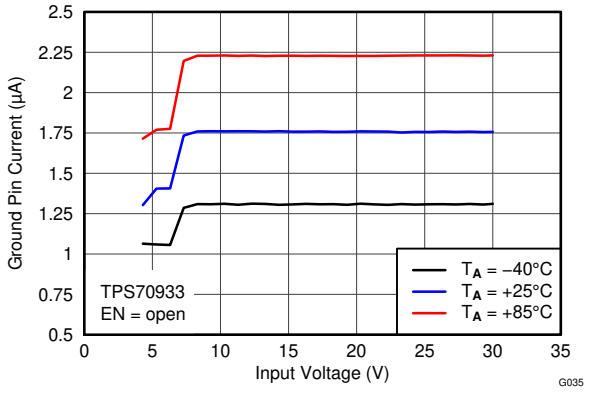


图 6-15. GND Current vs V_{IN} and Temperature

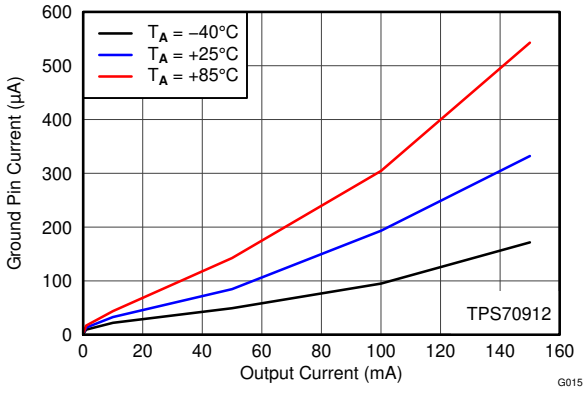


图 6-16. GND Current vs I_{OUT} and Temperature

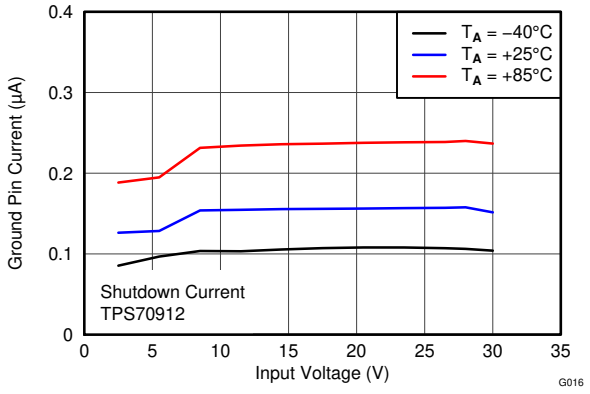


图 6-17. Shutdown Current vs V_{IN} and Temperature

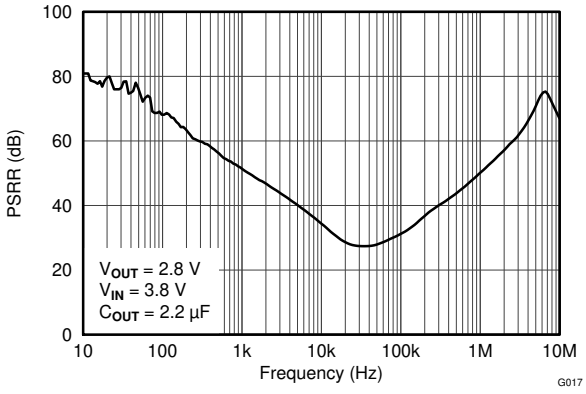


图 6-18. Power-Supply Rejection Ratio vs Frequency

6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

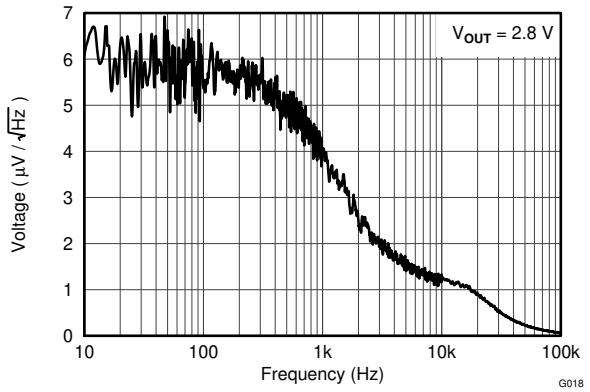


图 6-19. Noise

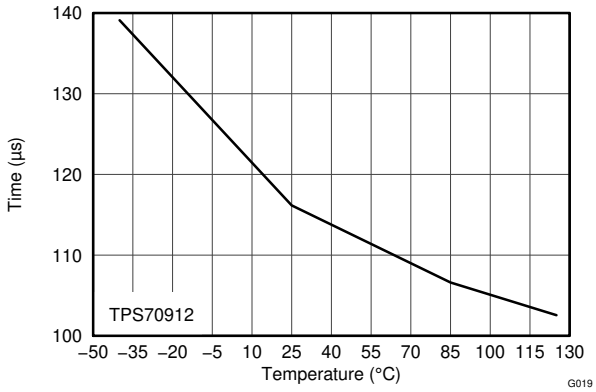


图 6-20. Start-Up Time vs Temperature

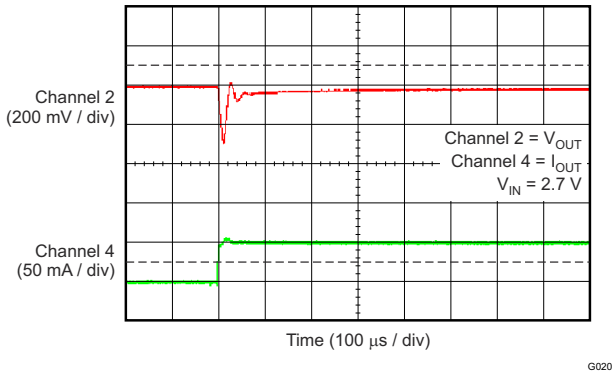


图 6-21. TPS70912 Load Transient (0 mA to 50 mA)

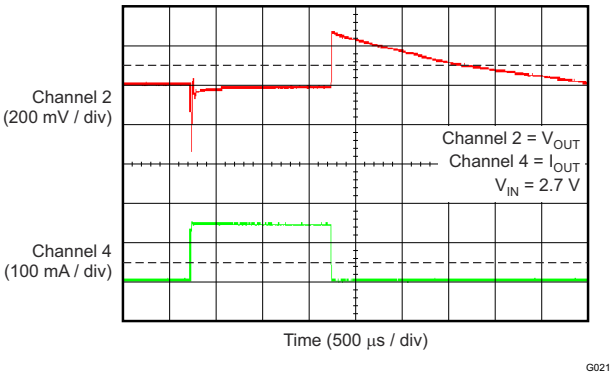


图 6-22. TPS70912 Load Transient (1 mA to 150 mA)

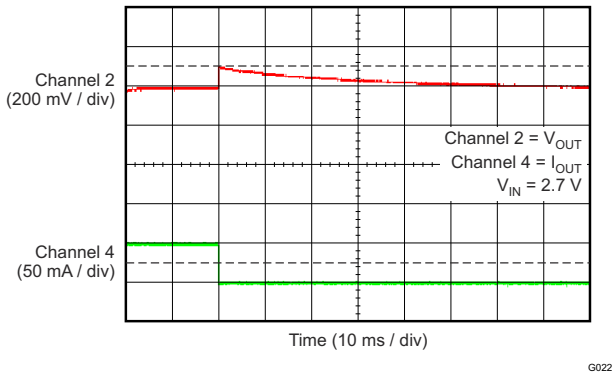


图 6-23. TPS70912 Load Transient (50 mA to 0 mA)

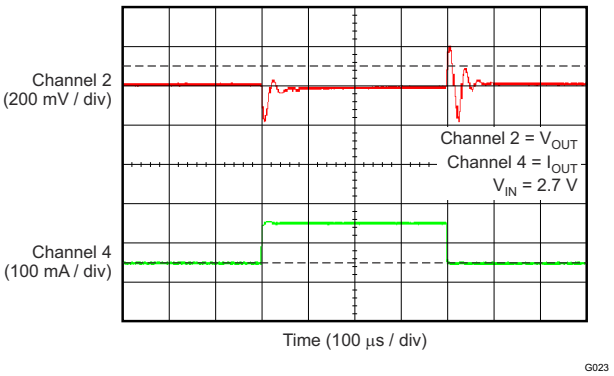


图 6-24. TPS70912 Load Transient (50 mA to 150 mA)

6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

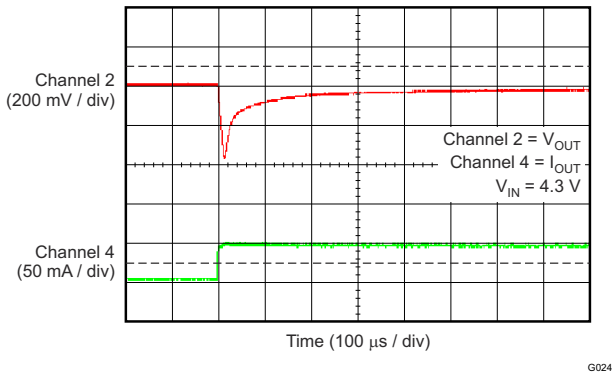


图 6-25. TPS70933 Load Transient (0 mA to 50 mA)

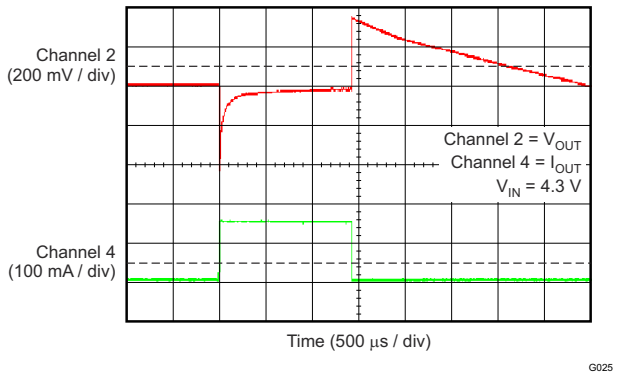


图 6-26. TPS70933 Load Transient (1 mA to 150 mA)

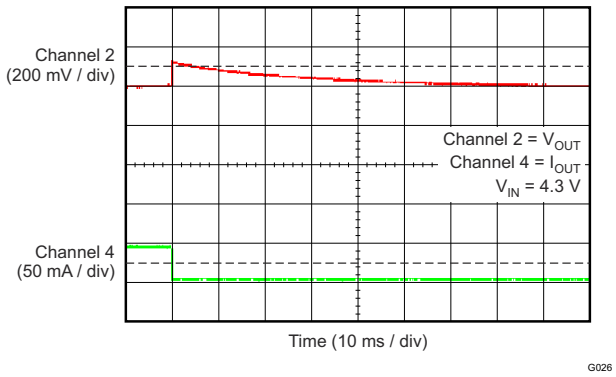


图 6-27. TPS70933 Load Transient (50 mA to 0 mA)

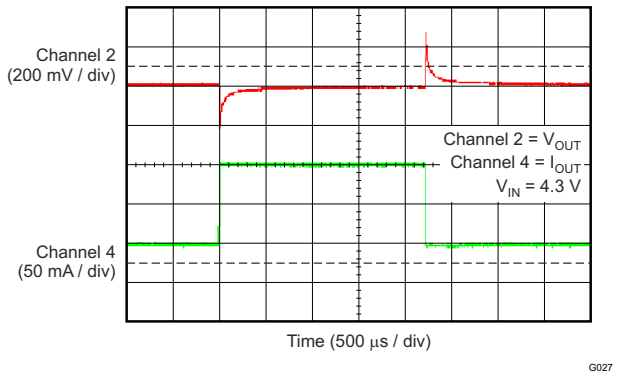


图 6-28. TPS70933 Load Transient (50 mA to 150 mA)

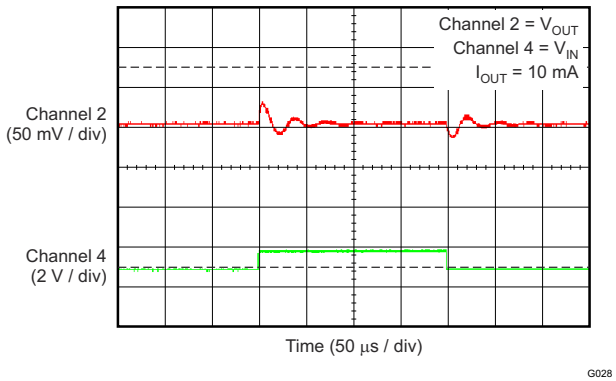


图 6-29. TPS70912 Line Transient (2.7 V to 3.7 V)

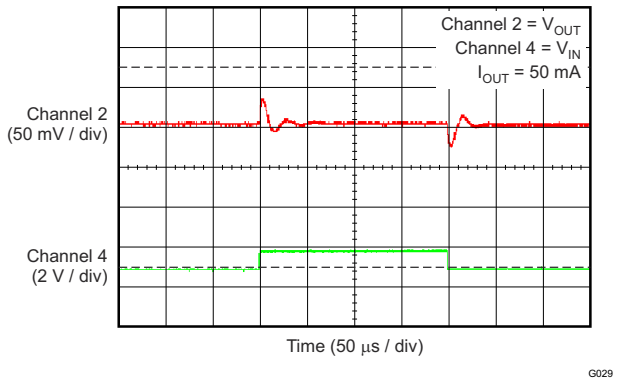


图 6-30. TPS70912 Line Transient (2.7 V to 3.7 V)

6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(typ)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

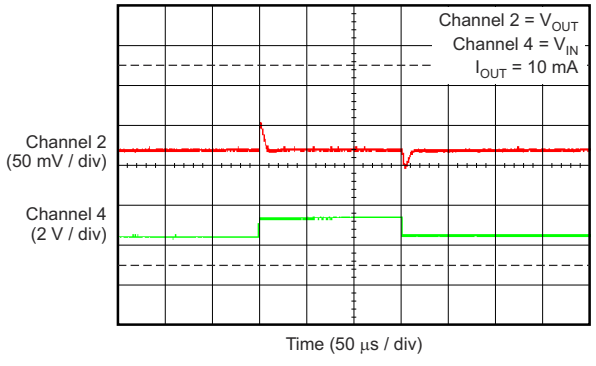


图 6-31. TPS70933 Line Transient (4.3 V to 5.3 V)

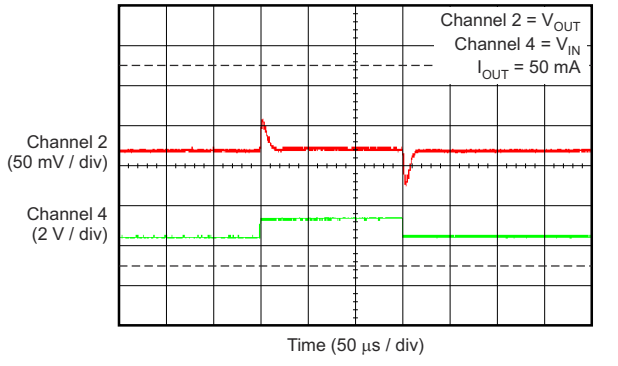


图 6-32. TPS70933 Line Transient (4.3 V to 5.3 V)

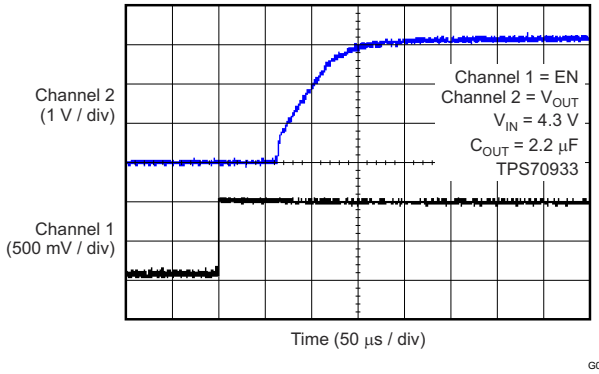


图 6-33. Power-Up With Enable

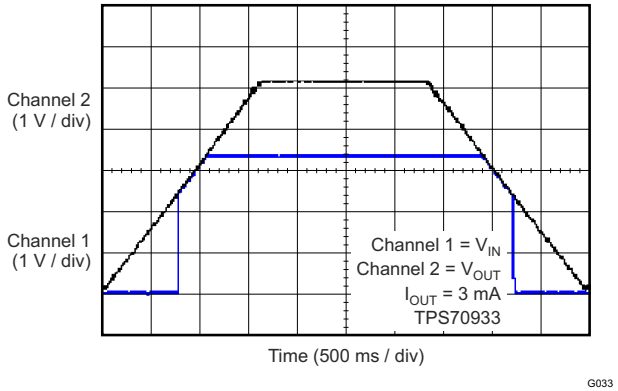


图 6-34. Power-Up and Power-Down Response

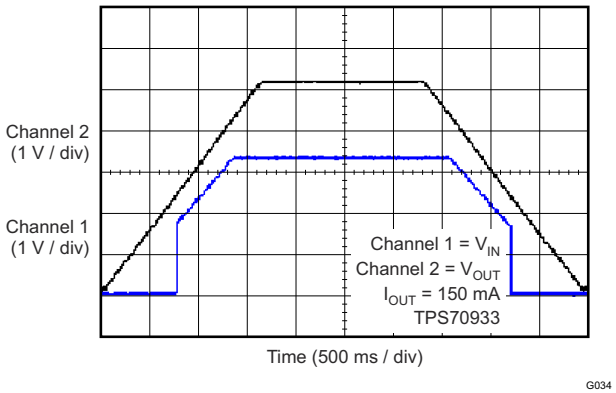


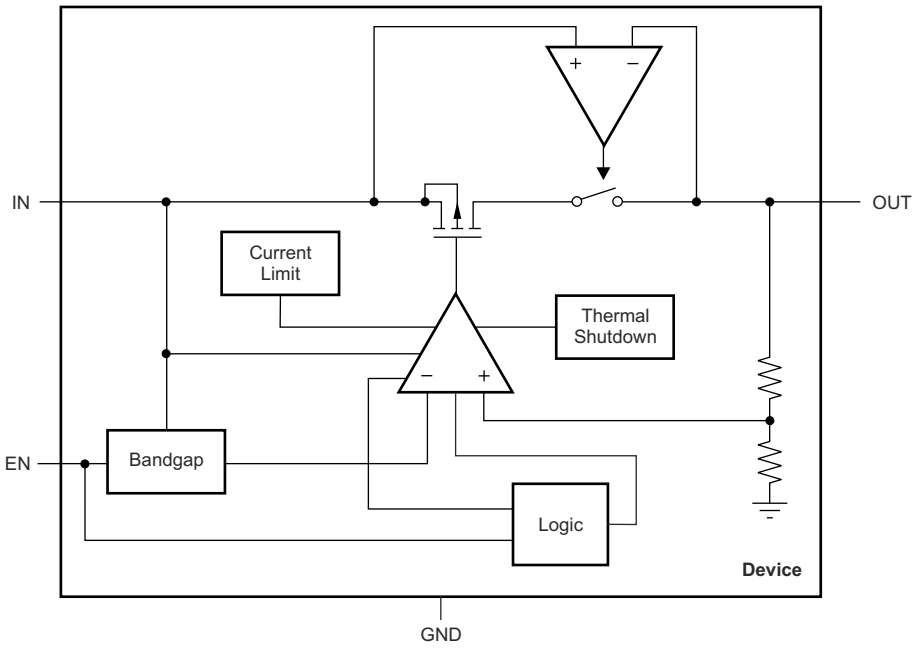
图 6-35. Power-Up and Power-Down Response

7 Detailed Description

7.1 Overview

The TPS709 series of devices are ultra-low quiescent current, low-dropout (LDO) linear regulators. The TPS709 offers reverse current protection to block any discharge current from the output into the input. The TPS709 also features current limit and thermal shutdown for reliable operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TPS709 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as ($V_{OUT} = I_{LIMIT} \times R_{LOAD}$). The PMOS pass transistor dissipates [(V_{IN} – V_{OUT}) × I_{LIMIT}] until a thermal shutdown is triggered and the device turns off. When cool, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Protection* section for more details.

The TPS709 is characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current. The TPS709 continues to operate for output currents between 150 mA and 200 mA but some data sheet parameters may not be met.

7.3.2 Dropout Voltage

The TPS709 use a PMOS pass transistor to achieve low dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device functions like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709 employs a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions that can greatly increase battery run times.

7.3.3 Undervoltage Lockout (UVLO)

The TPS709 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

7.3.4 Reverse-Current Protection

The TPS709 has integrated reverse-current protection. Reverse-current protection prevents the flow of current from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse-current protection circuitry places the power path in high impedance when the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 5.0-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

7.4 Device Functional Modes

The TPS709 has the following functional modes:

1. **Enabled:** When the enable pin (EN) goes above 0.9 V, the device is enabled. EN is pulled high by a 300-nA current source; therefore, EN can be left floating to enable the device. Do not connect EN to VIN. The EN pin is clamped by a 6.5-V Zener diode. Do not exceed the 7-V absolute maximum rating on the enable pin or excessive current flowing into the Zener clamp will destroy the device.
2. **Disabled:** When EN goes below 0.4 V, the device is disabled. During this time, OUT is high impedance and the current into IN ($I_{(SHUTDOWN)}$) is typically 150 nA.

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS709 is a series of devices that consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, makes this device ideal for RF portable applications, current limit, and thermal protection. The TPS709 is specified from –40°C to +125°C.

8.1.1 Input and Output Capacitor

The TPS709 devices are stable with output capacitors with an effective capacitance of 2.0 µF or greater for output voltages below 1.5 V. For output voltages equal or greater than 1.5 V, the minimum effective capacitance for stability is 1.5 µF. The maximum capacitance for stability is 47 µF. The equivalent series resistance (ESR) of the output capacitor must be between 0 Ω and 0.2 Ω for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 2.2-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is necessary if line transients greater than 10 V in magnitude are anticipated.

8.1.2 Transient Response

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

8.2 Typical Application

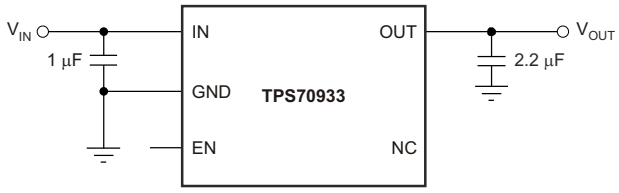


图 8-1. Wide Input, 3.3-V, Low-I_Q Rail

8.2.1 Design Requirements

表 8-1 summarizes the design requirements for 图 8-1.

表 8-1. Design Requirements for a Wide Input, 3.3-V, Low-I_Q Rail Application

PARAMETER	DESIGN SPECIFICATION
V_{IN}	5 V to 20 V
V_{OUT}	3.3 V
$I_{(IN)}$ (no load)	< 5 µA
I_{OUT} (max)	150 mA

8.2.2 Detailed Design Procedure

Select a 2.2-µF, 10-V X7R output capacitor to satisfy the minimum output capacitance requirement with a 3.3-V dc bias.

Select a 1.0-µF, 25-V X7R input capacitor to provide input noise filtering and eliminate high-frequency voltage transients.

8.2.3 Application Curves

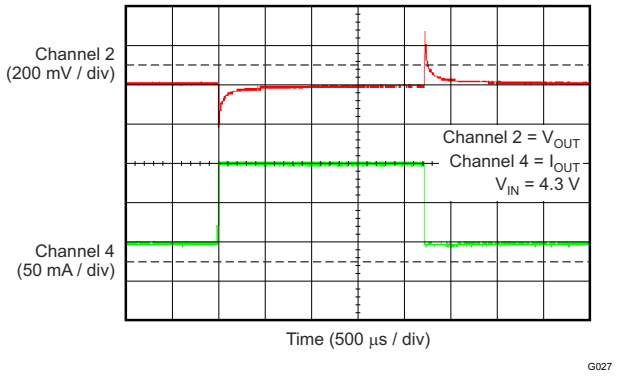


图 8-2. TPS70933 Load Transient (50 mA to 150 mA)

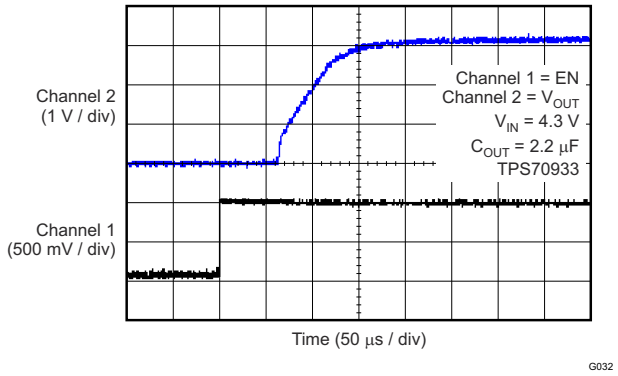


图 8-3. Power-Up With Enable

9 Power Supply Recommendations

This device is designed to operate with an input supply range of 2.7 V to 30 V. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance.

9.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC low and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_{DISS}) is equal to the product of the output current and the voltage drop across the output pass element, as shown in 方程式 1:

$$P_{DISS} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

10 Layout

10.1 Layout Guidelines

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the device GND pin.

10.1.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The TPS709 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS709 into thermal shutdown degrades device reliability.

10.2 Layout Example

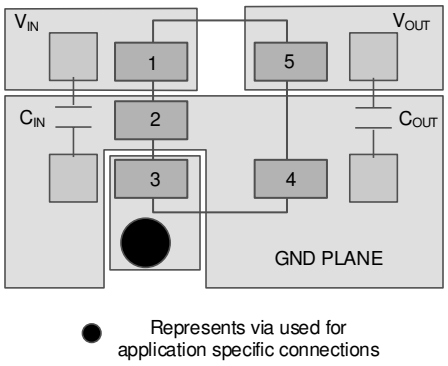


图 10-1. Layout Example for DBV Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS709xx. The TPS70933EVM-110 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS709 is available through the product folders under *Simulation Models*.

11.1.2 Device Nomenclature

表 11-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS709**xx(x)** ***yyy z*** ***or*** TPS709**xx(x)** ***yyy zM3***	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250). **M3** suffix device has same electrical specs as other devices and shares same design.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS70933EVM-110 Evaluation Module* user guide

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70912DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCX	Samples
TPS70912DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCX	Samples
TPS70912DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCX	Samples
TPS70912DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCX	Samples
TPS709135DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCY	Samples
TPS709135DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCY	Samples
TPS70915DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIM	Samples
TPS70915DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIM	Samples
TPS70915DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIM	Samples
TPS70915DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIM	Samples
TPS70916DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCZ	Samples
TPS70916DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCZ	Samples
TPS70918DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	Samples
TPS70918DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	Samples
TPS70918DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	Samples
TPS70918DRVRM3	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	Samples
TPS70918DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	Samples
TPS70919DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SDB	Samples
TPS70919DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SDB	Samples
TPS70925DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70925DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDC	Samples
TPS70925DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDC	Samples
TPS70925DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDC	Samples
TPS70927DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDD	Samples
TPS70927DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDD	Samples
TPS70928DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDE	Samples
TPS70928DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDE	Samples
TPS70930DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SDF	Samples
TPS70930DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SDF	Samples
TPS70930DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDF	Samples
TPS70930DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDF	Samples
TPS70933DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SDG	Samples
TPS70933DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SDG	Samples
TPS70933DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDG	Samples
TPS70933DRVRM3	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDG	Samples
TPS70933DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDG	Samples
TPS70936DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SEJ	Samples
TPS70936DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SEJ	Samples
TPS70936DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1FV	Samples
TPS70938DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIC	Samples
TPS70938DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70939DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SID	Samples
TPS70939DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SID	Samples
TPS70950DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SDH	Samples
TPS70950DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SDH	Samples
TPS70950DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDH	Samples
TPS70950DRVRM3	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDH	Samples
TPS70950DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDH	Samples
TPS70960DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIT	Samples
TPS70960DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIT	Samples
TPS709A30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11RF	Samples
TPS709A30DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11RF	Samples
TPS709A33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11SF	Samples
TPS709A33DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11SF	Samples
TPS709B33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13C7	Samples
TPS709B33DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13C7	Samples
TPS709B345DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XSW	Samples
TPS709B50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13D7	Samples
TPS709B50DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13D7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS709 :

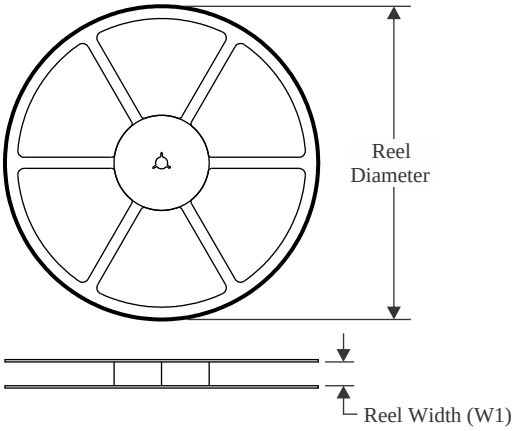
- Automotive : TPS709-Q1

NOTE: Qualified Version Definitions:

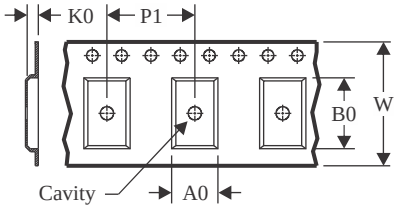
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

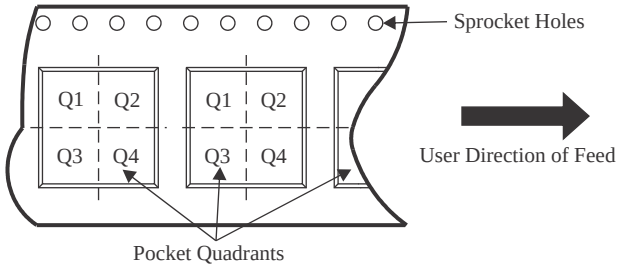


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



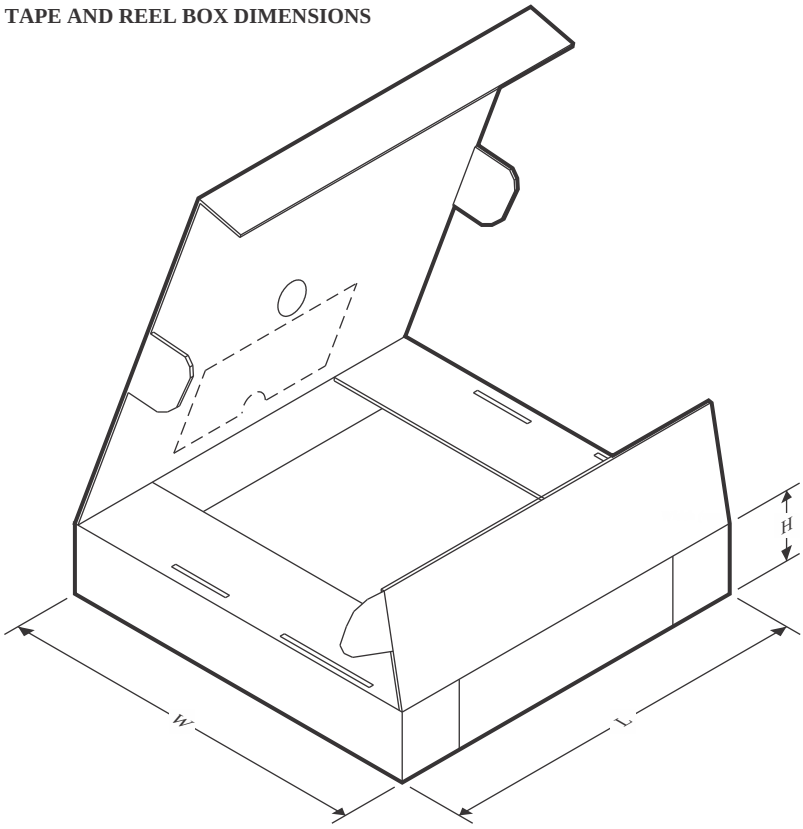
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70912DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70912DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70912DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70912DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS709135DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709135DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70915DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70915DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70915DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70915DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70915DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70915DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70916DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70916DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70918DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70918DRVRM3	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70918DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70919DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70919DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70925DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70925DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70925DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70927DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70927DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70930DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70930DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70930DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70933DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70933DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70933DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70933DRVRM3	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70933DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70936DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70936DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70936DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70938DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70938DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70939DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70939DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70950DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70950DRVRM3	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70950DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70960DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70960DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709A30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709A30DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709A33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709A33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS709B345DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B50DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70912DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70912DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70912DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70912DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS709135DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709135DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70915DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70915DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70915DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70915DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70915DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS70915DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70916DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70916DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70918DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70918DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70918DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70918DRVRM3	WSON	DRV	6	3000	182.0	182.0	20.0

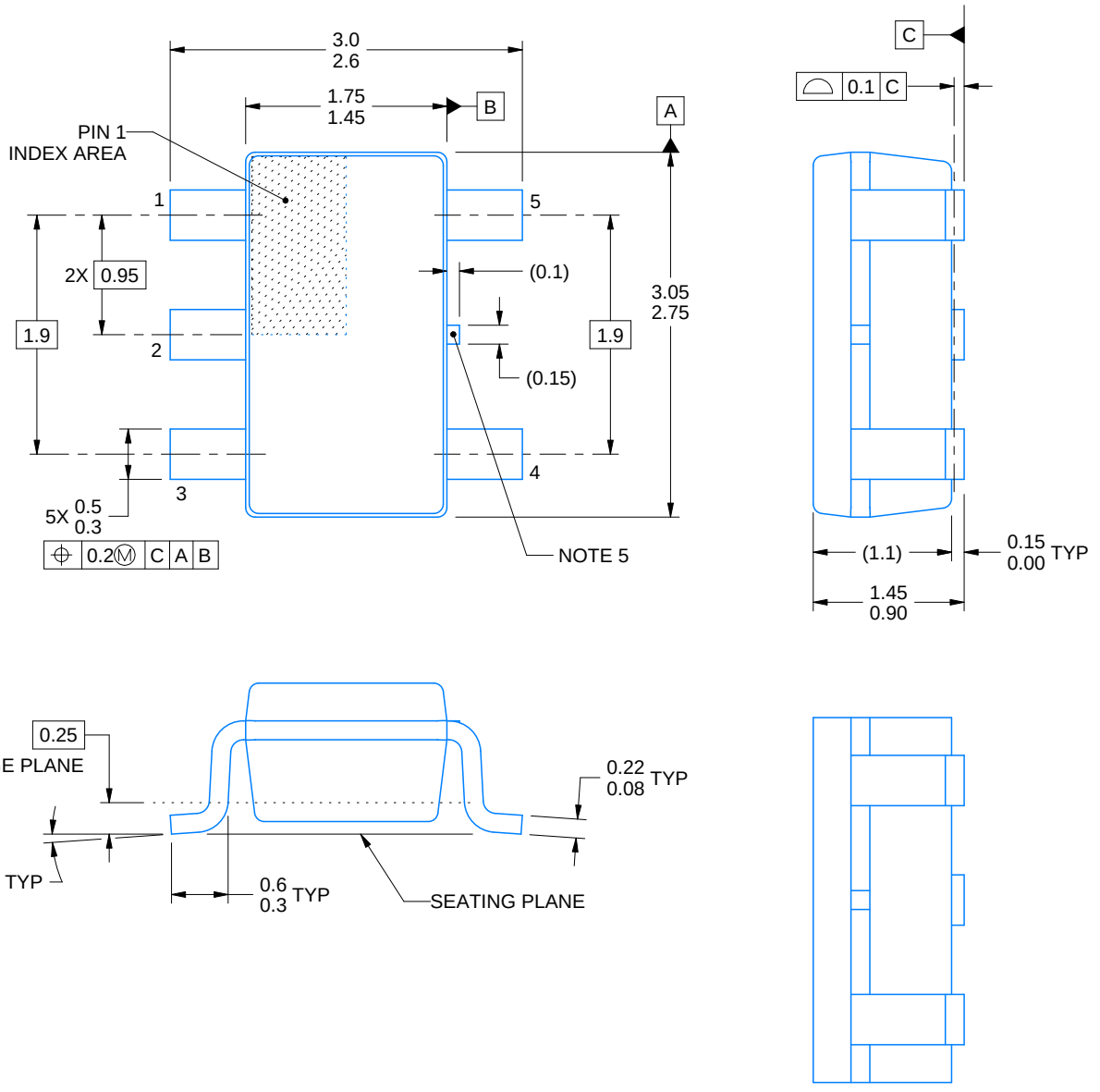
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70918DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70919DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS70919DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS70925DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70925DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70925DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70925DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70927DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70927DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70928DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70928DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70930DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS70930DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS70930DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70930DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70933DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS70933DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS70933DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70933DRVRM3	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70933DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70936DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS70936DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS70936DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS70938DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70938DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70939DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70939DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70950DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS70950DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70950DRVRM3	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70950DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70960DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70960DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS709A30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709A30DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS709A33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709A33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS709B33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709B33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS709B345DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709B50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709B50DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

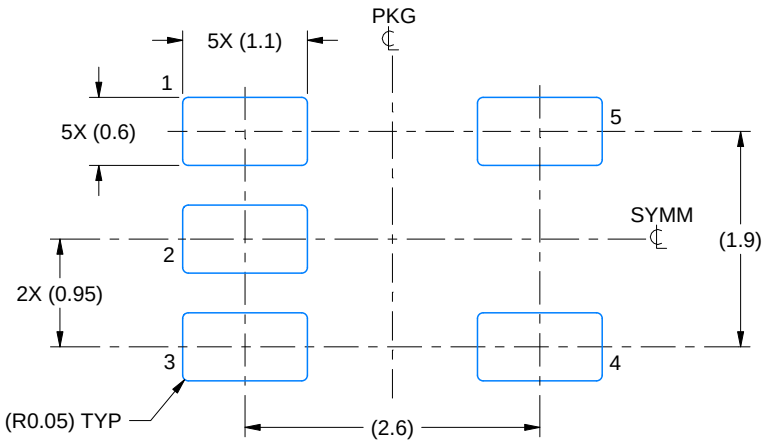


ALTERNATIVE PACKAGE SINGULATION VIEW

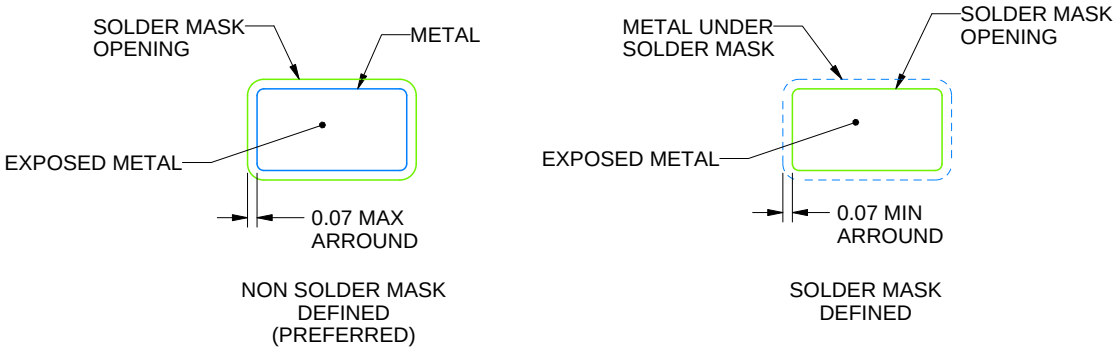
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

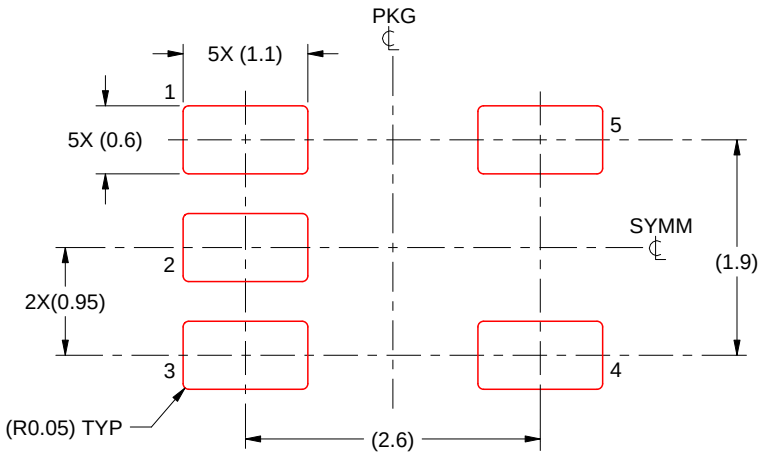


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

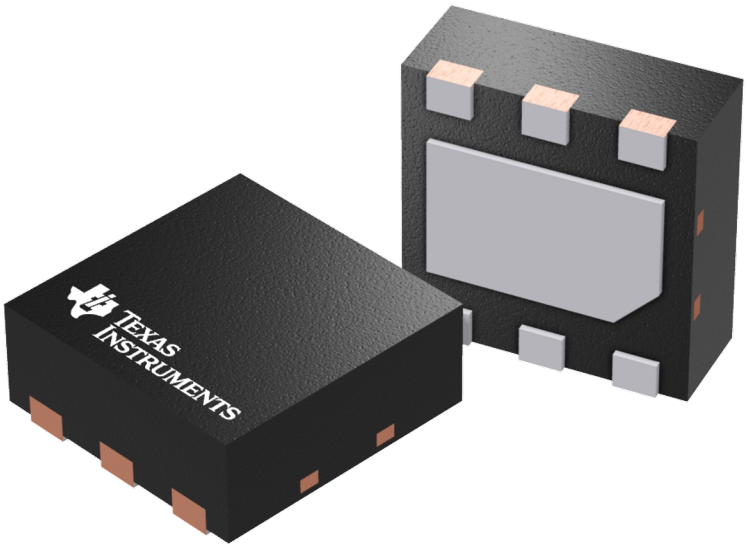
4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



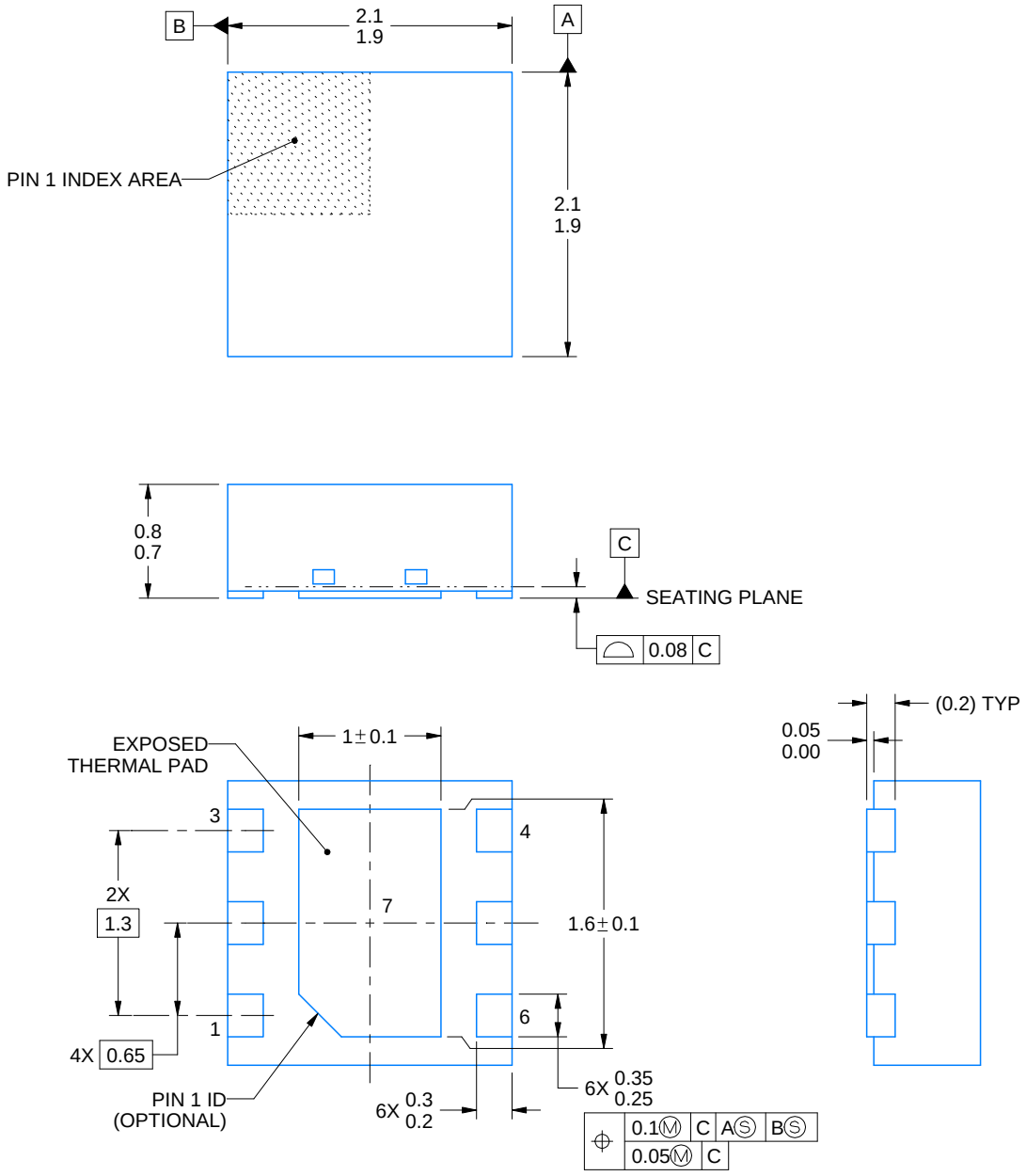
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

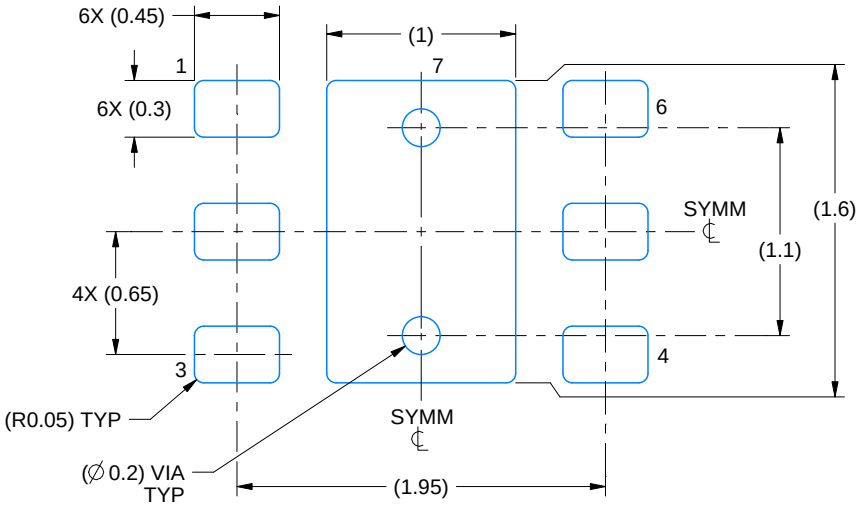
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

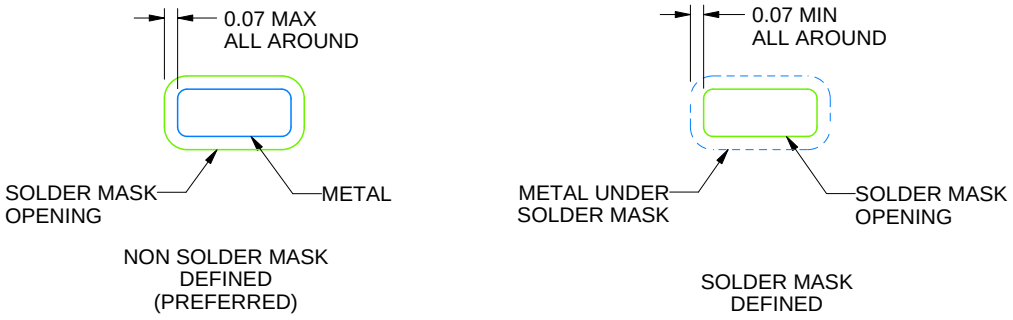


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

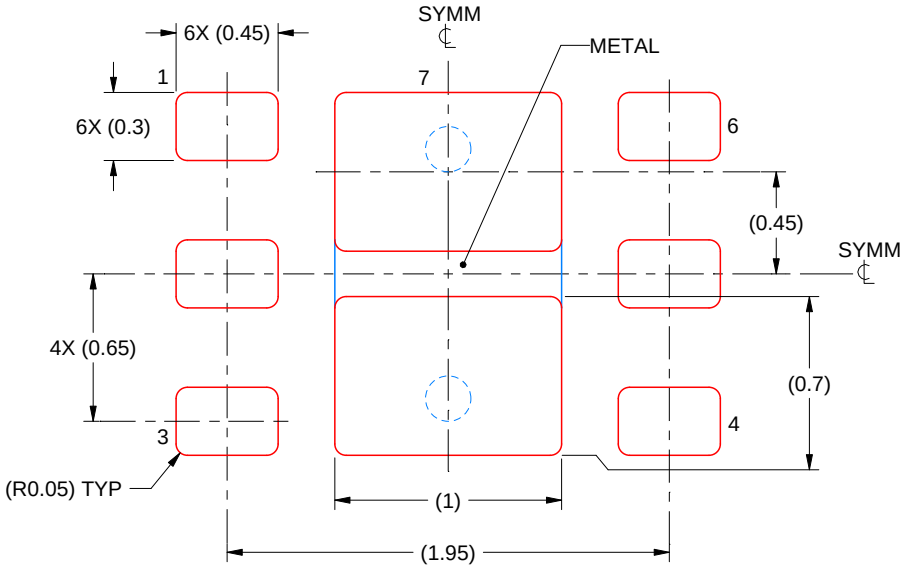
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

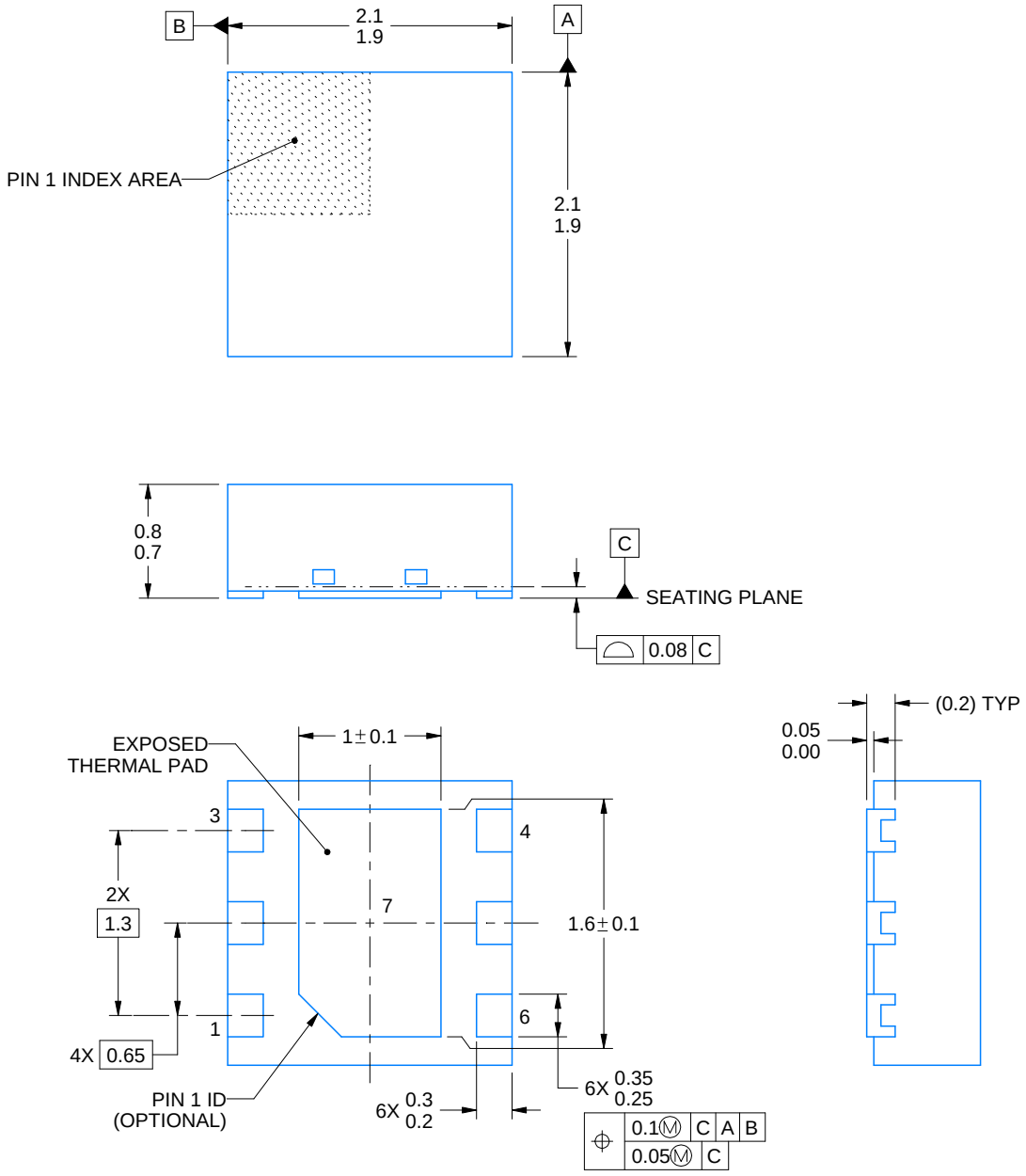
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

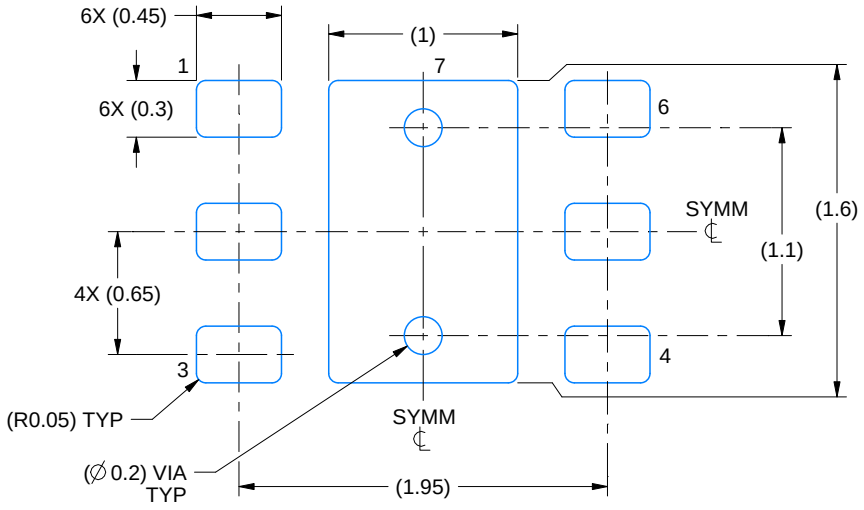
PLASTIC SMALL OUTLINE - NO LEAD



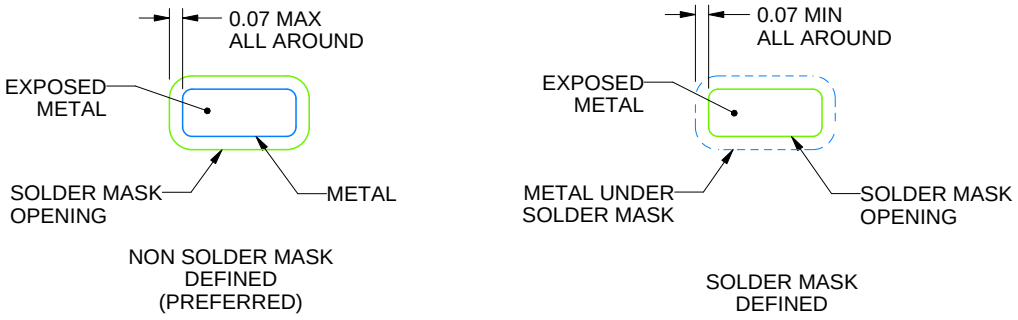
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

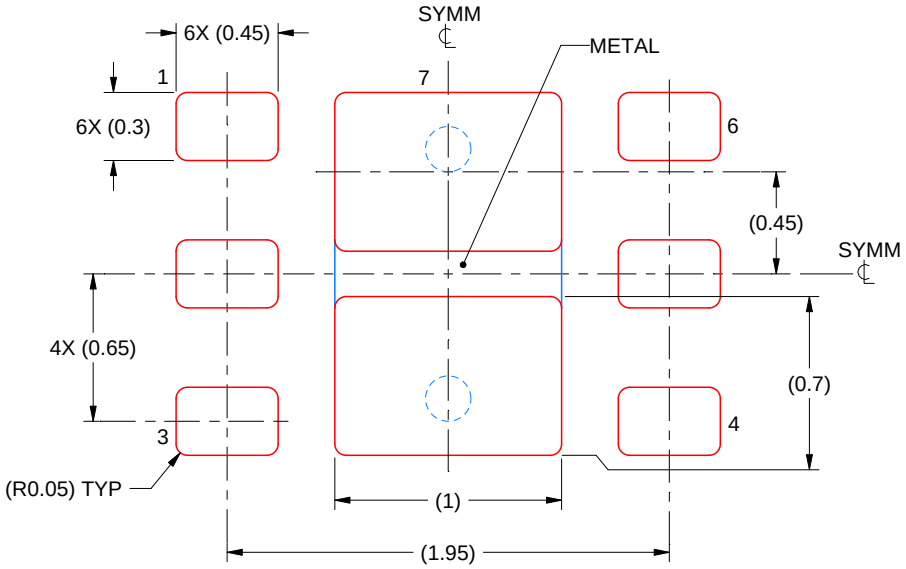


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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