TS3USB221A 具有单使能端和 ESD 保护的高速 USB 2.0 (480Mbps) 1:2 多路复用器和多路信号分离器开关

1 特性

- 在 2.5V 至 3.3V V_{CC} 下运行
- $V_{I/O}$ 支持高达 5.5V 的信号
- 1.8V 兼容控制引脚输入
- $\overline{OE}$ 禁用时采用低功耗模式 (1 µA)
- R_{ON} = 6 Ω（最大值）
- δ R_{ON} = 0.2 Ω（典型值）
- $C_{IO(ON)}$ = 6pf（典型值）
- 低功耗（最大值为 30 µA）
- 高带宽（典型值为 900MHz）
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- ESD 性能经测试符合 JEDEC JS-001 标准
  - 7000V 人体放电模型
  - 1000V 充电器件模型 (JEDEC JS-002)
- ESD 性能 I/O 接地
  - 12kV 人体放电模型

2 应用

- 为 USB 1.0、1.1 和 2.0 路由信号
- 手机
- 摄像头
- 笔记本电脑
- USB I/O 扩展

3 说明

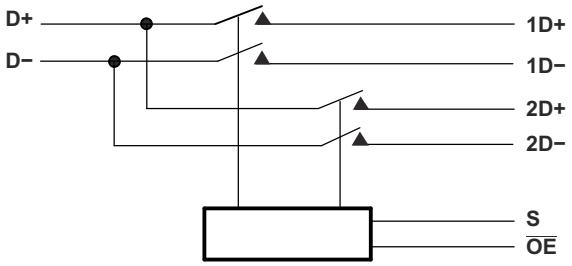
TS3USB221A 器件是一款高带宽开关，专为手持和消费类应用（例如手机、数码相机和具有集线器的笔记本电脑或具有受限 USB I/O 的控制器）中的高速 USB 2.0 信号切换而设计。此开关具有较宽的带宽 (900MHz)，这一特性使得信号传递具有最少的边缘失真和相位失真。该器件将 USB 主机器件差动输出复用到一个相应的输出（共两个输出）。此开关为双向开关，输出端高速信号具有极少或零衰减。该器件还具有低功耗模式，可将功耗降低至 1 µA，适用于使用电池或具有有限功率预算的便携式应用。该器件经过精心设计，可实现低位间偏移和高通道间噪声隔离，并且与高速 USB 2.0 (480Mbps) 等各种标准兼容。

TS3USB221A 器件在所有引脚上集成了 ESD 保护单元，采用微型 µQFN 封装 (2mm × 1.5mm)，在自然通风条件下的额定工作温度范围为 –40°C 至 85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
TS3USB221A	RSE（UQFN，10）	2mm × 1.5mm

(1) 有关所有可用封装，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



EN 是应用于开关的内部启用信号。

简化原理图

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4 Pin Configuration and Functions

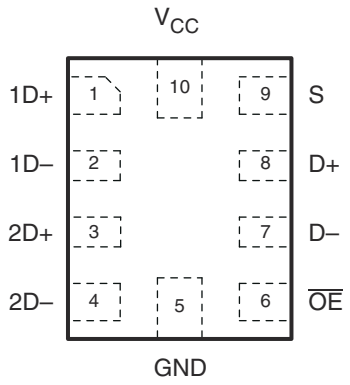


图 4-1. RSE Package, 10-Pin µQFN (Top View)

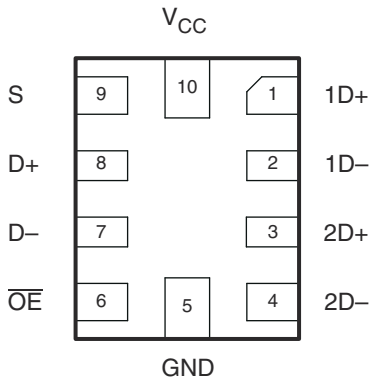


图 4-2. RSE Package, 10-Pin µQFN (Bottom View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1D+	1	I/O	USB port 1
1D–	2	I/O	
2D+	3	I/O	USB port 2
2D–	4	I/O	
GND	5	—	Ground
$\overline{OE}$	6	I	Bus-switch enable
D+	8	I/O	Common USB port
D—	7	I/O	
S	9	I	Select input
V_{CC}	10	—	Supply voltage

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	4.6	V
Control input voltage, V_S, $V_{\overline{OE}}$ (2) (3)		–0.5	7	V
Switch I/O voltage, $V_{I/O}$ (2) (3) (4)		–0.5	7	V
Control input clamp current, I_{IK}	$V_{IN} < 0$		–50	mA
I/O port clamp current, $I_{I/OK}$	$V_{I/O} < 0$		–50	mA
ON-state switch current, $I_{I/O}$ (5)			±120	mA
Continuous current through V_{CC} or GND			±100	mA
T_{stg} Storage temperature range		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except I/O to GND	±7000	V
			I/O to GND	±12000	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_S, $V_{\overline{OE}}$	High-level control input voltage	V_{CC} = 2.3V to 2.7V	0.46 × V_{CC}	V_{CC}	V
		V_{CC} = 2.7V to 3.6V	0.46 × V_{CC}	V_{CC}	
	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.25 × V_{CC}	V
		V_{CC} = 2.7V to 3.6V	0	0.25 × V_{CC}	
$V_{I/O}$	Data input/output voltage(1)		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) The I/O pins are 5.5V tolerant and functional for the entire range. However, for $V_{I/O}$ > 3.6V, channel RON will be high (up to 100Ω).

5.4 Thermal Information

THERMAL METRIC[1]		RSE (UQFN)	UNIT
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	118.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	121.5	
ψ_{JT}	Junction-to-top characterization parameter	13.9	
ψ_{JB}	Junction-to-board characterization parameter	121.2	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input-Source Clamp Voltage	V_{CC} = 3.6V, 2.7V, I_I = – 18 mA		– 1.8			V
I_{IN}	Input leakage current, control inputs	V_{CC} = 3.6V, 2.7V, 0V, V_{IN} = 0V to 3.6V				±1	μA
I_{OZ} (3)	Off-state leakage current	V_{CC} = 3.6V, 2.7V, V_O = 0V to 5.25V, V_I = 0V, V_{IN} = V_{CC} or GND, Switch OFF				±1	μA
$I_{(OFF)}$	Power-off leakage current	V_{CC} = 0V	$V_{I/O}$ = 0V to 5.25V			±2	μA
			$V_{I/O}$ = 0V to 3.6V			±2	
			$V_{I/O}$ = 0V to 2.7V			±1	
I_{CC}	Supply Current	V_{CC} = 3.6V, 2.7V, V_{IN} = V_{CC} or GND, $I_{I/O}$ = 0V, Switch ON or OFF				30	μA
I_{CC}	Supply Current (low power mode)	V_{CC} = 3.6V, 2.7V, V_{IN} = V_{CC} or GND, Switch disabled, $\overline{OE}$ in high state				1	μA
ΔI_{CC} (4)	Supply-current change, control inputs	One input at 1.8V, Other inputs at V_{CC} or GND	V_{CC} = 3.6V			20	μA
			V_{CC} = 2.7V			0.5	
C_{in}	Input capacitance, control inputs	V_{CC} = 3.3V, 2.5V, V_{IN} = V_{CC} or 0V			1.5	2.5	pF
$C_{io(OFF)}$	OFF capacitance	V_{CC} = 3.3V, 2.5V, $V_{I/O}$ = V_{CC} or 0V, Switch OFF			3.5	5	pF
$C_{io(ON)}$	ON capacitance	V_{CC} = 3.3V, 2.5V, $V_{I/O}$ = V_{CC} or 0V, Switch ON			6	7.5	pF
R_{ON} (5)	ON-state resistance	V_{CC} = 3V, 2.3V	V_I = 0V, I_O = 30mA		3	6	Ω
			V_I = 2.4V, I_O = – 15mA		3.4	6	
ΔR_{ON}	ON-state resistance match between channels	V_{CC} = 3V, 2.3V	V_I = 0V, I_O = 30mA		0.2		Ω
			V_I = 1.7, I_O = – 15mA		0.2		
$R_{ON(flat)}$	ON-state resistance flatness	V_{CC} = 3V, 2.3V	V_I = 0V, I_O = 30mA		1		Ω
			V_I = 1.7, I_O = – 15mA		1		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

5.6 Dynamic Electrical Characteristics, V_{CC} = 3.3V ±10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3V ±10%, GND = 0V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250MHz		–40		dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250MHz		–41		dB
BW	Bandwidth (–3 dB)	R_L = 50		0.9		GHz

5.7 Dynamic Electrical Characteristics, V_{CC} = 2.5V ±10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5V ±10%, GND = 0V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250MHz		–39		dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250MHz		-40		dB
BW	Bandwidth (3 dB)	R_L = 50		0.9		GHz

5.8 Switching Characteristics, V_{CC} = 3.3V ±10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3V ±10%, GND = 0V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			30	ns
		$\overline{OE}$ to D, nD			17	
t_{OFF}	Line disable time	S to D, nD			12	ns
		$\overline{OE}$ to D, nD			10	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)			0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. This time constant is much smaller than the rise/fall times of typical driving signals, therefore the time adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and the switch interactions with the load on the driven side.

5.9 Switching Characteristics, V_{CC} = 2.5V ±10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5V ±10%, GND = 0V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			50	ns
		$\overline{OE}$ to D, nD			32	
t_{OFF}	Line disable time	S to D, nD			23	ns
		$\overline{OE}$ to D, nD			12	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)			0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. This time constant is much smaller than the rise/fall times of typical driving signals, therefore the time adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and the switch interactions with the load on the driven side.

5.10 Typical Characteristics

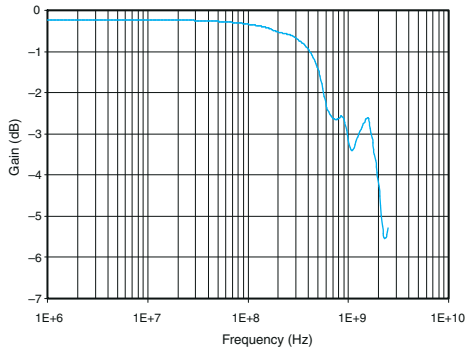


图 5-1. Gain vs Frequency

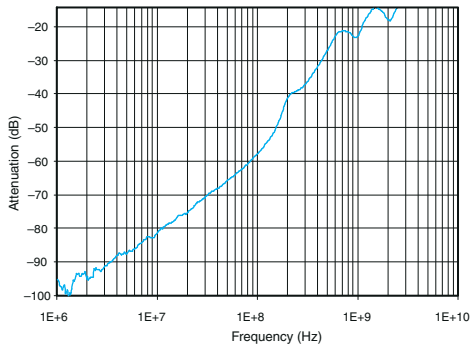


图 5-2. OFF Isolation vs Frequency

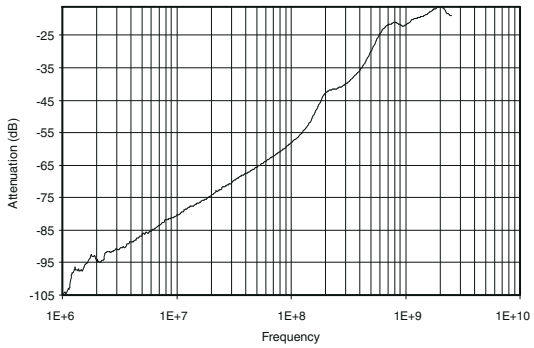


图 5-3. Crosstalk vs Frequency

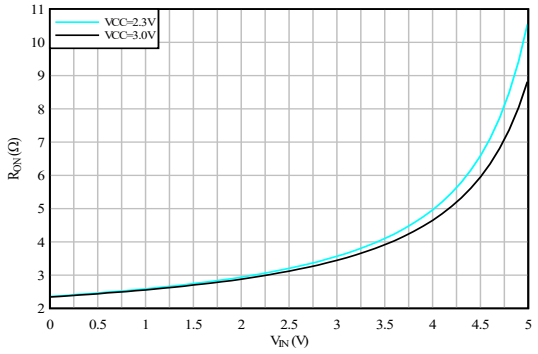
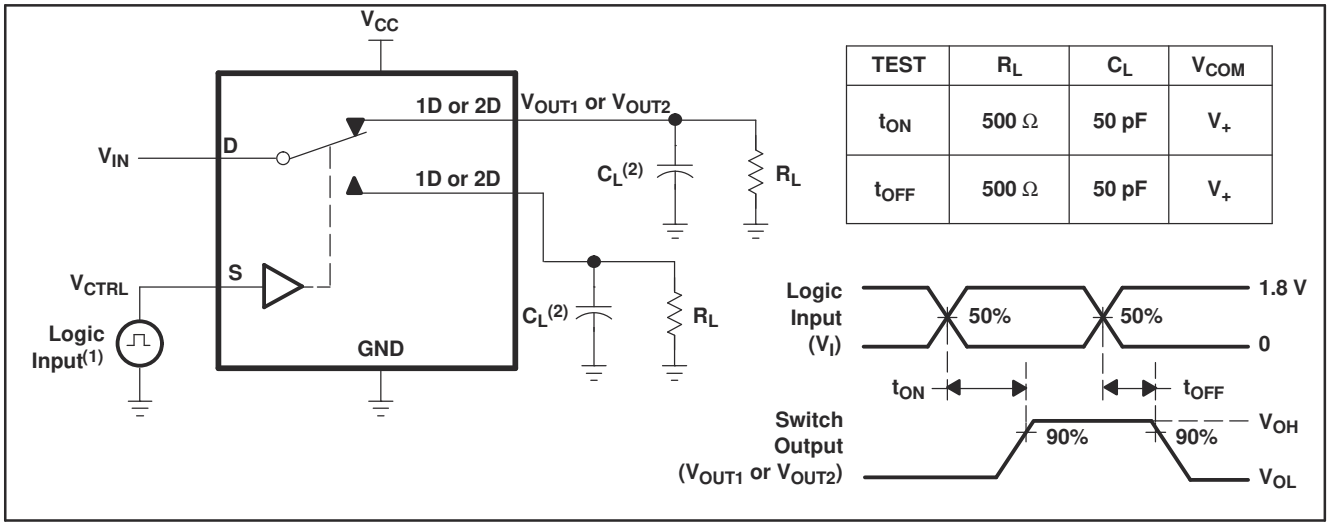


图 5-4. R_{on} vs V_{IN} (I_{OUT} = – 30 mA)

6 Parameter Measurement Information



TEST	R_L	C_L	V_{COM}
t_{ON}	500 Ω	50 pF	V_+
t_{OFF}	500 Ω	50 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

图 6-1. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

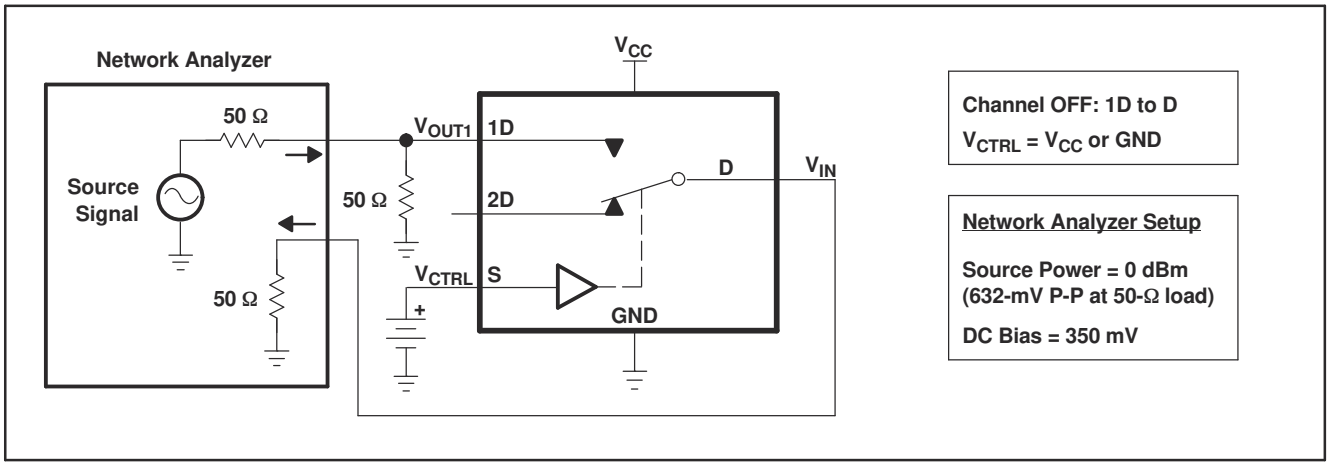


图 6-2. OFF Isolation (O_{ISO})

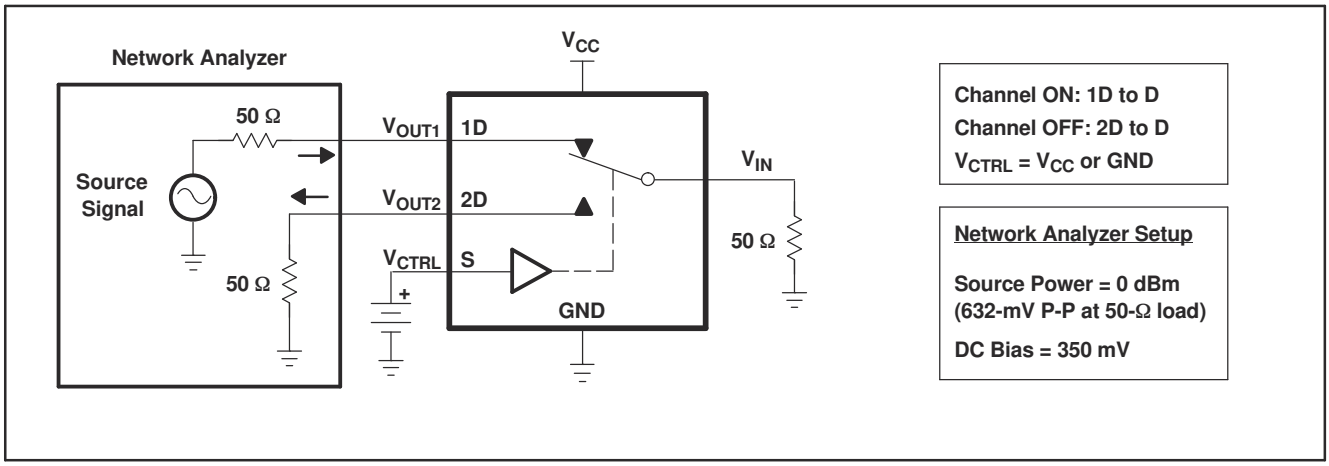


图 6-3. Crosstalk (X_{TALK})

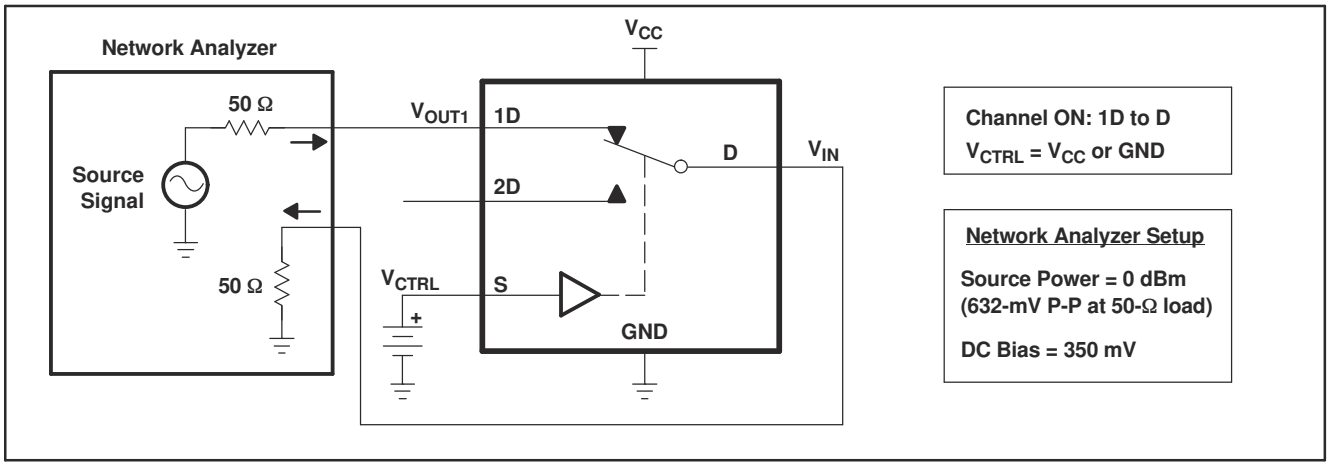


图 6-4. Bandwidth (BW)

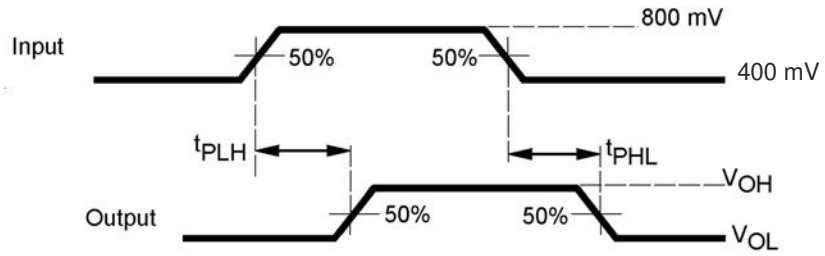


图 6-5. Propagation Delay

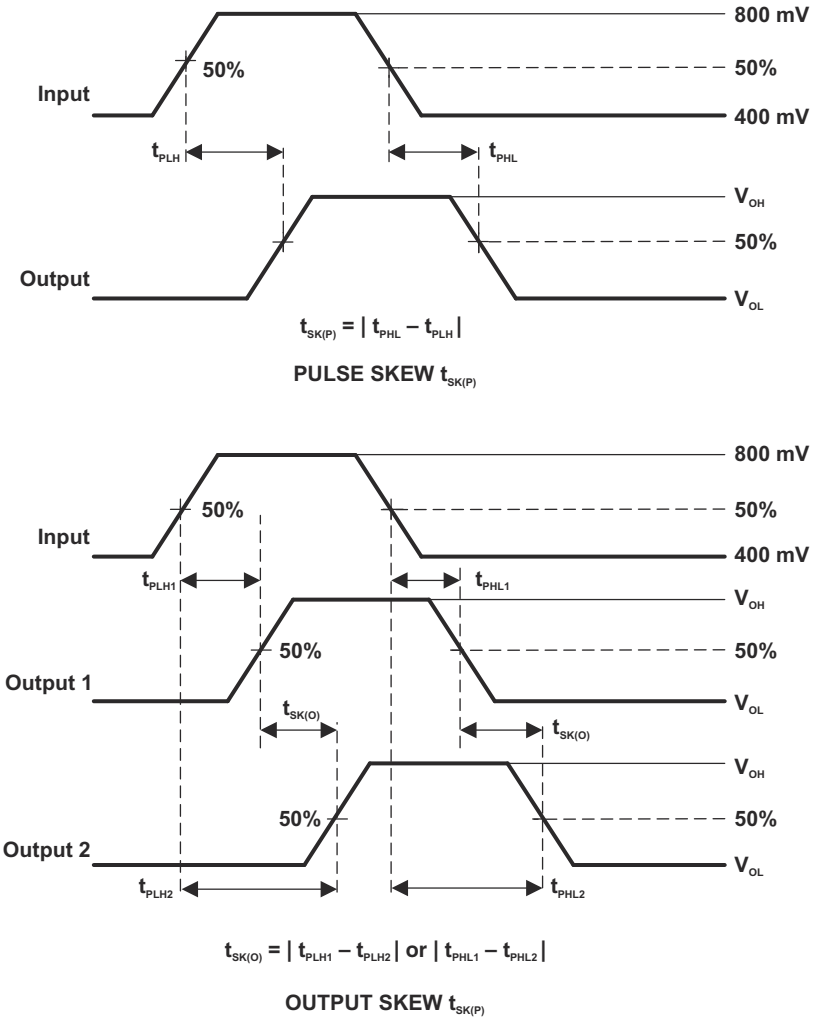


图 6-6. Skew Test

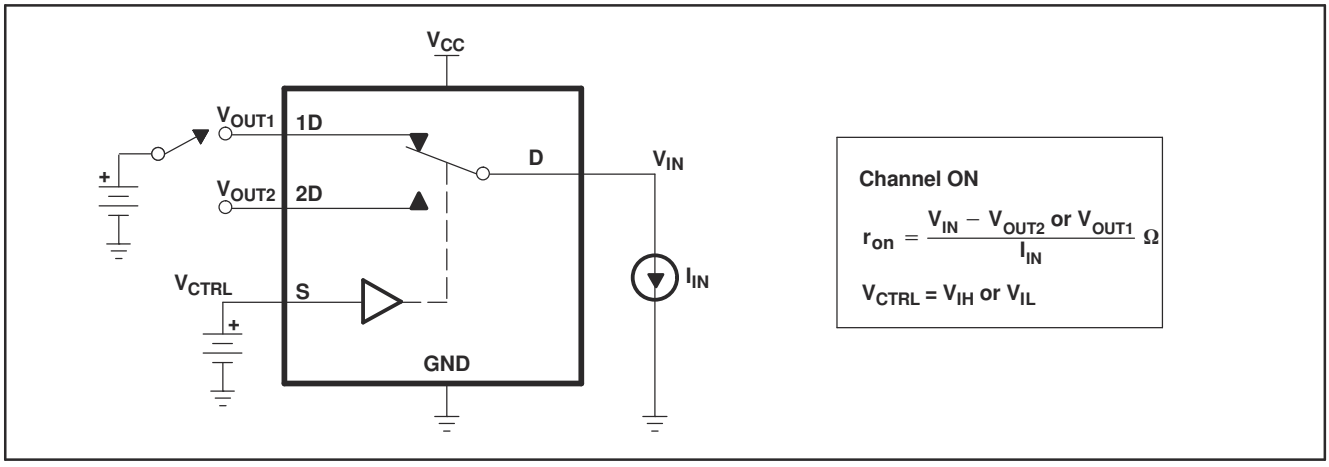


图 6-7. ON-State Resistance (r_{on})

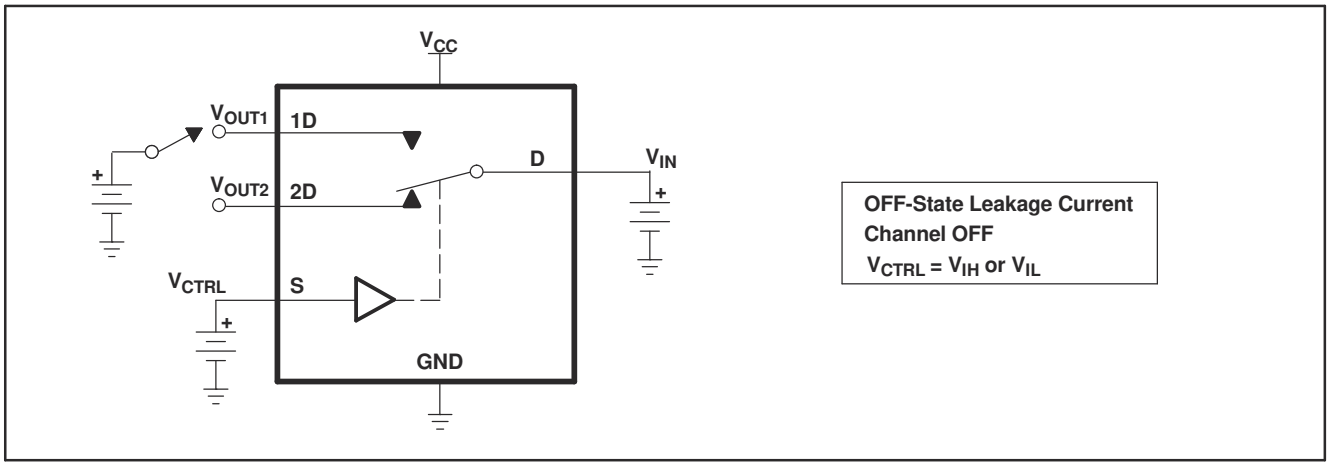


图 6-8. OFF-State Leakage Current

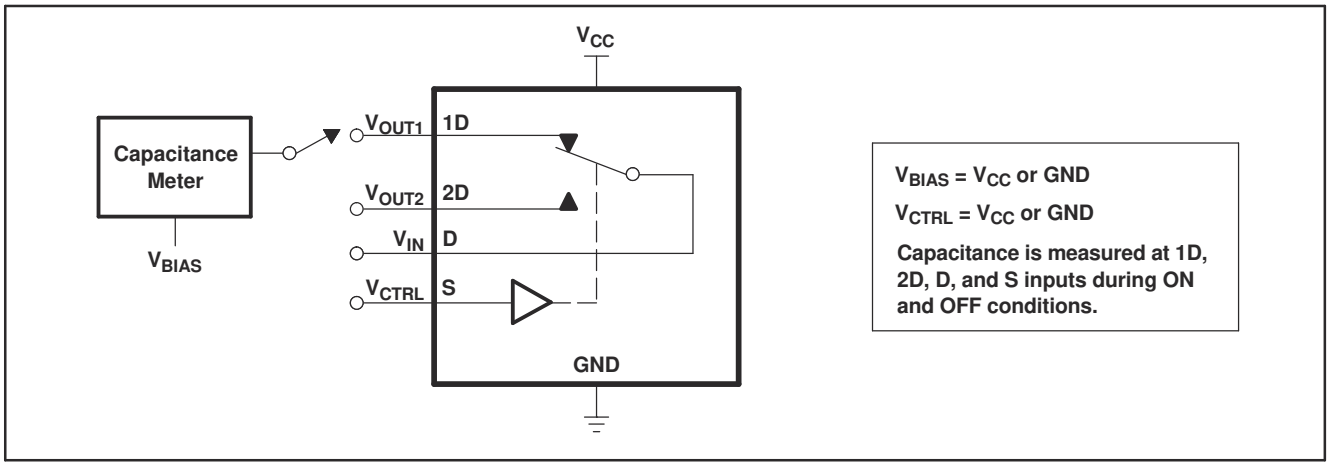


图 6-9. Capacitance

7 Detailed Description

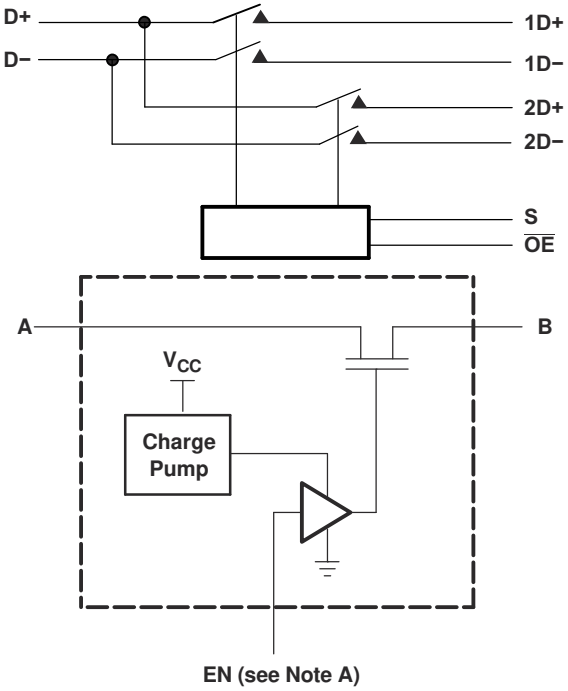
7.1 Overview

The TS3USB221A device is a 2-channel SPDT switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that can reduce the power consumption to 1 µA for portable applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480Mbps).

The TS3USB221A device integrates ESD protection cells on all pins, is available in a tiny µQFN package (2mm × 1.5mm) and is characterized over the free air temperature range from –40°C to 85°C.

7.2 Functional Block Diagram



A. EN is the internal enable signal applied to the switch.

图 7-1. Simplified Schematic of Each FET Switch (SW)

7.3 Feature Description

7.3.1 Low Power Mode

The TS3USB221A has a low power mode that reduces the power consumption to 1 μA while the devices is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{OE}$ must be supplied with a logic "High" signal.

7.4 Device Functional Modes

表 7-1. Truth Table

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB221A can effectively expand the limited USB I/Os by switching between multiple USB buses and interface with the buses on a single USB hub or controller.

8.2 Typical Application

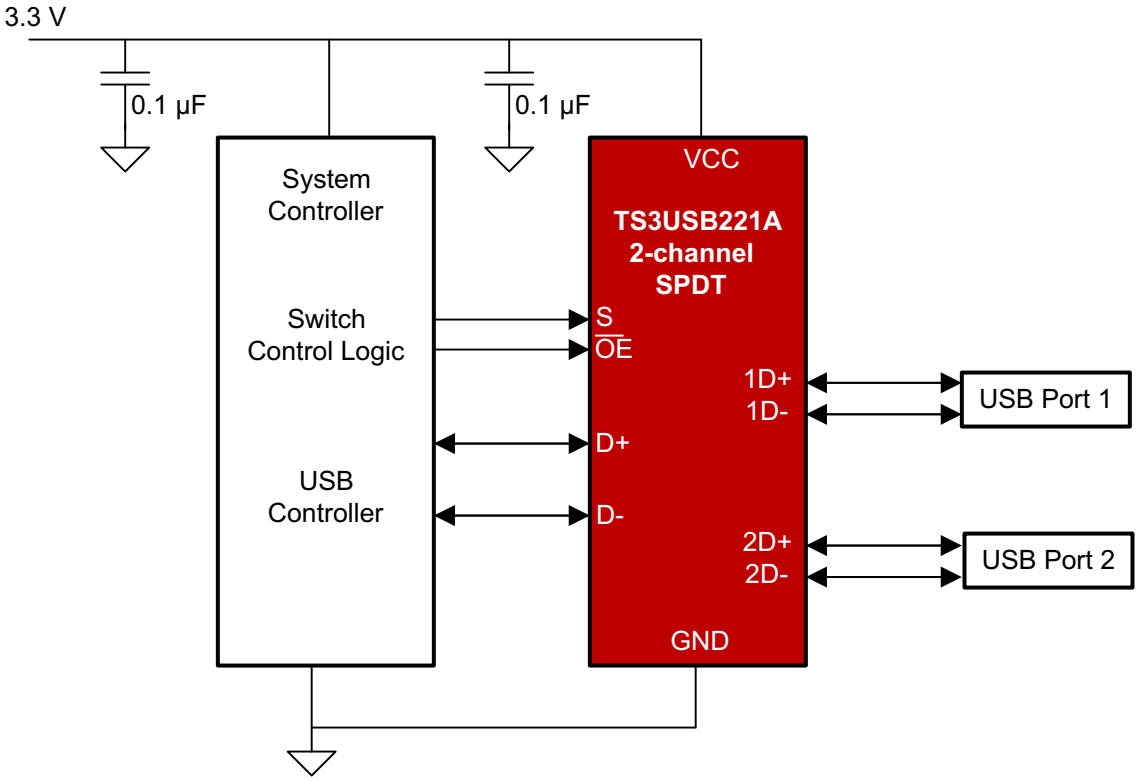


图 8-1. Application Schematic

8.2.1 Design Requirements

Follow the design requirements of the USB 1.0,1.1, and 2.0 standards.

TI recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that can result from the floating pin.

8.2.2 Detailed Design Procedure

The TS3USB221A can operate properly without any external components. However, TI recommends to connect unused pins to ground through a 50 Ω resistor to prevent signal reflections back into the device.

8.2.3 Application Curves

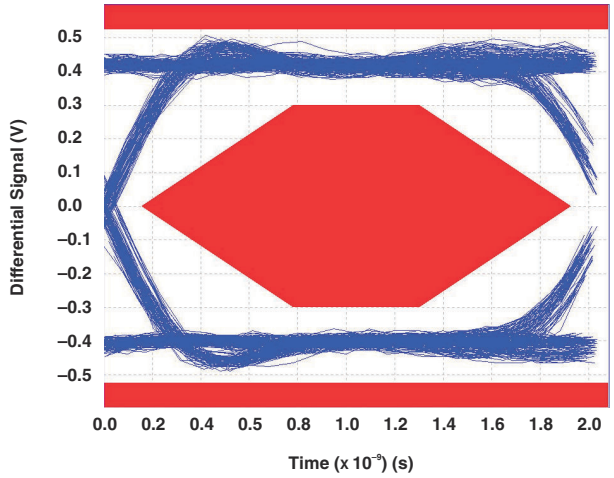


图 8-2. Eye Pattern: 480Mbps USB Signal With No Switch (Through Path)

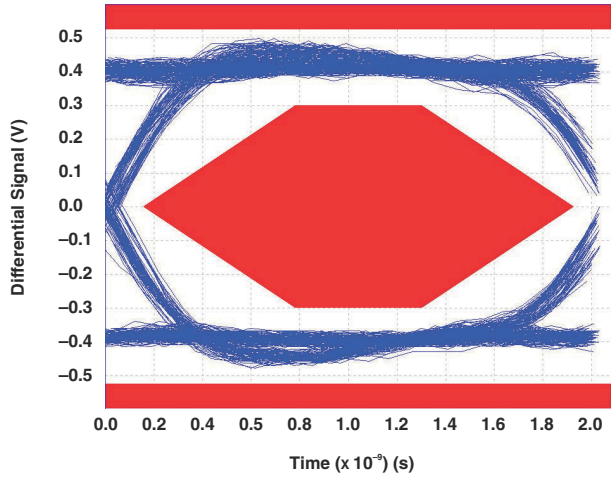


图 8-3. Eye Pattern: 480Mbps USB Signal With Switch NC Path

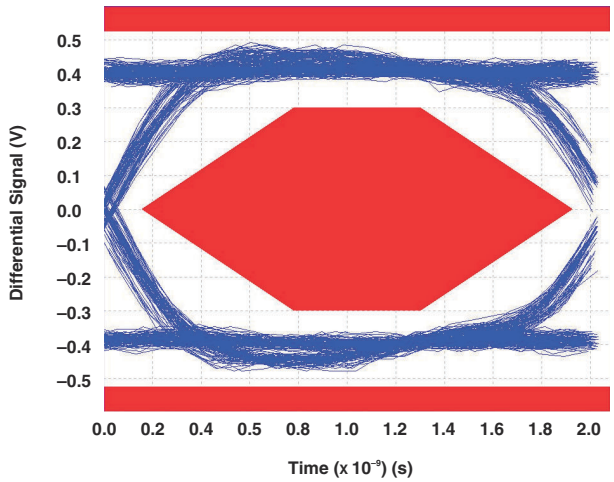


图 8-4. Eye Pattern: 480Mbps USB Signal With Switch NO Path

8.3 Power Supply Recommendations

Make sure the power to the device is supplied through the VCC pin and follows the USB 1.0, 1.1, and 2.0 standards. A bypass capacitor is recommended to be placed as close to the supply pin VCC to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

8.4 Layout

8.4.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D+/D – traces.

Make sure the high speed D+/D – trace lengths match and are no more than 4 inches; otherwise, the eye diagram performance can degrade. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, make sure the impedance of D+ and D – traces match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners to reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because stubs cause signal reflections. If a stub is unavoidable, keep the stub less than 200mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 图 8-5.

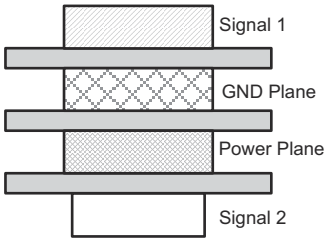


图 8-5. Four-Layer Board Stack-Up

Make sure the majority of signal traces run on a single layer, preferably Signal 1. Make sure the GND plane, which is solid with no cuts, is immediately next to this layer. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

8.4.2 Layout Example

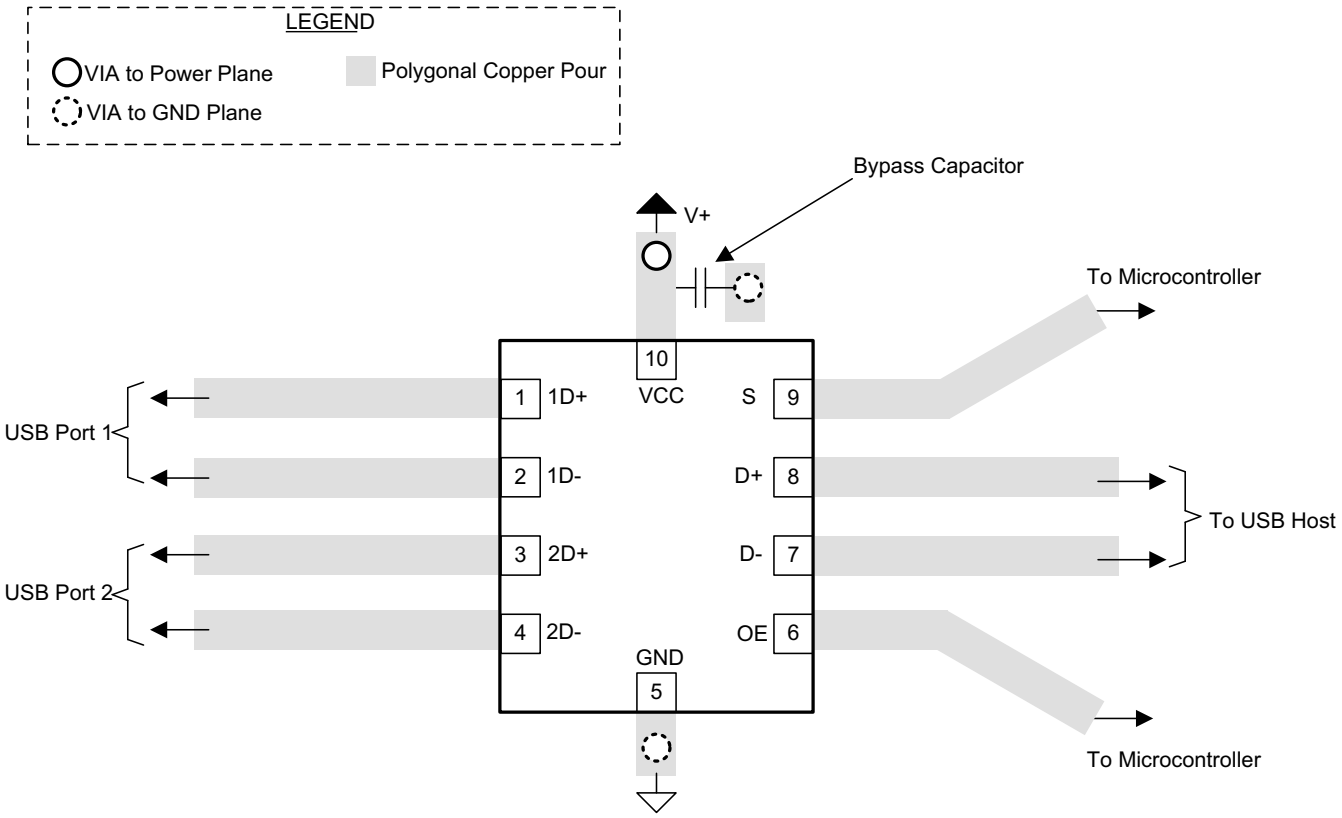


图 8-6. Package Layout Diagram

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

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9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (February 2015) to Revision B (July 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 更新了*特性* 部分中的 ESD 性能测试条件	1
• Changed CDM test conditions in the ESD Ratings table from: per JEDEC specification JESD22-C101 to: per ANSI/ESDA/JEDEC JS-002	4
• Added footnote to the $V_{I/O}$ parameter in the *Recommended Operating Conditions* table	4
• Changed RSE (UQFN) junction-to-ambient thermal resistance value from: 179.7°C/W to: 204.8°C/W	5
• Changed RSE (UQFN) junction-to-case (top) thermal resistance value from: 107.9°C/W to: 118.1°C/W	5
• Changed RSE (UQFN) junction-to-board thermal resistance value from: 100.7°C/W to: 121.5°C/W	5
• Changed RSE (UQFN) junction-to-top characterization parameter value from: 7.1°C/W to: 13.9°C/W	5
• Changed RSE (UQFN) junction-to-board characterization parameter value from: 100.0°C/W to: 121.2°C/W	5
• Changed the V_{IK} value in the *Electrical Characteristics* table from: –1.8V maximum to: –1.8V minimum	5
• Changed the *Typical Characteristics* section	7

Changes from Revision * (November 2008) to Revision A (February 2015)	Page
• 添加了“ESD 等级”表、“特性说明”部分、“器件功能模式”、“应用和实施”部分、“电源相关建议”部分、“布局”部分、“器件和文档支持”部分以及“机械、封装和可订购信息”部分	1
• 删除了数据表中的*订购信息* 表。如需了解订购信息，请参阅*机械、封装和可订购信息* 部分	1
• 将文档按全新 TI 数据表标准进行了更新	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB221ARSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LH7, LHH, LHO, LHR, LHV)	Samples
TS3USB221ARSERG4	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LH7, LHH, LHO, LHR, LHV)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TS3USB221A :

- Automotive : TS3USB221A-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

重要声明和免责声明

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