UCC2721x 120V 升压、4A 峰值电流的高频高侧/低侧驱动器

1 特性

- 可通过独立输入驱动两个采用高侧/低侧配置的 N 沟道金属氧化物半导体场效应晶体管 (MOSFET)
- 最大引导电压 120V 直流
- 4A 吸收，4A 源输出电流
- 0.9Ω 上拉和下拉电阻
- 输入引脚能够耐受 -10V 至 20V 的电压，并且与电源电压范围无关
- 晶体管-晶体管逻辑电路 (TTL) 或伪 CMOS 兼容输入版本
- 8V 至 17V VDD 运行范围（绝对最大值 20V）
- 7.2ns 上升时间和 5.5ns 下降时间（采用 1000pF 负载时）
- 短暂传播延迟时间（典型值 18ns)
- 2ns 延迟匹配
- 用于高侧和低侧驱动器的对称欠压锁定功能
- 可提供全部行业标准封装（小外形尺寸集成电路 (SOIC)-8 封装， PowerPAD™SOIC-8 封装，4mm × 4mm SON-8 封装以及 4mm × 4mm SON-10 封装）
- -40℃ 至 140℃ 的额定温度范围

2 应用

- 针对电信，数据通信和商用的电源
- 半桥和全桥转换器
- 推挽转换器
- 高电压同步降压转换器
- 两开关正激式转换器
- 有源箝位正激式转换器
- D 类音频放大器

3 说明

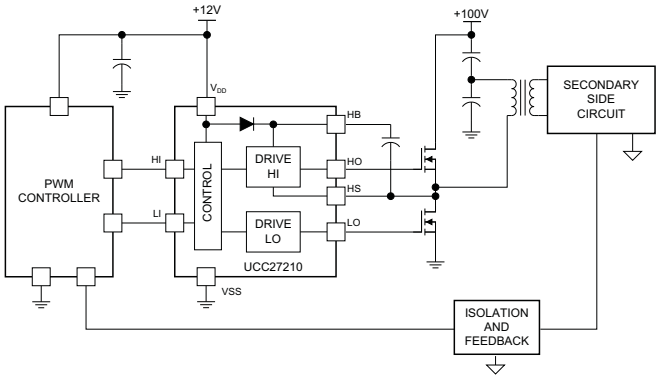
UCC27210 和 UCC27211 驱动器是基于广受欢迎的 UCC27200 和 UCC27201 MOSFET 驱动器，但性能得到了显著提升。峰值输出上拉和下拉电流已经被提高至 4A 拉电流和 4A 灌电流，并且上拉和下拉电阻已经被减小至 0.9Ω，因此可以在 MOSFET 的米勒效应平台转换期间用尽可能小的开关损耗来驱动大功率 MOSFET。现在，输入结构能够直接处理 -10 VDC，这提高了稳健耐用性，并且无需使用整流二极管即可实现与栅极驱动变压器的直接对接。这些输入与电源电压无关，并且具有 20V 的最大额定值。

器件信息(1)

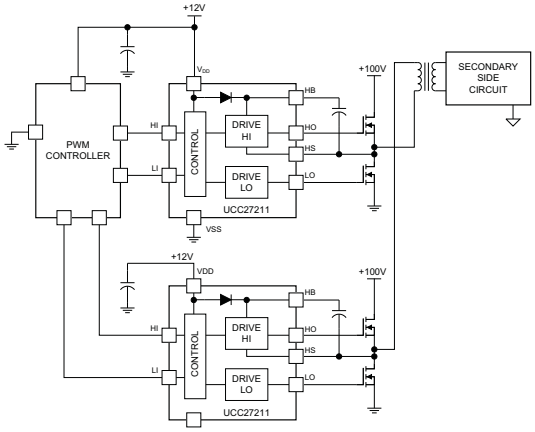
器件型号	封装	封装尺寸（标称值）
UCC27210、UCC27211	SOIC (8)	4.90mm x 3.91mm
	PowerPAD (8)	4.89mm × 3.90mm
	WSON (10)	4.00mm x 4.00mm
	VSON (8)	

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用：**UCC27210**



典型应用：**UCC27211**



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (August 2013) to Revision F **Page**

- 已添加 *引脚配置和功能*部分、*ESD 额定值*表、*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision D (November, 2012) to Revision E **Page**

- Added Note 2 to the Terminal Functions Table. ... 5
- Changed Repetitive pulse data from -18 V to -(24V-VDD). ... 5
- Added additional details to Note 2. ... 5
- Changed Voltage on HS, V_{HS} (repetitive pulse <100 ns) data from -15 to -(24V-VDD). ... 6
- 已删除 2.4-mA operating current min range in both places. ... 7
- 已更改 operating current max range extended to 5.2 in both places. ... 7
- 已删除 1.5 min Boot voltage operating current range. ... 7
- 已更改 Boot voltage operating current max range from 4.2 to 5.0. ... 7
- 已更改 HB to V_{SS} operating current max range from 1.1 to 1.2. ... 7
- 已更改 LO Gate Driver's Low-level output voltage max range from 0.17 to 0.19. ... 7
- 已更改 HO GATE Driver's Low-level output voltage max range from 0.17 to 0.19. ... 7

Changes from Revision C (March, 2012) to Revision D **Page**

- Changed capacitor range from 1.0 µF to 4.7 µF. ... 5
- Added Terminal Functions Note to HI and LI pin description. ... 5
- 已更改 bullet 2 in the Layout Recommendations. ... 21
- 已添加 Note: For systems using... ... 21
- 已添加 Note: Care should be taken... ... 21

Changes from Revision B (February) to Revision C **Page**

5 说明 （续）

UCC2721x 的开关节点（HS 引脚）最高可处理 -18V 电压，从而保护高侧通道不受寄生电感和杂散电容所固有的负电压影响。UCC27210（伪 CMOS 输入）和 UCC27211（TTL 输入）已经增加了滞后特性，从而使得到模拟或数字脉宽调制 (PWM) 控制器接口的抗扰度得到了增强。

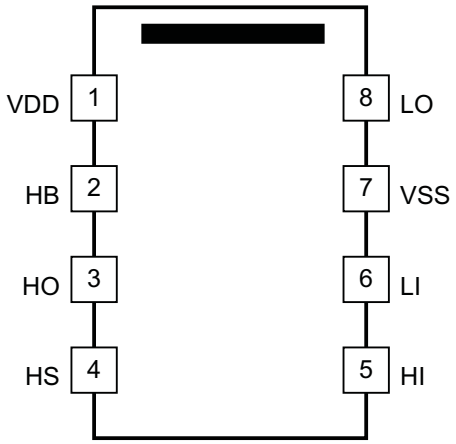
低侧和高侧栅极驱动器是独立控制的，并在彼此的接通和关断之间实现了 2ns 的延迟匹配。

由于在芯片上集成了一个额定电压为 120V 的自举二极管，因此无需采用外部分立式二极管。高侧和低侧驱动器均配有欠压锁定功能，可提供对称的导通和关断行为，并且能够在驱动电压低于指定阈值时将输出强制为低电平。

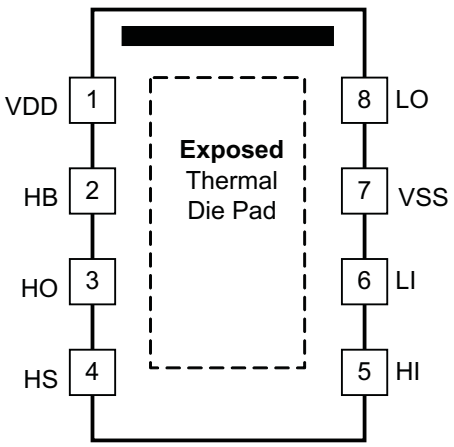
两款器件均提供 8 引脚 SOIC (D)、PowerPAD SOIC-8 (DDA)、4mm × 4mm SON-8 (DRM) 和 SON-10 (DPR) 封装。

6 Pin Configuration and Functions

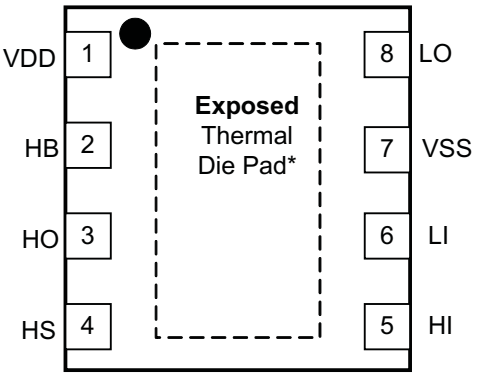
SOIC-8 (D)
TOP VIEW



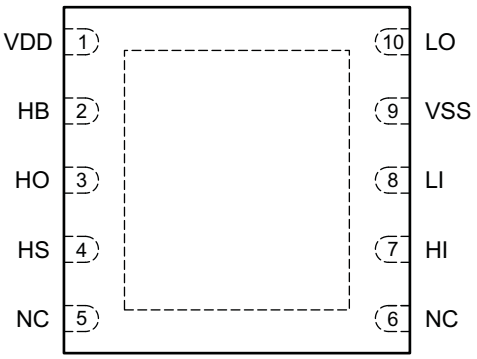
Power Pad™ SOIC-8 (DDA)
TOP VIEW



SON-8 (DRM)
TOP VIEW



SON-10 (DPR)
TOP VIEW



Pin Functions

PIN			I/O	DESCRIPTION
NAME	D/DDA/DRM	DPR		
VDD	1	1	P	Positive supply to the lower-gate driver. Decouple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22 µF to 4.7 µF (See (1)).
HB	2	2	P	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF. The capacitor value is dependant on the gate charge of the high-side MOSFET and should also be selected based on speed and ripple criteria
HO	3	3	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	4	P	High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin.
HI	5	7	I	High-side input.(2)
LI	6	8	I	Low-side input.(2)
VSS	7	9	G	Negative supply terminal for the device which is generally grounded.
LO	8	10	O	Low-side output. Connect to the gate of the low-side power MOSFET.
N/C	—	5/6	—	Not connected.
PowerPAD™ (3)	Pad	Pad	G	Used on the DDA, DRM and DPR packages only. Electrically referenced to V_{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) For cold temperature applications we recommend the upper capacitance range. Attention should also be made to PCB layout - see Layout.
(2) HI or LI input is assumed to connect to a low impedance source signal. The source output impedance is assumed less than 100 Ω. If the source impedance is greater than 100 Ω, add a bypassing capacitor, each, between HI and VSS and between LI and VSS. The added capacitor value depends on the noise levels presented on the pins, typically from 1 nF to 10 nF should be effective to eliminate the possible noise effect. When noise is present on two pins, HI or LI, the effect is to cause HO and LO malfunctions to have wrong logic outputs.
(3) The PowerPAD™ is not directly connected to any leads of the package. However it is electrically and thermally connected to the substrate which is the ground of the device.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range, V_{DD}(2), V_{HB} - V_{HS}		–0.3	20	V
Input voltages on LI and HI, V_{LI}, V_{HI}		–10	20	
Output voltage on LO, V_{LO}	DC	–0.3	V_{DD} + 0.3	
	Repetitive pulse <100 ns(3)	–2	V_{DD} + 0.3	
Output voltage on HO, V_{HO}	DC	V_{HS} – 0.3	V_{HB} + 0.3	
	Repetitive pulse <100 ns(3)	V_{HS} – 2	V_{HB} + 0.3	
Voltage on HS, V_{HS}	DC	–1	115	
	Repetitive pulse <100 ns(3)	–(24 V-VDD)	115	
Voltage on HB, V_{HB}		–0.3	120	
Operating virtual junction temperature, T_J		–40	150	°C
Lead temperature (soldering, 10 sec.)			300	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to VSS unless otherwise noted. Currents are positive into, negative out of the specified terminal.
(3) Verified at bench characterization. VDD is the value used in an application design.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

all voltages are with respect to V_{SS}; currents are positive into and negative out of the specified terminal. –40°C < T_J = T_A < 140°C (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, V_{DD}, V_{HB}-V_{HS}	8	12	17	V
Voltage on HS, V_{HS}	–1		105	
Voltage on HS, V_{HS} (repetitive pulse <100 ns)	–(24V-VDD)		110	
Voltage on HB, V_{HB}	V_{HS} +8, V_{DD} –1		V_{HS} +17, 115	
Voltage slew rate on HS			50	V/ns
Operating junction temperature range	–40		140	°C

7.4 Thermal Information

THERMAL METRIC		UCC27210, UCC27211				UNIT
		D	DDA	DRM	DPR	
		8 PINS	8 PINS	8 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance (1)	111.8	37.7	33.9	36.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (2)	56.9	47.2	33.2	36.0	
θ_{JB}	Junction-to-board thermal resistance (3)	53.0	9.6	11.4	14.0	
ψ_{JT}	Junction-to-top characterization parameter (4)	7.8	2.8	0.4	0.3	
ψ_{JB}	Junction-to-board characterization parameter (5)	52.3	9.4	11.7	14.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (6)	n/a	3.6	2.3	3.4	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, no load on LO or HO, T_A = T_J = –40°C to 140°C, (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I_{DD}	V_{DD} quiescent current		V(LI) = V(HI) = 0 V	0.05	0.085	0.17	mA
I_{DDO}	V_{DD} operating current	UCC27210	f = 500 kHz, C_{LOAD} = 0		2.6	5.2	mA
		UCC27211			2.5	5.2	
I_{HB}	Boot voltage quiescent current		V(LI) = V(HI) = 0 V	0.015	0.065	0.1	mA
I_{HBO}	Boot voltage operating current		f = 500 kHz, C_{LOAD} = 0		2.5	5.0	mA
I_{HBS}	HB to V_{SS} quiescent current		V(HS) = V(HB) = 115 V		0.0005	1.0	µA
I_{HBSO}	HB to V_{SS} operating current		f = 500 kHz, C_{LOAD} = 0		0.07	1.2	mA
INPUT							
V_{HIT}	Input voltage threshold		UCC27210	4.2	5.0	5.8	V
			UCC27210 (DDA only)	4.2	5.0	5.9	
V_{LIT}	Input voltage threshold		UCC27210	2.4	3.2	4.0	
			UCC27210 (DDA only)	2.4	3.2	4.0	
V_{IHYS}	Input voltage hysteresis		UCC27210		1.8		
R_{IN}	Input pulldown resistance				102		kΩ
V_{HIT}	Input voltage threshold		UCC27211	1.9	2.3	2.7	V
			UCC27211 (DDA only)	1.9	2.3	2.8	
V_{LIT}	Input voltage threshold		UCC27211	1.3	1.6	1.9	
			UCC27211 (DDA only)	1.3	1.6	2.1	
V_{IHYS}	Input voltage hysteresis		UCC27211		700		mV
R_{IN}	Input pulldown resistance				68		kΩ
UNDERVOLTAGE LOCKOUT (UVLO)							
V_{DDR}	V_{DD} turnon threshold			6.2	7.0	7.8	V
			DDA only	5.8	7.0	8.1	
V_{DDHYS}	Hysteresis				0.5		
V_{HBR}	V_{HB} turnon threshold			5.6	6.7	7.9	
			DDA only	5.3	6.7	8.0	
V_{HBHYS}	Hysteresis				1.1		
BOOTSTRAP DIODE							
V_F	Low-current forward voltage		I_{VDD-HB} = 100 µA		0.65	0.8	V
V_{FI}	High-current forward voltage		I_{VDD-HB} = 100 mA		0.85	0.95	
R_D	Dynamic resistance, ΔVF/ΔI		I_{VDD-HB} = 100 mA and 80 mA	0.3	0.5	0.85	Ω
LO GATE DRIVER							
V_{LOL}	Low-level output voltage		I_{LO} = 100 mA	0.05	0.09	0.19	V
V_{LOH}	High level output voltage		I_{LO} = -100 mA, V_{LOH} = V_{DD} - V_{LO}	0.1	0.16	0.29	
	Peak pull-up current(1)		V_{LO} = 0 V		3.7		A
	Peak pull-down current(1)		V_{LO} = 12 V		4.5		
HO GATE DRIVER							
V_{HOL}	Low-level output voltage		I_{HO} = 100 mA	0.05	0.09	0.19	V
V_{HOH}	High-level output voltage		I_{HO} = -100 mA, V_{HOH} = V_{HB} - V_{HO}	0.1	0.16	0.29	
	Peak pull-up current(1)		V_{HO} = 0 V		3.7		A
	Peak pull-down current(1)		V_{HO} = 12 V		4.5		

(1) Ensured by design.

7.6 Switching Characteristics: Propagation Delays

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{DLFF}	V_{LI} falling to V_{LO} falling	UCC27210, C_{LOAD} = 0	15	21	37	ns
T_{DHFF}	V_{HI} falling to V_{HO} falling		15	21	37	
T_{DLRR}	V_{LI} rising to V_{LO} rising		15	24	46	
T_{DHRR}	V_{HI} rising to V_{HO} rising		15	24	46	
T_{DLFF}	V_{LI} falling to V_{LO} falling	UCC27211, C_{LOAD} = 0	10	17	30	
T_{DHFF}	V_{HI} falling to V_{HO} falling		10	17	30	
T_{DLRR}	V_{LI} rising to V_{LO} rising		10	18	40	
T_{DHRR}	V_{HI} rising to V_{HO} rising		10	18	40	

7.7 Switching Characteristics: Delay Matching

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MON}	From HO OFF to LO ON	UCC27210	T_J = 25°C		3	11	ns
			T_J = –40°C to 140°C		3	14	
T_{MOFF}	From LO OFF to HO ON		T_J = 25°C		3	11	ns
			T_J = –40°C to 140°C		3	14	
T_{MON}	From HO OFF to LO ON	UCC27211	T_J = 25°C		2	9.5	ns
			T_J = –40°C to 140°C		2	14	
T_{MOFF}	From LO OFF to HO ON		T_J = 25°C		2	9.5	ns
			T_J = –40°C to 140°C		2	14	

7.8 Switching Characteristics: Output Rise and Fall Time

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	LO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		7.2		ns
t_R	HO rise time			7.2		
t_F	LO fall time	C_{LOAD} = 1000 pF, from 90% to 10%		5.5		
t_F	HO fall time			5.5		
t_R	LO, HO	C_{LOAD} = 0.1 µF, (3 V to 9 V)		0.36	0.6	µs
t_F	LO, HO	C_{LOAD} = 0.1 µF, (9 V to 3 V)		0.15	0.4	

7.9 Switching Characteristics: Miscellaneous

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Minimum input pulse width that changes the output				50	ns
	Bootstrap diode turnoff time(1)(2)	I_F = 20 mA, I_{REV} = 0.5 A(3)		20		

(1) Ensured by design.
(2) I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.
(3) Typical values for T_A = 25°C.

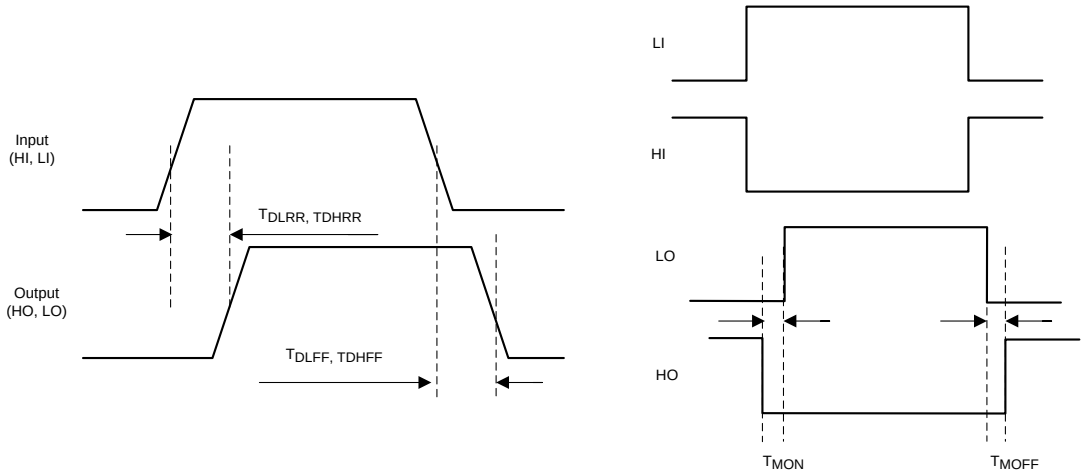


图 1. Timing Diagrams

7.10 Typical Characteristics

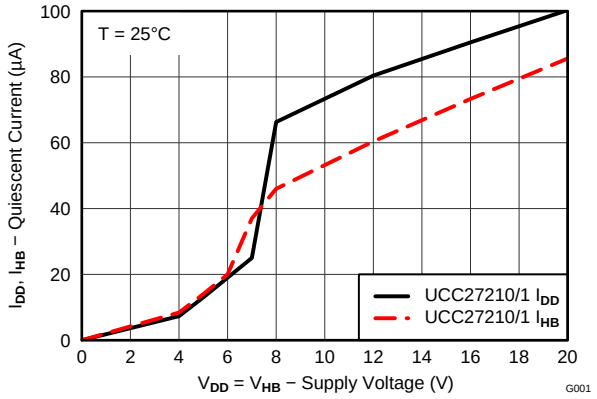


图 2. Quiescent Current vs Supply Voltage

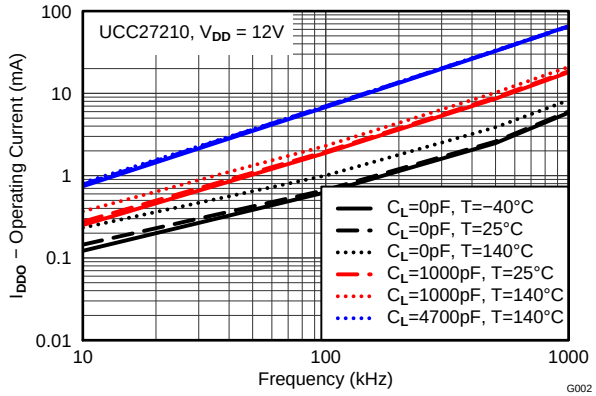


图 3. UCC27210 IDD Operating Current vs Frequency

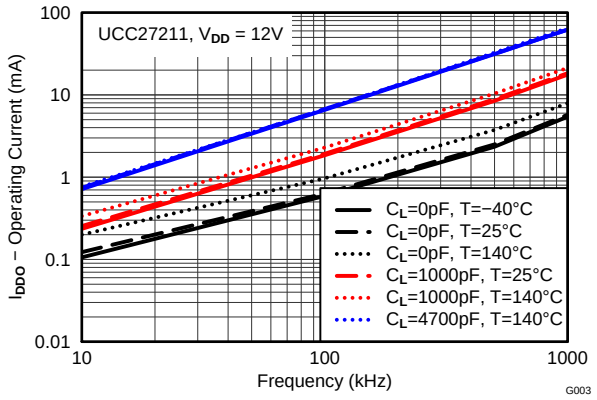


图 4. UCC27211 IDD Operating Current vs Frequency

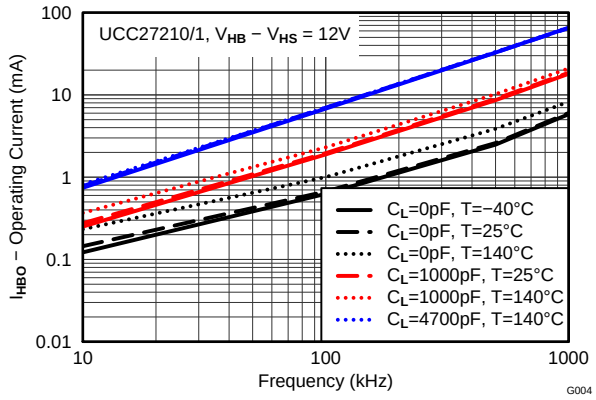


图 5. Boot Voltage Operating Current vs Frequency (HB to HS)

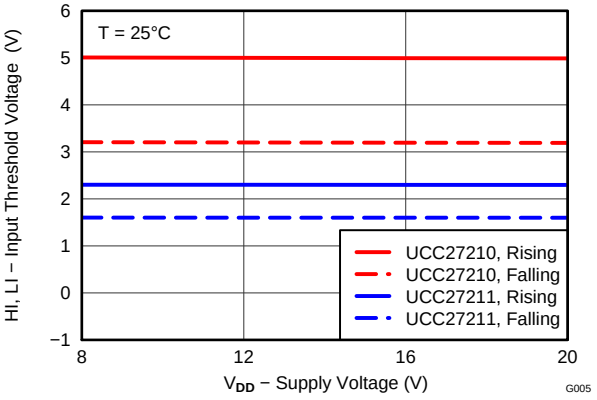


图 6. UCC27210 and UCC27211 Input Threshold vs Supply Voltage

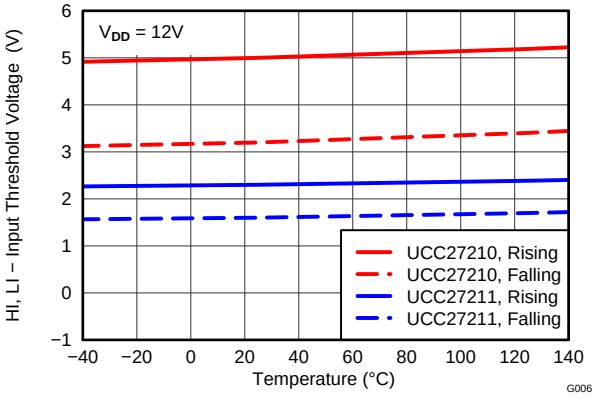


图 7. UCC27210 and UCC27211 Input Thresholds vs Temperature

Typical Characteristics (接下页)

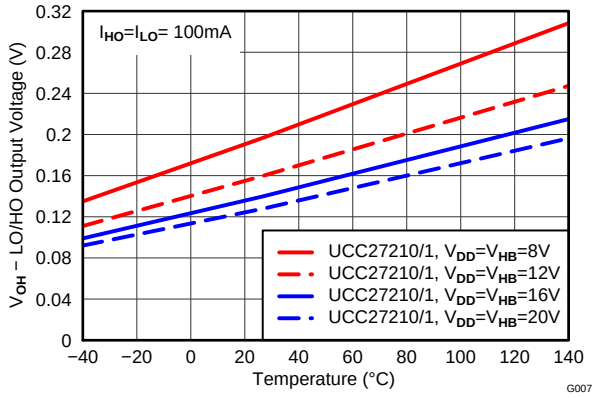


图 8. LO and HO High Level Output Voltage vs Temperature

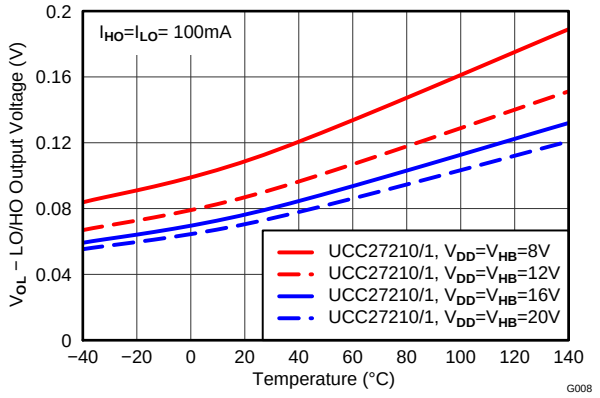


图 9. LO and HO Low Level Output Voltage vs Temperature

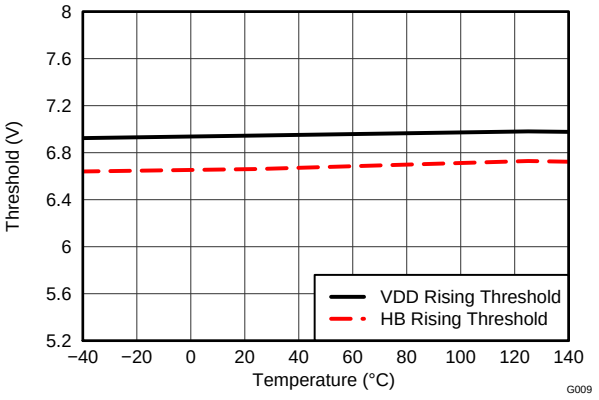


图 10. Undervoltage Lockout Threshold vs Temperature

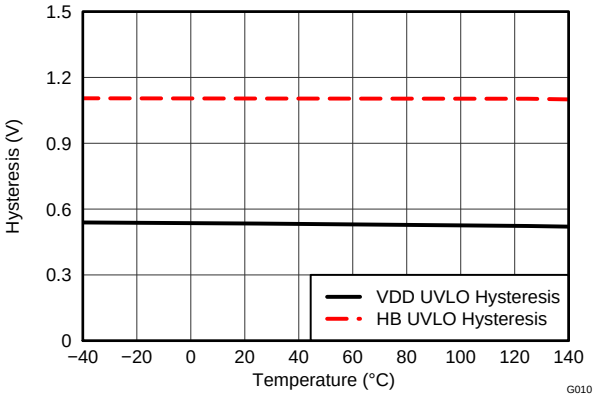


图 11. Undervoltage Lockout Threshold Hysteresis vs Temperature

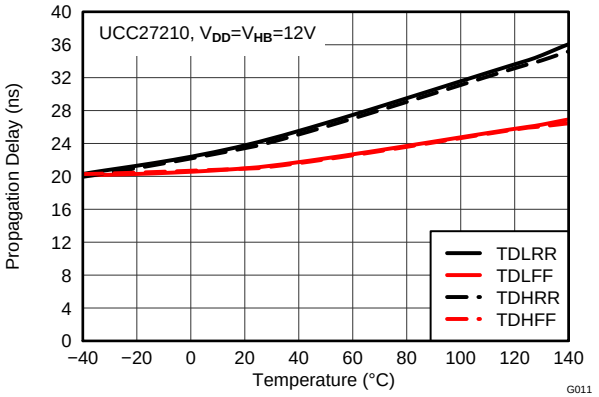


图 12. UCC27210 Propagation Delays vs Temperature

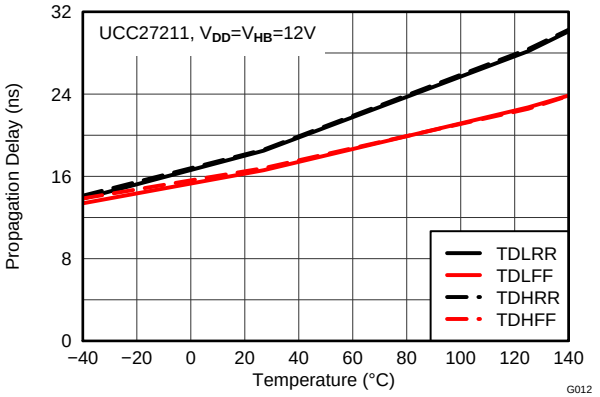


图 13. UCC27211 Propagation Delays vs Temperature

Typical Characteristics (接下页)

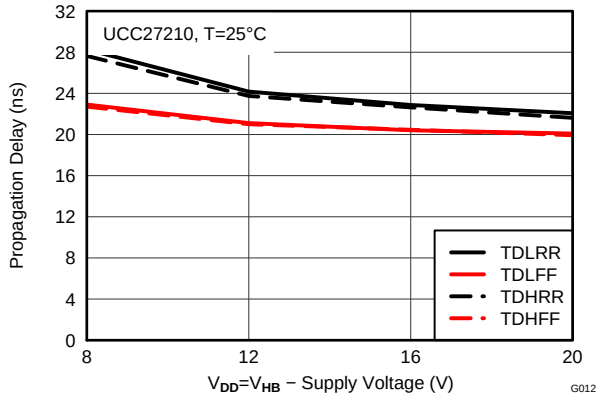


图 14. UCC27210 Propagation Delays vs Supply Voltage

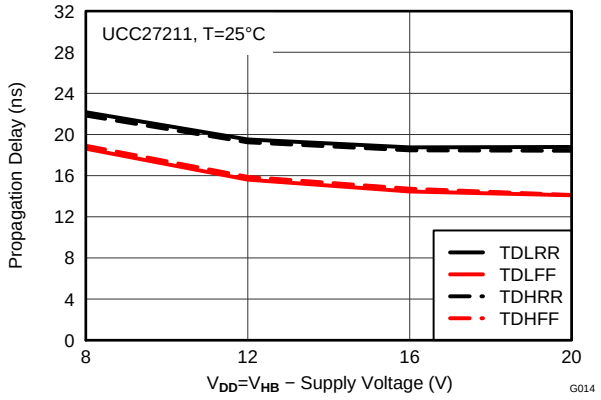


图 15. UCC27211 Propagation Delays vs Supply Voltage

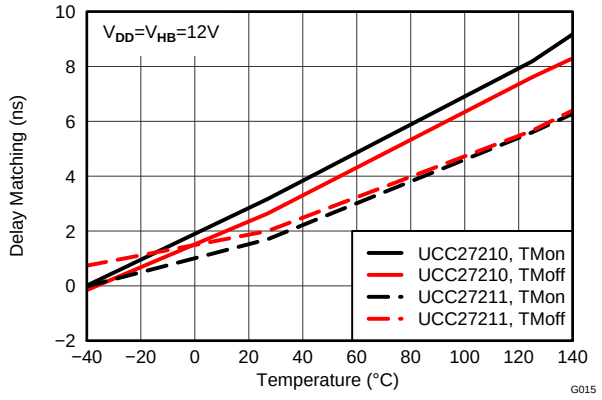


图 16. Delay Matching vs Temperature

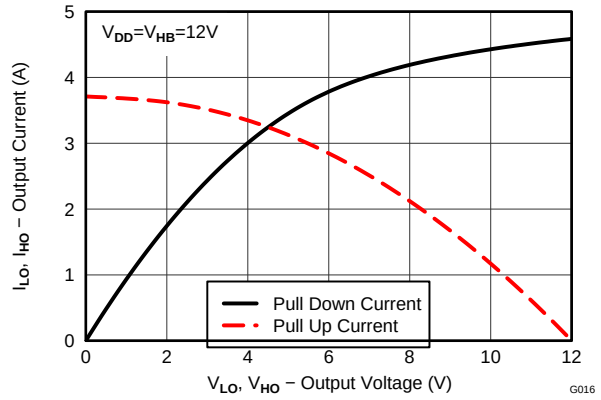


图 17. Output Current vs Output Voltage

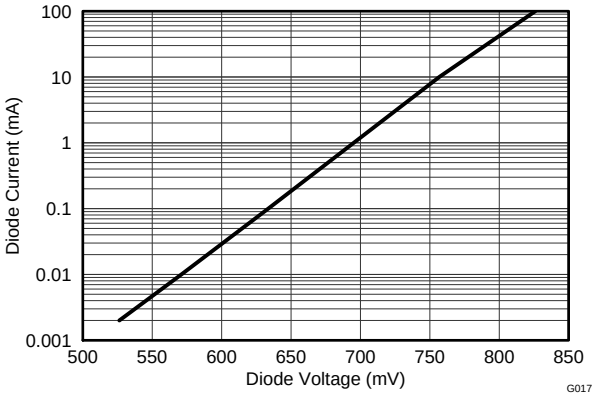


图 18. Diode Current vs Diode Voltage

8 Detailed Description

8.1 Overview

The UCC27210 and UCC27211 devices represent Texas Instruments' latest generation of high voltage gate drivers which are designed to drive both the high side and low side of N-channel MOSFETs in a half-/full-bridge or synchronous buck configuration. The floating high-side driver can operate with supply voltages of up to 120 V. This allows for N-channel MOSFET control in half-bridge, full-bridge, push pull, two-switch forward and active clamp forward converters.

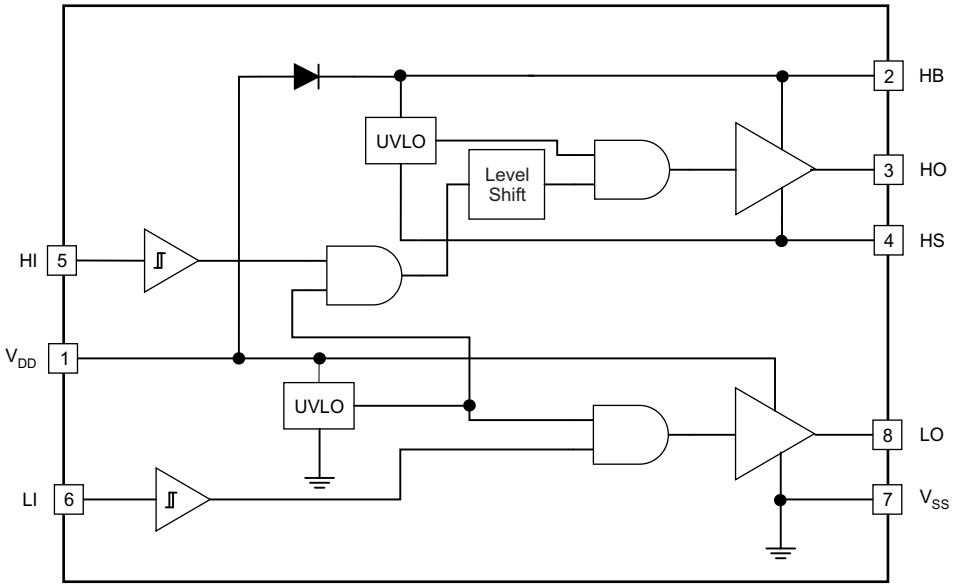
The UCC27210 and UCC27211 devices feature 4-A source/sink capability, industry best-in-class switching characteristics and a host of other features listed in 表 1. These features combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

表 1. UCC27210 and UCC27211 Highlights

FEATURE	BENEFIT
4-A source and sink current with 0.9-Ω output resistance	High peak current ideal for driving large power MOSFETs with minimal power loss (fast-drive capability at Miller plateau)
Input pins (HI and LI) can directly handle –10 VDC up to 20 VDC	Increased robustness and ability to handle under/overshoot. Can interface directly to gate-drive transformers without having to use rectification diodes
120-V internal boot diode	Provides voltage margin to meet telecom 100-V surge requirements
Switch node (HS pin) able to handle –18 V maximum for 100 ns	Allows the high-side channel to have extra protection from inherent negative voltages caused parasitic inductance and stray capacitance.
Robust ESD circuitry to handle voltage spikes	Excellent immunity to large dV/dT conditions
18-ns propagation delay with 7.2-ns / 5.5-ns rise/fall Times	Best-in-class switching characteristics and extremely low-pulse transmission distortion
2-ns (typ) delay matching between channels	Avoids transformer volt-second offset in bridge
Symmetrical UVLO circuit	Ensures high-side and low-side shut down at the same time
CMOS optimized threshold or TTL optimized thresholds with increased hysteresis	Complementary to analog or digital PWM controllers. Increased hysteresis offers added noise immunity

In the UCC27210 and UCC27211 devices, the high side and low side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27210 and UCC27211. The UCC27210 is the Pseudo-CMOS compatible input version and the UCC27211 is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS} which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27210 is 100 kΩ nominal and input capacitance is approximately 2 pF. The 100 kΩ is a pull-down resistance to V_{SS} (ground). The UCC27210 Pseudo-CMOS input structure has been designed to provide large hysteresis and at the same time to allows interfacing to a multitude of analog or digital PWM controllers. In some CMOS designs, the input thresholds are determined as a percentage of VDD. By doing so, the high-level input threshold can become unreasonably high and unusable. The UCC27210 recognizes the fact that VDD levels are trending downward and it therefore provides a rising threshold with 5.0 V (typical) and falling threshold with 3.2 V (typical). The input hysteresis of the UCC27210 is 1.8 V (typical).

The input stages of the UCC27211 have impedance of 70 kΩ nominal and input capacitance is approximately 2 pF. Pull-down resistance to V_{SS} (ground) is 70 kΩ. The logic level compatible input provides a rising threshold of 2.3 V and a falling threshold of 1.6 V.

8.3.2 Undervoltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. V_{DD} as well as V_{HB} to V_{HS} differential voltages are monitored. The V_{DD} UVLO disables both drivers when V_{DD} is below the specified threshold. The rising V_{DD} threshold is 7.0 V with 0.5-V hysteresis. The VHB UVLO disables only the high-side driver when the V_{HB} to V_{HS} differential voltage is below the specified threshold. The V_{HB} UVLO rising threshold is 6.7 V with 1.1-V hysteresis.

8.3.3 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

Feature Description (接下页)

8.3.4 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27210 and UCC27211 family of drivers. The diode anode is connected to V_{DD} and cathode connected to V_{HB}. With the V_{HB} capacitor connected to HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

8.3.5 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from V_{DD} to V_{SS} and the high side is referenced from V_{HB} to V_{HS}.

8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *Undervoltage Lockout (UVLO)* section for information on UVLO operation mode. In the normal mode the output state is dependent on states of the HI and LI pins. 表 2 lists the output states for different input pin combinations.

表 2. Device Logic Table

HI Pin	LI Pin	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.
(2) LO is measured with respect to VSS.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power, combining benefits of high-performance, low-cost component count and board-space reduction as well as simplified system design.

9.2 Typical Application

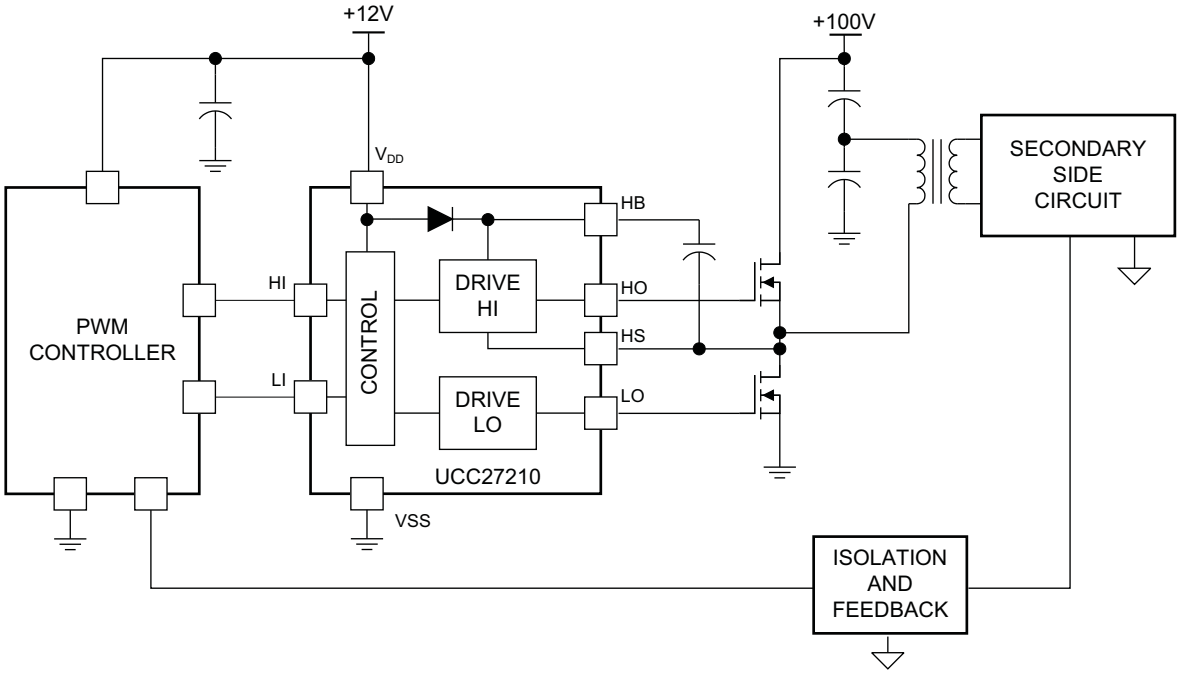


图 19. Typical Application Diagram: UCC27210

Typical Application (接下页)

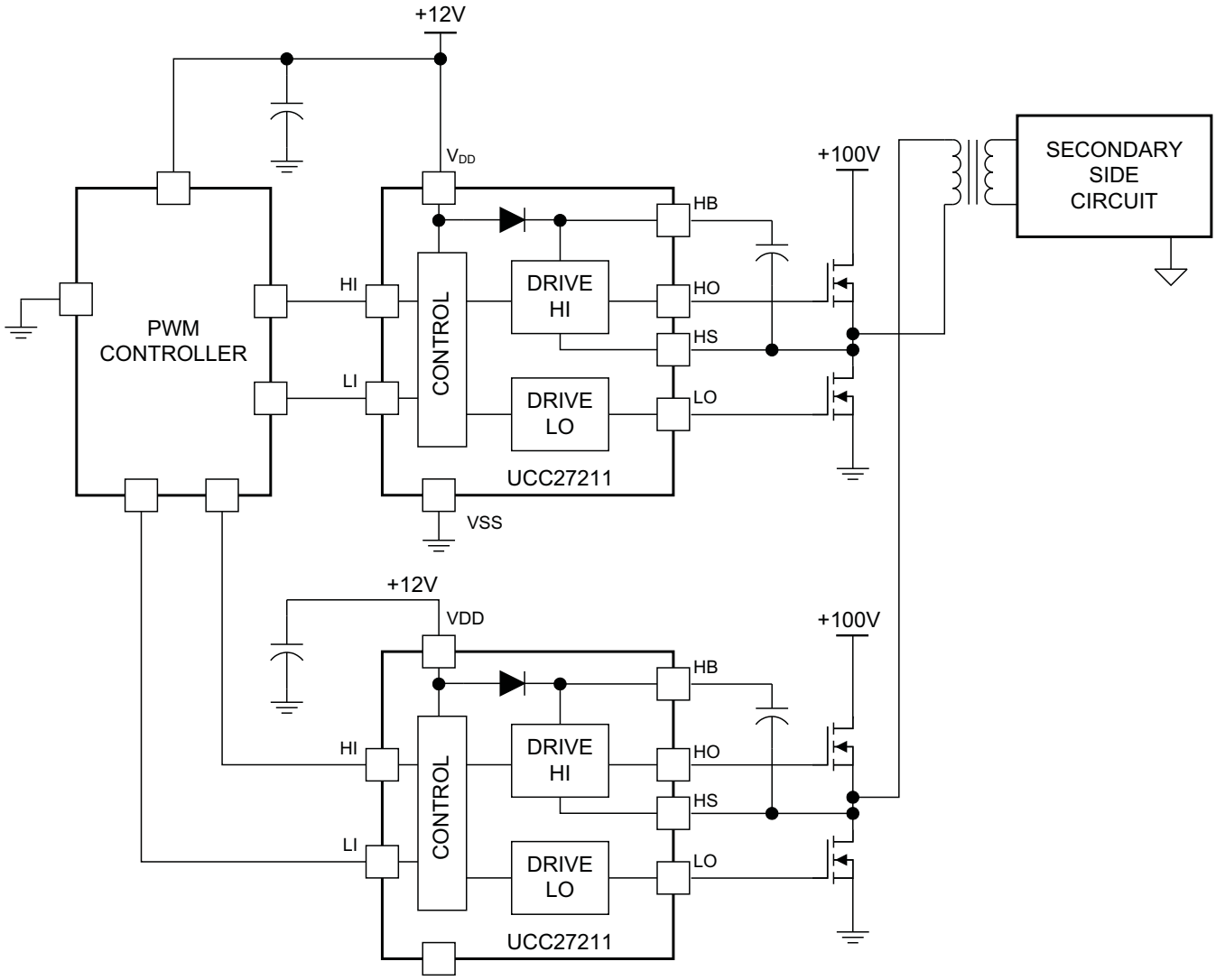


图 20. Typical Application Diagram: UCC27211

9.2.1 Design Requirements

表 3. Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, VDD	12 V
Voltage on HS, VHS	0 V to 100 V
Voltage on HB, VHB	12 V to 112 V
Output current rating, IO	–4 A to 4 A
Operating frequency	500 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Input Threshold Type

The UCC27210 and UCC27211 have an input maximum voltage range from –10 V to 20 V. This increased robustness means that both parts can be directly interfaced to gate drive transformers. The UCC27210 features pseudo CMOS compatible inputs and UCC27211 features TTL compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the *Electrical Characteristics* table for the actual input threshold voltage levels and hysteresis specifications for the UCC27210 and UCC27211 devices.

9.2.2.2 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the *Recommended Operating Conditions* table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 8 V to 17 V, the UCC27210 and UCC27211 devices can be used to drive a variety of power switches, such as Si MOSFETs, IGBTs, and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

9.2.2.3 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20V/ns or higher with a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 data sheet is 33 nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$.

To achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the Q_{GD} charge in 20 ns or less. In other words a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC27210 and UCC27211 gate driver is capable of providing 4-A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 2.4x overdrive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ $\times I_{PEAK}$ × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

9.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27210 features 21 ns and the UCC27211 features 17 ns (typical) propagation delays which ensures very little pulse distortion and allows operation at very high-frequencies. See the *Electrical Characteristics* table for the propagation and switching characteristics of the UCC27210 and UCC27211 devices.

9.2.2.5 Power Dissipation

Power dissipation of the gate driver has two portions as shown in 公式 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is PDC = I_Q x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27210 and UCC27211 features very low quiescent currents (less than 0.17 mA, refer to the *Electrical Characteristics* table and contain internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage VG, which is very close to input bias supply voltage VDD)
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by 公式 2.

$$EG = \tfrac{1}{2} C_{LOAD} V_{DD}^2 f_{SW}$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver (2)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by 公式 3.

$$PG = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when charging a capacitor which is calculated using the equation $Q_G = C_{LOAD}$ x V_{DD} to provide 公式 4 for power.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_G V_{DD} f_{SW} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

9.2.3 Application Curves

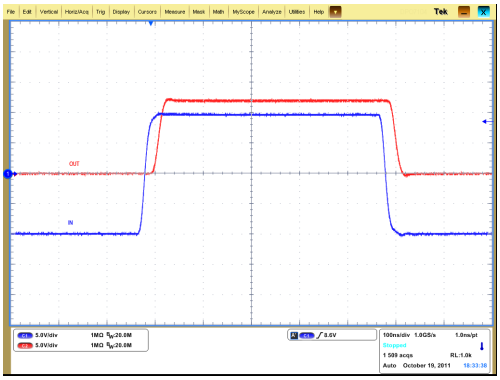


图 21. Negative 10-V Input

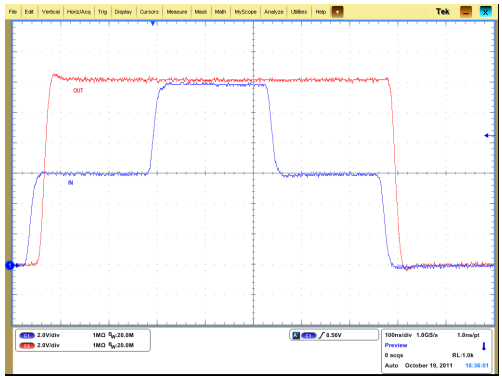


图 22. Step Input

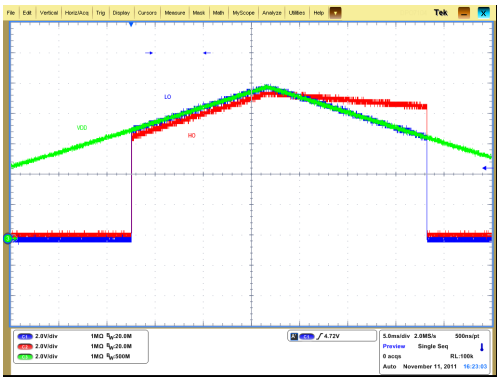


图 23. Symmetrical UVLO

10 Power Supply Recommendations

The bias supply voltage range for which the UCC27210 and UCC27211 device is rated to operate is from 8 V to 17 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 17 V. The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$.Therefore, ensuring that, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the V_{DD} pin voltage has exceeded above the $V_{(ON)}$ threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the HO pin is also supplied through the same V_{DD} pin is important. As a result, every time a current is sourced out of the HO pin a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus ensuring that a local bypass capacitor is provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends using a capacitor in the range 0.22 uF to 4.7 uF between V_{DD} and GND. In a similar manner, the current pulses delivered by the LO pin are sourced from the HB pin. Therefore a 0.022-uF to 0.1-uF local decoupling capacitor is recommended between the HB and HS pins.

11 Layout

11.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD}-V_{SS} and V_{HB}-V_{HS} (bootstrap) capacitors as close as possible to the device (see *图 24*).
- Pay close attention to the GND trace. Use the thermal pad of the DDA and DRM package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.
- Use similar rules for the HS node as for GND for the high-side driver.
- For systems using multiple UCC27210 and UCC27211 devices we recommend that dedicated decoupling capacitors be located at V_{DD}-V_{SS} for each device.
- Care should be taken to avoid VDD traces being close to LO, HS, and HO signals.
- Use wide traces for LO and HO closely following the associated GND or HS traces. 60 to 100-mils width is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node must be routed from one layer to another. For GND the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid LI and HI (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

Keep in mind that a poor layout can cause a significant drop in efficiency or system malfunction versus a good PCB layout and can even lead to decreased reliability of the whole system.

11.2 Layout Example

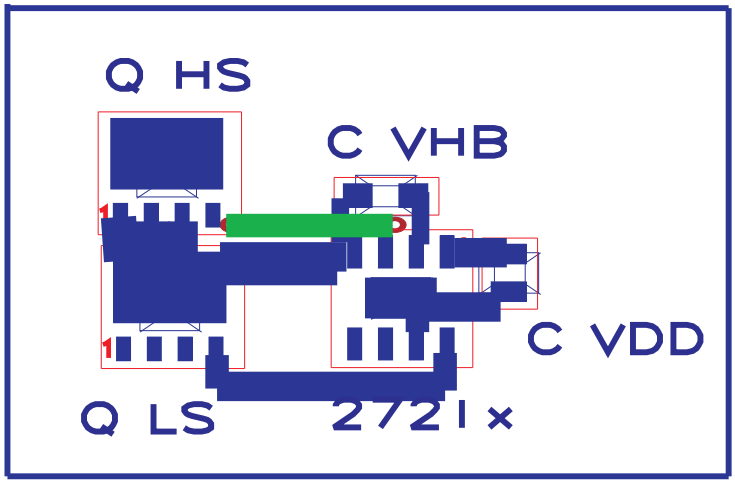


图 24. UCC27210/11 Component Placement

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is listed in *Device Functional Modes*. For detailed information regarding the table, please refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (SPRA953). The UCC27210 and UCC27211 devices are offered in SOIC (8), PowerPad (8), WSON (10) or VSON (8). The *Thermal Information* section lists the thermal performance metrics related to SOT-23 package.

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

这些参考文档和附加信息的链接均可在 www.ti.com 网站上获取

- 关于 PCB 焊盘图案的附加布局指南，请参见应用简介《*QFN/SON PCB 连接*》（文献编号：SLUA271）
- 关于附加的热性能指南，请参见应用报告《*PowerPAD™ 耐热增强型封装应用报告*》（文献编号：SLMA002）
- 关于附加的热性能指南，请参见应用报告《*PowerPAD™ 速成*》（文献编号：SLMA004）

12.2 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 **4.** 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
UCC27210	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC27211	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 商标

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27210D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27210	Samples
UCC27210DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27210	Samples
UCC27210DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27210	Samples
UCC27210DPRR	ACTIVE	WSON	DPR	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	UCC 27210	Samples
UCC27210DPRT	ACTIVE	WSON	DPR	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	UCC 27210	Samples
UCC27210DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27210	Samples
UCC27210DRMR	ACTIVE	VSON	DRM	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27210	Samples
UCC27210DRMT	ACTIVE	VSON	DRM	8	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27210	Samples
UCC27211D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27211	
UCC27211DDA	LIFEBUY	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27211	
UCC27211DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27211	Samples
UCC27211DPRR	ACTIVE	WSON	DPR	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	UCC 27211	Samples
UCC27211DPRT	LIFEBUY	WSON	DPR	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	UCC 27211	
UCC27211DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27211	Samples
UCC27211DRMR	ACTIVE	VSON	DRM	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27211	Samples
UCC27211DRMT	LIFEBUY	VSON	DRM	8	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27211	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

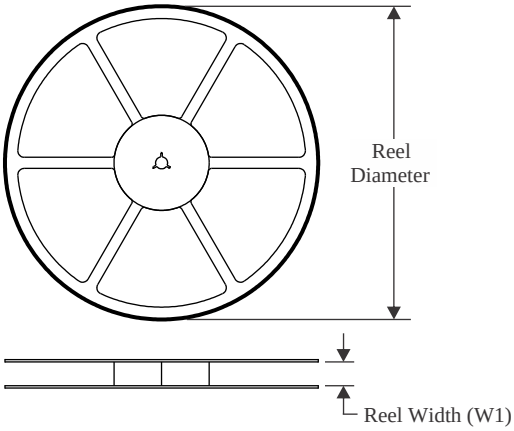
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

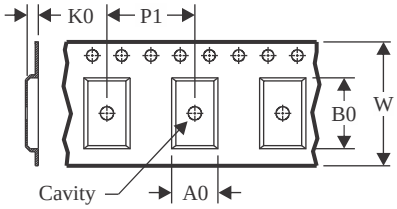
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

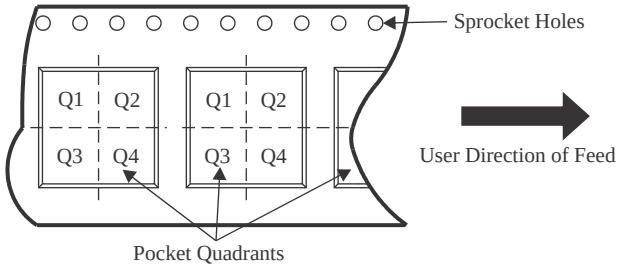


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

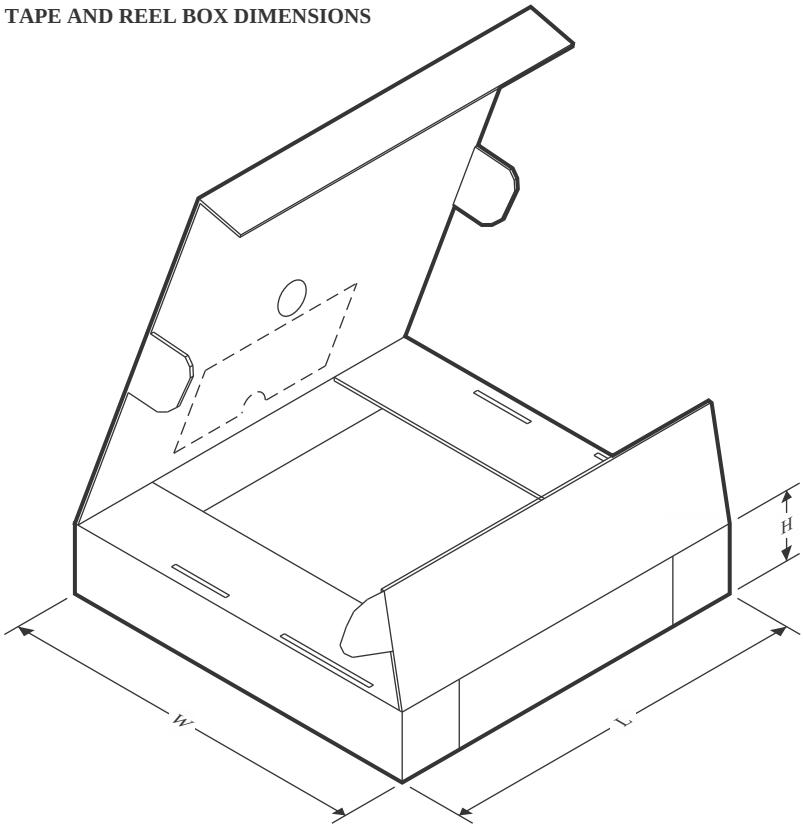
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27210DDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UCC27210DPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27210DPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27210DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27210DRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27210DRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211DDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UCC27211DPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211DPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27211DRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211DRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

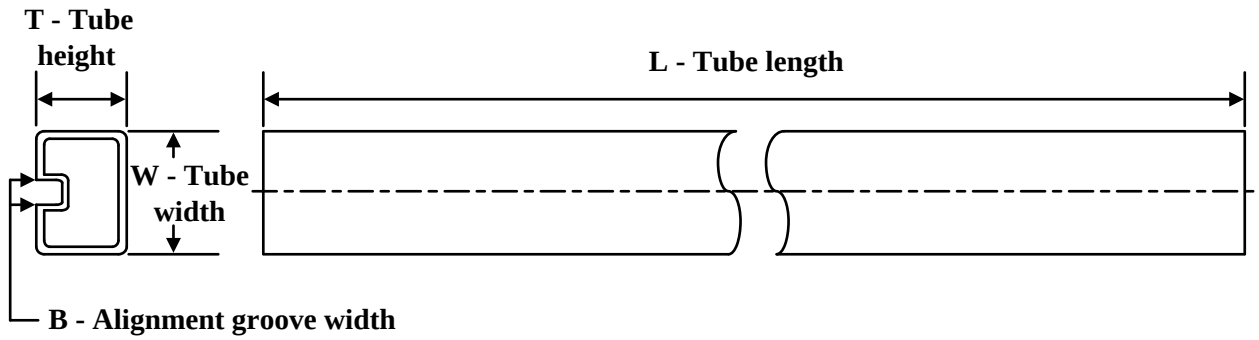
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27210DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0
UCC27210DPRR	WSON	DPR	10	3000	346.0	346.0	33.0
UCC27210DPRT	WSON	DPR	10	250	182.0	182.0	20.0
UCC27210DR	SOIC	D	8	2500	356.0	356.0	35.0
UCC27210DRMR	VSON	DRM	8	3000	356.0	356.0	35.0
UCC27210DRMT	VSON	DRM	8	250	210.0	185.0	35.0
UCC27211DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0
UCC27211DPRR	WSON	DPR	10	3000	346.0	346.0	33.0
UCC27211DPRT	WSON	DPR	10	250	182.0	182.0	20.0
UCC27211DR	SOIC	D	8	2500	356.0	356.0	35.0
UCC27211DRMR	VSON	DRM	8	3000	356.0	356.0	35.0
UCC27211DRMT	VSON	DRM	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

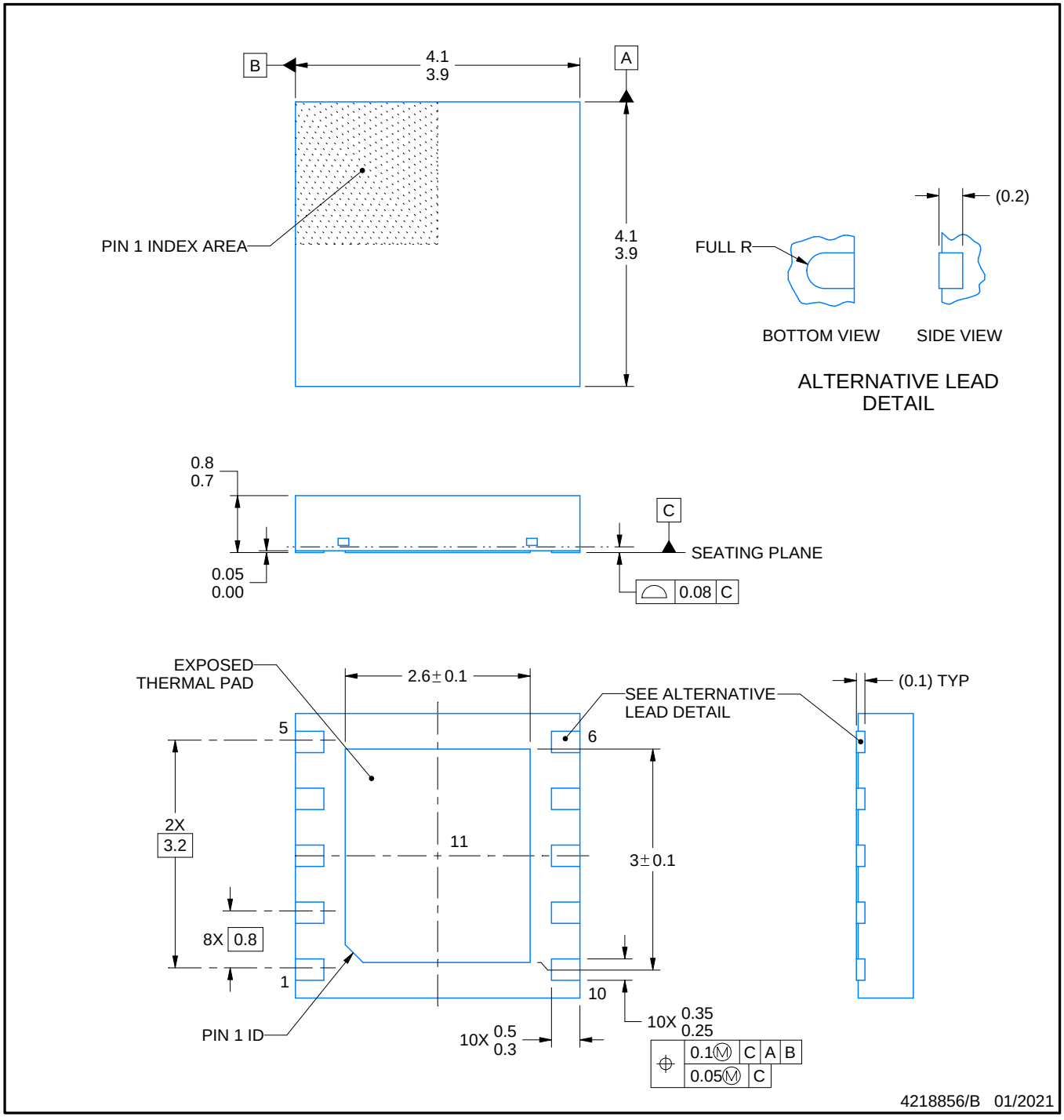
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC27210D	D	SOIC	8	75	506.6	8	3940	4.32
UCC27210DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
UCC27211D	D	SOIC	8	75	506.6	8	3940	4.32
UCC27211DDA	DDA	HSOIC	8	75	517	7.87	635	4.25

PACKAGE OUTLINE

DPR0010A

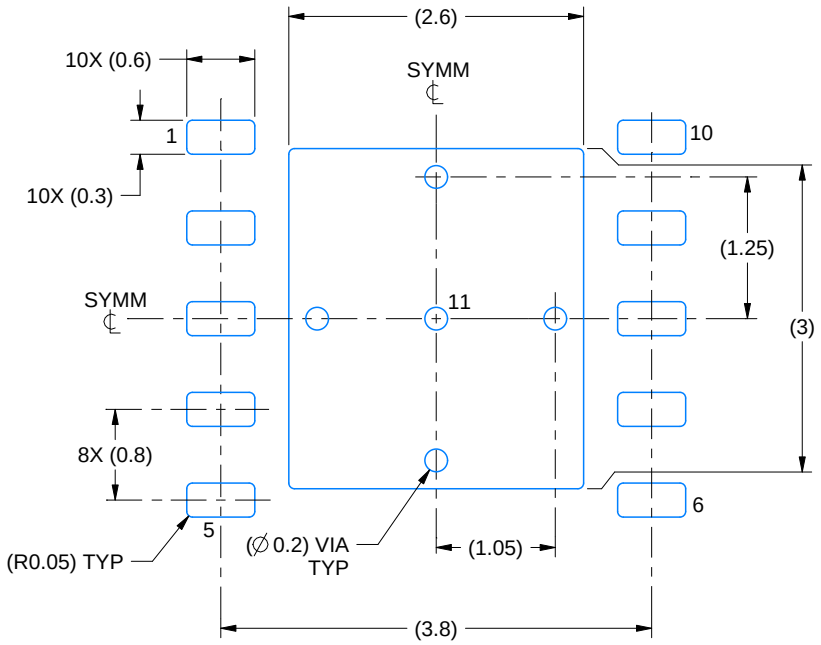
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

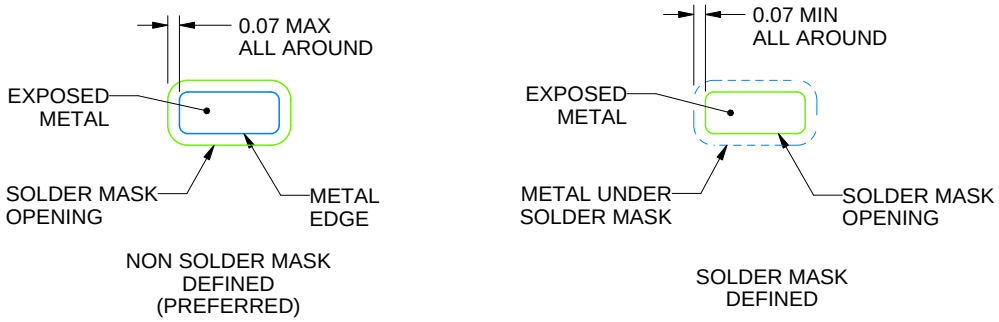


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

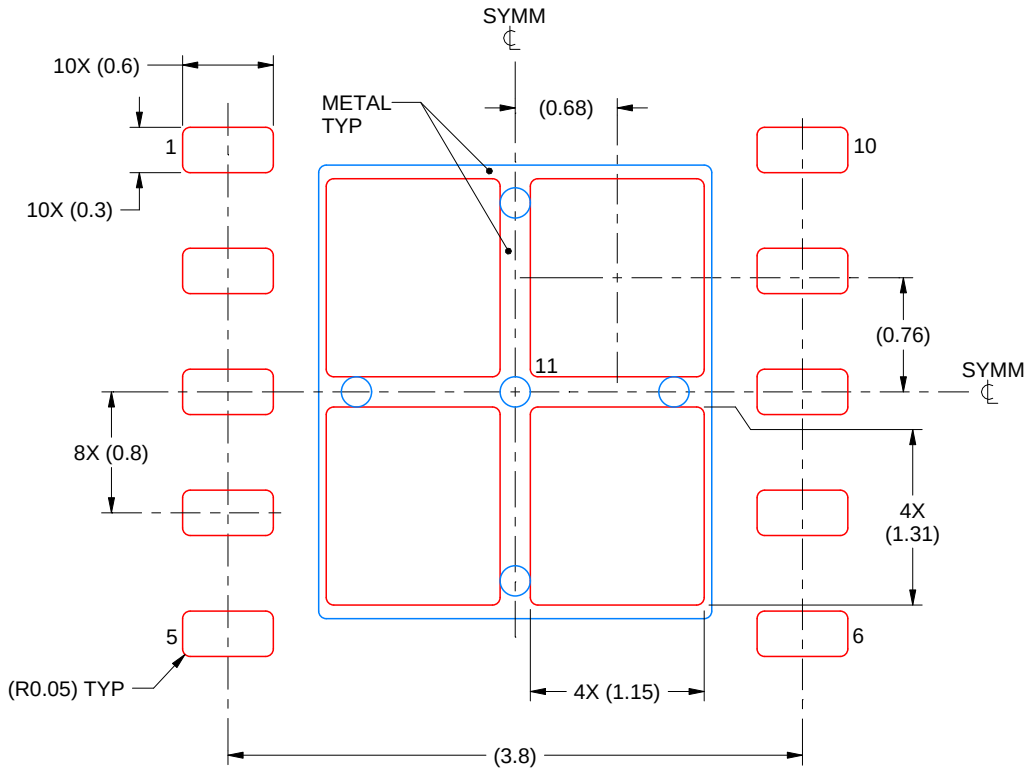


SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

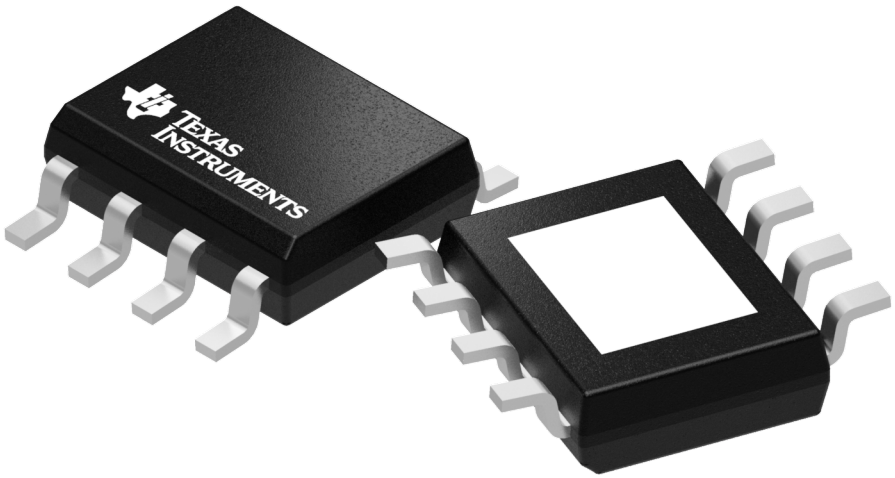
4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

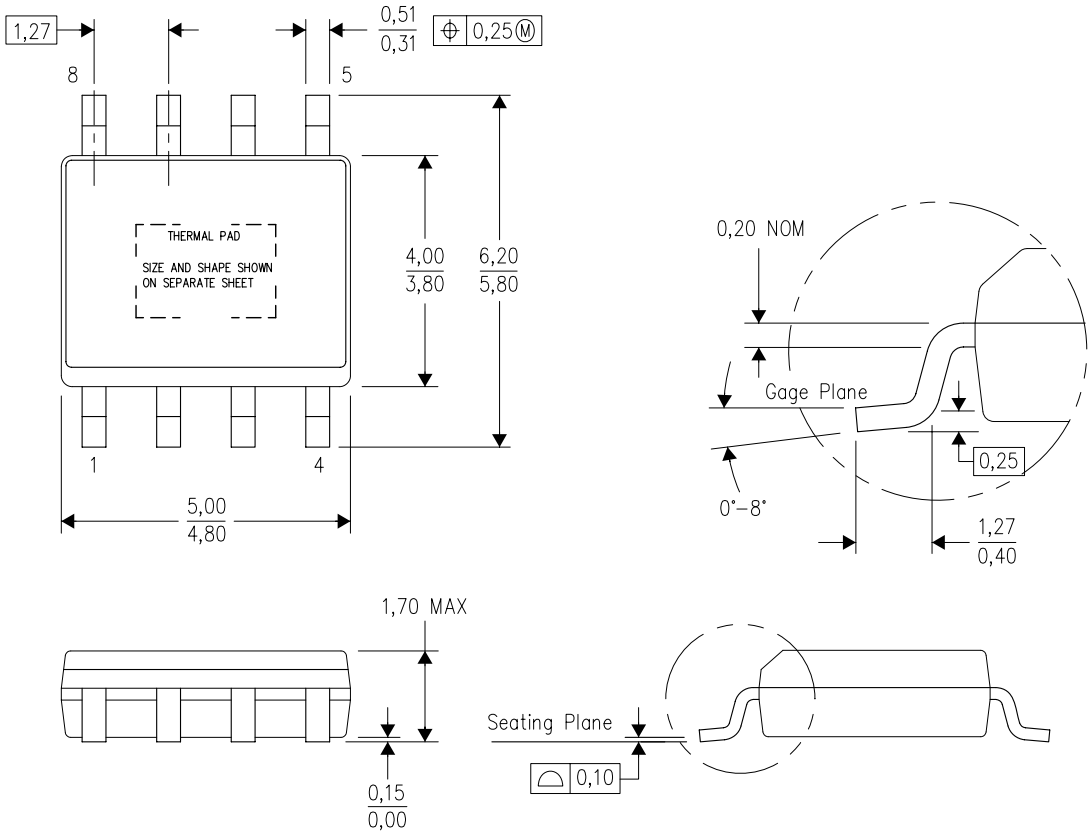
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

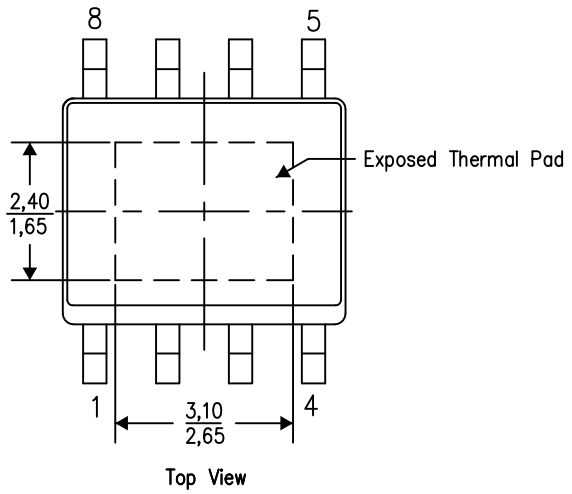
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



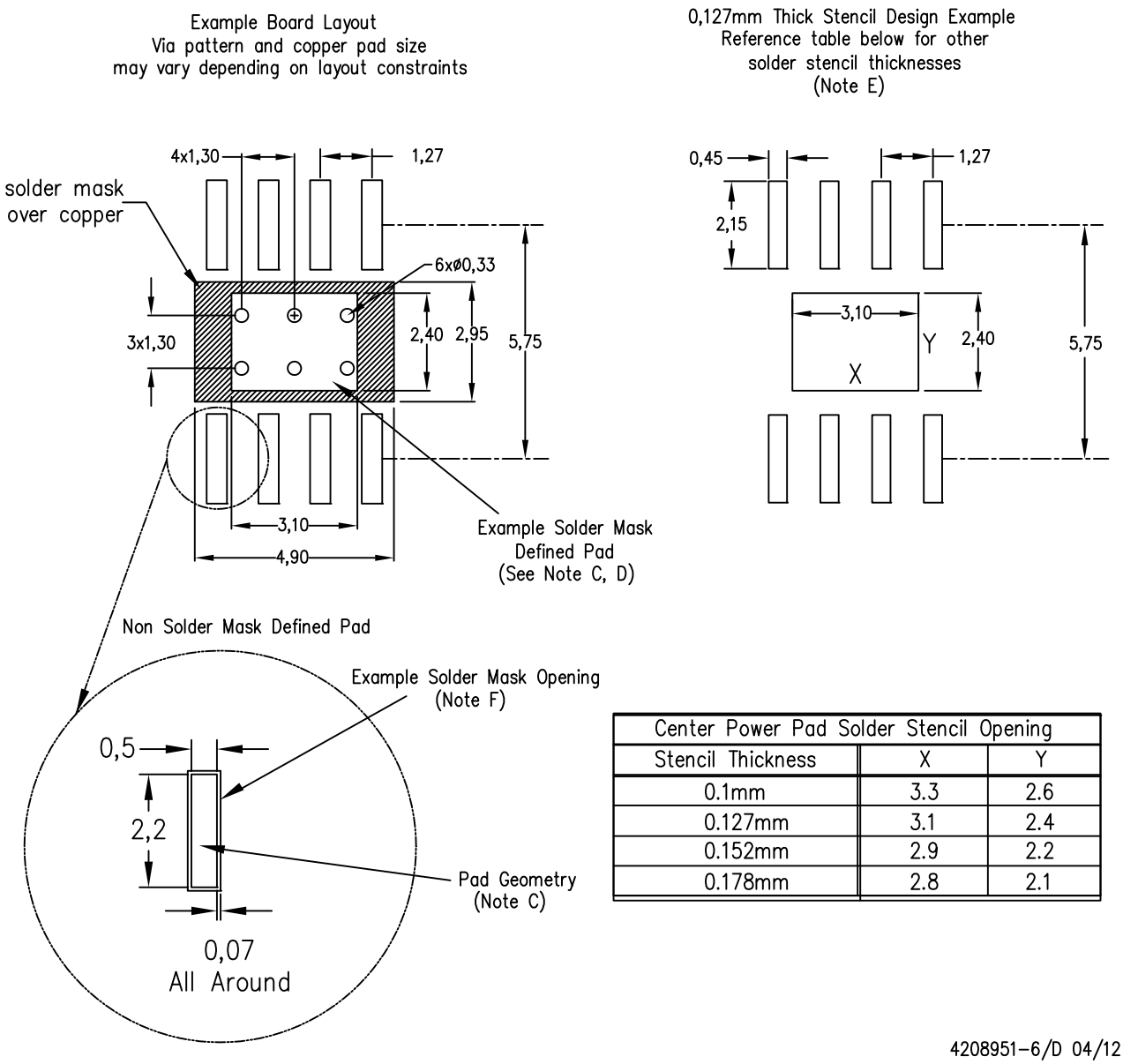
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

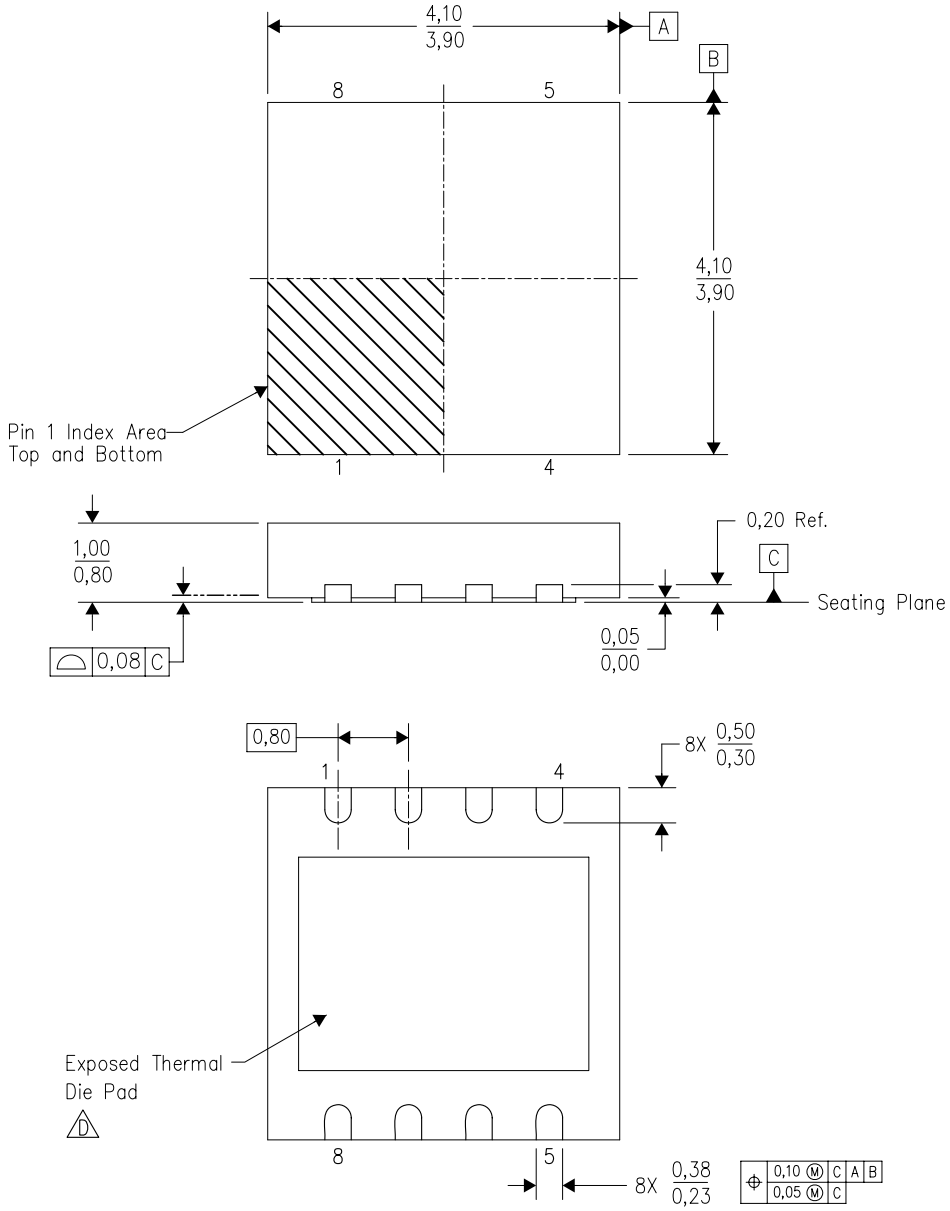


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

DRM (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

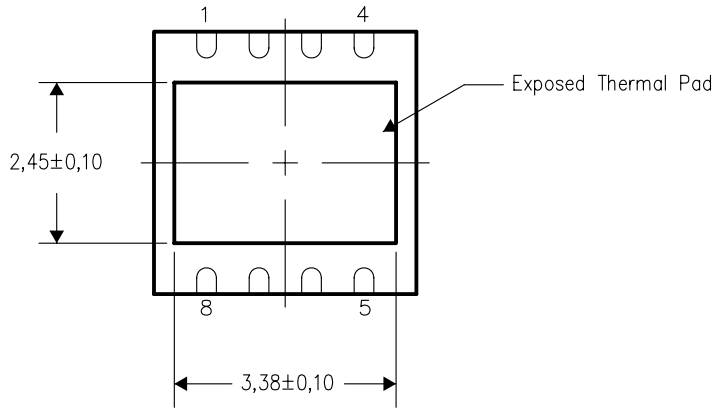
DRM (S–PDSO–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

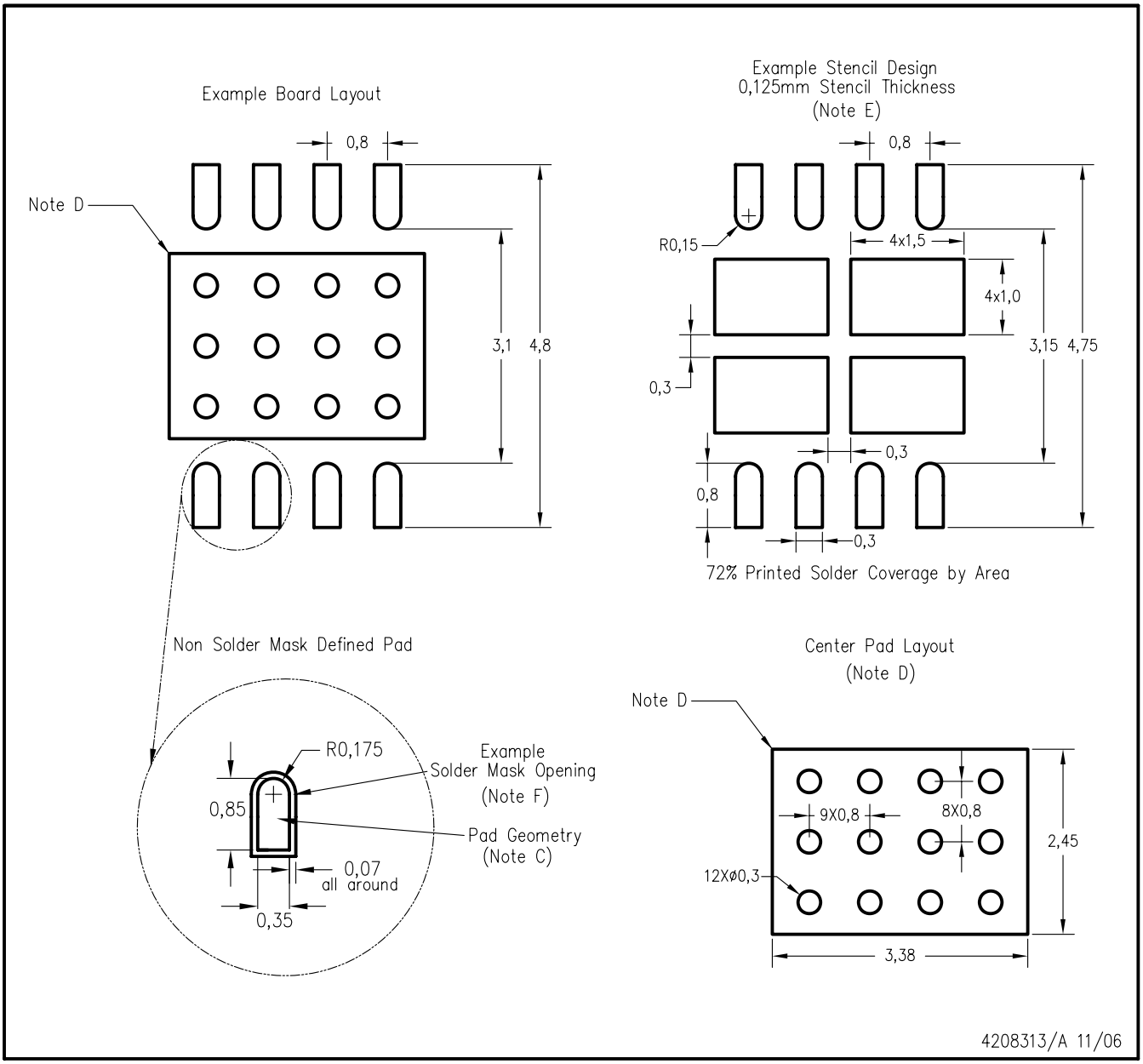


Bottom View

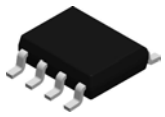
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRM (S–PDSO–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

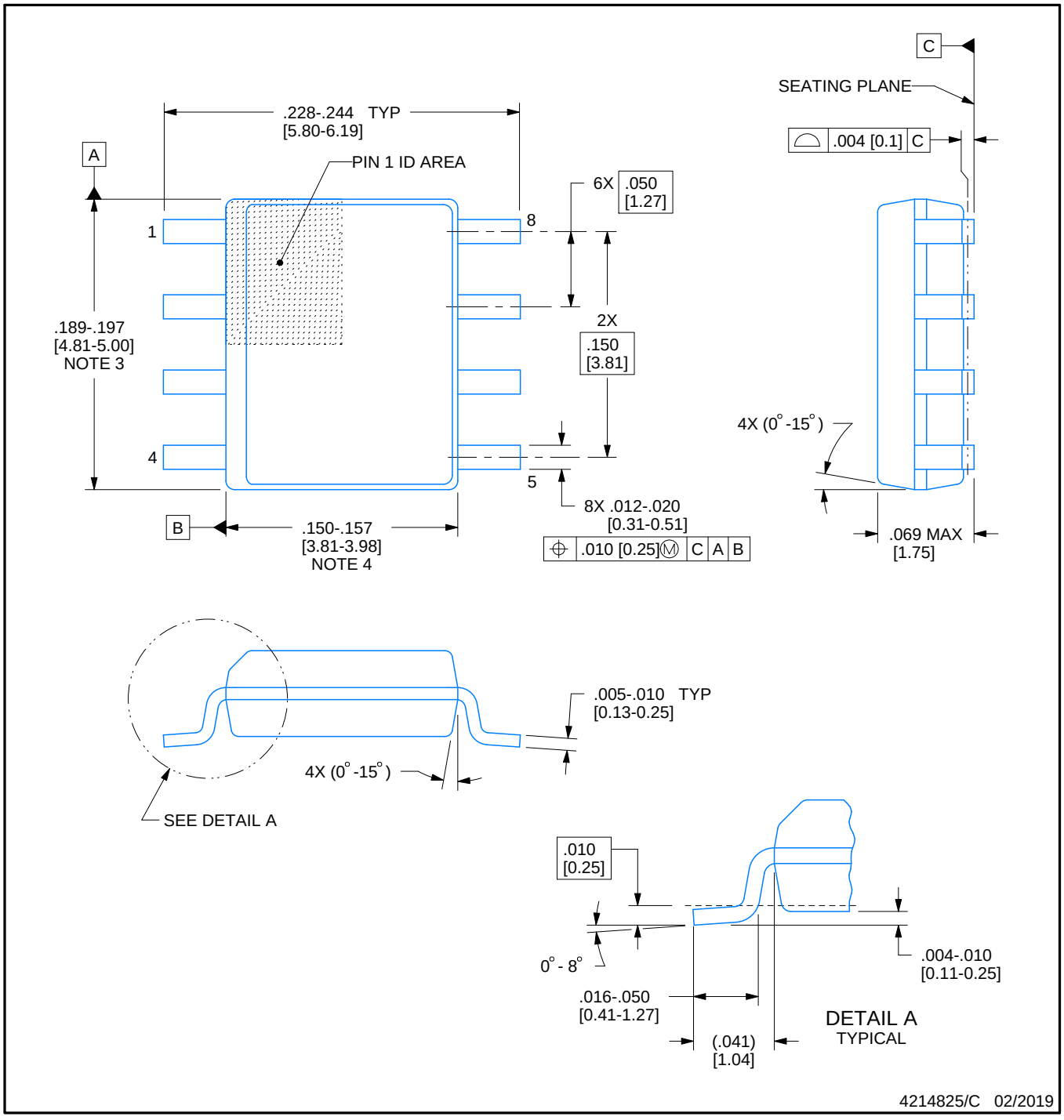


PACKAGE OUTLINE

D0008A

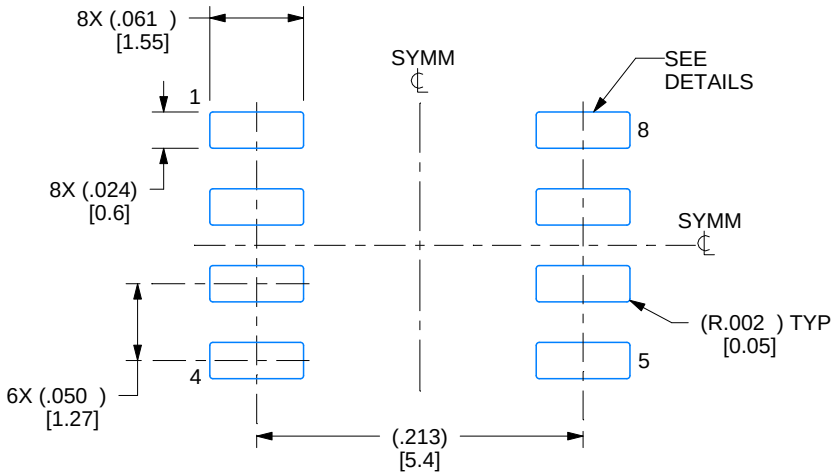
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

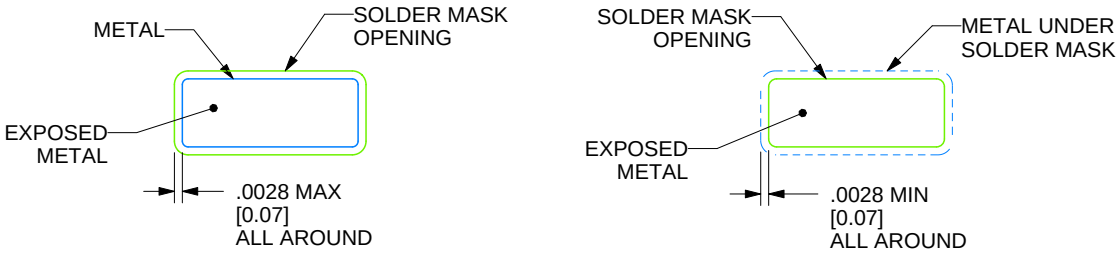


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

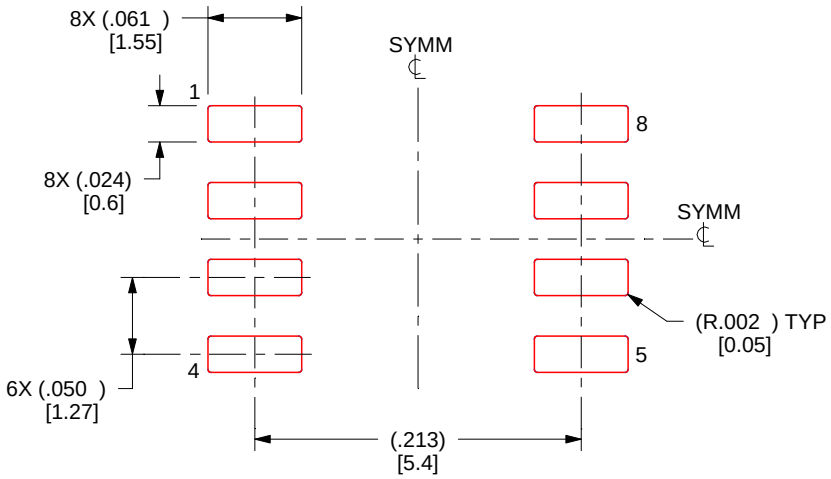
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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