

# 具有 12GSPS DAC 和 3GSPS ADC 的 AFE7950 4T6R 射频采样 AFE

## 1 特性

- [申请完整数据表](#)
- 四通道射频采样 12 GSPS 发送 DAC
- 四通道射频采样 3 GSPS 接收 ADC
- 双通道射频采样 3 GSPS 反馈 (辅助 RX) ADC
- 最大射频信号带宽：
  - 4TX 或 2FB : 1200 MHz 或 2TX : 2400 MHz
  - RX ) : 1200 MHz (无 FB)、600 MHz (带 FB)
- 射频频率范围：
  - TX : 600MHz - 12GHz
  - RX/FB : 600MHz -12GHz
- 数字步进衰减器 (DSA) :
  - TX : 40 dB 范围, 0.125 dB 步进
  - RX 或 FB : 25 dB 范围, 0.5 dB 步进
- 用于 TX 和 RX 的单频带或双频带 DUC/DDC
- 每个 TX/RX 和 FB 为 16 个 NCO
- 可选内部 PLL/VCO, 提供 DAC 或 ADC 采样率下的 DAC/ADC 时钟或外部时钟
- 串行器/解串器数据接口：
  - 可兼容 JESD204B 和 JESD204C
  - 8 个高达 29.5 Gbps 的串行器/解串器收发器
  - 子类 1 多器件同步
- 封装 : 17mm × 17mm FCBGA, 间距 0.8 mm

## 2 应用

- [雷达](#)
- [导引头前端](#)
- [国防无线电](#)
- [战术通信基础设施](#)
- [无线通信测试](#)

## 3 说明

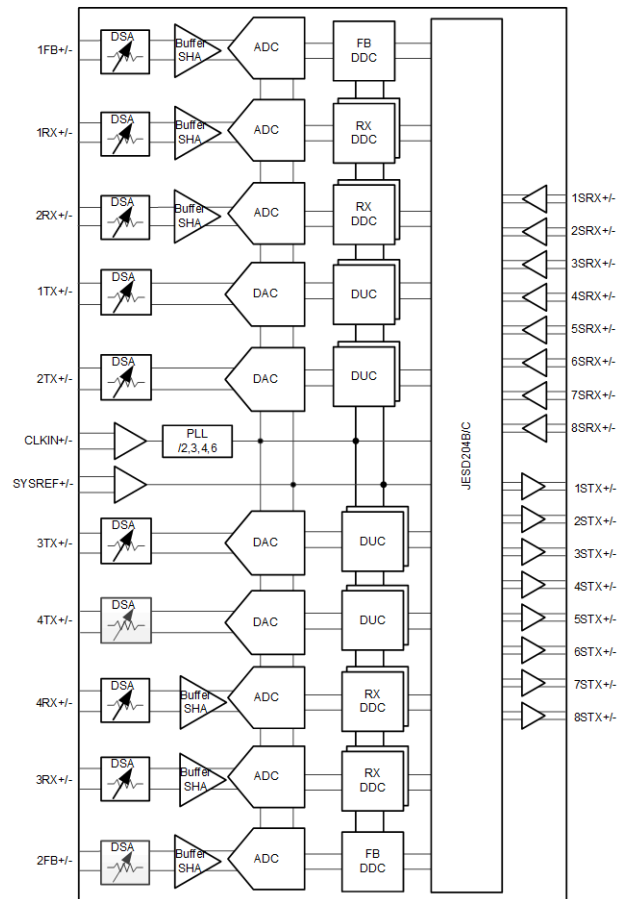
AFE7950 是一款高性能、高带宽、多通道收发器, 集成了四个射频采样发送链、四个射频采样接收链和两个射频采样反馈链 (总计六个射频采样 ADC)。此器件具有高达 12GHz 的工作频率, 支持直接在 L、S、C 和 X 频带频率范围内进行射频采样, 无需额外的频率转换级。密度和灵活性提高后可支持高通道数、多任务系统。

TX 信号路径支持插值和数字上变频选项, 从而为四个 TX 提供高达 1200MHz 的信号带宽, 或者为两个 TX 提供高达 2400MHz 的信号带宽。DUC 的输出驱动一个 12GSPS DAC (数模转换器), 通过混合模式输出选项增强在第二奈奎斯特区的运行。DAC 输出包括一个具有 40dB 范围以及 1dB 模拟和 0.125dB 数字步进的可选增益放大器 (TX DSA)。

### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
AFE7950	FC-BGA	17 mm × 17 mm

- (1) 如需了解更多信息, 请参阅 [机械、封装和可订购信息](#)。
- (2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



功能方框图



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## 4 说明 (续)

每个接收器链均包含一个 25dB 范围的数字步进衰减器 (DSA)，后跟一个 3GSPS 模数转换器 (ADC)。每个接收器通道都有多个模拟峰值功耗检测器和各种数字功耗检测器，可辅助进行外部或内部自主自动增益控制器，另外还具有一个射频过载检测器，用于提供器件可靠性保护。灵活的抽取选项可为数据带宽提供高达 1200MHz 的优化（对于四条不带 FB 路径的 RX），或为带两条 FB 路径（每条 1200MHz 带宽）提供 600MHz 的优化。

## 5 Revision History

注：以前版本的页码可能与当前版本的页码不同

### Changes from July 12, 2022 to June 12, 2023 (from Revision C (July 2022) to Revision D (June 2023))

	Page
• 更改了“封装信息”表以加入注释 2.....	1
• Changed $I_{IH}$ and $I_{IL}$ units to $\mu A$ .....	19
• Removed dither from conditions.....	28
• Changed captions to read 1.8 GHz in 1.8 GHz section and removed dither from conditions.....	37
• Removed dither from conditions.....	45
• Changed 0TX to 1TX in plot notes and removed dither from conditions and dither plot.....	53
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### Changes from March 9, 2022 to July 12, 2022 (from Revision B (March 2022) to Revision C (July 2022))

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• Removed dither from conditions.....	28
• Changed captions to read 1.8 GHz in 1.8 GHz section and removed dither from conditions.....	37
• Removed dither from conditions.....	45
• Changed 0TX to 1TX in plot notes and removed dither from conditions and dither plot.....	53
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### Changes from Revision A (August 2021) to Revision B (March 2022)

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• 向“申请完整数据表”添加了特性.....	1
• Added the <a href="#">Specification</a> tables to the data sheet.....	4

### Changes from Revision \* (February 2021) to Revision A (August 2021)

	Page
• 将数据表状态从 <a href="#">預告信息</a> 更改为 <a href="#">量产数据</a> .....	1

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	- 0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	- 0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVC0, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	- 0.5	2.1	V
Pin Voltage Range	{1/2/3/4}RXIN+/-	- 0.5	VDDR1P8+0.3	V
	1FBIN+/-, 2FB+/-	- 0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	- 0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	- 0.3	1.4	V
	{1:8}SRX+/-	- 0.3	1.4	V
	{1:8}STX+/-	- 0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	- 0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	- 0.3	VDDCLK1P8 + 0.3	V
SRDAMUX1, SRDAMUX2	- 0.3	VDDA1P8+0.3	V	
Peak Input Current	any input		20	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	1000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins	150	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T <sub>A</sub>	Ambient temperature	- 40		85	°C
T <sub>J</sub>	Operating Junction Temperature			110 <sup>(1)</sup>	°C
	Maximum Operating Junction Temperature	125			°C

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		AFE7950		UNIT
		ABJ or ALK (FC-BGA)		
		400 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	16.2		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.42		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	4.85		°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.12		°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	4.6		°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Transmitter Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC <sub>RES</sub>	DAC resolution			14		bits
f <sub>RFout</sub>	RF output frequency range	f <sub>DAC</sub> = 12 GSPS, 1 <sup>st</sup> Nyquist	600		6000	MHz
		f <sub>DAC</sub> = 12 GSPS, 2 <sup>nd</sup> Nyquist	6000		12000	
		f <sub>DAC</sub> = 9 GSPS, 1 <sup>st</sup> Nyquist	600		4500	
		f <sub>DAC</sub> = 9 GSPS, 2 <sup>nd</sup> Nyquist	4500		9000	
		f <sub>DAC</sub> = 6 GSPS, 1 <sup>st</sup> Nyquist	600		3000	
		f <sub>DAC</sub> = 6 GSPS, 2 <sup>nd</sup> Nyquist	3000		6000	
P <sub>max_FS</sub>	Max Full Scale Output Power, max gain 1 tone, at device pins	f <sub>out</sub> = 850 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS		4.2		dBm
		f <sub>out</sub> = 1800 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS		4.6		dBm
		f <sub>out</sub> = 2600 MHz, f <sub>DAC</sub> = 8847.36 MSPS, -0.5dBFS		4.0		dBm
		f <sub>out</sub> = 3500 MHz, -0.5dBFS		3.9		dBm
		f <sub>out</sub> = 4900 MHz, -0.5dBFS		3.1		dBm
		f <sub>out</sub> = 3500 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS, straight mode		1.0		dBm
		f <sub>out</sub> = 4900 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS, straight mode		0.1		dBm
		f <sub>out</sub> = 4900 MHz, f <sub>DAC</sub> = 8847.36 MSPS, -0.5dBFS, straight mode		-0.7		dBm
		f <sub>out</sub> = 8100 MHz, -0.1dBFS, mixed mode		-2.8		dBm
f <sub>out</sub> = 9600 MHz, -0.1dBFS, mixed mode		-4.3		dBm		
R <sub>TERM</sub>	Output termination resistor	Default setting		50		Ω
ATT <sub>range</sub>	DSA Attenuation range			40		dB
ATT <sub>step</sub>	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		±0.2		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, after calibration		±0.1		dB
ATT <sub>phase-err</sub>	DSA Gain Steps Phase accuracy, any 8dB range	f <sub>out</sub> = 850MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 1800MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 2600MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 3500MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 4900MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 8100MHz <sup>(2)</sup>		±2		deg
G <sub>flat</sub>	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F <sub>out</sub> < 4.9G		1.2		

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion, 2 tones at $f_{\text{IF}} \pm 10\text{ MHz}$	$f_{\text{out}} = 850\text{MHz}$ , -7dBFS each tone		-66		dBc
		$f_{\text{out}} = 1800\text{MHz}$ , -7dBFS each tone		-63		dBc
		$f_{\text{out}} = 2600\text{MHz}$ , -7dBFS each tone		-62		dBc
		$f_{\text{out}} = 3500\text{MHz}$ , -7dBFS each tone		-61		dBc
		$f_{\text{out}} = 4900\text{MHz}$ , -7dBFS each tone		-57		dBc
		$f_{\text{out}} = 8100\text{MHz}$ , -7dBFS each tone		-55		dBc
		$f_{\text{out}} = 9600\text{MHz}$ , -7dBFS each tone		-52		dBc
		$f_{\text{out}} = 850\text{MHz}$ , -13dBFS each tone		-74.4		dBc
		$f_{\text{out}} = 1800\text{MHz}$ , -13dBFS each tone		-71.1		dBc
		$f_{\text{out}} = 2600\text{MHz}$ , -13dBFS each tone		-73		dBc
		$f_{\text{out}} = 3500\text{MHz}$ , -13dBFS each tone		-72		dBc
		$f_{\text{out}} = 4900\text{MHz}$ , -13dBFS each tone		-67.8		dBc
		$f_{\text{out}} = 8100\text{MHz}$ , -13dBFS each tone		-64		dBc
		$f_{\text{out}} = 9600\text{MHz}$ , -13dBFS each tone		-68		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		50.8		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		51.9		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		42		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		44		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		46.1		dBc
$f_{\text{S}}/2 - f_{\text{OUT}}$	Interleaving Image	$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode		-51.9		dBc
		$f_{\text{DAC}} = 8847.36\text{ MSPS}$ , interleave mode		-46.0		dBc
		$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode		-41		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-49		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-48		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-47		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 850\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 1800\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-64		dBc
		$f_{\text{out}} = 2600\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-45		dBc
		$f_{\text{out}} = 3500\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-57		dBc
		$f_{\text{out}} = 4900\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-58		dBc
		$f_{\text{out}} = 8100\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 9600\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-62		dBc

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-62		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-55		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-57		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-60		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-54		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-54		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-56		dBc
		$f_{\text{out}} = 850\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
		$f_{\text{out}} = 1800\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 2600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 3500\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 4900\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-78		dBc
		$f_{\text{out}} = 8100\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{out}} = 9600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-81		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-88		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-79		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-87		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-85		dBc
		$f_{\text{out}} = 850\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{out}} = 1800\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-98		dBc
		$f_{\text{out}} = 2600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 3500\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 4900\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 8100\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 9600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{out}} = 850\text{ MHz}$		68.5		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		79.4		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		77		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		75		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		76		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		61		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		64		dBc
$f_s/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-64		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-75		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-67		dBFS
$f_s/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-49		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-48		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-48		dBFS



## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3*f <sub>s</sub> /4	Fixed Spur	2nd Nyquist, f <sub>DAC</sub> = 5898.24MSPS		-76		dBFS
		2nd Nyquist, f <sub>DAC</sub> = 8847.36MSPS		-89		dBFS
		2nd Nyquist, f <sub>DAC</sub> = 11796.48MSPS		-63		dBFS
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 0.85 GHz	Atten=0dB, Pout=-13dBFS		-68.5		dBc
		Atten=20dB, Pout=-13dBFS		-67.2		dBc
		Atten=28dB, Pout=-13dBFS		-64.5		dBc
		Atten=39dB, Pout=-13dBFS		-53.9		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 1.8425 GHz	Atten=0dB, Pout=-13dBFS		-70.7		dBc
		Atten=20dB, Pout=-13dBFS		-68.3		dBc
		Atten=28dB, Pout=-13dBFS		-62.9		dBc
		Atten=39dB, Pout=-13dBFS		-52.0		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 2.6 GHz	Atten=0dB, Pout=-13dBFS		-71		dBc
		Atten=20dB, Pout=-13dBFS		-68		dBc
		Atten=28dB, Pout=-13dBFS		-62		dBc
		Atten=39dB, Pout=-13dBFS		-51.3		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 3.5 GHz	Atten=0dB, Pout=-13dBFS		-70		dBc
		Atten=20dB, Pout=-13dBFS		-67		dBc
		Atten=28dB, Pout=-13dBFS		-60		dBc
		Atten=39dB, Pout=-13dBFS		-49.8		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 4.9 GHz	Atten=0dB, Pout=-13dBFS		-68.8		dBc
		Atten=20dB, Pout=-13dBFS		-65.9		dBc
		Atten=28dB, Pout=-13dBFS		-60.6		dBc
		Atten=39dB, Pout=-13dBFS		-49.5		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 2.6 GHz	Atten=0dB, Pout=-13dBFS		-65		dBc
		Atten=20dB, Pout=-13dBFS		-62		dBc
		Atten=20dB, Pout=-13dBFS		-55		dBc
		Atten=39dB, Pout=-13dBFS		-44.3		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 3.5 GHz	Atten=0dB, Pout=-13dBFS		-64		dBc
		Atten=20dB, Pout=-13dBFS		-59		dBc
		Atten=28dB, Pout=-13dBFS		-52		dBc
		Atten=39dB, Pout=-13dBFS		-41.1		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 4.9 GHz	Atten=0dB, Pout=-13dBFS		-64.1		dBc
		Atten=20dB, Pout=-13dBFS		-60.4		dBc
		Atten=28dB, Pout=-13dBFS		-53.5		dBc
		Atten=39dB, Pout=-13dBFS		-42.5		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 8.1 GHz	Atten=0dB, Pout=-13dBFS		-58		dBc
		Atten=20dB, Pout=-13dBFS		-53		dBc
		Atten=28dB, Pout=-13dBFS		-46		dBc
		Atten=39dB, Pout=-13dBFS		-36		dBc

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-57		dBc
		Atten=20dB, Pout=-13dBFS		-50		dBc
		Atten=28dB, Pout=-13dBFS		-42		dBc
		Atten=39dB, Pout=-13dBFS		-31		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.2		%
		$F_{\text{out}} = 1.8425\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.3		%
		$F_{\text{out}} = 2.6\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.28		%
		$F_{\text{out}} = 3.5\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.38		%
		$F_{\text{out}} = 4.9\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.4		%
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-157.6		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-153.3		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-147.9		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-136.9		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-158.4		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-152.2		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-145.6		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-134.6		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-157		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-151		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-144		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-133.0		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-158		dBFS/Hz
		Atten=20dB, Pout=-13dBFS		-150		dBFS/Hz
		Atten=28dB, Pout=-13dBFS		-143		dBFS/Hz
		Atten=39dB, Pout=-13dBFS		-131.8		dBFS/Hz

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-155.5		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147.8		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140.8		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129.6		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 50MHz offset $F_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-153		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 50MHz offset $F_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-152		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
S22	Output Return Loss, <6GHz, +/- fc * 10%	with matching		-17		dB
	Output Return Loss, >8GHz, +/- fc * 10%	with matching		-10		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT <sup>(1)</sup>	$f_{\text{out}} = 900\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-49		dB
		$f_{\text{out}} = 1850\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-59		dB
		$f_{\text{out}} = 2600\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-65		dB
		$f_{\text{out}} = 3500\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-66		dB
		$f_{\text{out}} = 4900\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-60		dB
		$f_{\text{out}} = 900\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-90		dB
		$f_{\text{out}} = 1850\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-91		dB
		$f_{\text{out}} = 2600\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-93		dB
		$f_{\text{out}} = 3500\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-94		dB
		$f_{\text{out}} = 4900\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-83		dB

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN <sub>TXADD</sub>	Additive Phase Noise External Clock Mode <sup>(3)</sup>	$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{Hz}$		-88		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{kHz}$		-102		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{kHz}$		-110		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{kHz}$		-123		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{MHz}$		-136		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{MHz}$		-143		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{MHz}$		-146		dBc/Hz

- (1) Measured with differential 50 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
- (2) After DSA calibration procedure
- (3) Single side band, input clock phase noise subtracted.

## 6.6 RF ADC Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{ADC} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{REF} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{CLK} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC <sub>RES</sub>	ADC resolution			14		bits
F <sub>RFIn</sub>	RF input frequency range		600		12000	MHz
P <sub>FS,CW,min</sub>	Min Full scale input power, at device pins <sup>(1)</sup>	f <sub>IN</sub> = 830 MHz, DSA=0dB		-2.9		dBm
		f <sub>IN</sub> = 1760 MHz, DSA=0dB		-2.8		dBm
		f <sub>IN</sub> = 2610 MHz, DSA=0dB		-1.8		dBm
		f <sub>IN</sub> = 3610 MHz, DSA=0dB		-0.4		dBm
		f <sub>IN</sub> = 4910 MHz, DSA=0dB		0.1		dBm
		f <sub>IN</sub> = 8150 MHz, DSA=0dB		2.1		dBm
		f <sub>IN</sub> = 9610 MHz, DSA=0dB		4.3		dBm
P <sub>FS,CW,MAX</sub>	MAX Full scale input power - reliability limited, at device pins	f <sub>IN</sub> = 830 MHz, DSA = 20dB		16.7		dBm
		f <sub>IN</sub> = 1760 MHz, DSA = 20dB		17.0		dBm
		f <sub>IN</sub> = 2610 MHz, DSA = 20dB		18		dBm
		f <sub>IN</sub> = 3610 MHz, DSA = 20dB		18.5		dBm
		f <sub>IN</sub> = 4910 MHz, DSA = 20dB		19.3		dBm
		f <sub>IN</sub> = 8150 MHz, DSA = 20dB		21.3		dBm
		f <sub>IN</sub> = 9610 MHz, DSA = 20dB		23.5		dBm
S11	Input Return Loss	with matching network		-12.0		dB
ATT <sub>range</sub>	DSA Attenuation range			25.0		dB
ATT <sub>step</sub>	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F <sub>in</sub> =3610MHz, after calibration		±0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F <sub>in</sub> =3610MHz, after calibration		±0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F <sub>in</sub> =4910MHz, after calibration		±1.8		deg
NSD	Noise Density (small signal)	f <sub>IN</sub> = 830 MHz, DSA = 3dB <sup>(3)</sup>		-155.2		dBFS/Hz
		f <sub>IN</sub> = 1760 MHz, DSA = 3dB <sup>(3)</sup>		-155.0		dBFS/Hz
		f <sub>IN</sub> = 2610 MHz, DSA = 3dB <sup>(3)</sup>		-154.4		dBFS/Hz
		f <sub>IN</sub> = 3610 MHz, DSA = 3dB <sup>(3)</sup>		-154.1		dBFS/Hz
		f <sub>IN</sub> = 4910 MHz, DSA = 3dB <sup>(3)</sup>		-155.1		dBFS/Hz
		f <sub>IN</sub> = 8150 MHz, DSA = 3dB <sup>(3)</sup>		-150		dBFS/Hz
		f <sub>IN</sub> = 9610 MHz, DSA = 3dB <sup>(3)</sup>		-151		dBFS/Hz
		f <sub>IN</sub> = 830 MHz, 3<=Atten<=22		-156.0		dBFS/Hz
		f <sub>IN</sub> = 1760 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f <sub>IN</sub> = 2610 MHz, 3<=Atten<=25		-155.7		dBFS/Hz
		f <sub>IN</sub> = 3610 MHz, 3<=Atten<=25		-155.4		dBFS/Hz
		f <sub>IN</sub> = 4910 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f <sub>IN</sub> = 8150 MHz, 3<=Atten<=25		-152.5		dBFS/Hz
		f <sub>IN</sub> = 9610 MHz, 3<=Atten<=25		-152.5		dBFS/Hz

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF <sub>min</sub>	Noise Figure min DSA Atten=0 - 3dB	$f_{\text{IN}} = 830 \text{ MHz}$		19.1		dB
		$f_{\text{IN}} = 1760 \text{ MHz}$		19.0		dB
		$f_{\text{IN}} = 2610 \text{ MHz}$		20.9		dB
		$f_{\text{IN}} = 3610 \text{ MHz}$		22.8		dB
		$f_{\text{IN}} = 4910 \text{ MHz}$		22.4		dB
		$f_{\text{IN}} = 8150 \text{ MHz}$		27.3		dB
		$f_{\text{IN}} = 9610 \text{ MHz}$		30		dB
NF	Noise Figure DSA Atten=4dB	$f_{\text{IN}} = 830 \text{ MHz}^{(4)}$		20.0		dB
		$f_{\text{IN}} = 1760 \text{ MHz}^{(4)}$		20.6		dB
		$f_{\text{IN}} = 2610 \text{ MHz}^{(4)}$		21.9		dB
		$f_{\text{IN}} = 3610 \text{ MHz}^{(4)}$		23.5		dB
		$f_{\text{IN}} = 4910 \text{ MHz}^{(4)}$		22.3		dB
		$f_{\text{IN}} = 8150 \text{ MHz}^{(4)}$		27.9		dB
		$f_{\text{IN}} = 9610 \text{ MHz}^{(4)}$		30.7		dB
NF <sub>max</sub>	Noise Figure DSA Atten=20dB	$f_{\text{IN}} = 830 \text{ MHz}$		34.7		dB
		$f_{\text{IN}} = 1760 \text{ MHz}$		35.2		dB
		$f_{\text{IN}} = 2610 \text{ MHz}$		36.0		dB
		$f_{\text{IN}} = 3610 \text{ MHz}$		37.3		dB
		$f_{\text{IN}} = 4910 \text{ MHz}$		37.6		dB
		$f_{\text{IN}} = 8150 \text{ MHz}$		42.8		dB
		$f_{\text{IN}} = 9610 \text{ MHz}$		45		dB
IMD3	3 <sup>rd</sup> order intermodulation 2 tones at at $f_{\text{IN}} \pm 10\text{MHz}$ -7dBFS each tone	$f_{\text{IN}} = 840 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-82.4		dBc
		$f_{\text{IN}} = 1770 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-84.1		dBc
		$f_{\text{IN}} = 2610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-74		dBc
		$f_{\text{IN}} = 3610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-77		dBc
		$f_{\text{IN}} = 4920 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-75.9		dBc
		$f_{\text{IN}} = 8150 \text{ MHz}, 3 \leq \text{Atten} \leq 12$ , 25MHz tone spacing		-55		dBc
		$f_{\text{IN}} = 9610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$ , 25MHz tone spacing		-60		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3$ dBFS	$f_{\text{IN}} = 830 \text{ MHz}$		88.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		80.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		84		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		78.9		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		78		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		71		dBFS

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -3 \text{ dBFS}^{(2)}$	$f_{\text{IN}} = 830 \text{ MHz}$		-85.5		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-90.5		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-87		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-84.2		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-70		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -3 \text{ dBFS}$	$f_{\text{IN}} = 830 \text{ MHz}$		-80.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-85.3		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-75.4		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-70		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -3 \text{ dBFS}$	$f_{\text{IN}} = 830 \text{ MHz}$		-88.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-80.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-81.7		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-78		dBFS
SFDR	Spurious Free Dynamic Range $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830 \text{ MHz}$		89.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		88.8		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		95		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		90		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		89.8		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		83		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		80		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830 \text{ MHz, with board trim}$		-79.0		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz, with board trim}$		-101.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz, with board trim}$		-100		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz, with board trim}$		-101		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz, with board trim}$		-99.1		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz, with board trim}$		-107		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz, with board trim}$		-107		dBFS

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		-95.4		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-95.2		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-98		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-97		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-94		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-100		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-102		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		-89.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-88.8		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-83		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-80		dBFS
RX-RX Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN	$f_{\text{IN}} = 830\text{ MHz}$		-76.6		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-70.9		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-73.5		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-76.9		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-65.3		dBc
		$f_{\text{IN}} = 8150\text{ MHz}$		-64		dBc
		$f_{\text{IN}} = 9610\text{ MHz}$		-60		dBc
TX-FB Isolation	Near Channel: 2TXOUT to 1FBIN 4TXOUT to 2FBIN	$f_{\text{IN}} = 830\text{ MHz}$		-84.3		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-87.7		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-85		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-75		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-81.5		dBc
		$f_{\text{IN}} = 8150\text{ MHz}$		-71		dBc
		$f_{\text{IN}} = 9610\text{ MHz}$		-69		dBc
TX-RX Isolation	Far Channel: 2TXOUT to 1RXIN 4TXOUT to 3RXIN	$f_{\text{IN}} = 830\text{ MHz}$		-85.9		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-86.9		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-91		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-83		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-81.9		dBc
		$f_{\text{IN}} = 8150\text{ MHz}$		-68		dBc
		$f_{\text{IN}} = 9610\text{ MHz}$		-68		dBc

- (1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) NLE correction of HD2
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB



## 6.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f<sub>DAC</sub> = f<sub>VCO</sub>, f<sub>OUT</sub> = f<sub>DAC</sub>/4, normalized to f<sub>VCO</sub>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>VCO1</sub>	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f <sub>VCO2</sub>	VCO2 min frequency				8.8	GHz
	VCO2 max frequency		9.1			GHz
f <sub>VCO3</sub>	VCO3 min frequency				9.7	GHz
	VCO3 max frequency		10.24			GHz
f <sub>VCO4</sub>	VCO4 min frequency				11.6	GHz
	VCO4 max frequency		12.08			GHz
DIV <sub>DAC</sub>	DAC sample rate divider			1, 2 or 3		
DIV <sub>FBAD</sub> C	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
DIV <sub>RXAD</sub> C	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN <sub>VCO</sub>	Closed Loop Phase Noise F <sub>PLL</sub> = 11.79848 GHz F <sub>REF</sub> =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		-141		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> =8.84736 GHz F <sub>REF</sub> =491.52MHz	600kHz		-114		dBc/Hz
		800kHz		-118		dBc/Hz
		1MHz		-120		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-135		dBc/Hz
		50MHz		-142		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> = 9.8403 GHz F <sub>REF</sub> =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-134		dBc/Hz
		50MHz		-140		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> = 7.86432GHz F <sub>REF</sub> =491.52MHz	600kHz		-116		dBc/Hz
		800kHz		-119		dBc/Hz
		1MHz		-122		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-136		dBc/Hz
		50MHz		-143		dBc/Hz
F <sub>rms</sub>	Clock PLL integrated phase error <sup>(1)</sup>	f <sub>PLL</sub> =11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f <sub>PLL</sub> =8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f <sub>PLL</sub> =9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f <sub>PDF</sub>	PFD frequency		100		500	MHz
PN <sub>pll_flat</sub>	Normalized PLL flat Noise	f <sub>VCO</sub> = 11796.48MHz		-226.5		dBc/Hz

## 6.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is TA,MIN = -40°C to TJ,MAX = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f<sub>DAC</sub> = f<sub>VCO</sub>, f<sub>OUT</sub> = f<sub>DAC</sub>/4, normalized to f<sub>VCO</sub>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F <sub>REF</sub>	Input Clock frequency		0.1		12	GHz
V <sub>SS</sub>	Input Clock level		0.6		1.8	Vppdiff
Coupling				AC Coupling Only		
	REFCLK input impedance <sup>(2)</sup>	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

- (1) Single Sideband, not including the reference clock contribution  
 (2) Refer to S11 data available from TI for impedance vs frequency

## 6.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CML SerDes Inputs [8:1]SRX+/-</b>						
V <sub>SRDIFF</sub>	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V <sub>SRCOM</sub>	SerDes Input Common Mode		0.4	0.5	0.6	V
Z <sub>SRdiff</sub>	SerDes Internal Differential Termination <sup>(1)</sup>			100		Ω
F <sub>SerDes</sub>	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance <sup>(2)</sup>	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
<b>CML SerDes Outputs [8:1]STX+/-</b>						
V <sub>STDIFF</sub>	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V <sub>STCOM</sub>	SerDes Output Common Mode		0.4	0.45	0.55	V
Z <sub>STdiff</sub>	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
<b>CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1</b>						
V <sub>IH</sub>	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V <sub>IL</sub>	Low-Level Input Voltage				0.4×VDD1 P8GPIO	V
I <sub>IH</sub>	High-Level Input Current		- 250		250	μA
I <sub>IL</sub>	Low-Level Input Current		- 250		250	μA
C <sub>L</sub>	CMOS input capacitance			2		pF
V <sub>OH</sub>	High-Level Output Voltage		VDD1P8G PIO - 0.2			V
V <sub>OL</sub>	Low-Level Output Voltage				0.2	V
<b>Differential Inputs: SYSREF+/- Mode A</b>						
Clock <sub>MODE</sub>				PLL Clock Mode Only		
F <sub>SYSREFMAX</sub>	SYSREF Input Frequency Maximum			40		MHz
V <sub>SWINGSRMAX</sub>	SYSREF Input Swing Maximum			1.8		Vppdiff <sup>(3)</sup>
V <sub>SWINGSRMIN</sub>	SYSREF Input Swing Minimum	f <sub>REF</sub> < 500MHz		0.3		Vppdiff <sup>(3)</sup>
V <sub>SWINGSRMIN</sub>	SYSREF Input Swing Minimum	f <sub>REF</sub> > 500MHz		0.6		Vppdiff <sup>(3)</sup>
V <sub>COMSRMAX</sub>	SYSREF Input Common Mode Voltage Maximum			0.8		V
V <sub>COMSRMIN</sub>	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z <sub>T</sub>	Input termination	differential		100 <sup>(1)</sup>		Ω
C <sub>L</sub>	Input capacitance	Each pin to GND		0.5		pF
<b>LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-</b>						
V <sub>ICOM</sub>	Input Common Voltage			1.2		V
V <sub>ID</sub>	Differential Input Voltage swing			450		Vppdiff <sup>(3)</sup>

## 6.8 Digital Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_T$	Input termination	differential		100		$\Omega$
<b>LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-</b>						
$V_{\text{OCOM}}$	Output Common Voltage			1.2		V
$V_{\text{OD}}$	Differential Output Voltage swing			500		$V_{\text{ppdiff}}^{(3)}$
$Z_T$	Internal Termination			100		$\Omega$

- (1) SYSREF termination is programmable between  $100\ \Omega$ ,  $150\ \Omega$  and  $300\ \Omega$
- (2) Loss tolerance is bump to bump from STX to SRX
- (3)  $V_{\text{ppdiff}}$  is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

## 6.9 Power Supply Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T2F - FDD FB 100% on, no RX TX/FB Rate: 491.52 Msps Single Band: 12x Int, FB 6x Dec $f_{\text{DAC}} = 5898.24\ \text{SPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 1.85\ \text{GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1		948.2		mA	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			533.7		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			77.3		mA	
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX				299.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC				804.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF				49.1		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				2041.3		mA
$P_{\text{diss}}$	Power Dissipation				6027.1		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 2: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 12x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 8847.36\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{OUT}}=f_{\text{IN}} = 1.9, 2.6\ \text{GHz}$ 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		820.4		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			735.2		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			74.4		mA	
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX				289.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC				822.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF				45.6		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				2263.8		mA
$P_{\text{diss}}$	Power Dissipation				6359.2		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{DAC} = 8847.36\text{MSPS}$  interleave mode;  $f_{ADC} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R2F - FDD FB 100% on TX Dual Band: 12x Int, FB 6x Dec RX Dual Band: RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{DAC} = 11796.48$ MSPS $f_{ADC} = 2949.12$ MSPS $f_{TX} = 1.85 + 2.15$ GHz $f_{RX} = 1.75 + 1.88$ GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		1668.6		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			965.1		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			77.6		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			893.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			879.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			50.7		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			3826.9		mA
$P_{diss}$	Power Dissipation			10513.0		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 4: 4T4R2F - FDD FB 100% on 7.5 GSPS DAC, 2.5 GSPS ADC Single Band: 15x Int, FB 5x Dec Dual Band: RX 20x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{DAC} = 7372.8$ MSPS $f_{ADC} = 2457.6$ MSPS $f_{TX} = 1.85 + 2.15$ GHz $f_{RX} = 1.75 + 1.88$ GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-16-16-1		1611.5	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			694.5		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			72.8		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			768.5		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			940.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			45.5		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			3000.5		mA
$P_{diss}$	Power Dissipation			9087.4		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps $f_{DAC} = 11796.48$ MSPS $f_{ADC} = 2949.12$ MSPS $f_{TX} = 3.5$ GHz $f_{RX} = 3.5$ GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1			821.8	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			808.5		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			77.4		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			289.5		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			682.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			49.0		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			2123.3		mA
$P_{diss}$	Power Dissipation			6209.3		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7a: TDD 4T1FB (RX in Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode RX 3G : 368.64M. 16 bit, Standby Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		658.1		mA	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			431.1		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			75.3		mA	
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX				189.2		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC				1041.1		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF				39.0		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				2208.7		mA
$P_{\text{diss}}$	Power Dissipation				5607.0		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 7b: TDD 4R (TX in Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, Standby RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		789.5		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			471.3		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			73.4		mA	
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX				599.3		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC				169.6		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF				39.1		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				1645.3		mA
$P_{\text{diss}}$	Power Dissipation				4851.9		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7c: TDD 4T4R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, 75% on RX 3G : 368.64M. 16 bit 25% on Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx			691.0		mA
$I_{\text{VDD1P8}}$	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			441.2		mA	
$I_{\text{VDD1P8}}$	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			74.8		mA	
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX				291.7		mA
$I_{\text{VDD1P2}}$	Group 2B: VDD1P2TXCLK + VDD1P2TXENC				823.2		mA
$I_{\text{VDD1P2}}$	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF				39.0		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				2067.9		mA
$P_{\text{diss}}$	Power Dissipation				5418.2		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{DAC} = 8847.36\text{MSPS}$  interleave mode;  $f_{ADC} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7d: FDD 4T4R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		1283.8		mA
$I_{VDD1P8}$	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			752.0		mA
$I_{VDD1P8}$	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			74.6		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			750.5		mA
$I_{VDD1P2}$	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1077.6		mA
$I_{VDD1P2}$	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			47.7		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			2695.5		mA
$P_{diss}$	Power Dissipation			8475.5		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 8: same configuration as mode 7, Sleep Mode. SLEEP pin is pull high.		20.3		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			292.8		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			12.6		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			4.6		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			54.3		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			15.3		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			313.1		mA
$P_{diss}$	Power Dissipation			956.8		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 9: 4T4R2F - FDD FB 100% on TX Single Band: 24x Int, FB 12x Dec RX Single Band: RX 24x TX/FB Rate 245.76 Msp RX Rate 122.88 Msp $f_{DAC} = 5898.24\text{MSPS}$ $f_{ADC} = 2949.12\text{MSPS}$ $f_{TX} = 0.85\text{GHz}$ $f_{RX} = 0.8\text{GHz}$ 8/10 coding, 9.8304Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-8-8-1		1593.2	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			840.6		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			77.3		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			905.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			817.7		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			52.1		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			2405.2		mA
$P_{diss}$	Power Dissipation			8814.3		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10: 4T4R2F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msps RX Rate 245.76 Msps $f_{\text{DAC}} = 8847.36\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 1.85\text{ GHz}$ $f_{\text{RX}} = 1.75\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 8-8-2-1, FB: 4-4-2-1, RX: 4-8-4-1	1626.2			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		976.4			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		74.6			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX		902.7			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		1111.9			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		48.0			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		3578.9			mA
$P_{\text{diss}}$	Power Dissipation		10515.0			mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 11a: TDD 4T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	800		
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8	840				mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0	73				mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	190				mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC	1440				mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF	75				mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9	3070				mA
$P_{\text{diss}}$	Power Dissipation	8010				mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2		750		
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		890			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		72			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX		610			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		280			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		72			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		2360			mA
$P_{\text{diss}}$	Power Dissipation		6460			mW



## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11c: TDD 4T4R1FB average TX/FB: 75%, RX 25% Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48$ MSPS $f_{\text{ADC}} = 2949.12$ MSPS $f_{\text{TX}} = f_{\text{RX}} = 8$ GHz 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2		790		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			850		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			73		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			300		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1150		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			75		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			2890		mA
$P_{\text{diss}}$	Power Dissipation			7620		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 11d: FDD 4T4R Single Band: 8x Int, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48$ MSPS $f_{\text{ADC}} = 2949.12$ MSPS $f_{\text{TX}} = f_{\text{RX}} = 8$ GHz 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2		1260	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			940		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			73		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			630		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1480		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			78		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			4200		mA
$P_{\text{diss}}$	Power Dissipation			10640		mW

## 6.10 Timing Requirements

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
<b>Timing: SYSREF+/-</b>					
$t_{\text{s}}(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{\text{h}}(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
<b>Timing: Serial ports</b>					
$t_{\text{s}}(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK		15		ns
$t_{\text{h}}(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK <sup>(1)</sup>		$5 + t_{\text{sCLK}}$		ns
$t_{\text{s}}(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{\text{h}}(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{\text{s}}(\text{SCLK\_W})$	Minimum SCLK period: registers write		25		ns
$t_{\text{s}}(\text{SCLK\_R})$	Minimum SCLK period: registers read		50		ns
$t_{\text{d}}(\text{data\_out})$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
$t_{\text{RESET}}$	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\ need to be held one more extra clock cycle with the last SCLK edge

## 6.11 Switching Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

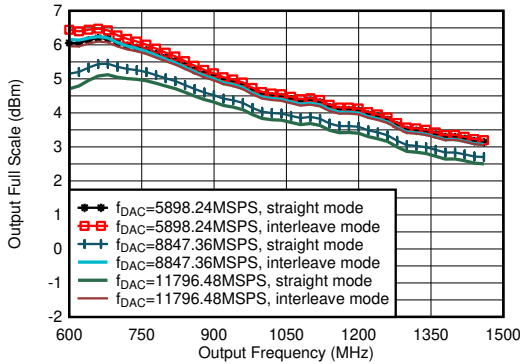
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TX Channel Latency</b>						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
$t_{\text{JESD TX}}$	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles <sup>(1)</sup>
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
<b>RX Channel Latency</b>						
	SerDes Transmitter Analog Delay			3.6		ns
$t_{\text{JESD RX}}$	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles <sup>(1)</sup>
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
<b>FB Channel Latency</b>						
	SerDes Transmitter Analog Delay			3.6		ns
$t_{\text{JESD FB}}$	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles <sup>(1)</sup>
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

## 6.12 Typical Characteristics

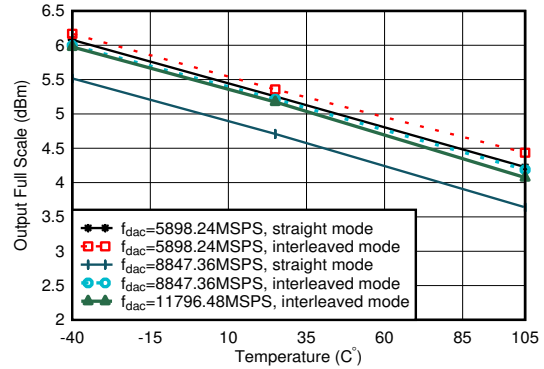
### 6.12.1 TX Typical Characteristics 800 MHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



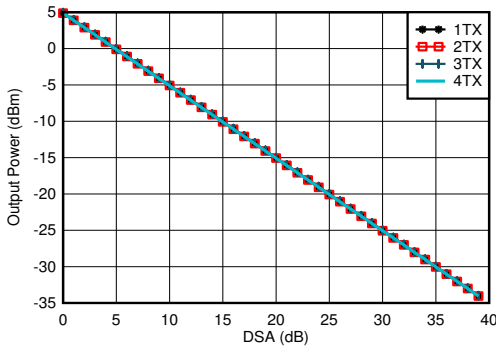
including PCB and cable losses,  $A_{\text{out}} = -0.5\text{dBFS}$ , DSA = 0, 0.8 GHz matching

图 6-1. TX Output Fullscale vs Output Frequency



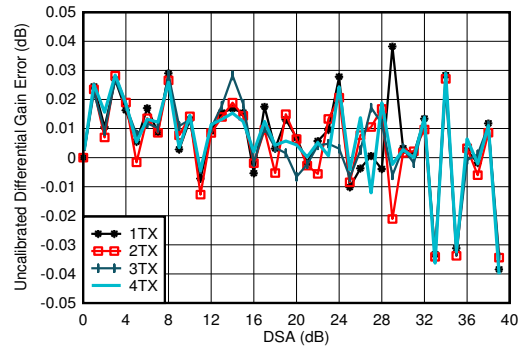
including PCB and cable losses,  $A_{\text{out}} = -0.5\text{dBFS}$ , DSA = 0, 0.8 GHz matching

图 6-2. TX Output Fullscale vs Temperature



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{out}} = -0.5\text{dBFS}$ , matching 0.8 GHz

图 6-3. TX Output Power vs DSA Setting and Channel at 0.85 GHz

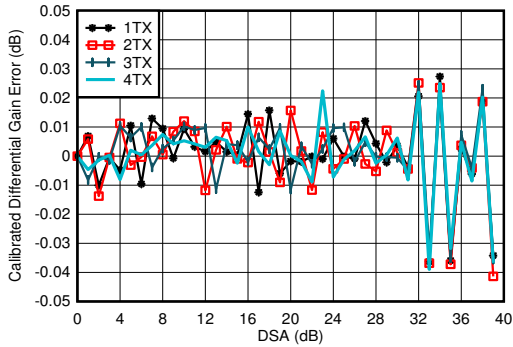


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-4. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz

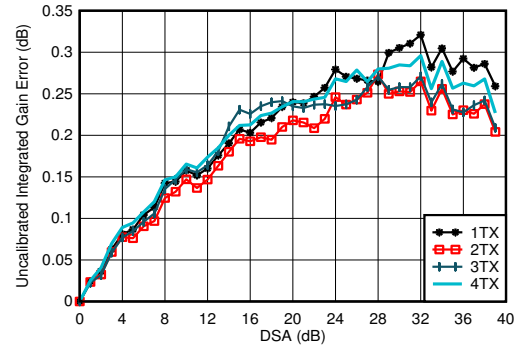
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



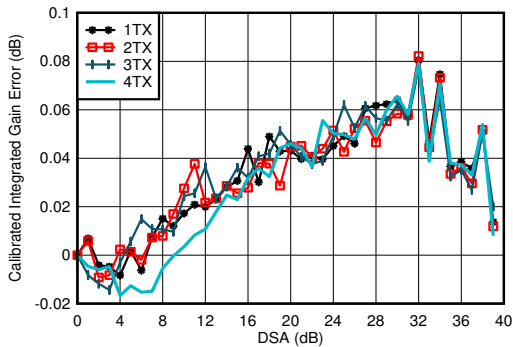
$f_{\text{DAC}}=5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-5. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



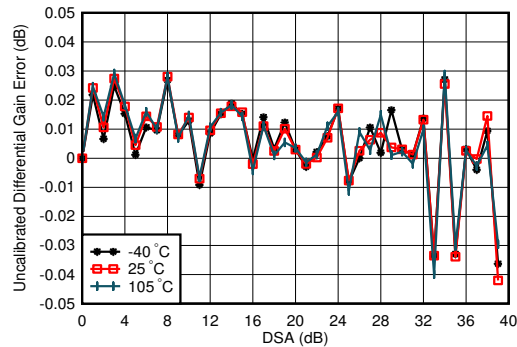
$f_{\text{DAC}}=5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Settings}$

图 6-6. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



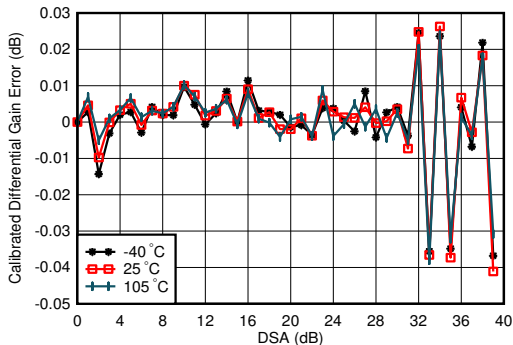
$f_{\text{DAC}}=5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

图 6-7. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



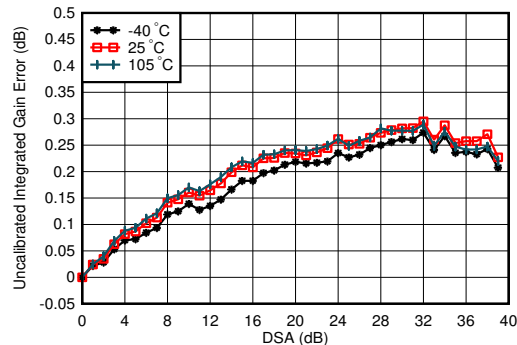
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-8. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-9. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz

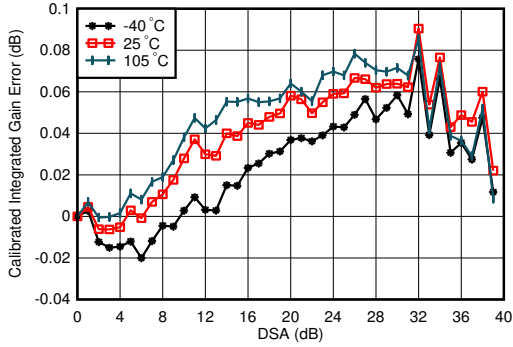


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

图 6-10. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz

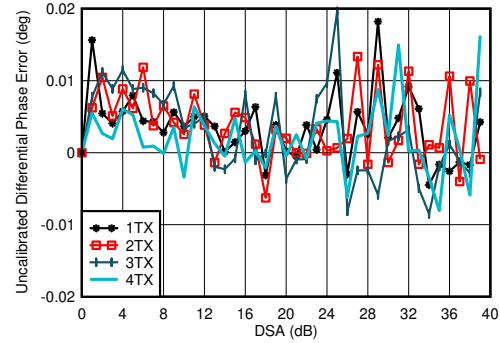
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



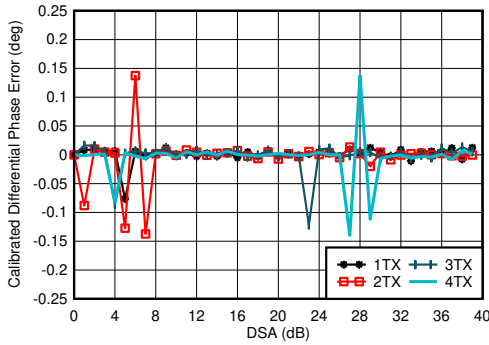
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

图 6-11. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz



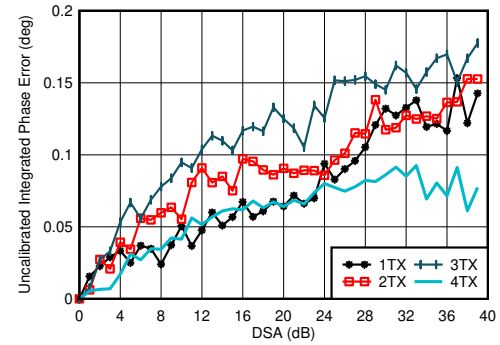
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-12. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
Phase DNL spike may occur at any DSA setting.

图 6-13. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz

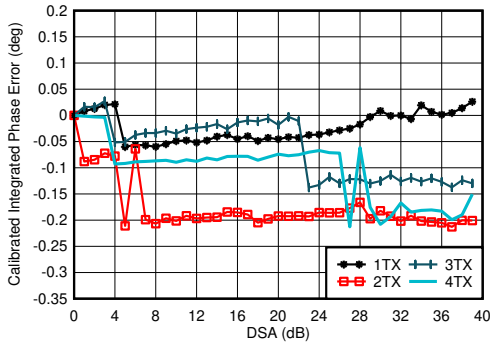


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

图 6-14. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz

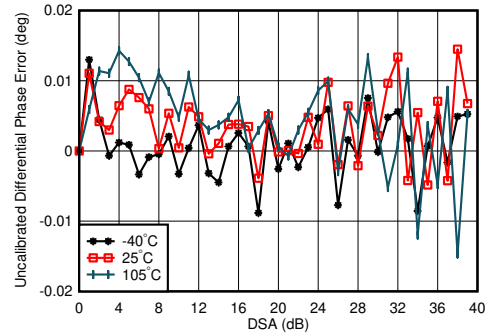
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



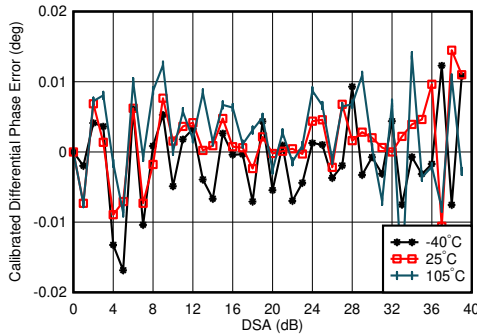
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

图 6-15. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



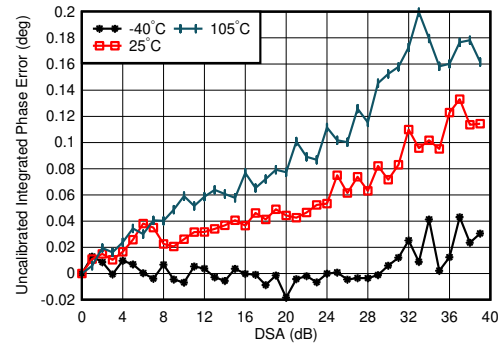
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-16. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-17. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz

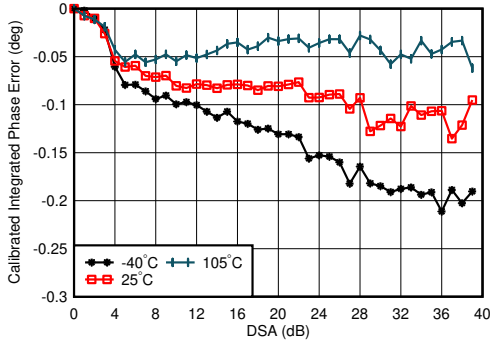


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

图 6-18. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz

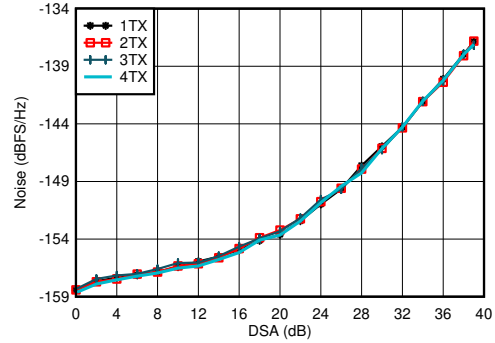
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



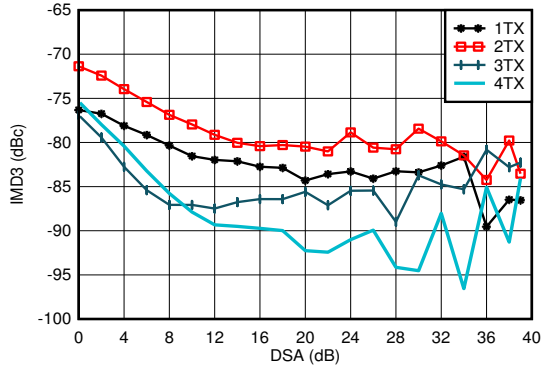
$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{OUT}(\text{DSA Setting}) - \text{Phase}_{OUT}(\text{DSA Setting} = 0)$

图 6-19. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



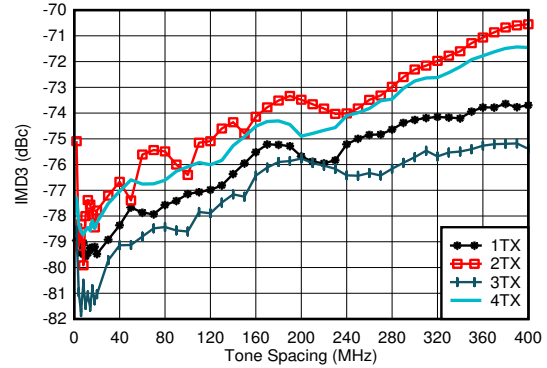
$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz,  
 $P_{OUT} = -13\text{ dBFS}$

图 6-20. TX Output Noise vs Channel and Attenuation at 0.85 GHz



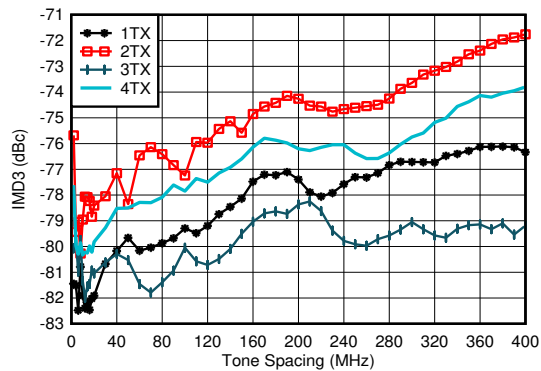
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 0.85\text{ GHz}$ ,  
matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone

图 6-21. TX IMD3 vs DSA Setting at 0.85 GHz



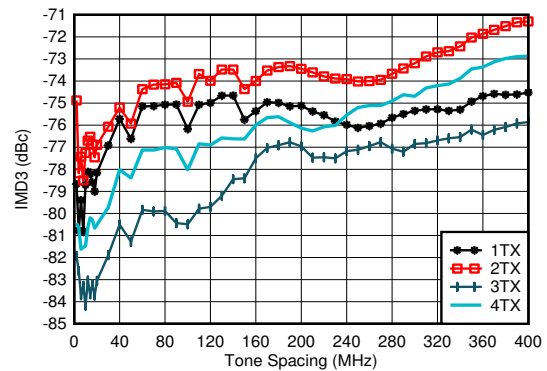
$f_{DAC} = 5898.24\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{ GHz}$ ,  
matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone

图 6-22. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



$f_{DAC} = 8847.36\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{ GHz}$ ,  
matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone

图 6-23. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



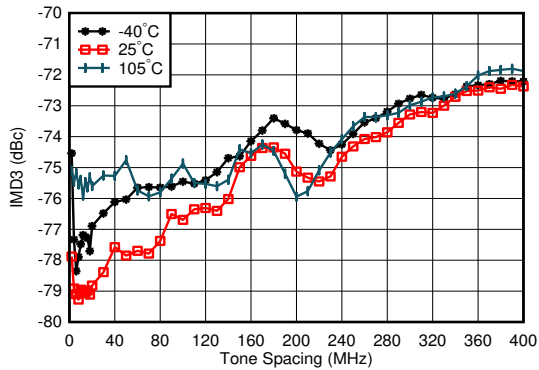
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 0.85\text{ GHz}$ ,  
matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone

图 6-24. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



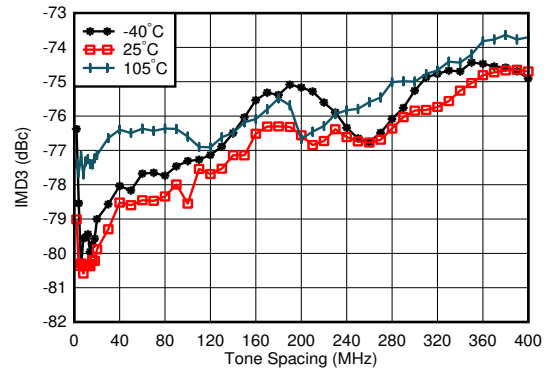
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



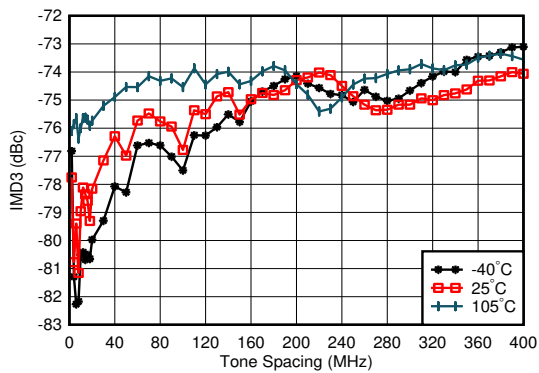
$f_{DAC} = 5898.24\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone, worst channel

图 6-25. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



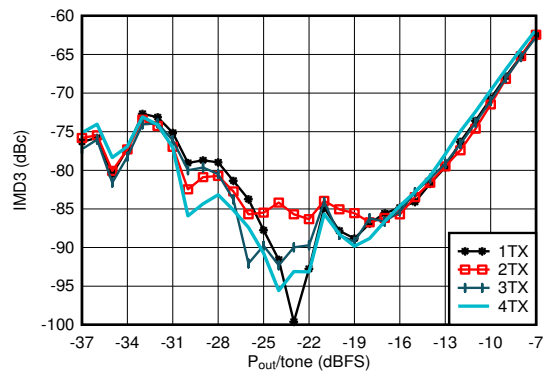
$f_{DAC} = 8847.36\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone, worst channel

图 6-26. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



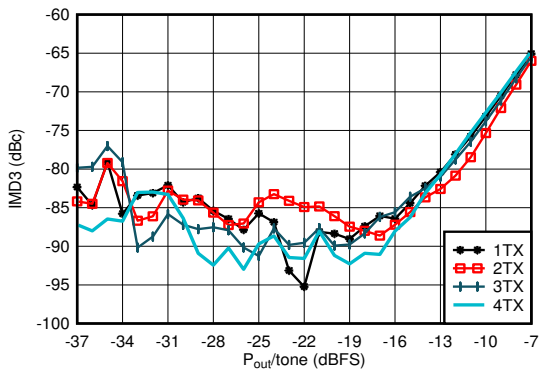
$f_{DAC} = 11796.48\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone, worst channel

图 6-27. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



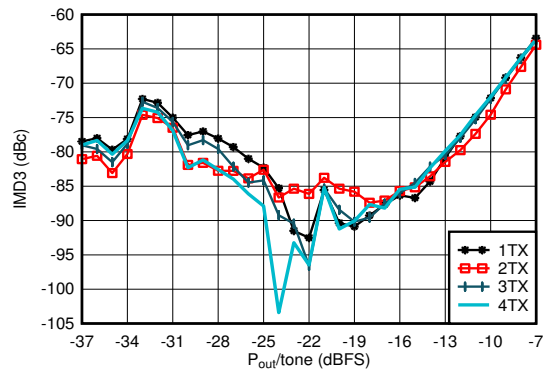
$f_{DAC} = 5898.24\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{ GHz}$ ,  $f_{SPACING} = 20\text{ MHz}$ , matching at 0.8 GHz

图 6-28. TX IMD3 vs Digital Level at 0.85 GHz



$f_{DAC} = 8847.36\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{ GHz}$ ,  $f_{SPACING} = 20\text{ MHz}$ , matching at 0.8 GHz

图 6-29. TX IMD3 vs Digital Level at 0.85 GHz

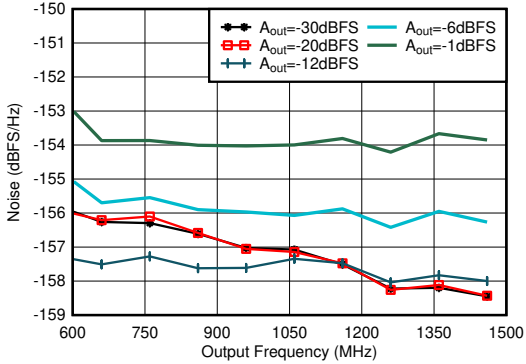


$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 0.85\text{ GHz}$ ,  $f_{SPACING} = 20\text{ MHz}$ , matching at 0.8 GHz

图 6-30. TX IMD3 vs Digital Level at 0.85 GHz

### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



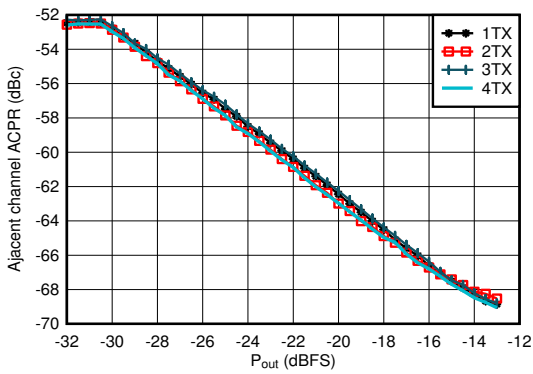
Matching at 2.6 GHz, Single tone,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset, DSA = 0dB

图 6-31. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz



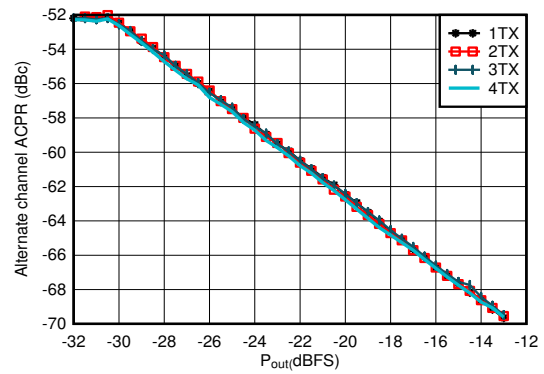
TM1.1,  $P_{OUT\_RMS} = -13\text{ dBFS}$

图 6-32. TX 20-MHz LTE Output Spectrum at 0.85 GHz



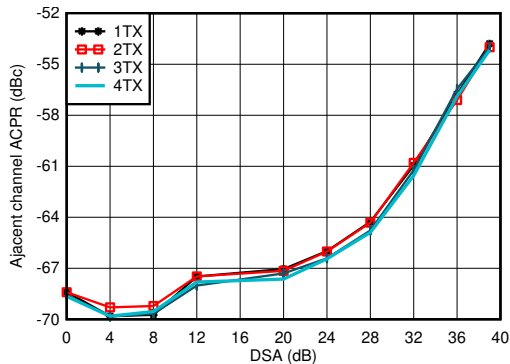
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-33. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz



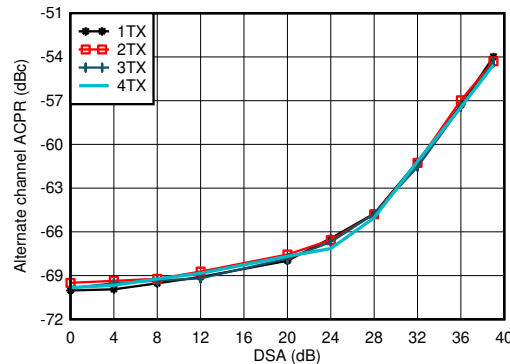
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-34. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz



Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-35. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz

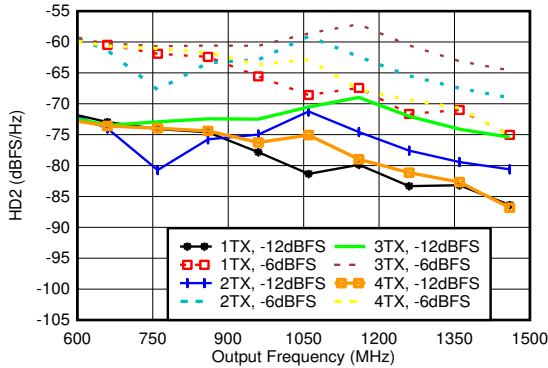


Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-36. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz

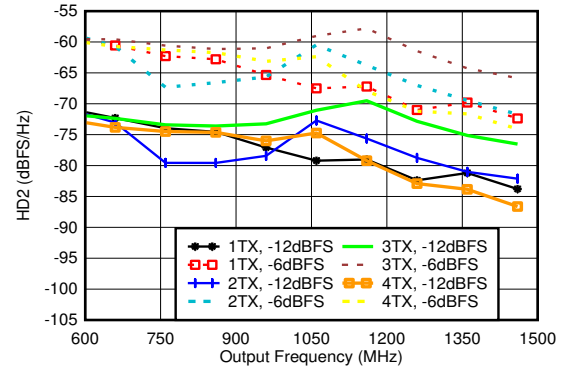
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



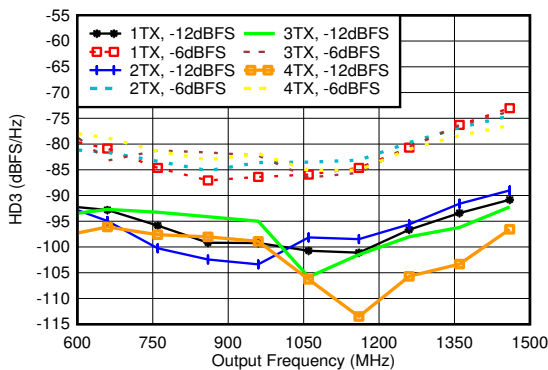
Matching at 0.8 GHz,  $f_{DAC} = 5898.24\text{GSPS}$ , straight mode

图 6-37. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



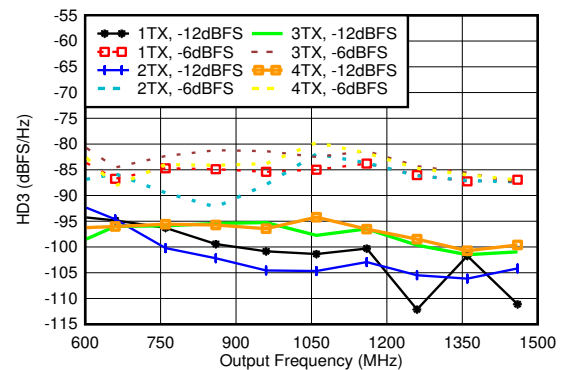
Matching at 0.8 GHz,  $f_{DAC} = 8847.36\text{GSPS}$ , straight mode

图 6-38. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



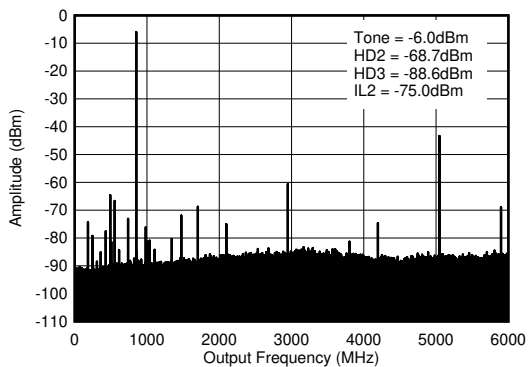
Matching at 0.8 GHz,  $f_{DAC} = 5898.24\text{MSPS}$ , straight mode, normalized to output power at harmonic frequency

图 6-39. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



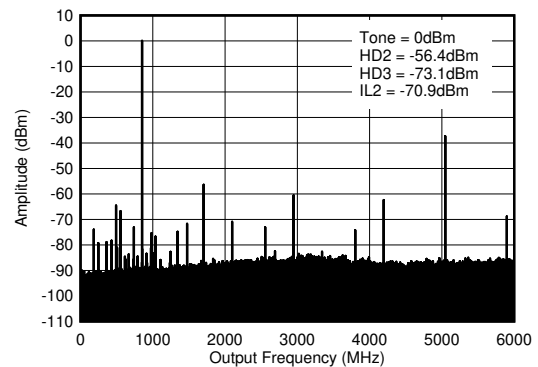
Matching at 0.8 GHz,  $f_{DAC} = 8847.36\text{MSPS}$ , straight mode, normalized to output power at harmonic frequency

图 6-40. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$ .

图 6-41. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{DAC}$ )

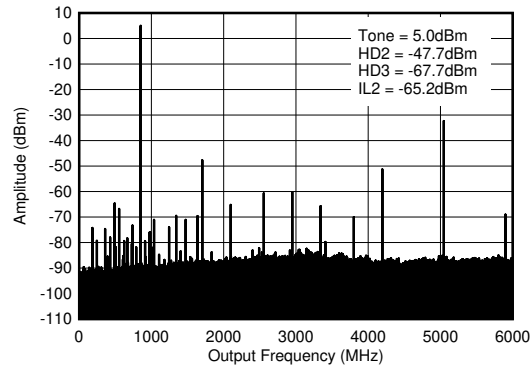


$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$ .

图 6-42. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{DAC}$ )

### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled

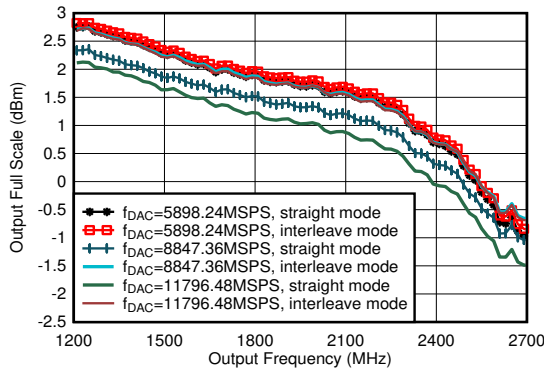


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

图 6-43. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )

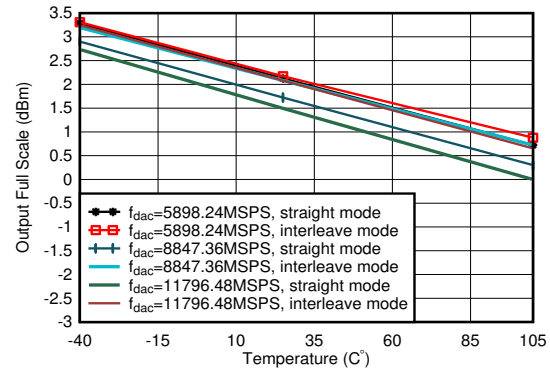
### 6.12.2 TX Typical Characteristics at 1.8 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



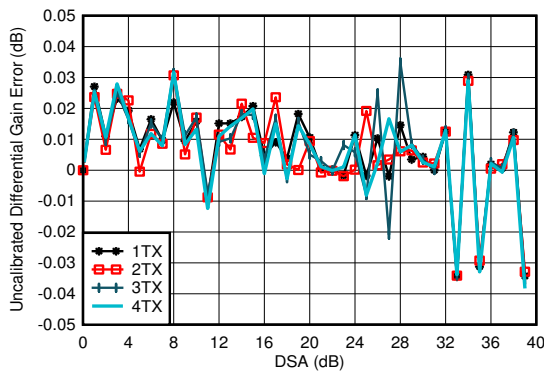
including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 1.8 GHz matching

图 6-44. TX Output Fullscale vs Output Frequency



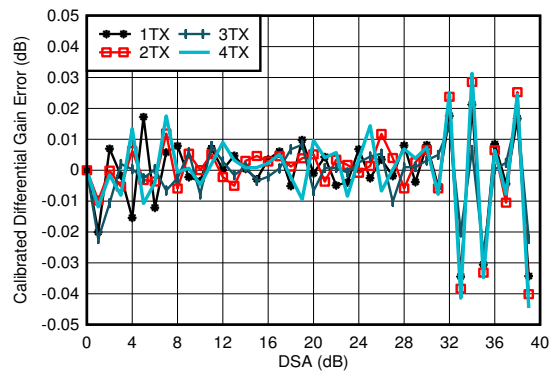
$A_{out} = -0.5\text{dBFS}$ , matching 1.8 GHz

图 6-45. TX Output Power vs Temperature at 1.8 GHz



$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

图 6-46. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz

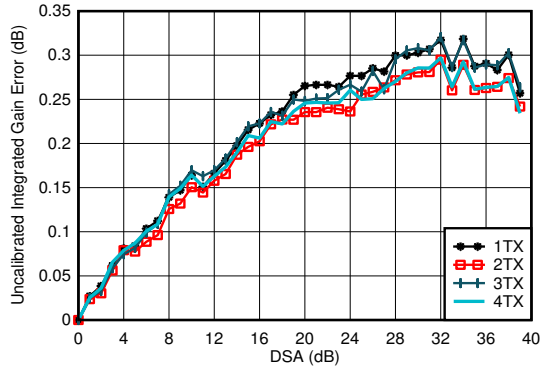


$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

图 6-47. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz

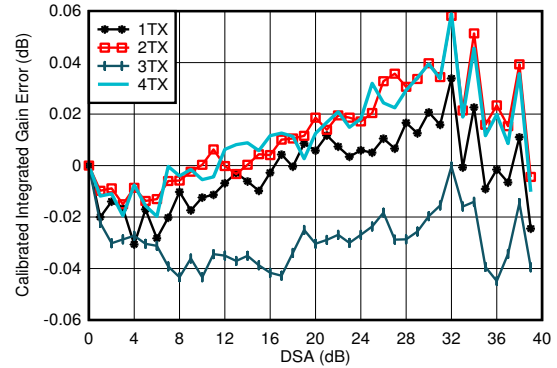
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



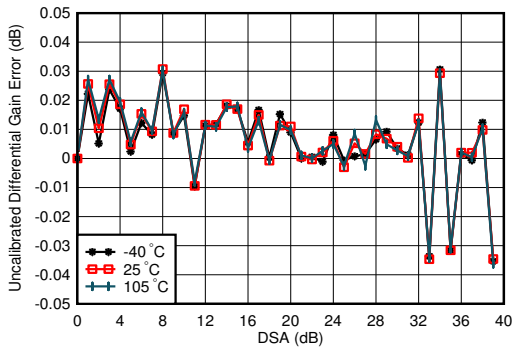
$f_{\text{DAC}}=5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-48. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz



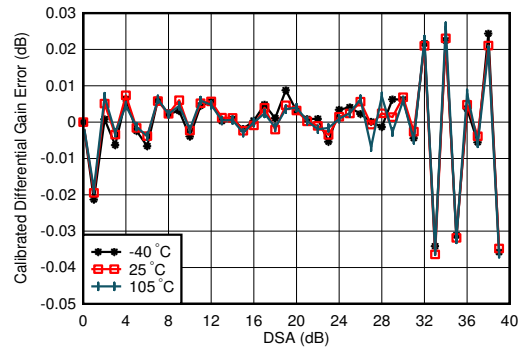
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-49. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-50. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz

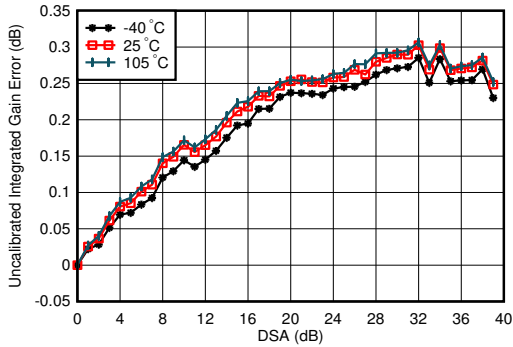


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-51. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz

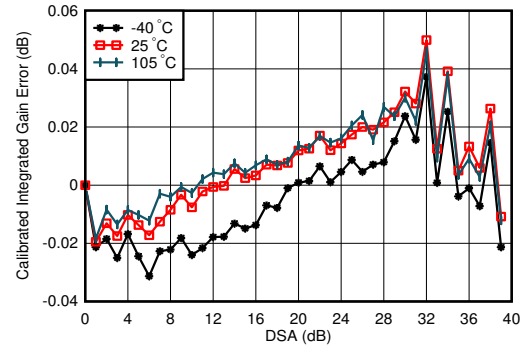
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



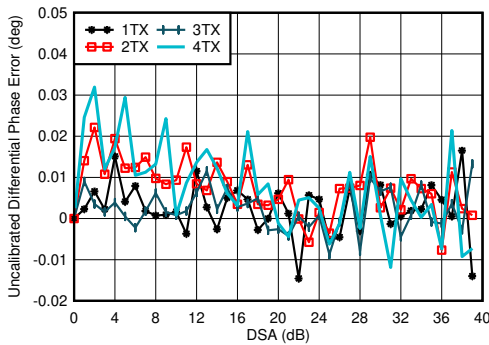
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-52. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz



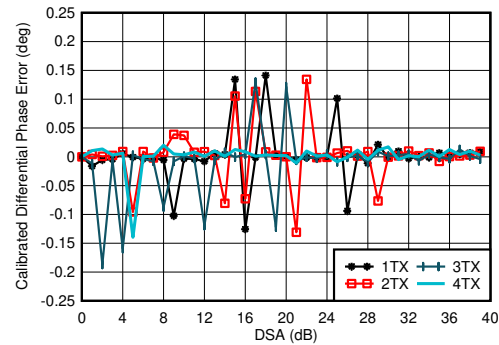
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-53. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-54. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz

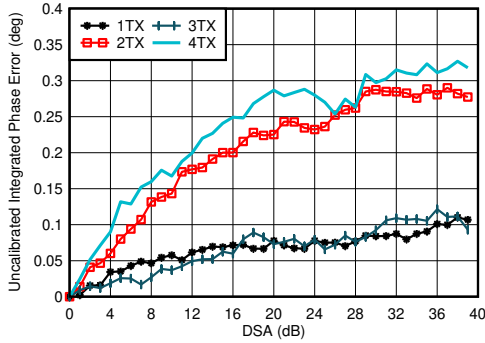


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
Phase DNL spike may occur at any DSA setting.

图 6-55. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz

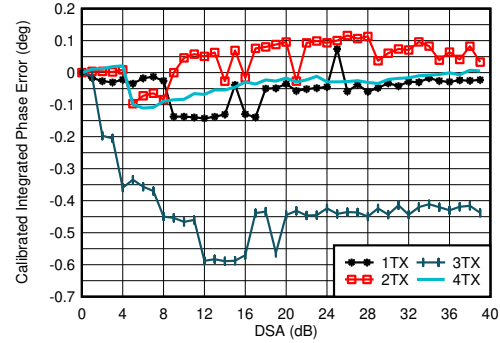
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



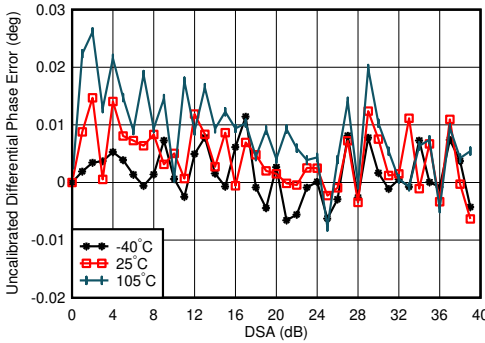
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-56. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz



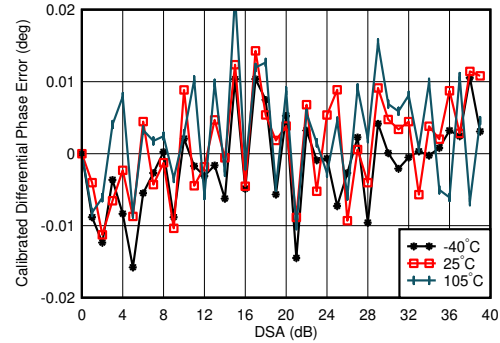
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-57. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-58. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz



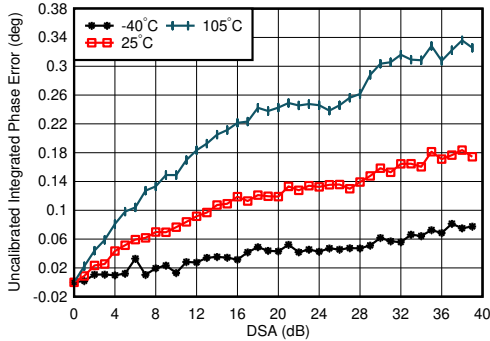
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-59. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz



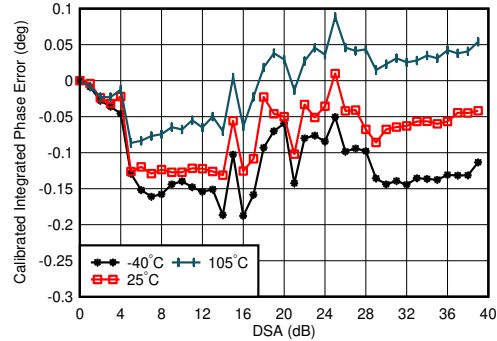
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



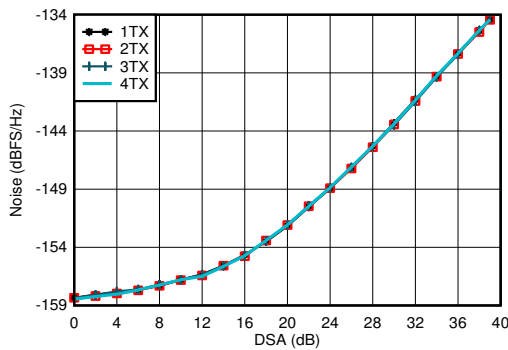
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-60. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz



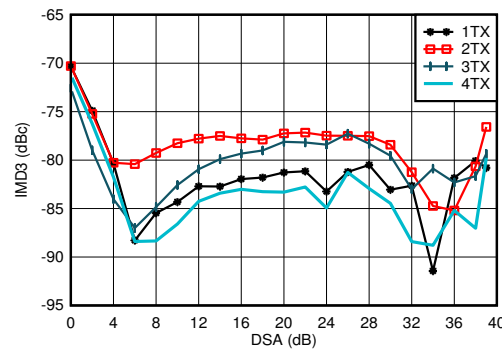
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-61. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz



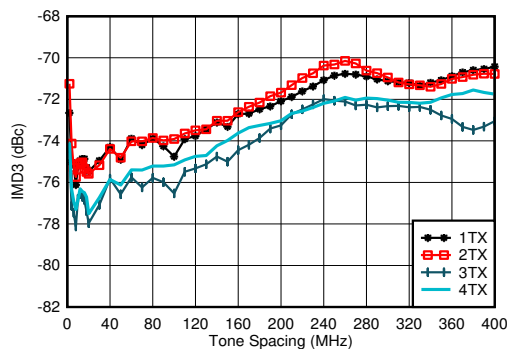
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8 GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

图 6-62. TX Output Noise vs Channel and Attenuation at 1.8 GHz



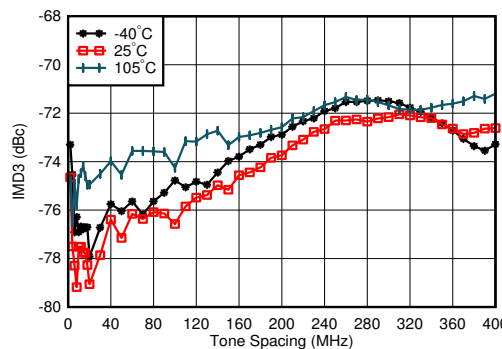
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 1.8\text{ GHz}$ , matching at 1.8 GHz,  $-13\text{ dBFS}$  each tone

图 6-63. TX IMD3 vs DSA Setting at 1.8 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 1.8\text{ GHz}$ , matching at 1.8 GHz,  $-13\text{ dBFS}$  each tone

图 6-64. TX IMD3 vs Tone Spacing and Channel at 1.8 GHz

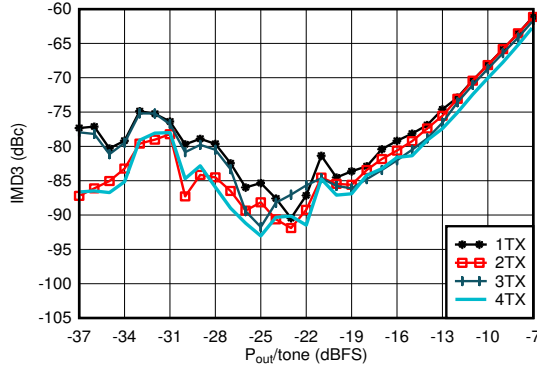


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 1.8\text{ GHz}$ , matching at 1.8 GHz,  $-13\text{ dBFS}$  each tone, worst channel

图 6-65. TX IMD3 vs Tone Spacing and Temperature at 1.8 GHz

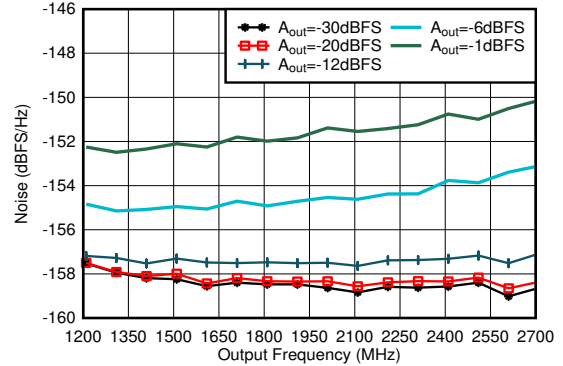
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



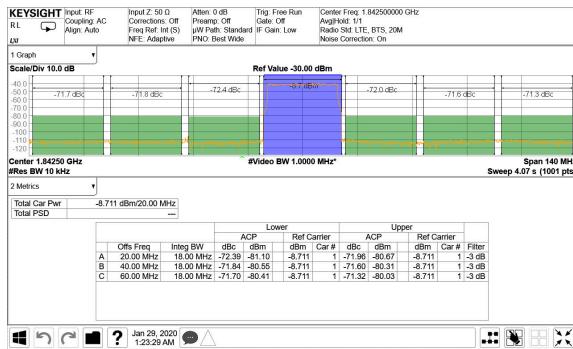
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 1.8\text{ GHz}$ ,  
 $f_{SPACING} = 20\text{ MHz}$ , matching at 1.8 GHz

图 6-66. TX IMD3 vs Digital Level at 1.8 GHz



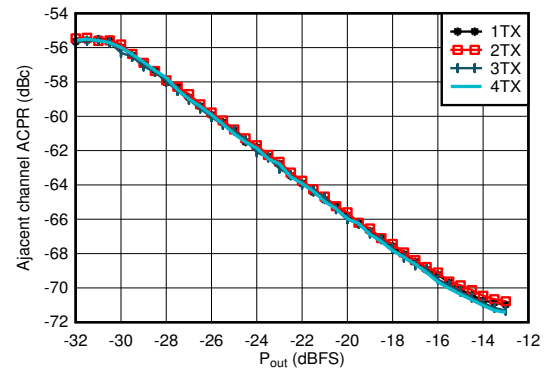
Matching at 2.6 GHz, Single tone,  $f_{DAC} = 11.79648\text{GSPS}$ ,  
interleave mode, 40-MHz offset

图 6-67. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz



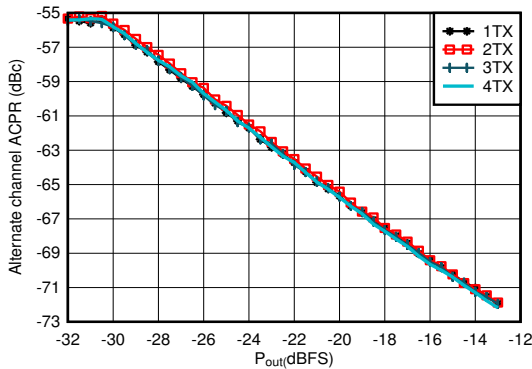
TM1.1,  $P_{OUT\_RMS} = -13\text{ dBFS}$

图 6-68. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



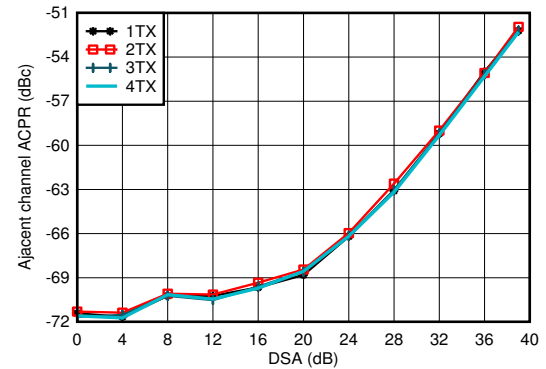
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-69. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-70. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz

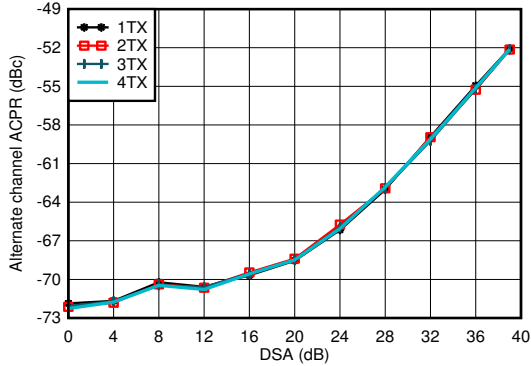


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-71. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz

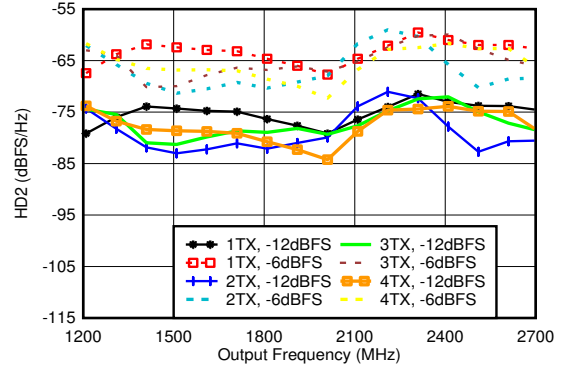
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



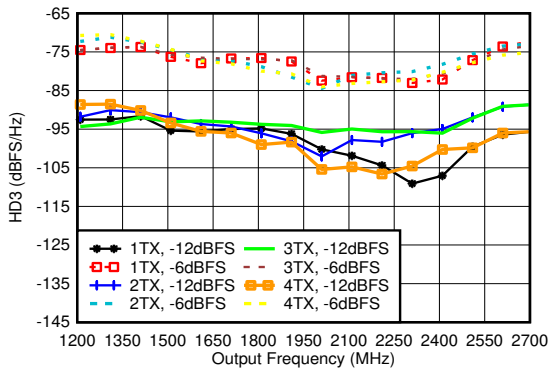
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-72. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz



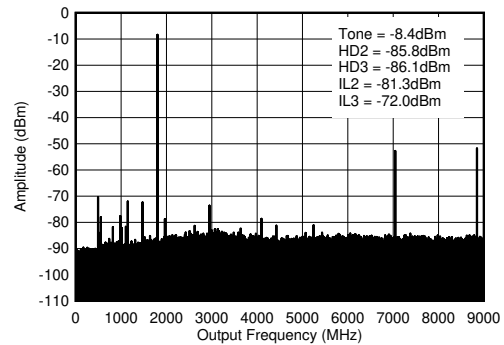
Matching at 1.8 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

图 6-73. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz



Matching at 1.8 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

图 6-74. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz

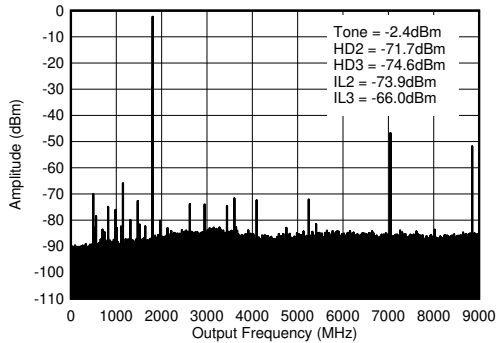


$f_{DAC} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$  and is due to mixing with digital clocks.

图 6-75. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{DAC}$ )

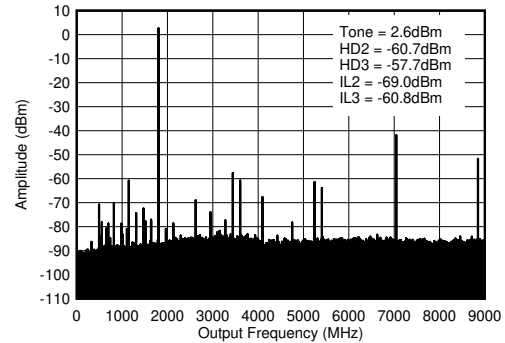
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

图 6-76. TX Single Tone ( - 6 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{\text{DAC}}$ )

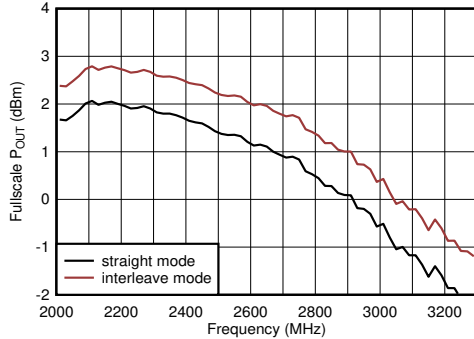


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

图 6-77. TX Single Tone ( - 1 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{\text{DAC}}$ )

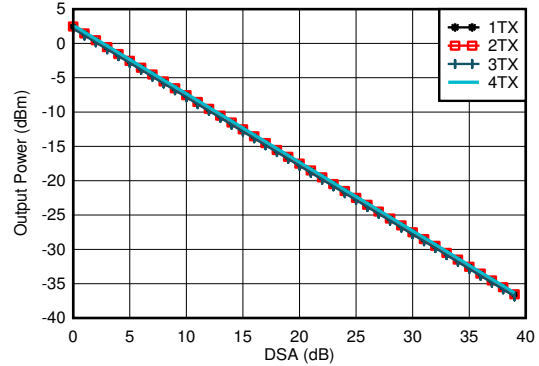
### 6.12.3 TX Typical Characteristics at 2.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



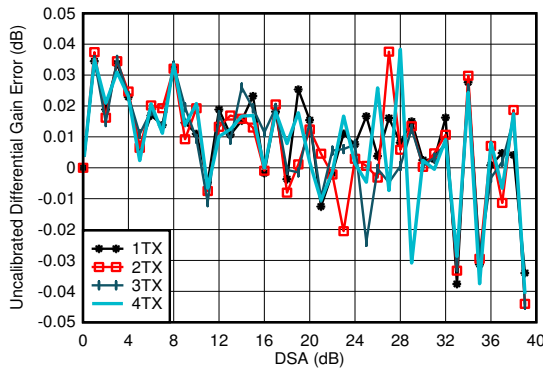
Including PCB and cable losses,  $A_{\text{out}} = -0.5\text{dBFS}$ , DSA = 0, 2.6 GHz matching

**图 6-78. TX Full Scale vs RF Frequency at 11796.48MSPS**



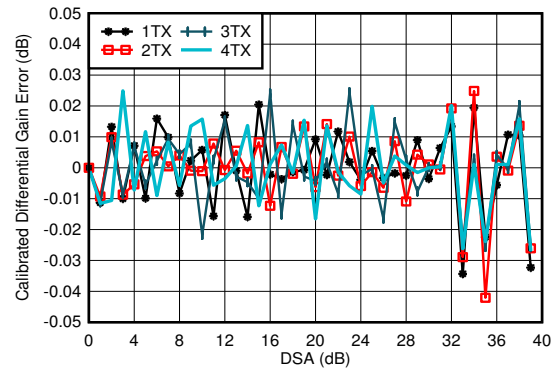
$f_{\text{DAC}} = 8847.36\text{ MSPS}$ ,  $A_{\text{out}} = -0.5\text{dBFS}$ , matching 2.6 GHz

**图 6-79. TX Output Power vs DSA Setting and Channel at 2.6 GHz**



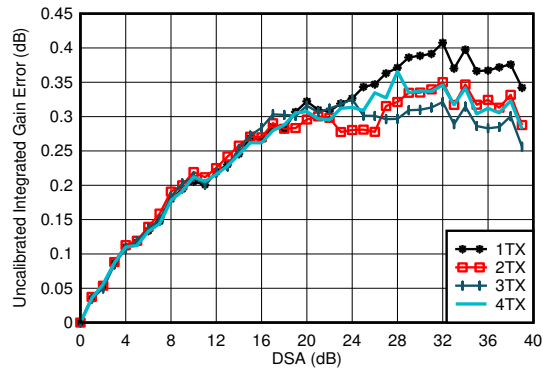
$f_{\text{DAC}}=8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**图 6-80. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz**



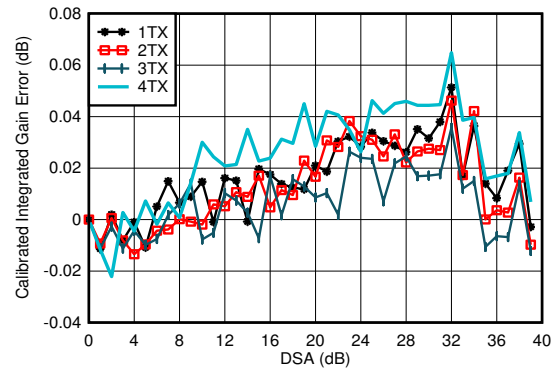
$f_{\text{DAC}}=8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**图 6-81. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz**



$f_{\text{DAC}}=8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**图 6-82. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz**

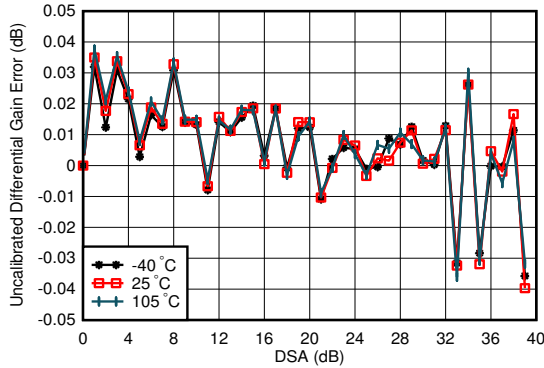


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**图 6-83. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz**

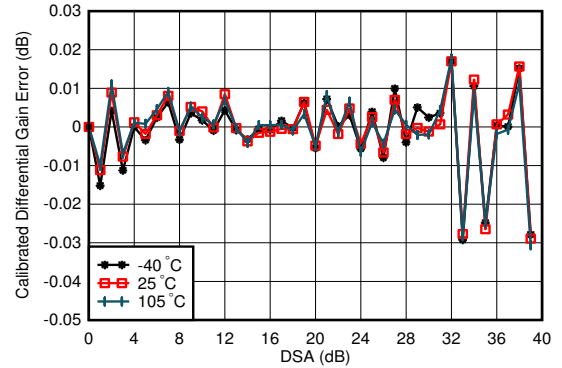
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



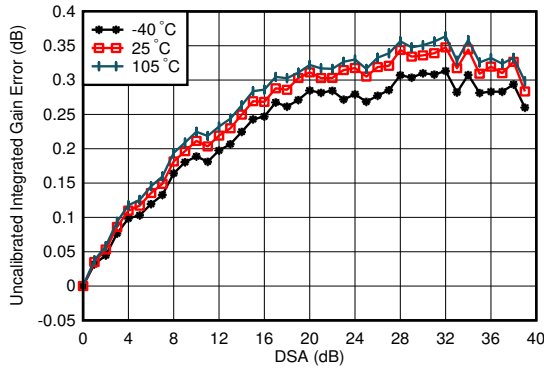
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-84. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



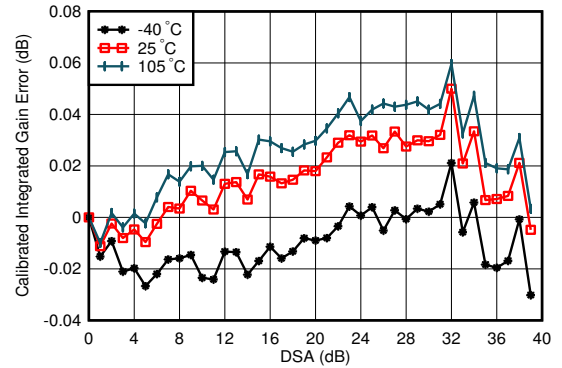
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-85. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-86. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

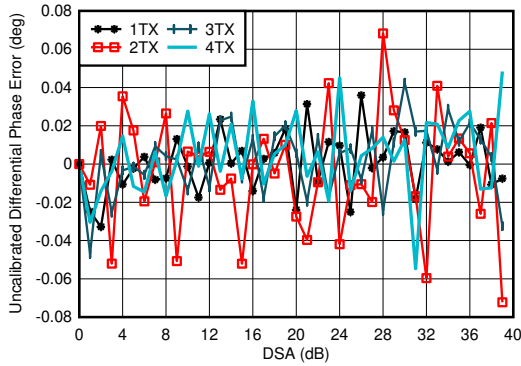


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-87. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

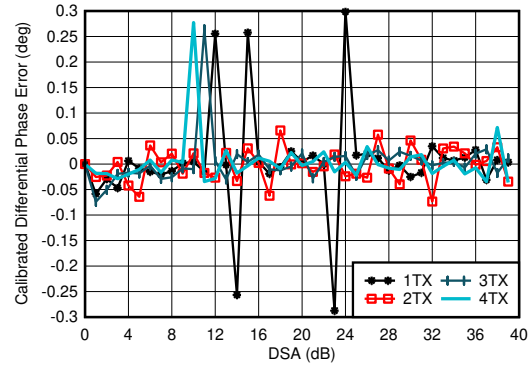
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



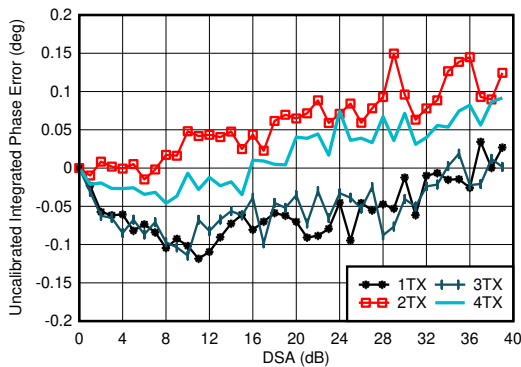
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-88. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



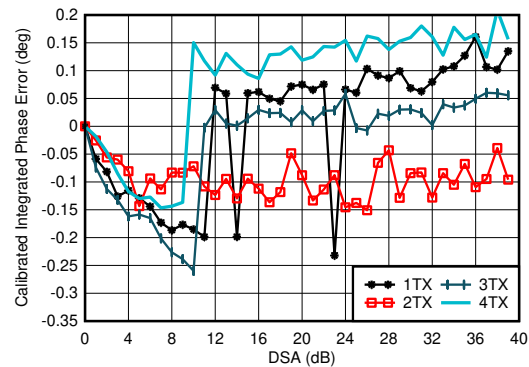
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
Phase DNL spike may occur at any DSA setting.

图 6-89. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-90. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

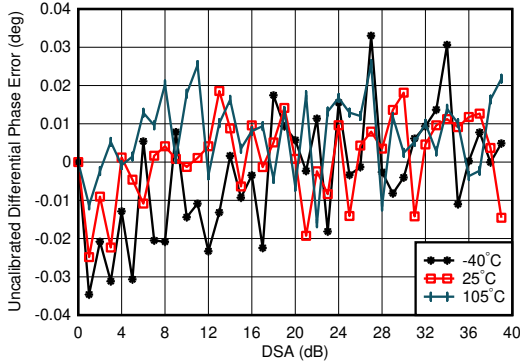


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-91. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

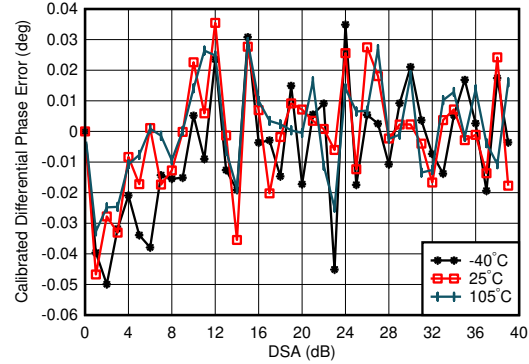
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



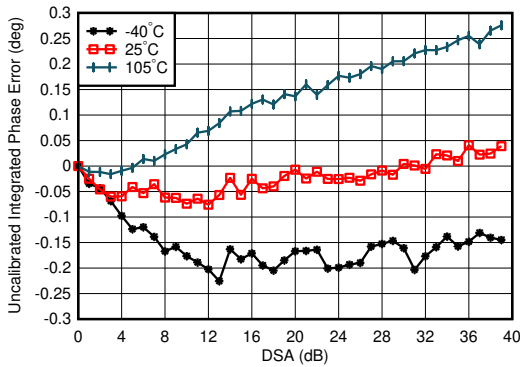
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-92. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



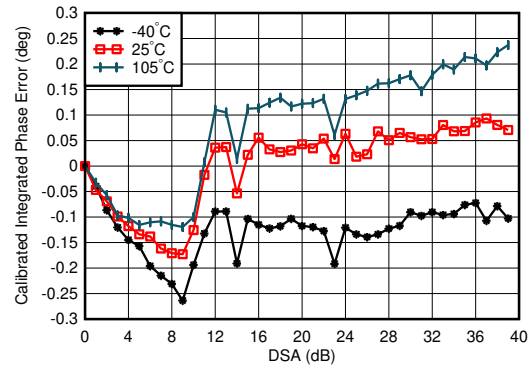
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-93. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at 25°C  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-94. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



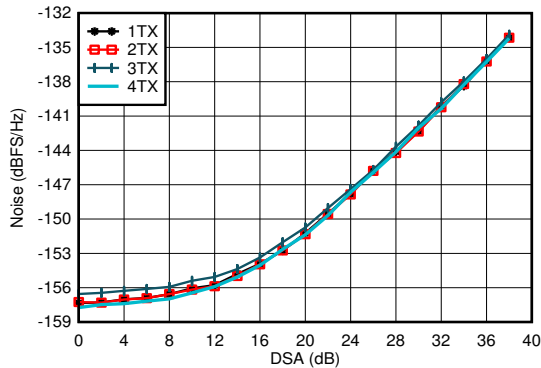
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-95. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



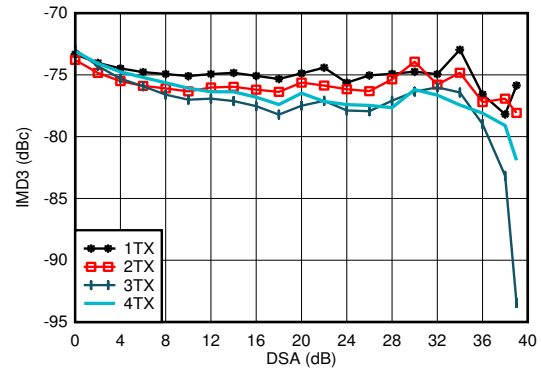
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



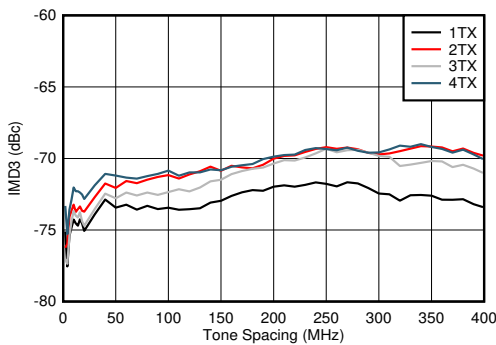
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

图 6-96. TX Output Noise vs Channel and Attenuation at 2.6 GHz



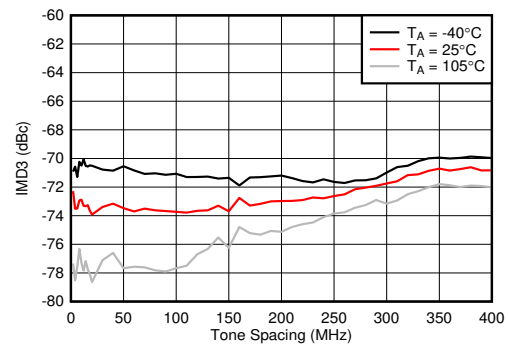
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ , matching at 2.6 GHz,  $-13\text{ dBFS}$  each tone

图 6-97. TX IMD3 vs DSA Setting at 2.6 GHz



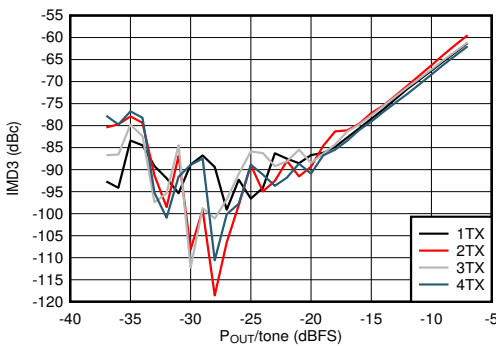
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ , matching at 2.6 GHz,  $-13\text{ dBFS}$  each tone

图 6-98. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz



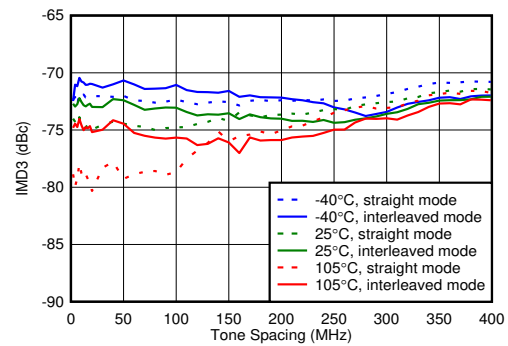
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ , matching at 2.6 GHz,  $-13\text{ dBFS}$  each tone, worst channel.

图 6-99. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ ,  $f_{\text{SPACING}} = 20\text{ MHz}$ , matching at 2.6 GHz

图 6-100. TX IMD3 vs Digital Level at 2.6 GHz

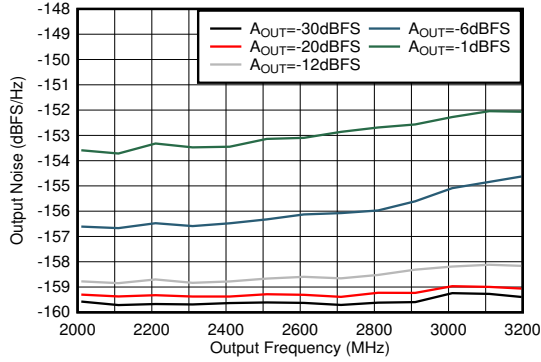


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ , matching at 2.6 GHz,  $-13\text{ dBFS}$  each tone

图 6-101. TX IMD3 vs Tone Spacing and Temperature

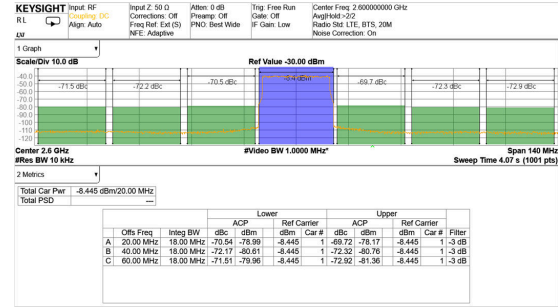
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



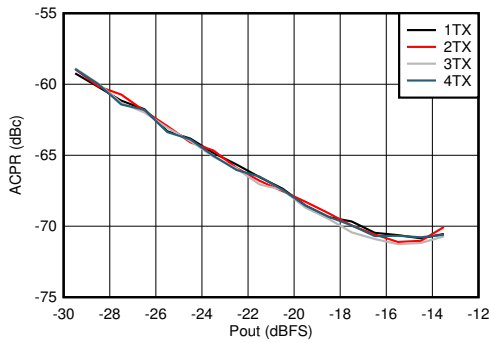
Matching at 2.6 GHz, Single tone,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset

图 6-102. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz



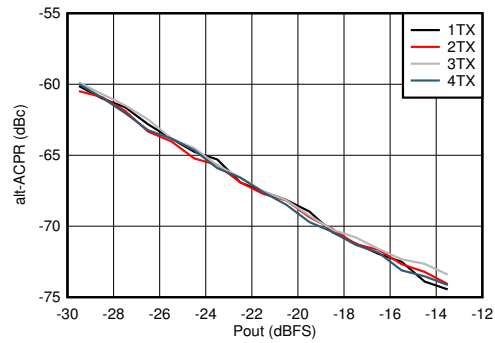
TM1.1,  $P_{OUT\_RMS} = -13\text{ dBFS}$

图 6-103. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)



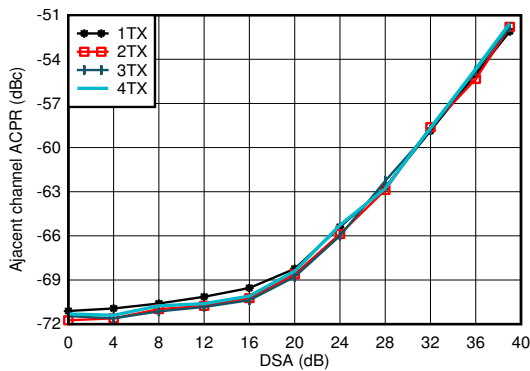
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-104. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz



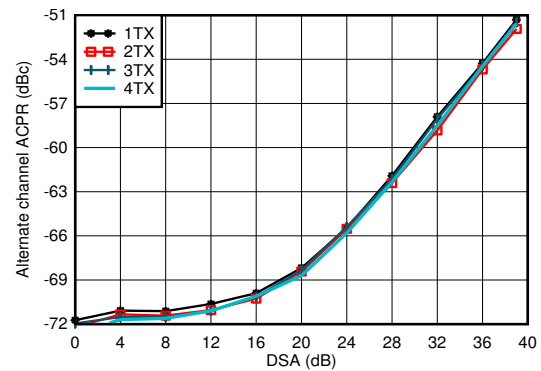
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-105. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-106. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz

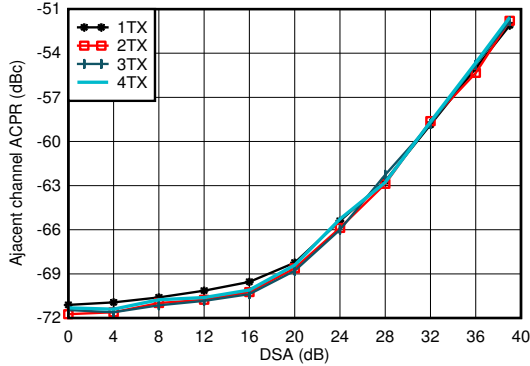


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-107. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz

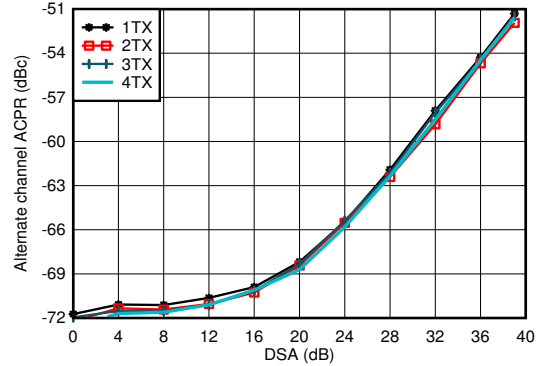
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



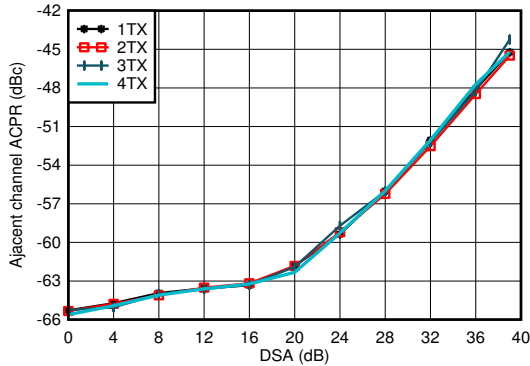
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-108. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



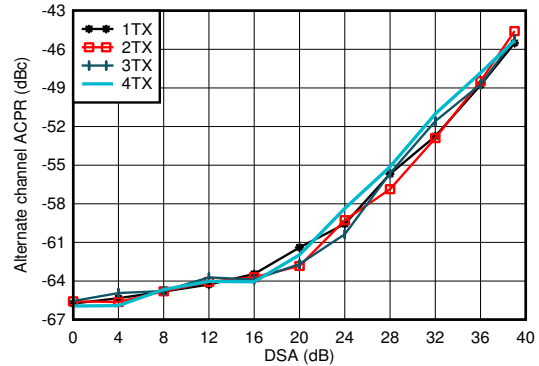
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-109. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



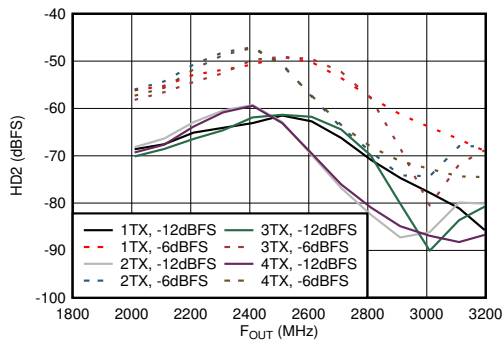
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

图 6-110. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



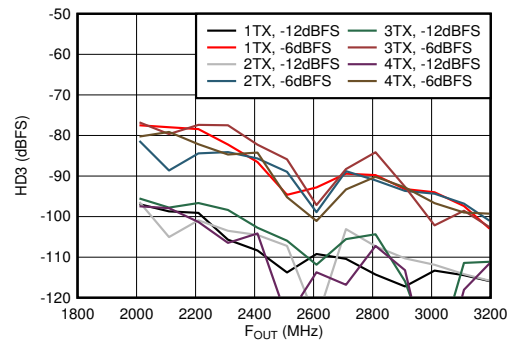
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

图 6-111. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

图 6-112. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz

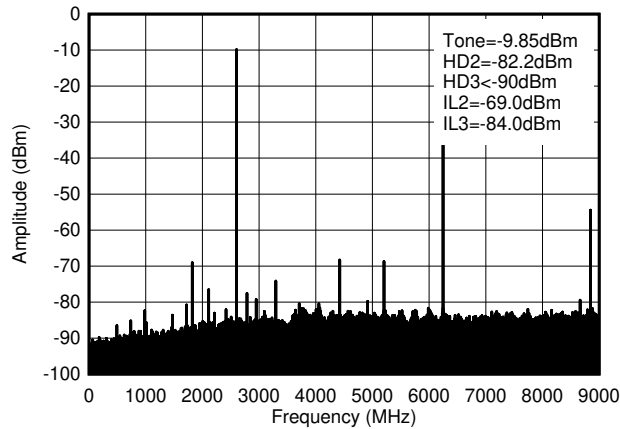


Matching at 2.6 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

图 6-113. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz

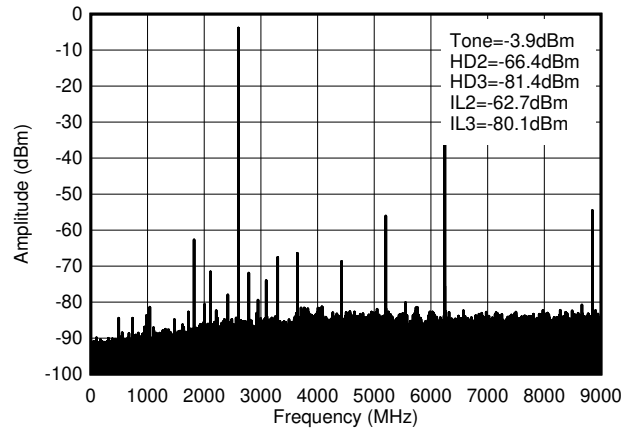
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



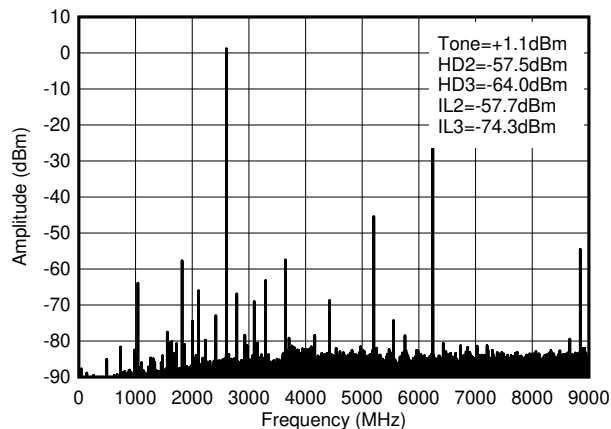
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

图 6-114. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )



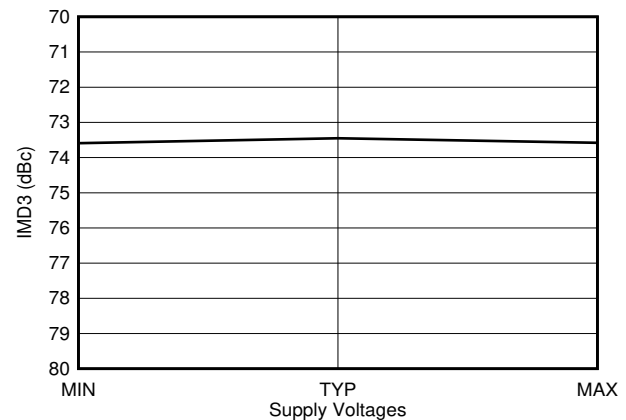
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

图 6-115. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

图 6-116. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )

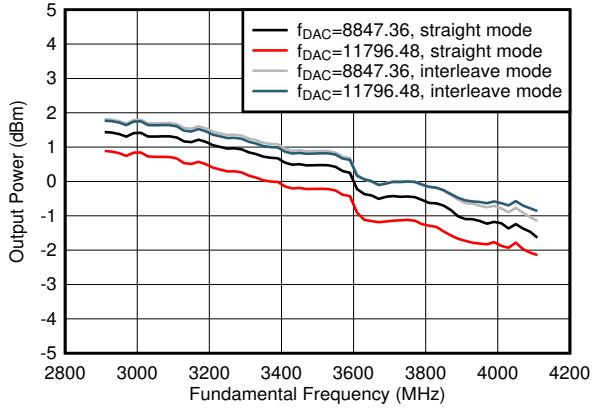


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = -13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

图 6-117. TX IMD3 vs Supply Voltage at 2.6 GHz

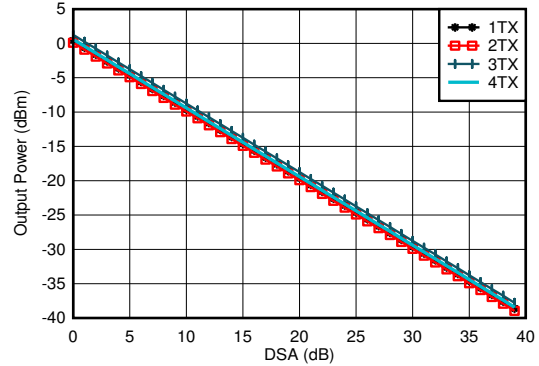
### 6.12.4 TX Typical Characteristics at 3.5 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



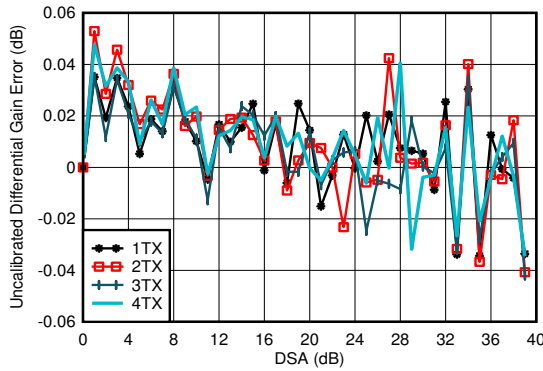
$A_{\text{out}} = -0.5\text{dBFS}$ , 3.5 GHz Matching, included PCB and cable losses

图 6-118. TX Output Power vs Frequency



$A_{\text{out}} = -0.5\text{dBFS}$ , 3.5 GHz Matching, included PCB and cable losses

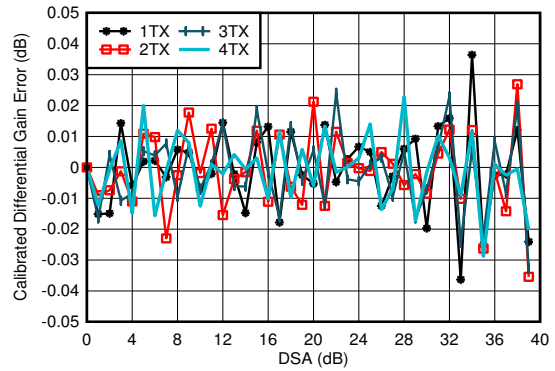
图 6-119. TX Output Power vs DSA Setting at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

$$\text{Differential Gain Error} = P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$$

图 6-120. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



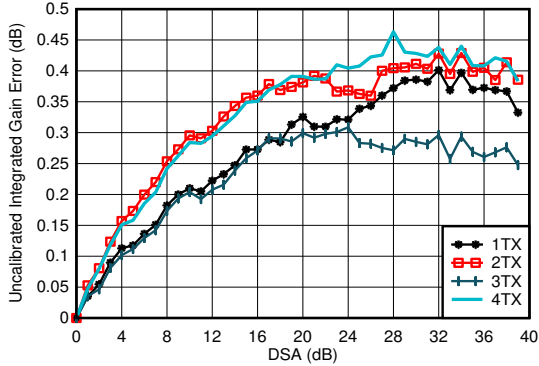
3.5 GHz Matching, included PCB and cable losses

$$\text{Differential Gain Error} = P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$$

图 6-121. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz

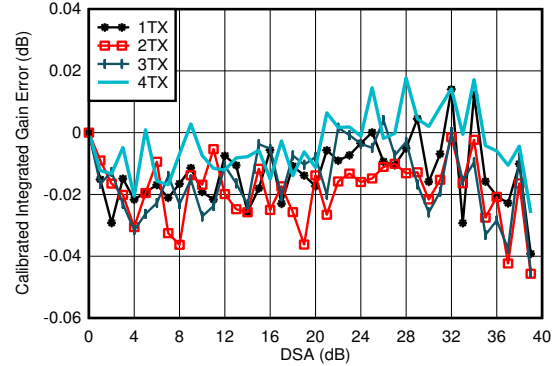
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



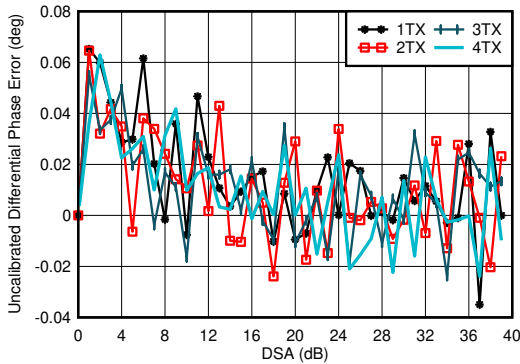
3.5 GHz Matching, included PCB and cable losses  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-122. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz



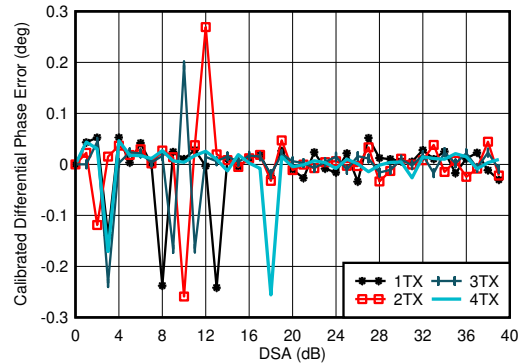
3.5 GHz Matching, included PCB and cable losses  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-123. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz



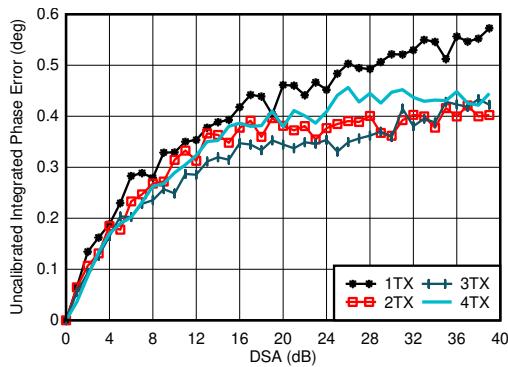
3.5 GHz Matching, included PCB and cable losses

图 6-124. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



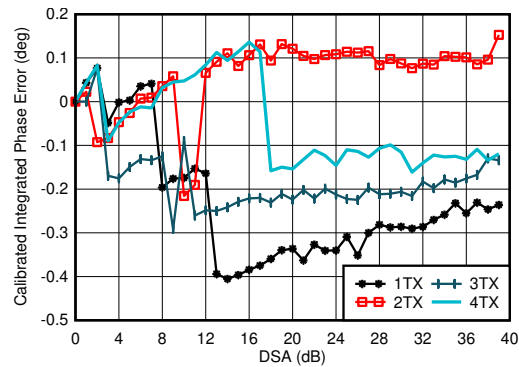
3.5 GHz Matching, included PCB and cable losses  
Phase DNL spike may occur at any DSA setting.

图 6-125. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

图 6-126. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz

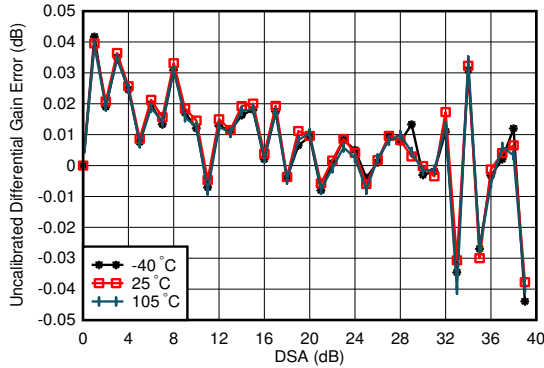


3.5 GHz Matching, included PCB and cable losses

图 6-127. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz

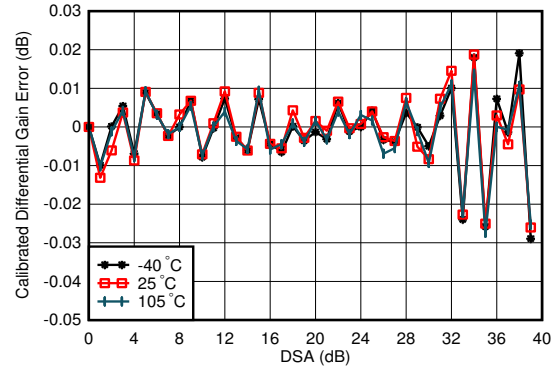
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



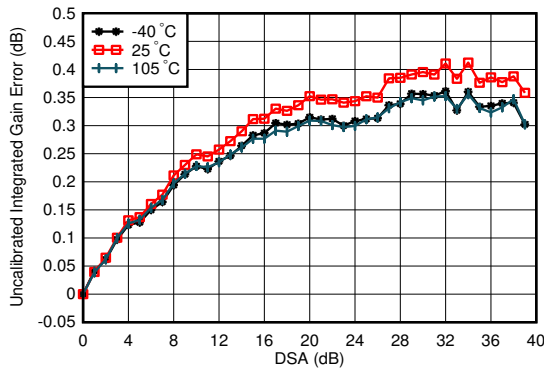
3.5 GHz Matching, 1TX

图 6-128. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz



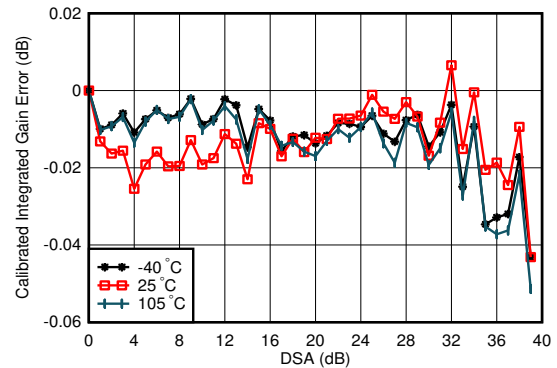
3.5 GHz Matching, 1TX, Calibrated at 25°C

图 6-129. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz



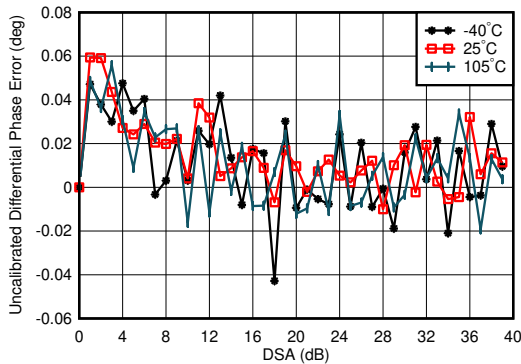
3.5 GHz Matching, 1TX

图 6-130. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

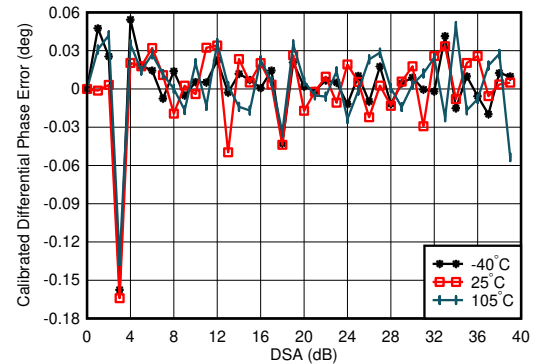
图 6-131. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-132. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



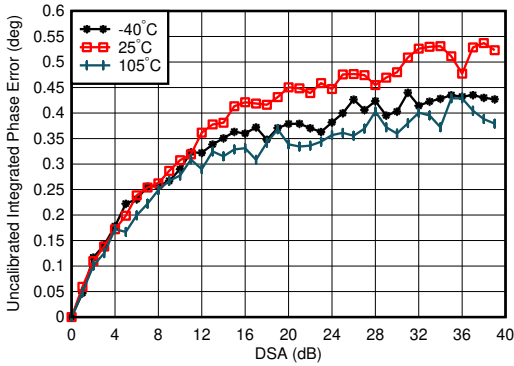
3.5 GHz Matching, 1TX, Calibrated at 25°C

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-133. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz

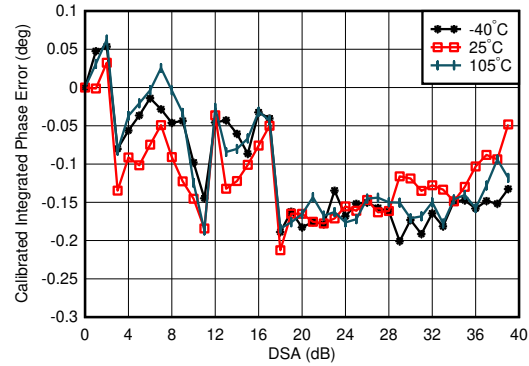
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



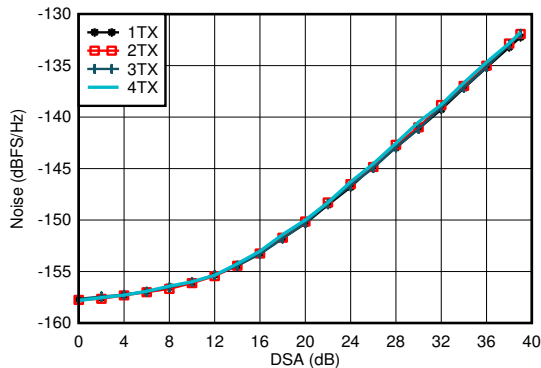
3.5 GHz Matching, 1TX  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting=0)

图 6-134. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



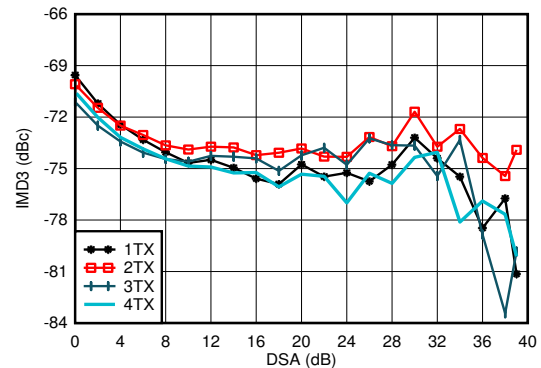
3.5 GHz Matching, 1TX, Calibrated at 25°C  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-135. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



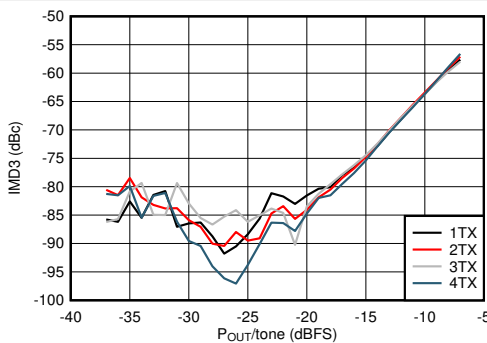
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode, matching at 3.5GHz,  
 $A_{out} = -13\text{ dBFS}$ .

图 6-136. TX NSD vs DSA Setting at 3.5 GHz



20-MHz tone spacing, 3.5 GHz Matching, -13 dBFS each tone, included PCB and cable losses

图 6-137. TX IMD3 vs DSA Setting at 3.5 GHz



20-MHz tone spacing, 3.5 GHz Matching

图 6-138. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz



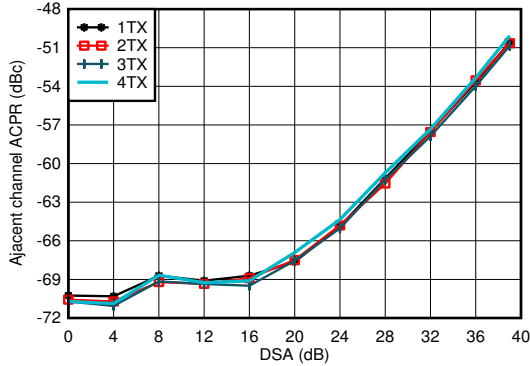
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

图 6-139. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



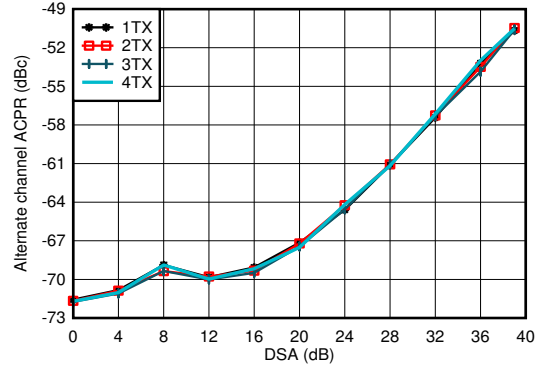
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



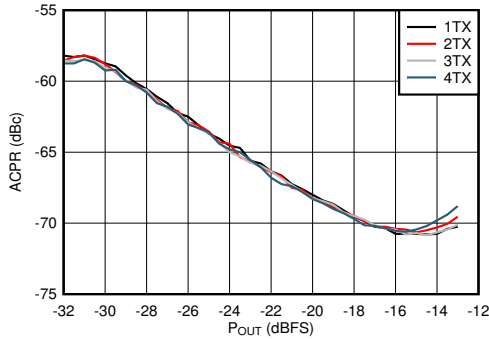
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

图 6-140. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz



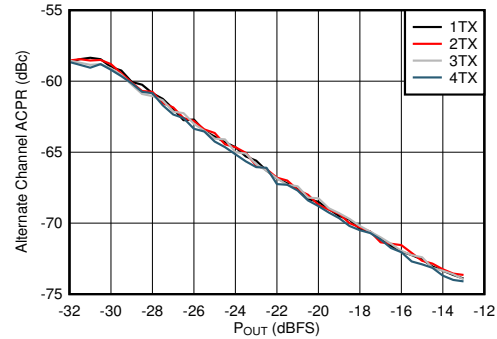
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

图 6-141. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz



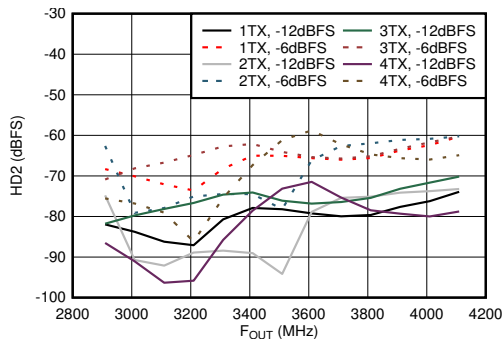
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

图 6-142. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz



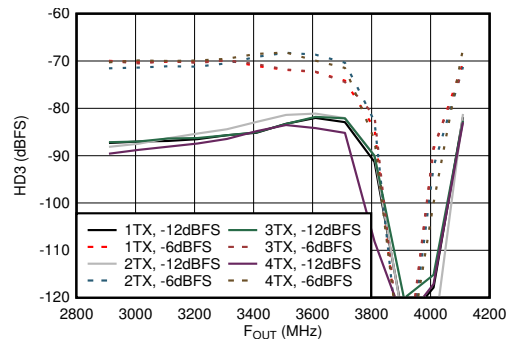
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

图 6-143. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz



Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

图 6-144. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz

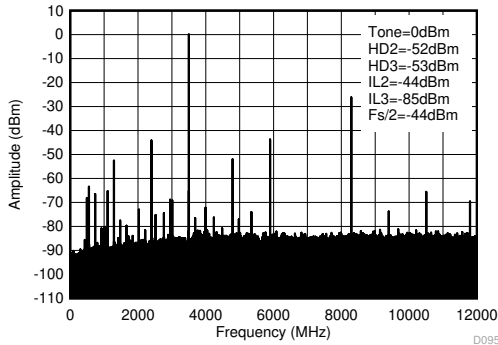


Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

图 6-145. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz

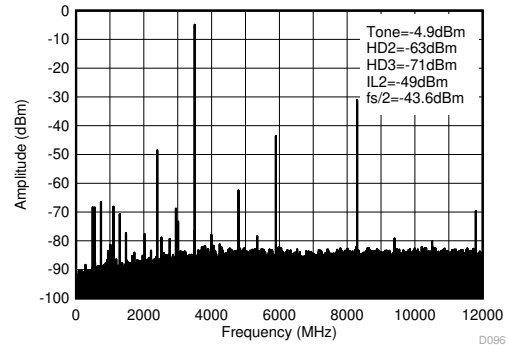
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



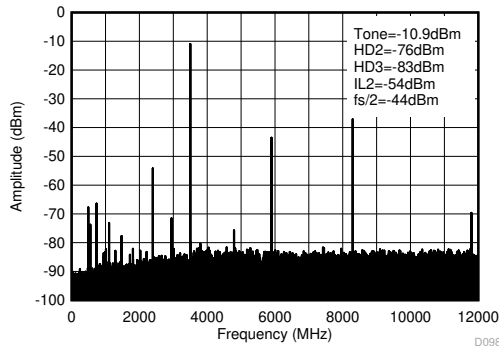
Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

图 6-146. TX Single Tone ( - 1 dBFS) Output Spectrum at 3.5 GHz (0 -  $f_{DAC}$ )



Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

图 6-147. TX Single Tone ( - 6 dBFS) Output Spectrum at 3.5 GHz (0 -  $f_{DAC}$ )

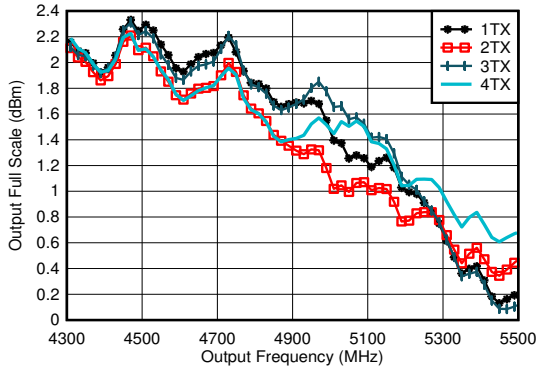


Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

图 6-148. TX Single Tone ( - 12 dBFS) Output Spectrum at 3.5 GHz (0 -  $f_{DAC}$ )

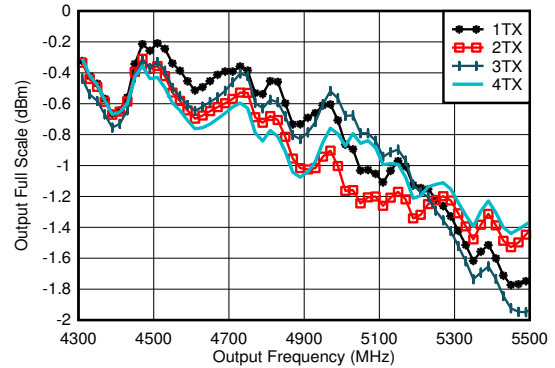
### 6.12.5 TX Typical Characteristics at 4.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



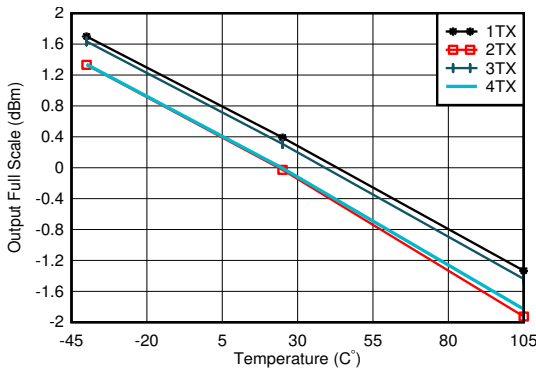
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{dBFS}$ , DSA = 0, 4.9 GHz matching

图 6-149. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS



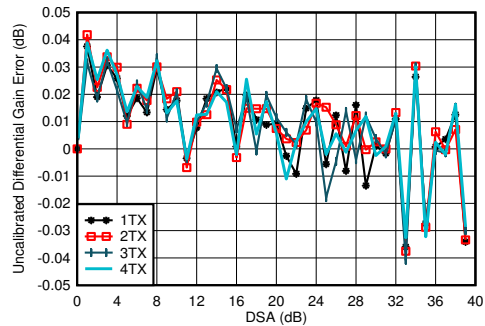
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{dBFS}$ , DSA = 0, 4.9 GHz matching

图 6-150. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode, 2nd Nyquist Zone



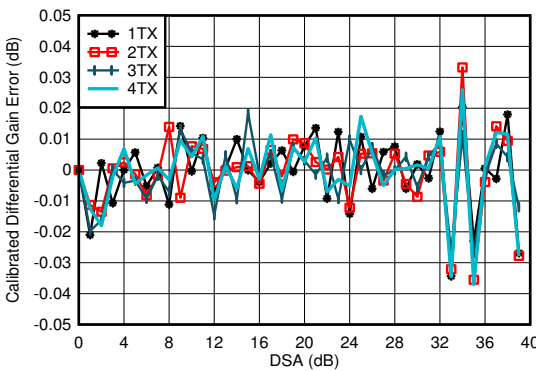
$f_{\text{DAC}} = 11796.48\text{ MSPS}$ ,  $A_{\text{out}} = -0.5\text{dBFS}$ , matching 4.9 GHz

图 6-151. TX Output Power vs DSA Setting and Channel at 4.9 GHz



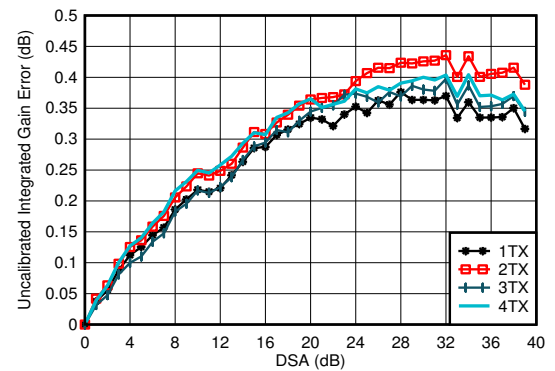
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-152. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-153. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

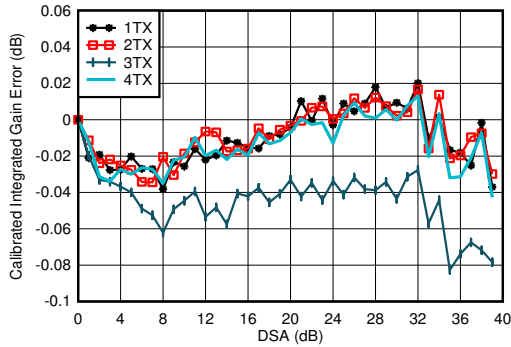


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-154. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz

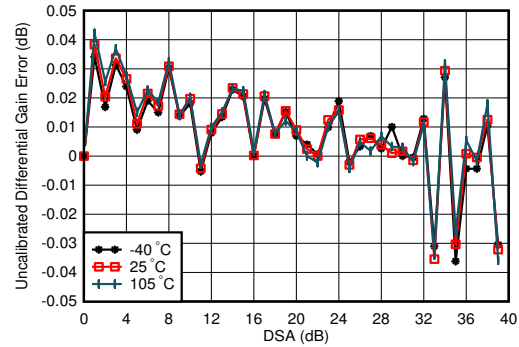
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



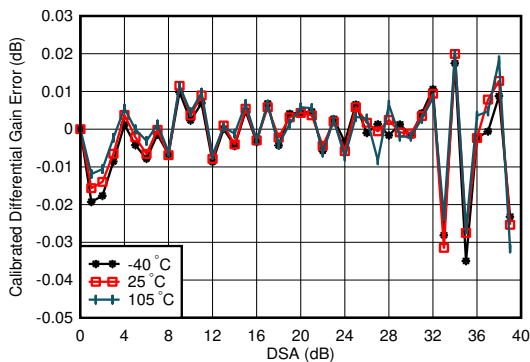
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-155. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



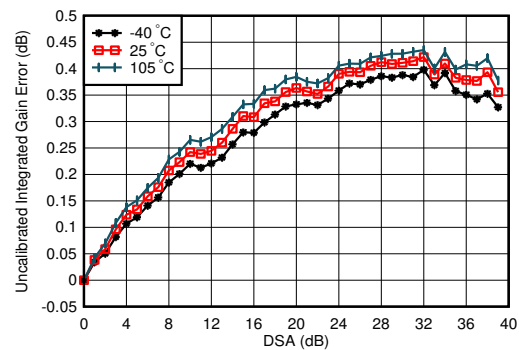
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-156. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

图 6-157. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

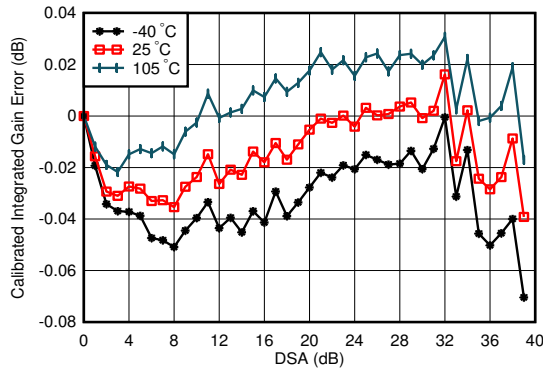


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-158. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz

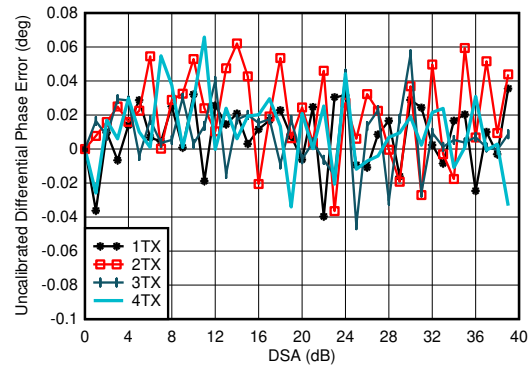
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleaved mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



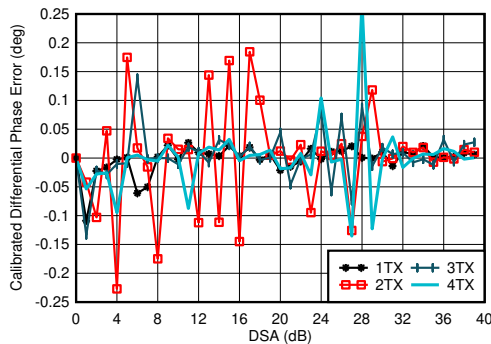
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-159. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



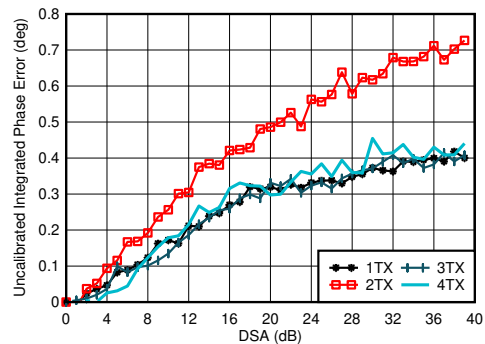
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-160. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
Phase DNL spike may occur at any DSA setting.

图 6-161. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

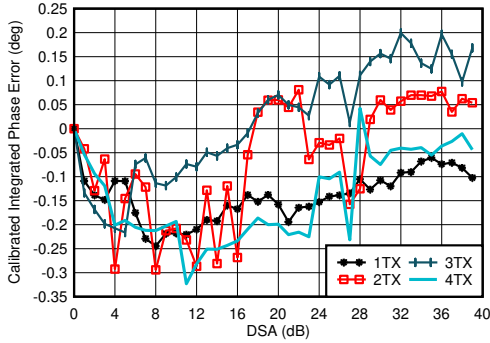


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-162. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz

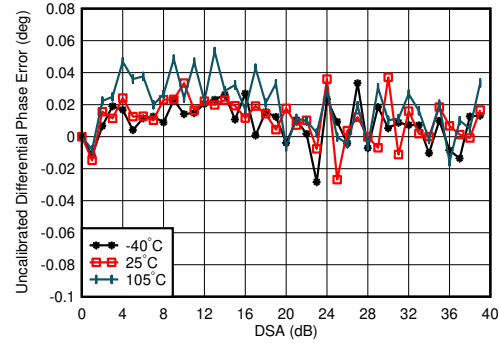
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



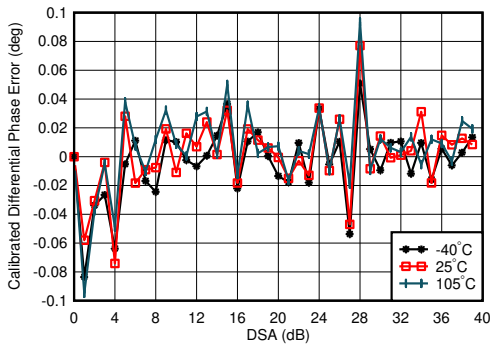
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-163. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



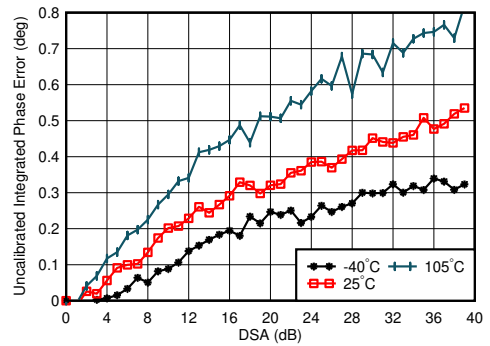
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-164. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

图 6-165. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz

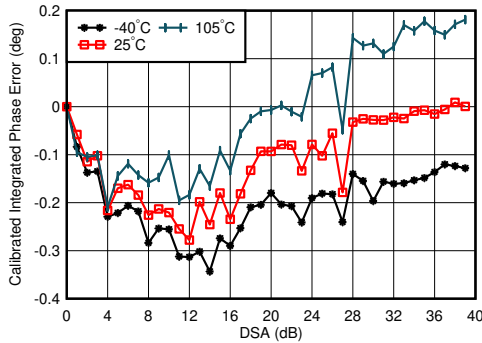


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-166. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz

### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

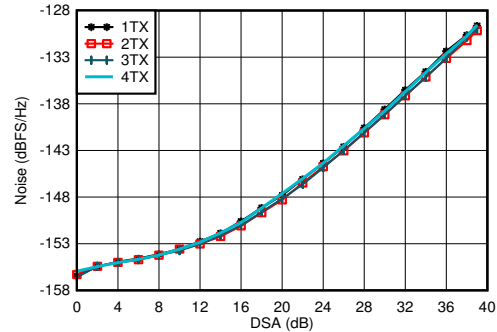
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleaved mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz, channel with the median variation over DSA setting at  $25^\circ\text{C}$

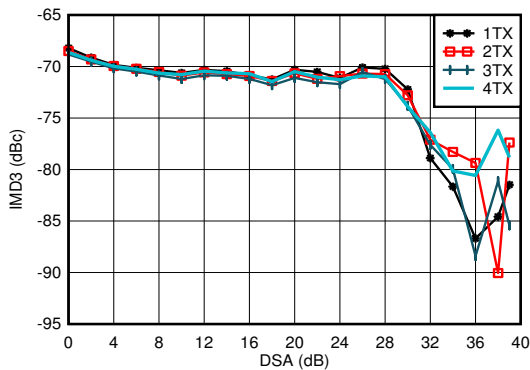
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-167. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



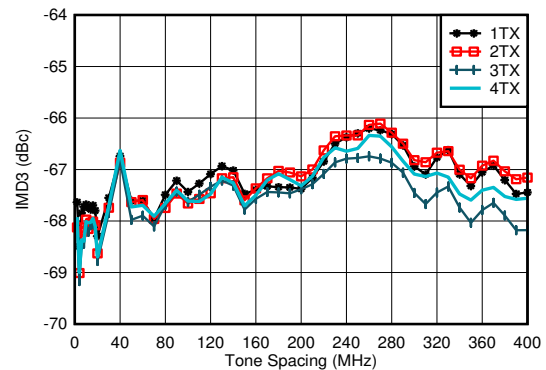
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

图 6-168. TX Output Noise vs Channel and Attenuation at 2.6 GHz



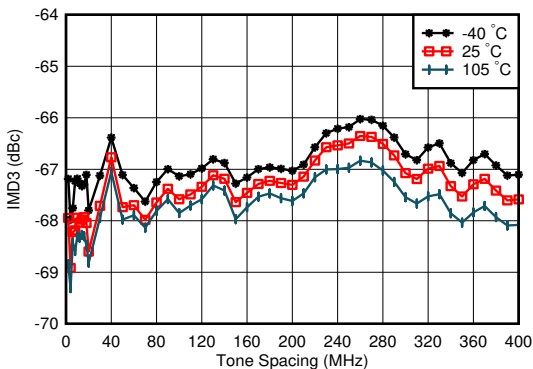
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone

图 6-169. TX IMD3 vs DSA Setting at 4.9 GHz



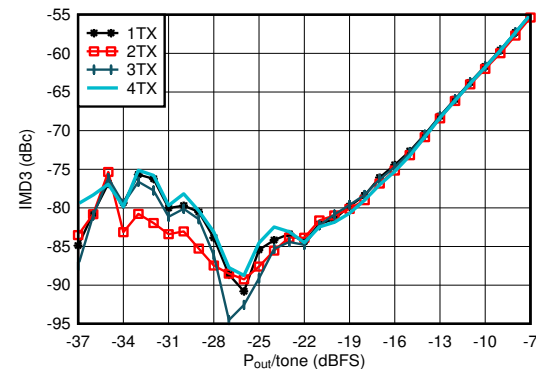
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone

图 6-170. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone, worst channel

图 6-171. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz

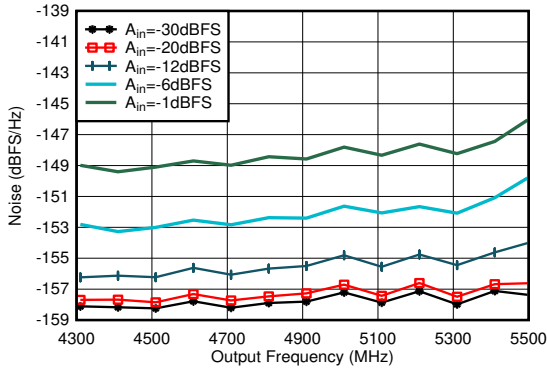


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ ,  $f_{\text{SPACING}} = 20\text{ MHz}$

图 6-172. TX IMD3 vs Digital Level at 4.9 GHz

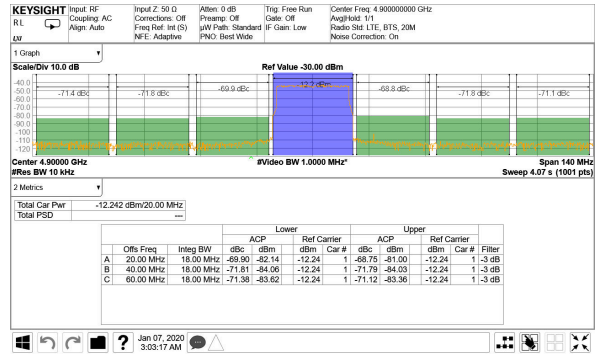
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



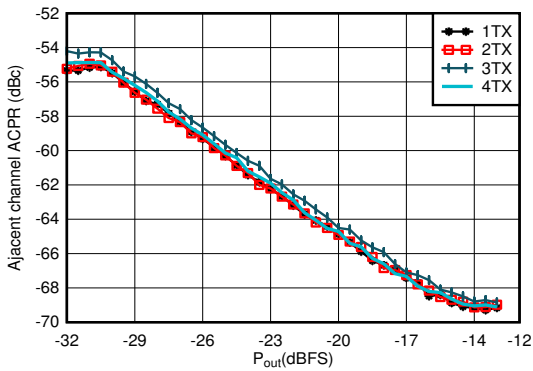
Matching at 4.9 GHz, Single tone,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset, DSA=0dB

图 6-173. TX Single Tone Output Noise vs Frequency and Amplitude at 4.9 GHz



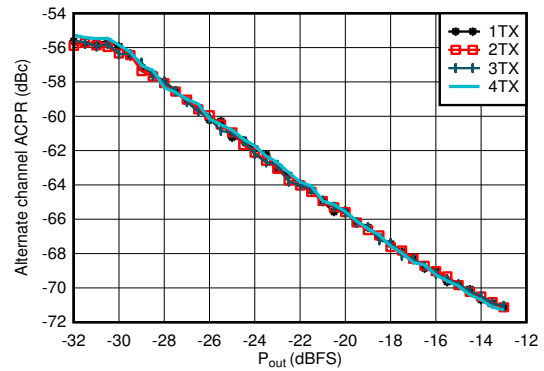
TM1.1,  $P_{OUT\_RMS} = -13\text{ dBFS}$

图 6-174. TX 20-MHz LTE Output Spectrum at 4.9 GHz



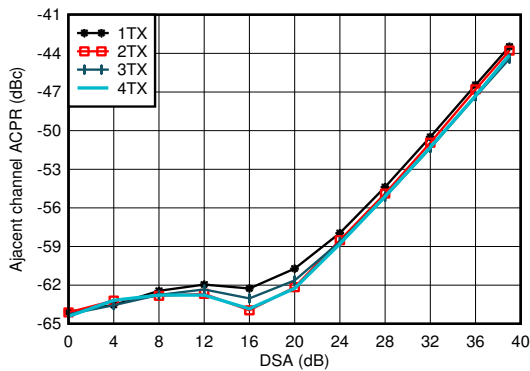
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-175. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



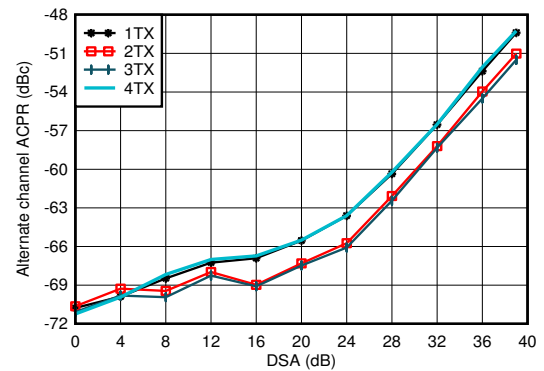
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-176. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-177. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz



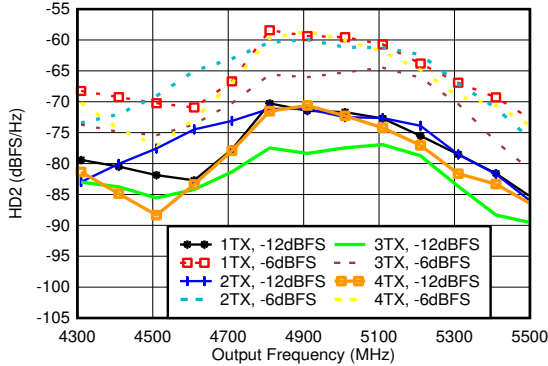
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

图 6-178. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz



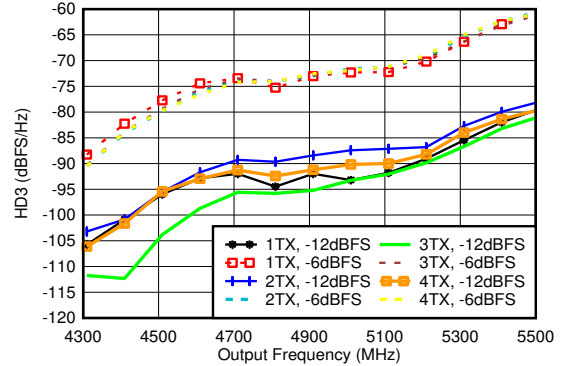
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



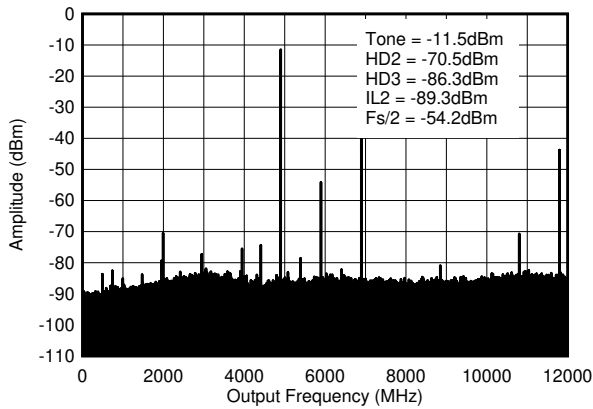
Matching at 4.9 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

图 6-179. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz



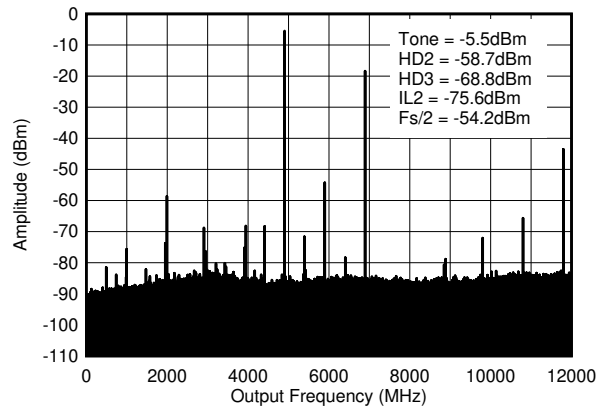
Matching at 4.9 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

图 6-180. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz



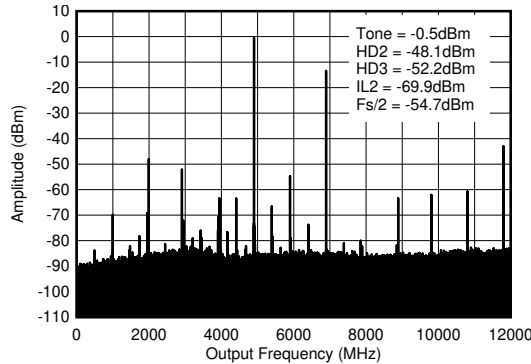
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .

图 6-181. TX Single Tone (-12 dBFS) Output Spectrum at 4.9 GHz ( $0-f_{\text{DAC}}$ )



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .

图 6-182. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz ( $0-f_{\text{DAC}}$ )

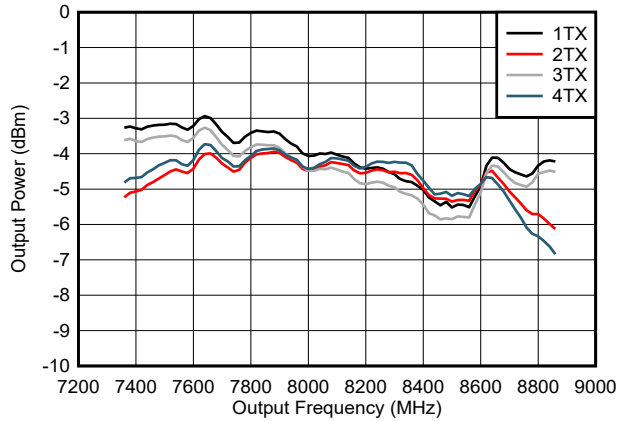


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .

图 6-183. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz ( $0-f_{\text{DAC}}$ )

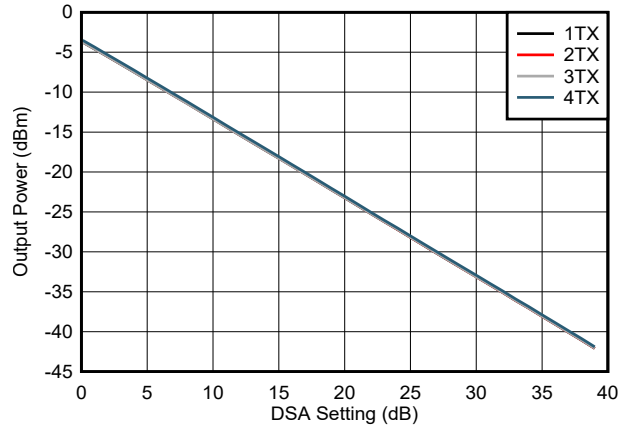
### 6.12.6 TX Typical Characteristics at 8.1 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



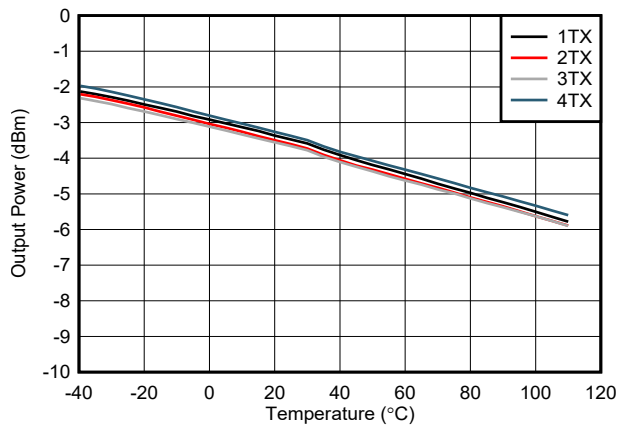
includes PCB and cable losses.

图 6-184. TX Output Power vs Frequency at 8.11 GHz



includes PCB and cable losses.

图 6-185. TX Output Power vs DSA Setting at 8.11 GHz



includes PCB and cable losses.

图 6-186. TX Output Power vs Temperature at 8.11 GHz

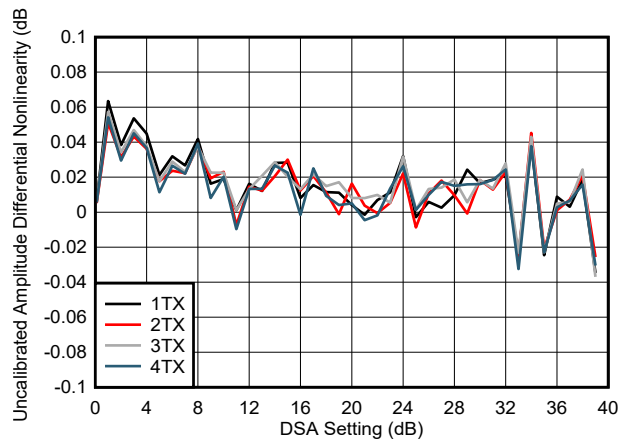


图 6-187. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz

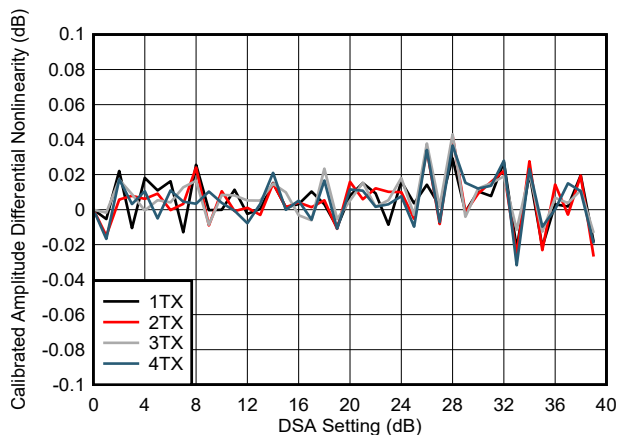


图 6-188. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz

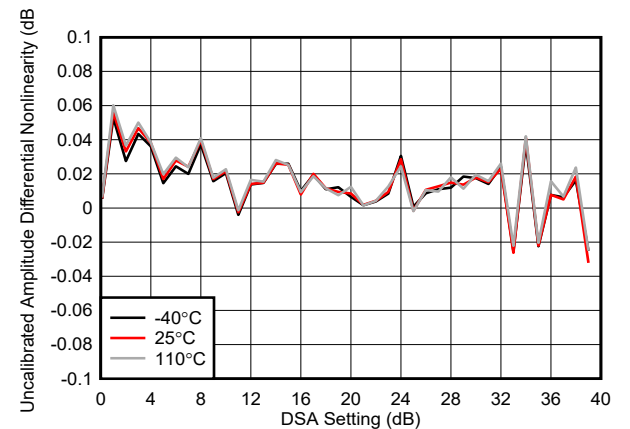


图 6-189. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching

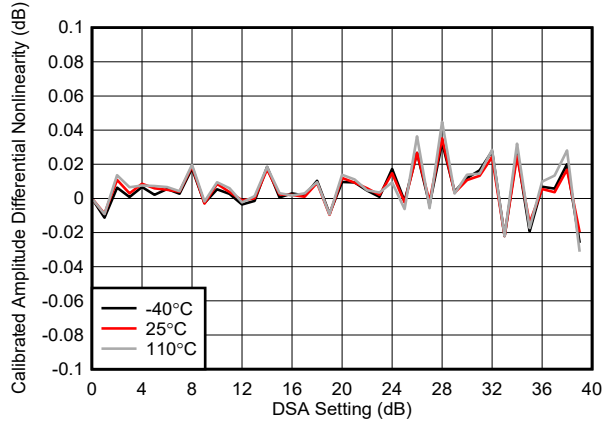


图 6-190. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz

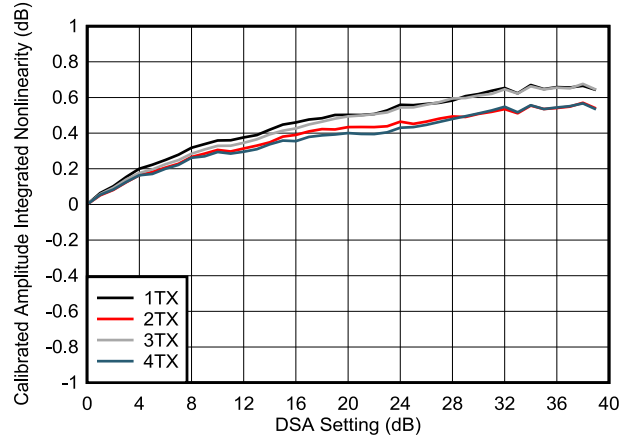


图 6-191. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

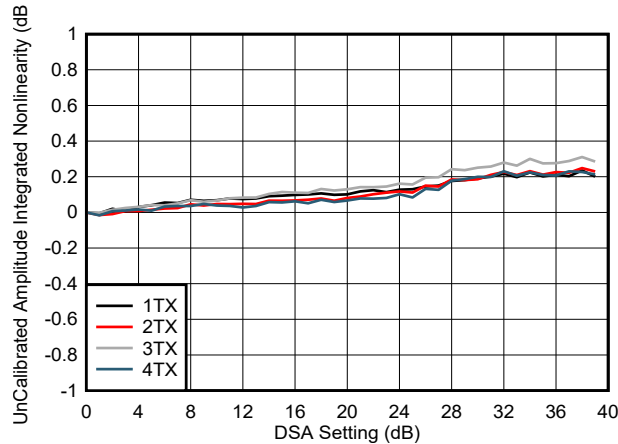


图 6-192. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

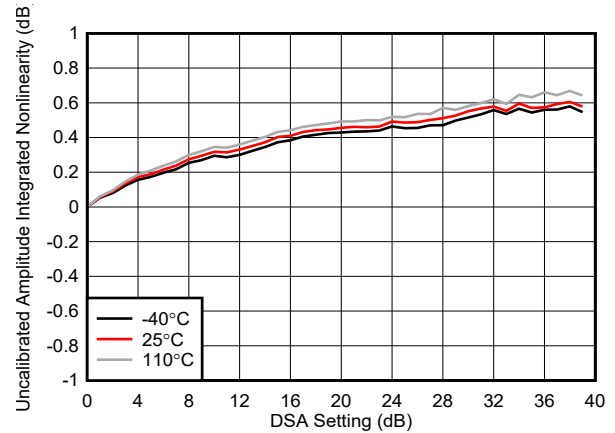


图 6-193. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

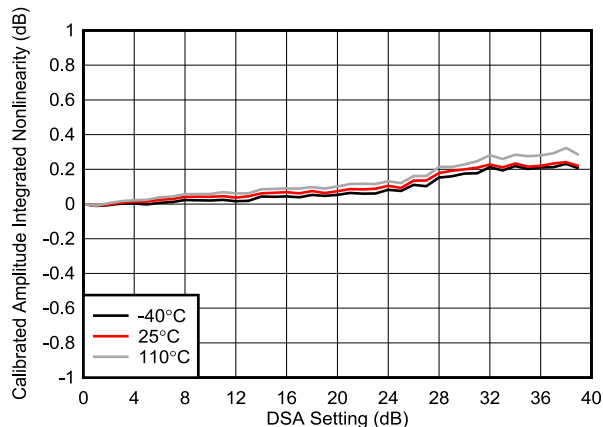


图 6-194. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

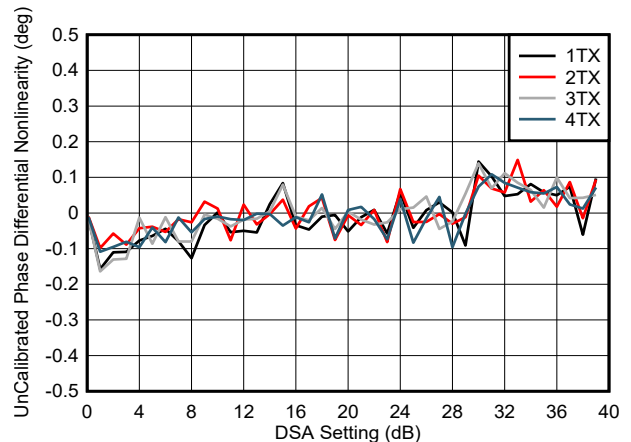


图 6-195. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching

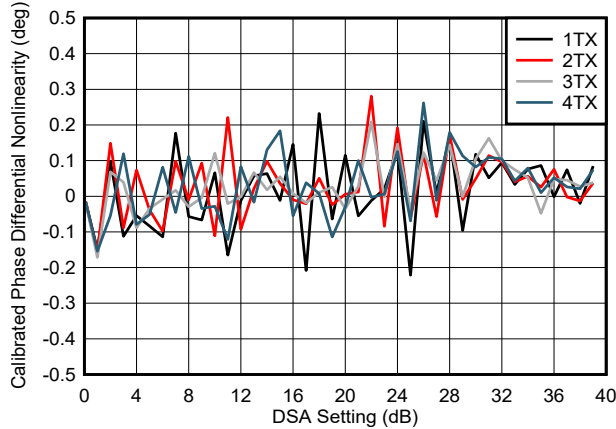


图 6-196. TX DSA Calibrated Phase Differential Nonlinearity at 8.1 GHz

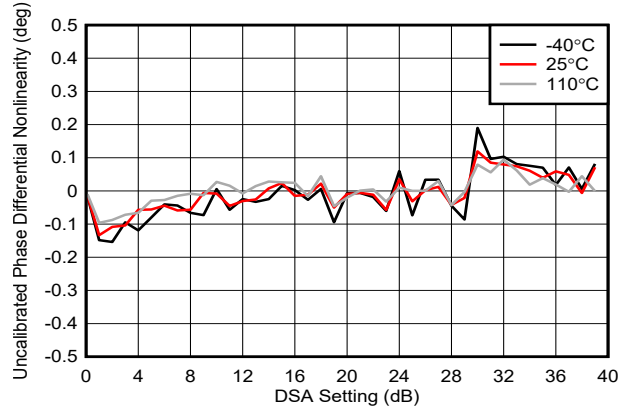


图 6-197. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.1 GHz

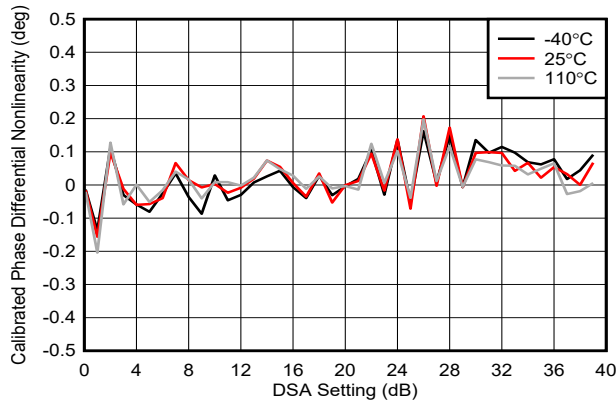


图 6-198. TX DSA Calibrated Phase Differential Nonlinearity at 8.1 GHz

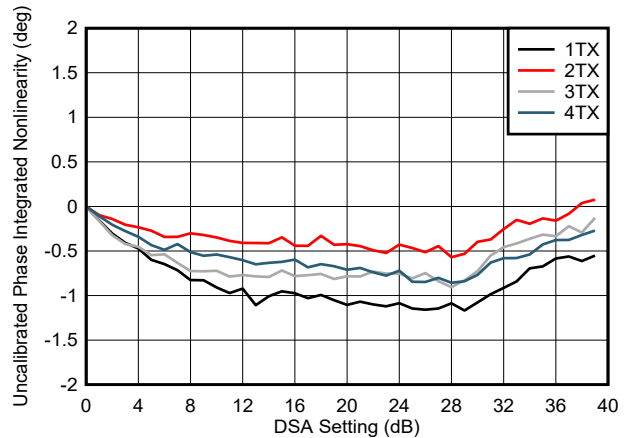


图 6-199. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.1 GHz

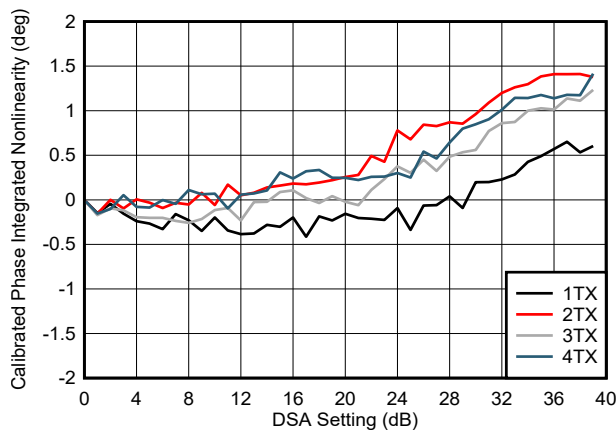


图 6-200. TX DSA Calibrated Phase Integrated Nonlinearity at 8.1 GHz

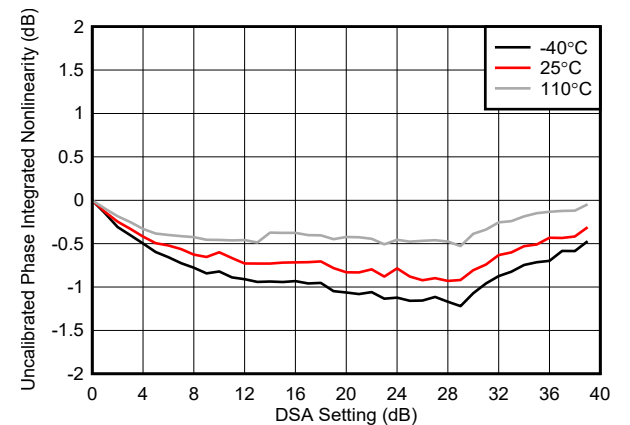


图 6-201. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.1 GHz

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching

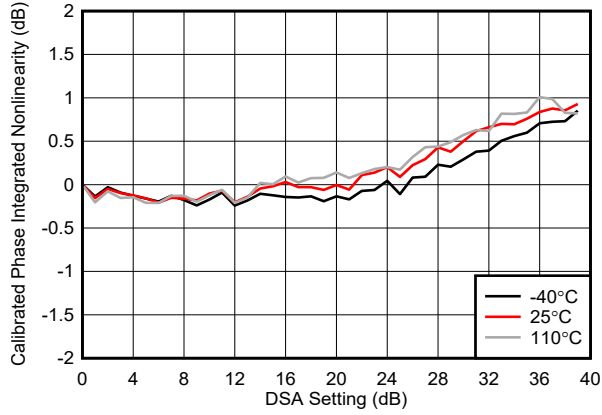


图 6-202. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz

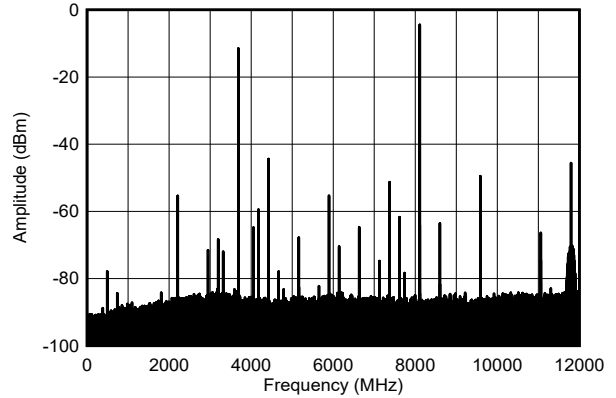
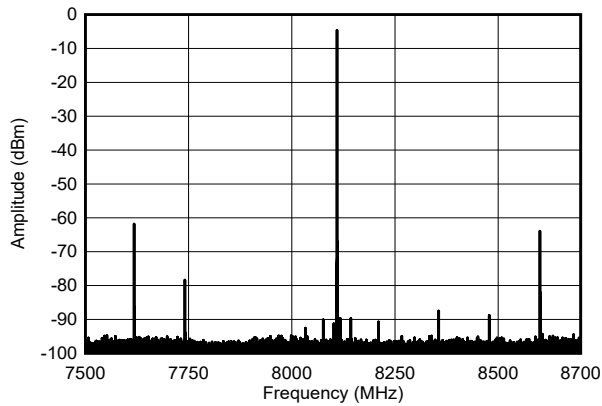
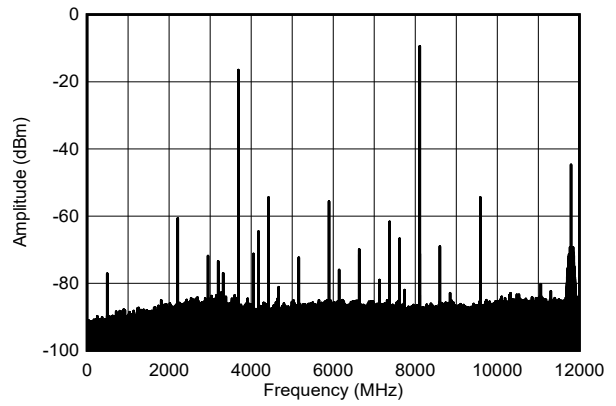


图 6-203. TX Single Tone Output Spectrum at 8.11 GHz



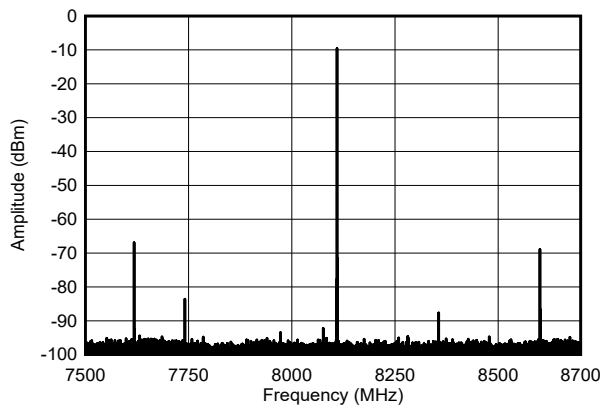
- 1 dBFS

图 6-204. TX Single Tone Output Spectrum at 8.11 GHz



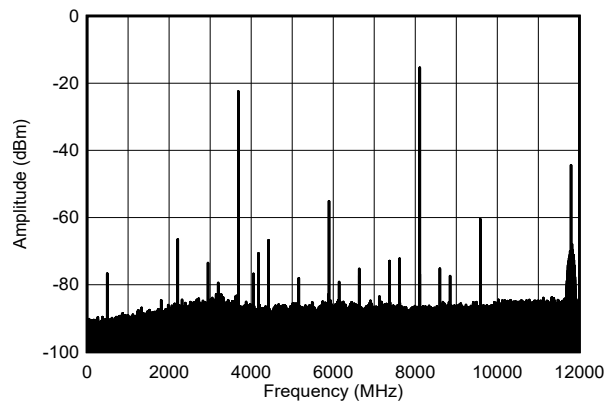
- 6 dBFS

图 6-205. TX Single Tone Output Spectrum at 8.11 GHz



- 6 dBFS

图 6-206. TX Single Tone Output Spectrum at 8.11 GHz

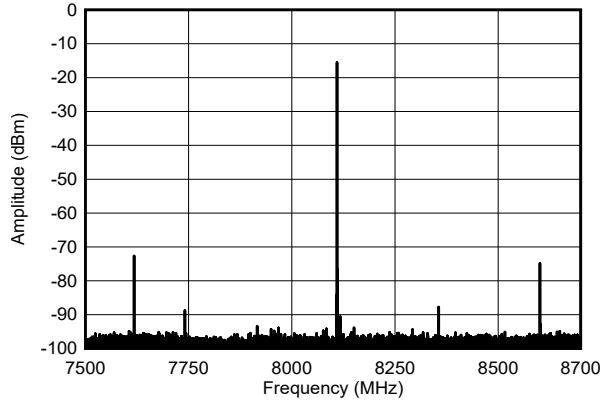


- 12 dBFS

图 6-207. TX Single Tone Output Spectrum at 8.11 GHz

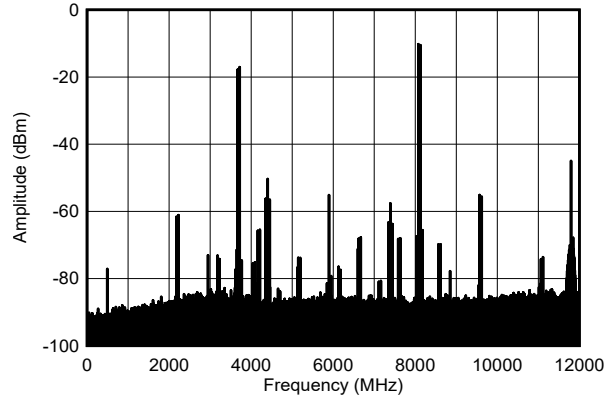
### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



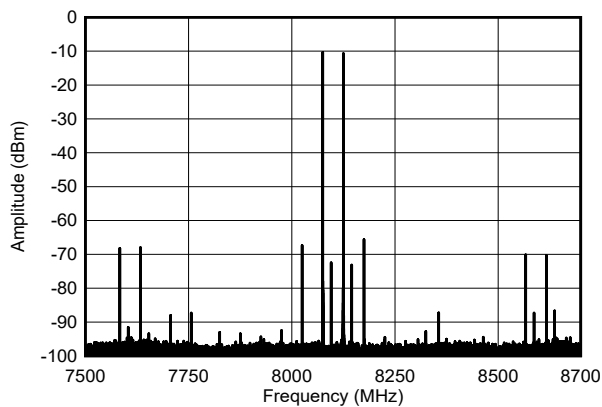
- 12 dBFS

图 6-208. TX Single Tone Output Spectrum at 8.11 GHz



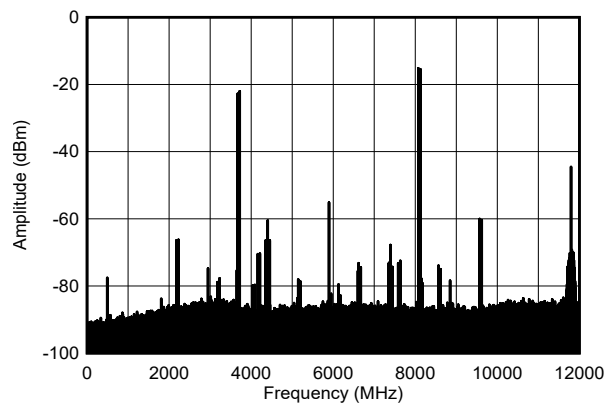
50-MHz tone spacing, - 7 dBFS each tone

图 6-209. TX Dual Tone Output Spectrum at 8.11 GHz



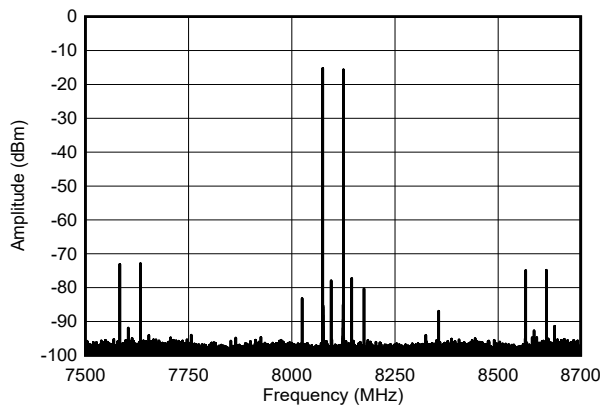
50-MHz tone spacing, - 7 dBFS each tone

图 6-210. TX Dual Tone Output Spectrum at 8.11 GHz



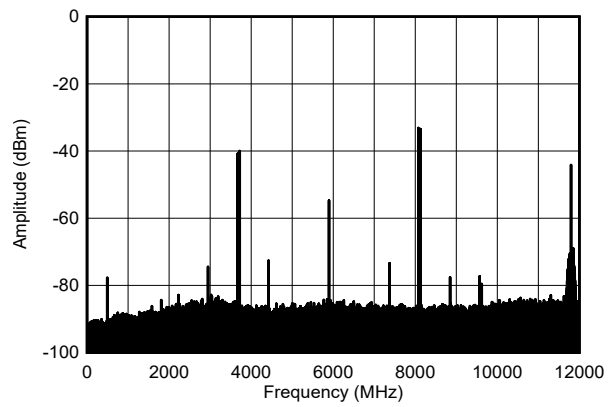
50-MHz tone spacing, - 12 dBFS each tone

图 6-211. TX Dual Tone Output Spectrum at 8.11 GHz



50-MHz tone spacing, - 12 dBFS each tone

图 6-212. TX Dual Tone Output Spectrum at 8.11 GHz

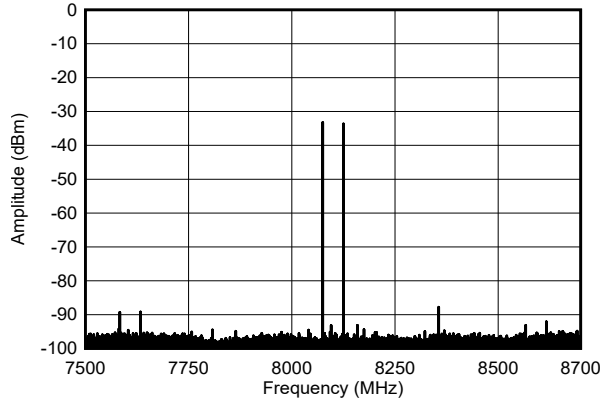


50-MHz tone spacing, - 30 dBFS each tone

图 6-213. TX Dual Tone Output Spectrum at 8.11 GHz

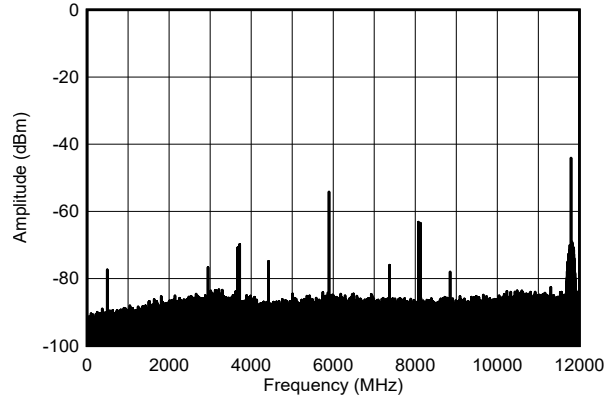
### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



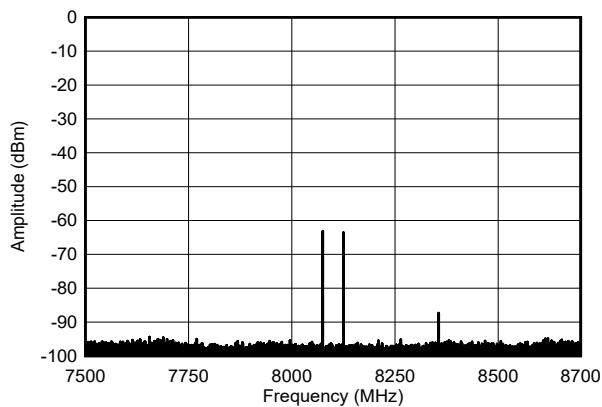
50-MHz tone spacing, -30 dBFS each tone

图 6-214. TX Dual Tone Output Spectrum at 8.1 GHz



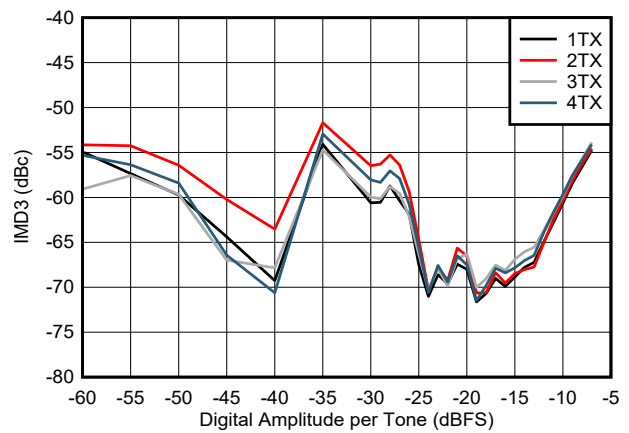
50-MHz tone spacing, -60 dBFS each tone

图 6-215. TX Dual Tone Output Spectrum at 8.1 GHz



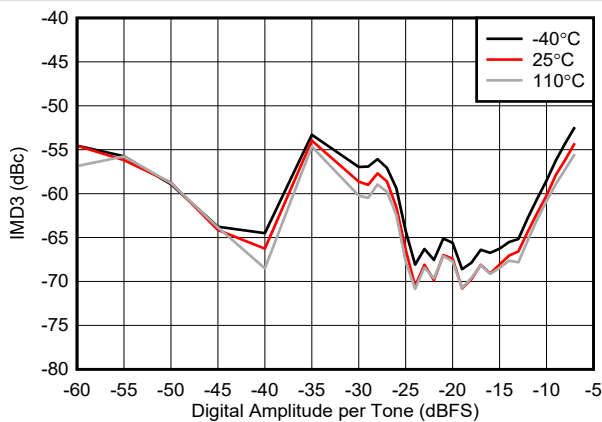
50-MHz tone spacing, -60 dBFS each tone

图 6-216. TX Dual Tone Output Spectrum at 8.1 GHz



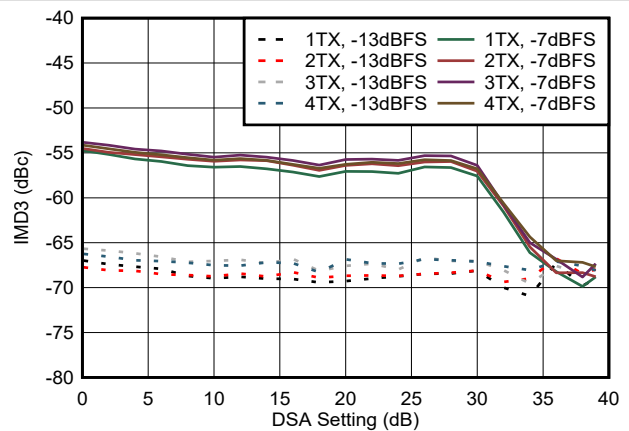
50-MHz tone spacing

图 6-217. TX IMD3 vs Digital Amplitude at 8.1 GHz



50-MHz tone spacing

图 6-218. TX IMD3 vs Digital Amplitude at 8.1 GHz

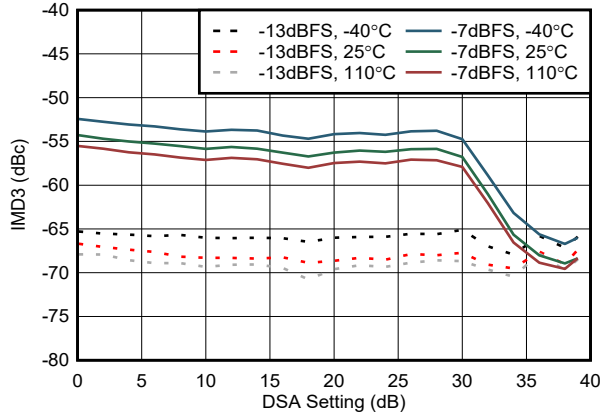


50-MHz tone spacing

图 6-219. TX IMD3 vs DSA Setting at 8.1 GHz

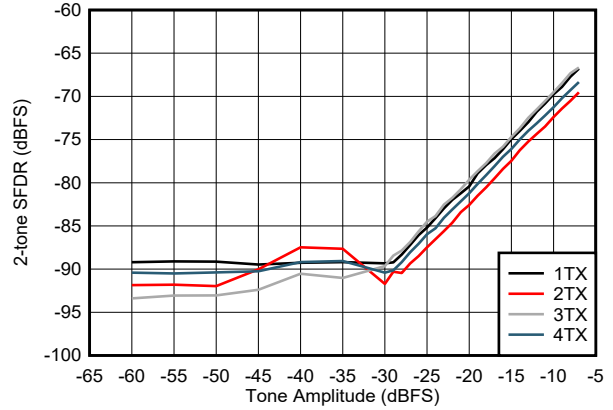
### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



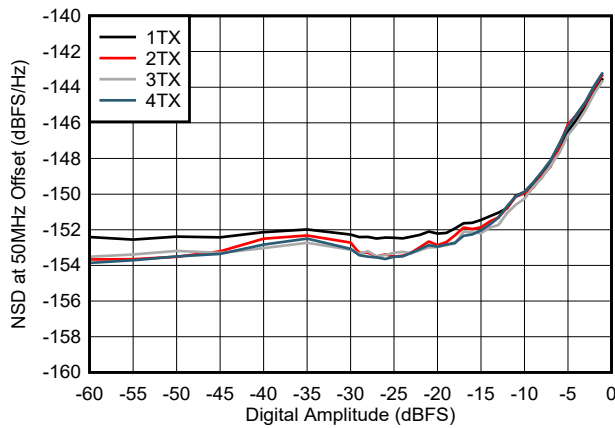
50-MHz tone spacing

图 6-220. TX IMD3 vs DSA Setting at 8.1 GHz



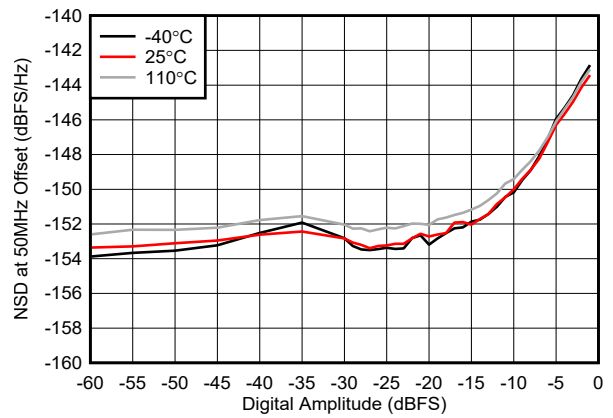
50-MHz tone spacing

图 6-221. TX 2-Tone SFDR vs Digital Amplitude at 8.1 GHz



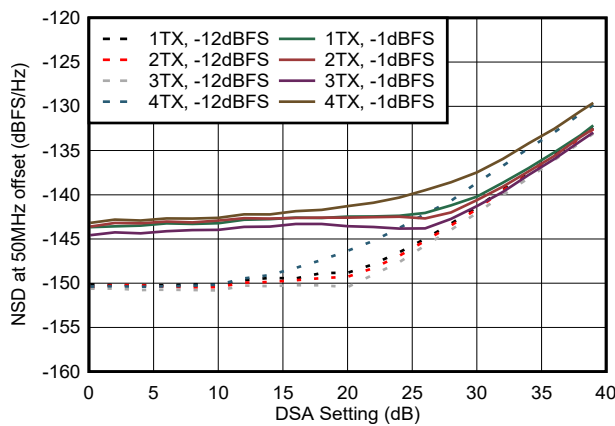
50-MHz offset

图 6-222. TX NSD vs Digital Amplitude at 8.1 GHz



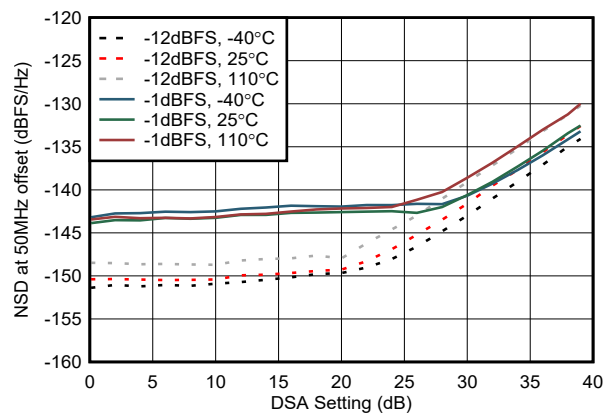
50-MHz offset

图 6-223. TX NSD vs Digital Amplitude at 8.1 GHz



50-MHz offset

图 6-224. TX NSD vs DSA Setting at 8.1 GHz



50-MHz offset

图 6-225. TX NSD vs DSA Setting at 8.1 GHz



### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching

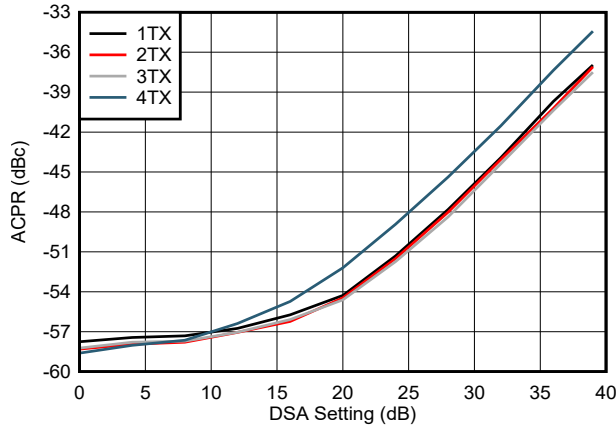


图 6-226. TX NR100MHz ACPR vs DSA Setting 8.11 GHz

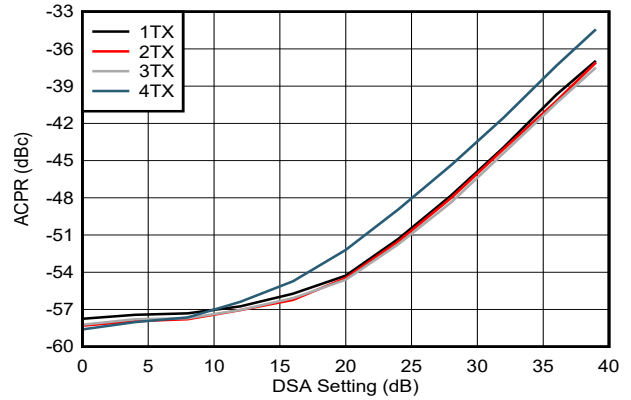


图 6-227. TX NR100MHz alt-ACPR vs DSA Setting 8.11 GHz

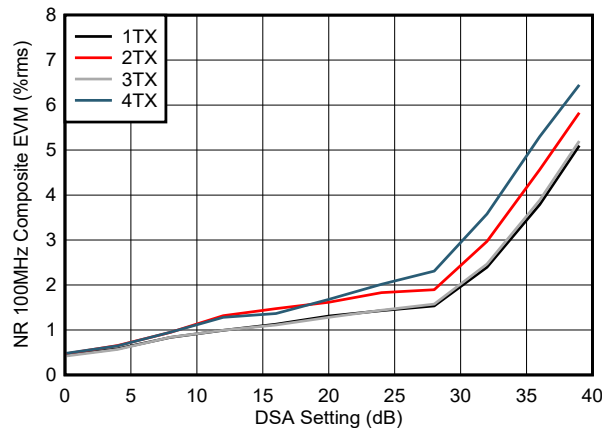


图 6-228. TX NR100MHz EVM vs DSA Setting 8.11 GHz

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching

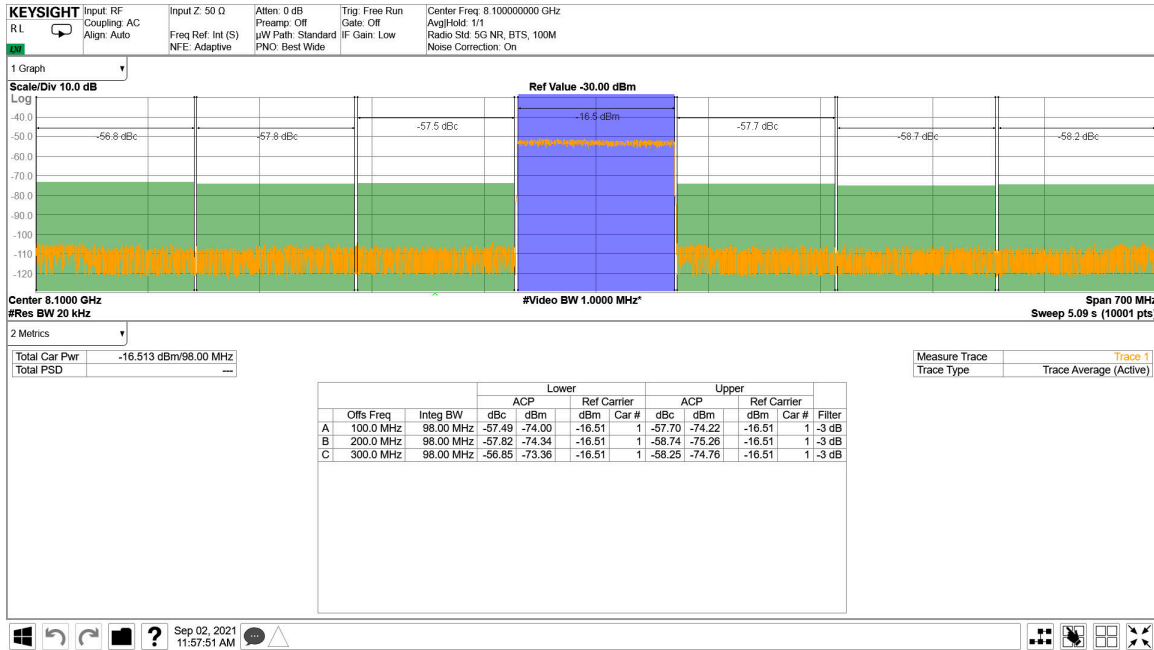


图 6-229. TX 100MHz NR Output Spectrum at 8.11 GHz



图 6-230. TX 100MHz NR EVM at 8.11 GHz

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching

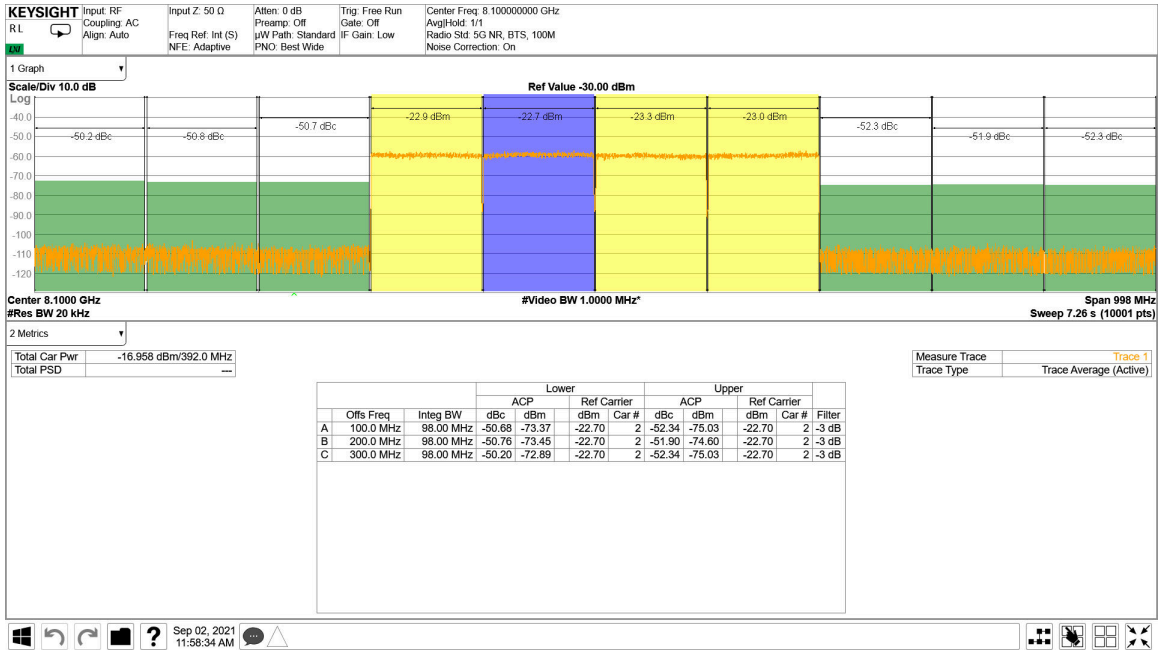


图 6-231. TX 4x100MHz NR Output Spectrum 8.11 GHz

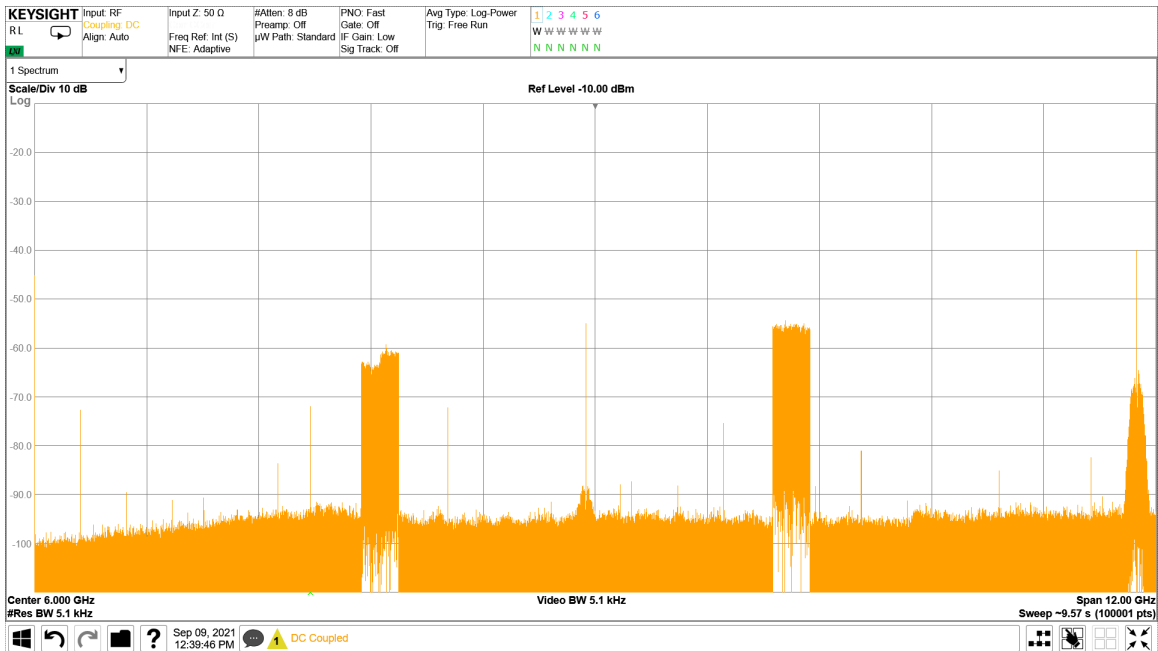
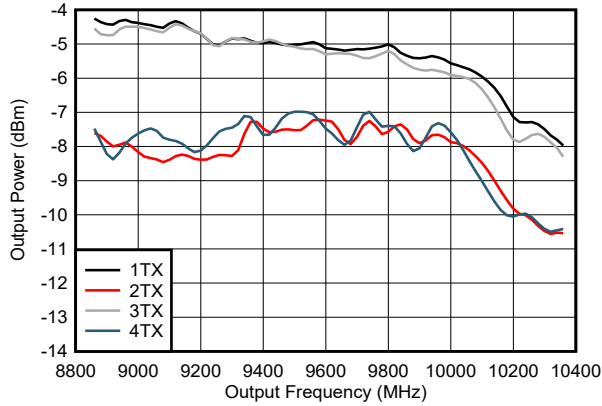


图 6-232. TX 4x100MHz NR Output Spectrum 8.11 GHz

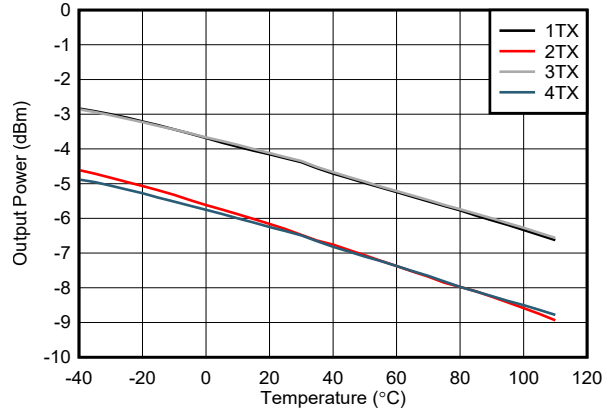
### 6.12.7 TX Typical Characteristics at 9.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



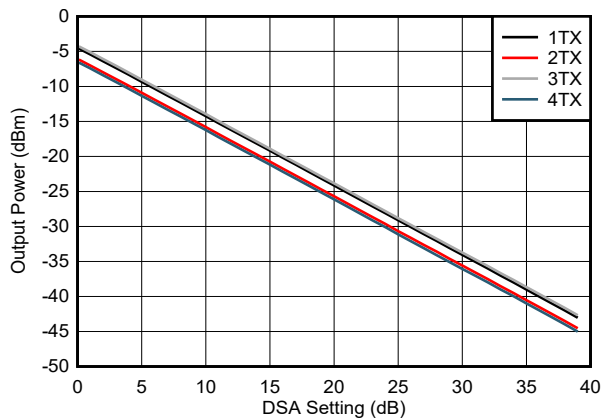
Includes PCB and cable losses.

图 6-233. TX Output Power vs Frequency at 9.61 GHz



Includes PCB and cable losses.

图 6-234. TX Output Power vs Frequency at 9.61 GHz



Includes PCB and cable losses.

图 6-235. TX Output Power vs DSA Setting at 9.61 GHz

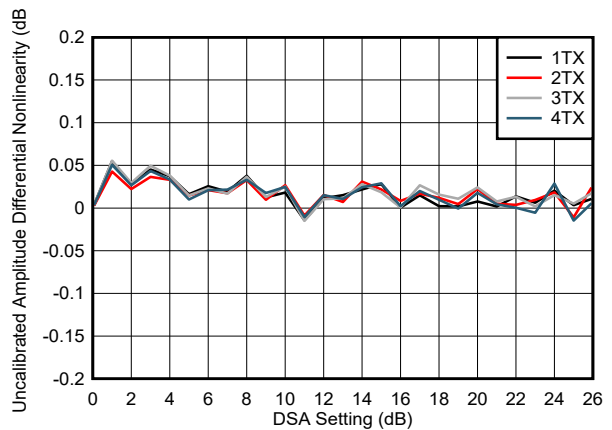


图 6-236. TX DSA Uncalibrated Amplitude Differential Nonlinearity

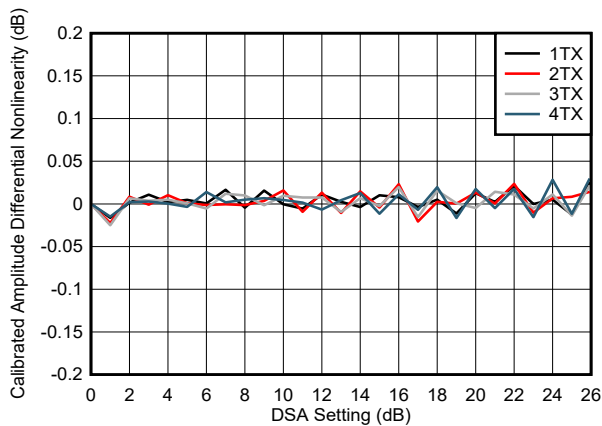


图 6-237. TX DSA Calibrated Amplitude Differential Nonlinearity

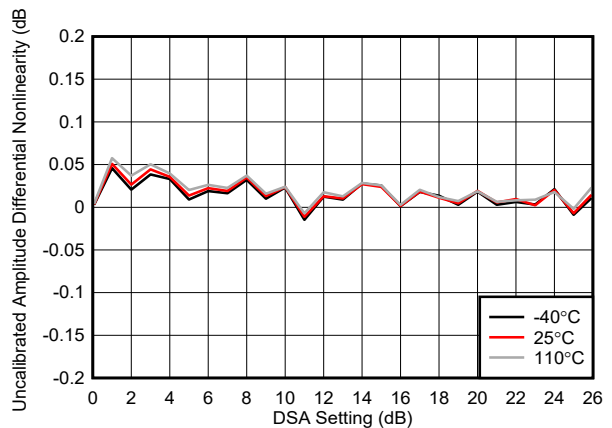


图 6-238. TX DSA Uncalibrated Amplitude Differential Nonlinearity

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

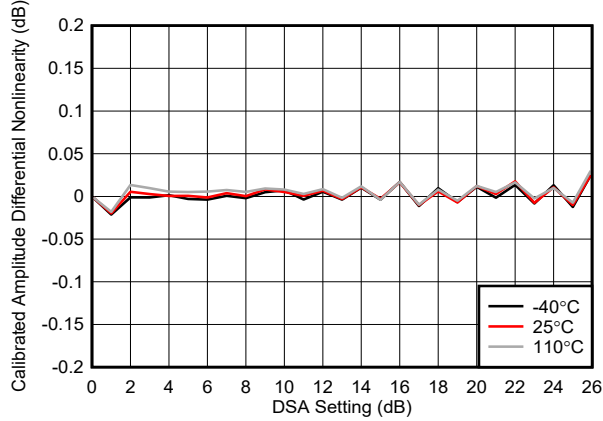


图 6-239. TX DSA Calibrated Amplitude Differential Nonlinearity

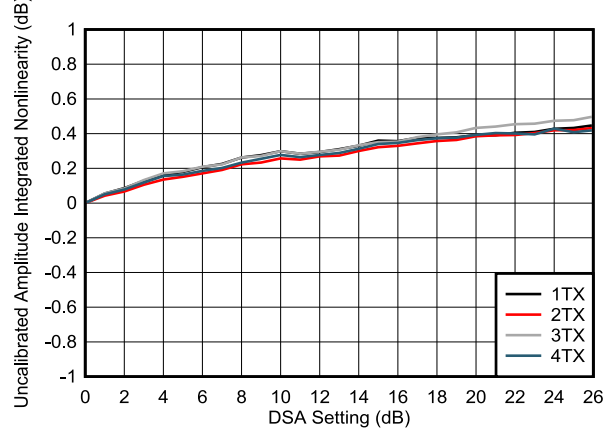


图 6-240. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

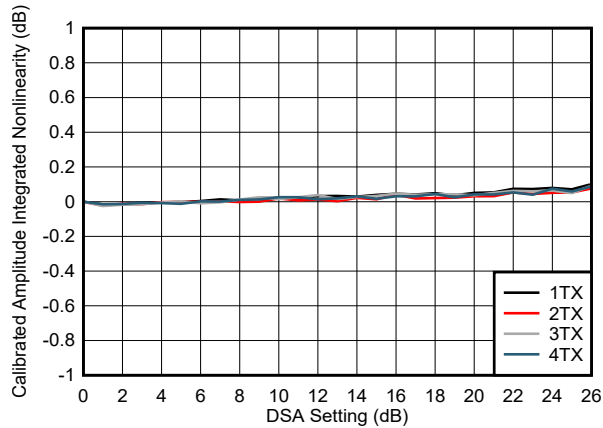


图 6-241. TX DSA Calibrated Amplitude Integrated Nonlinearity

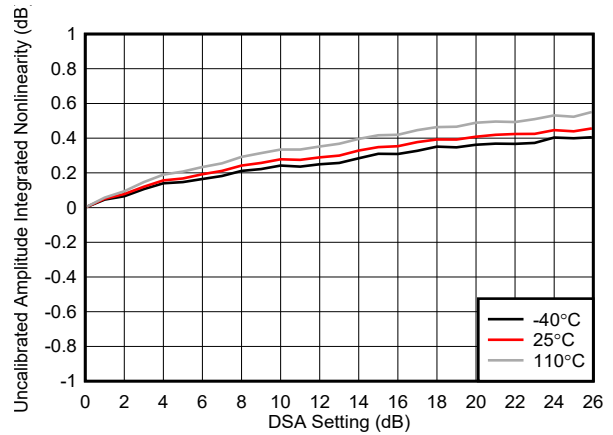


图 6-242. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

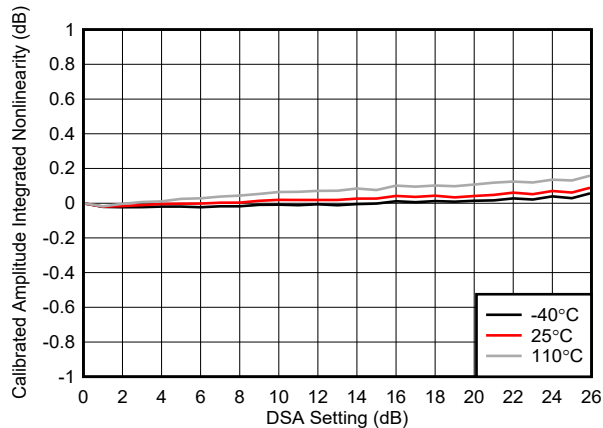


图 6-243. TX DSA Calibrated Amplitude Integrated Nonlinearity

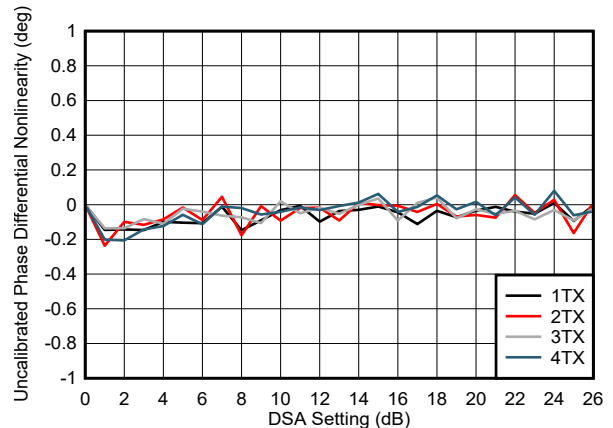


图 6-244. TX DSA Uncalibrated Phase Differential Nonlinearity

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

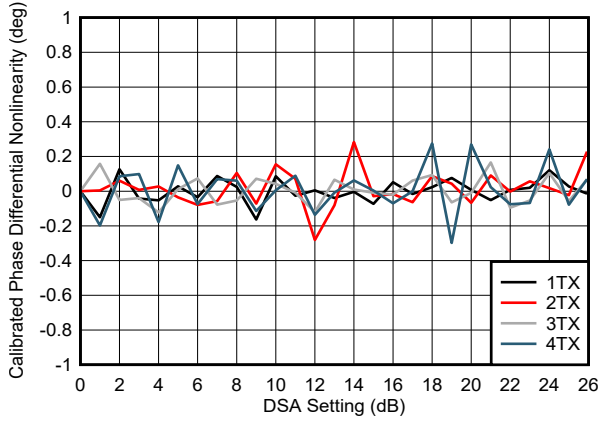


图 6-245. TX DSA Calibrated Phase Differential Nonlinearity

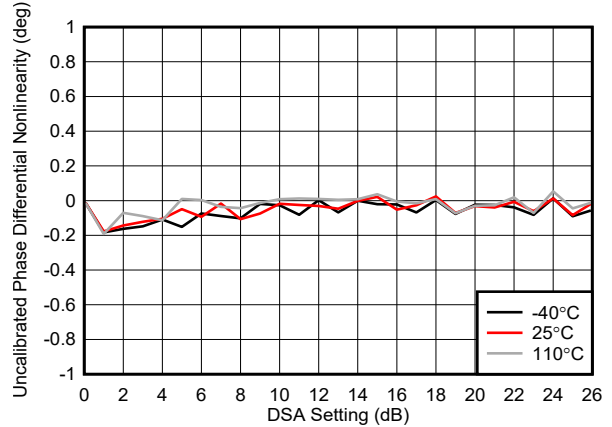


图 6-246. TX DSA Uncalibrated Phase Differential Nonlinearity

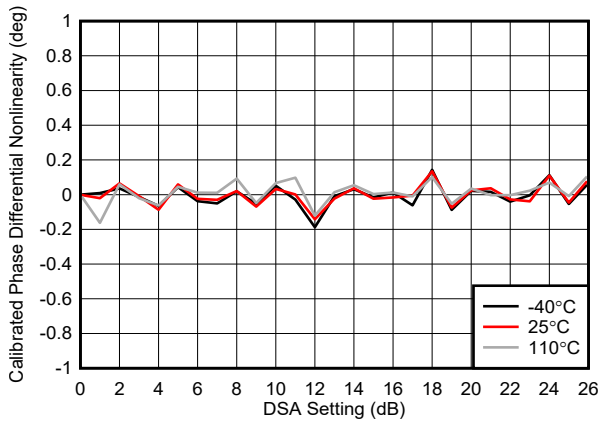


图 6-247. TX DSA Calibrated Phase Differential Nonlinearity

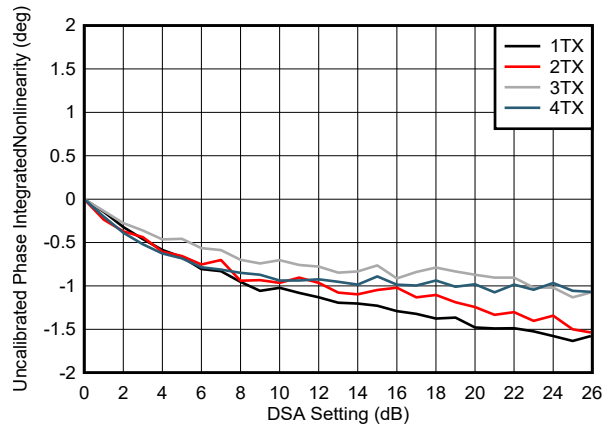


图 6-248. TX DSA Uncalibrated Phase Integrated Nonlinearity

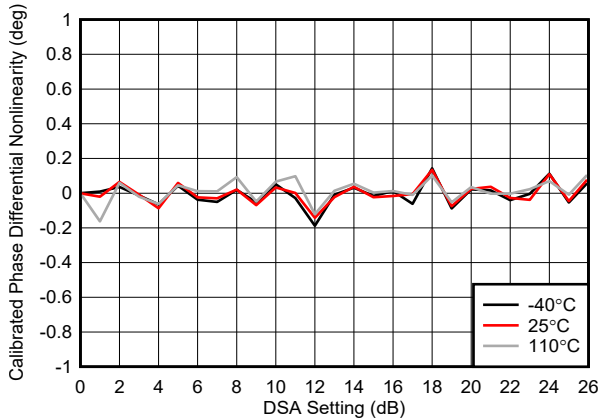


图 6-249. TX DSA Calibrated Phase Integrated Nonlinearity

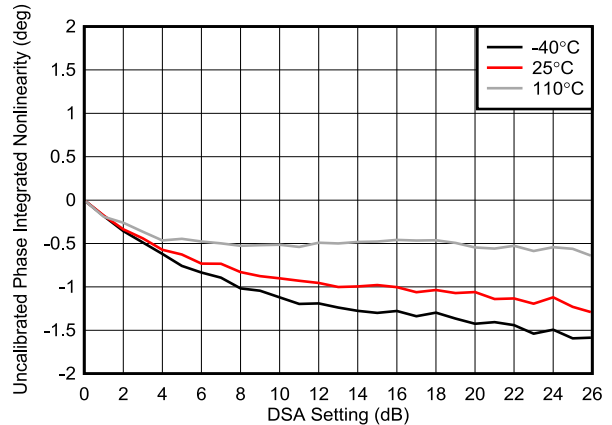


图 6-250. TX DSA Uncalibrated Phase Integrated Nonlinearity

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

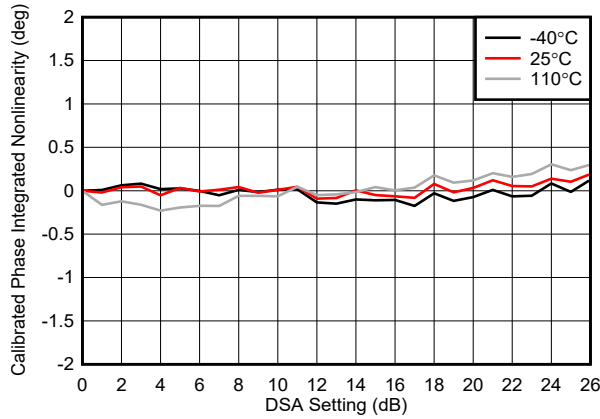
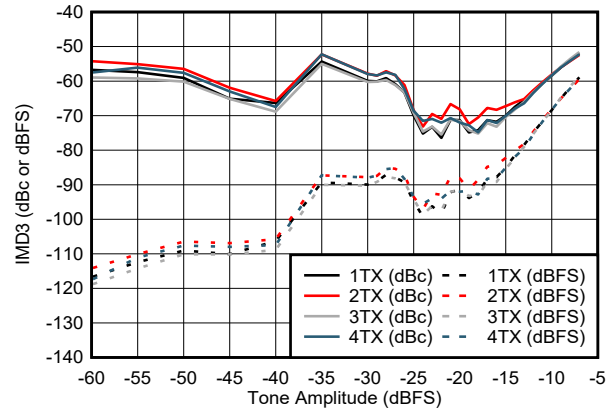
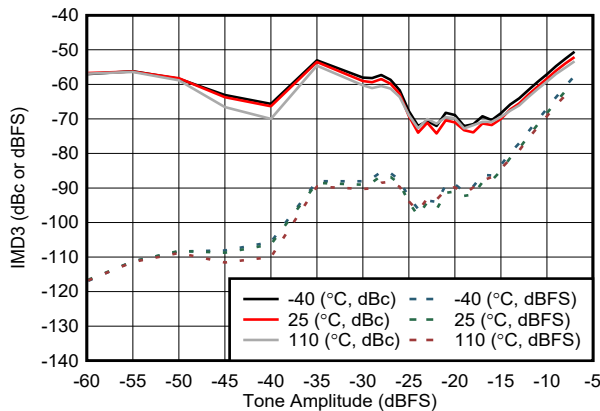


图 6-251. TX DSA Calibrated Amplitude Integrated Nonlinearity



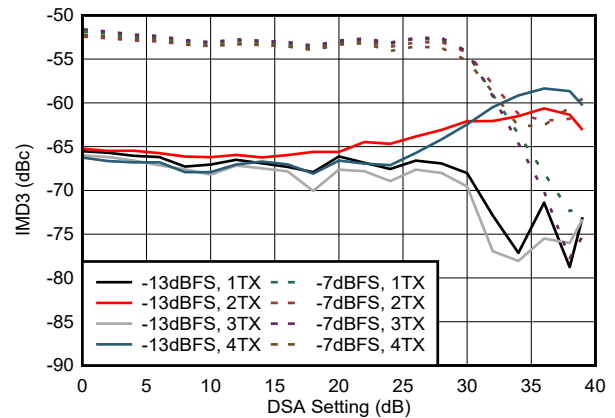
50-MHz tone spacing

图 6-252. TX IMD3 vs Digital Amplitude at 9.61 GHz



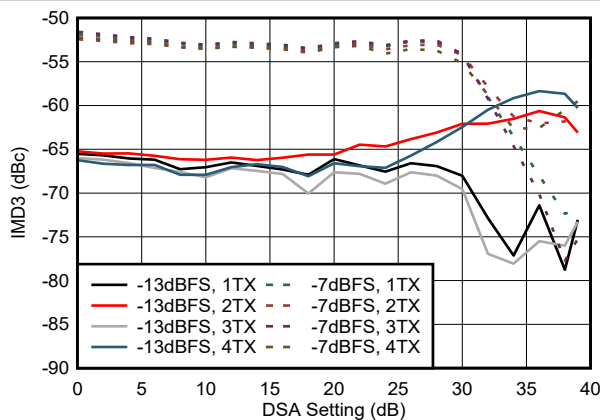
50-MHz tone spacing

图 6-253. TX IMD3 vs Digital Amplitude at 9.61 GHz



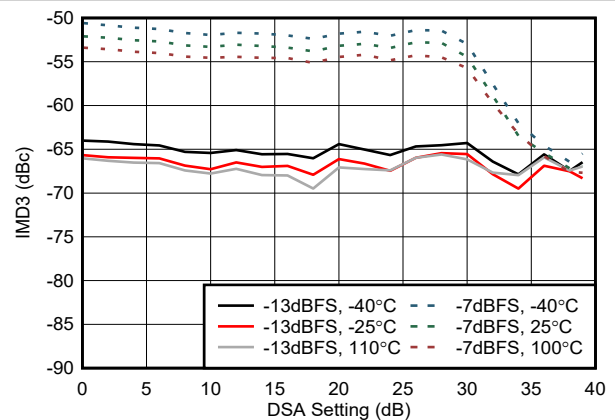
50-MHz tone spacing

图 6-254. TX IMD3 vs DSA Setting at 9.61 GHz



50-MHz tone spacing

图 6-255. TX IMD3 vs DSA Setting at 9.61 GHz



50-MHz tone spacing

图 6-256. TX IMD3 vs DSA Setting at 9.61 GHz

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

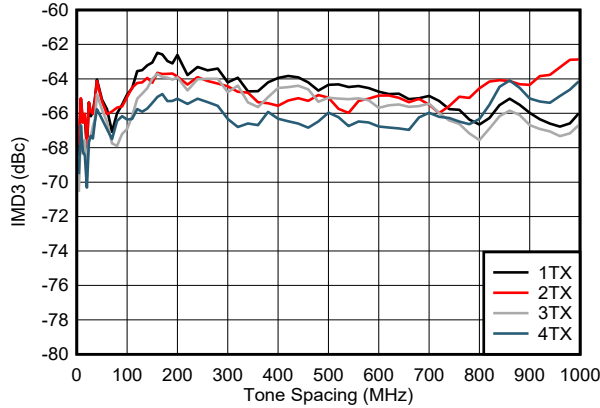


图 6-257. TX IMD3 vs Tone Spacing at 9.61 GHz

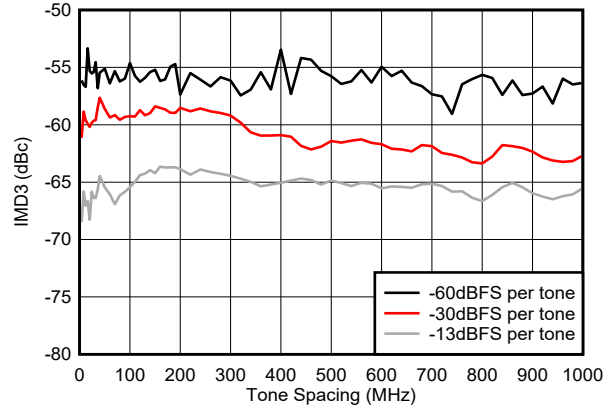


图 6-258. TX IMD3 vs Tone Spacing at 9.61 GHz

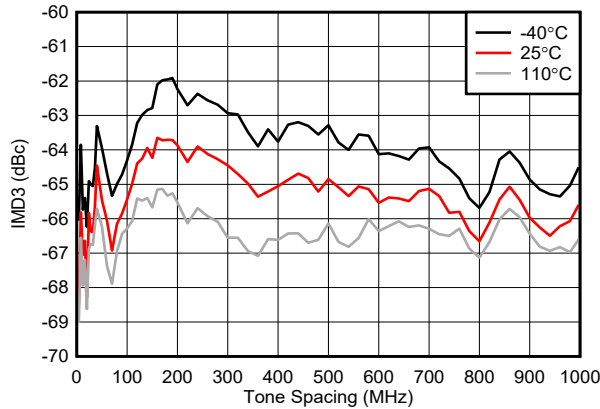


图 6-259. TX IMD3 vs Tone Spacing at 9.61 GHz

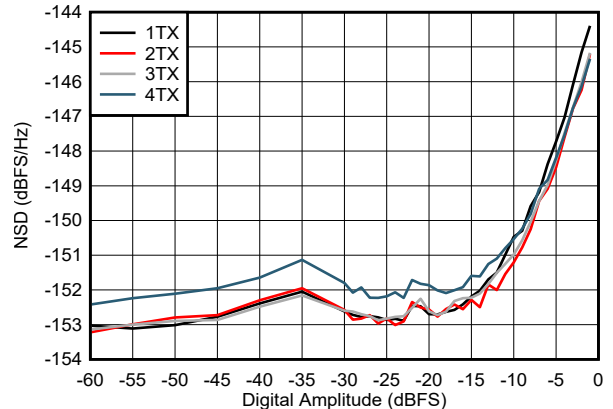


图 6-260. TX NSD vs Digital Amplitude at 9.61 GHz

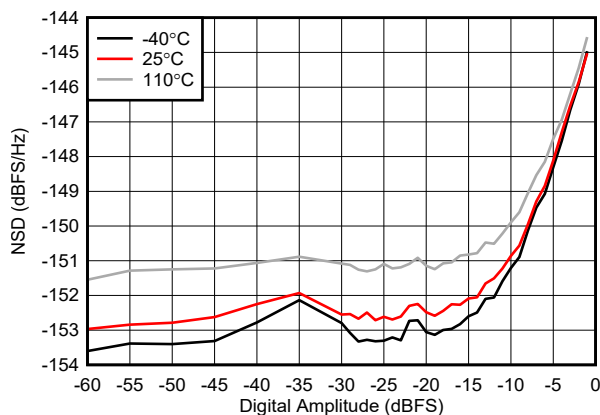


图 6-261. TX NSD vs Digital Amplitude at 9.61 GHz

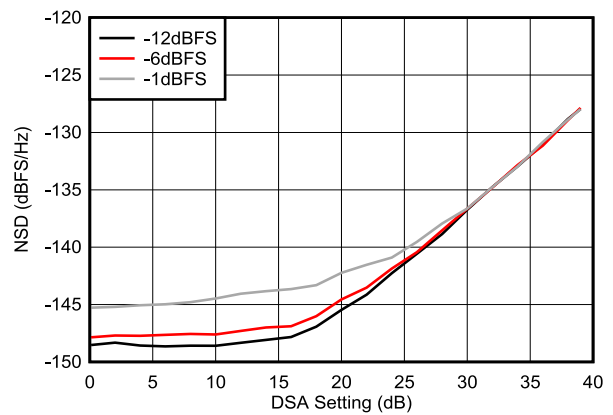


图 6-262. TX NSD vs DSA Setting at 9.61 GHz



### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

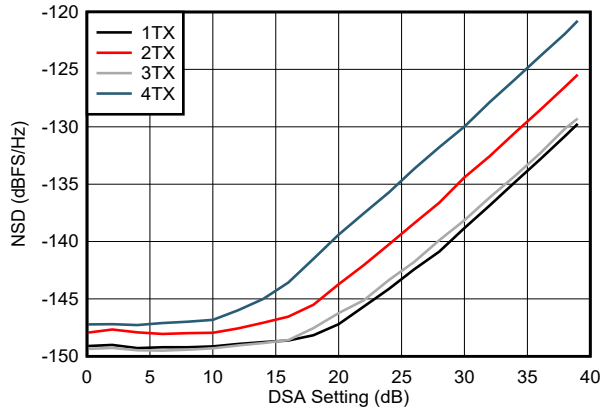


图 6-263. TX NSD vs DSA Setting at 9.61 GHz

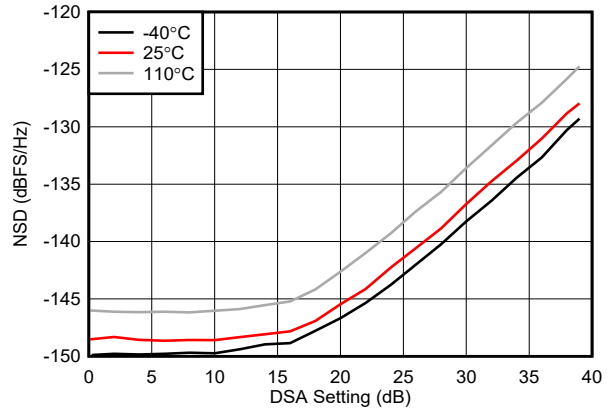
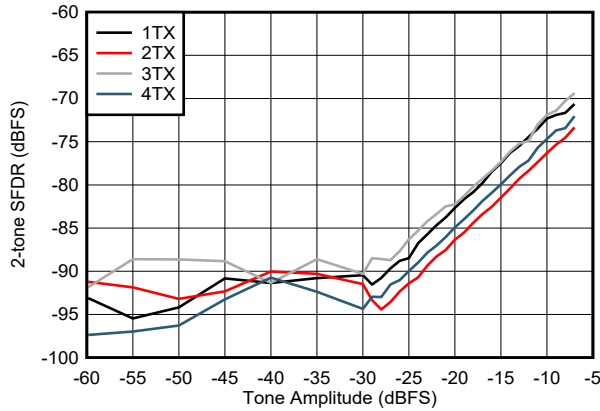
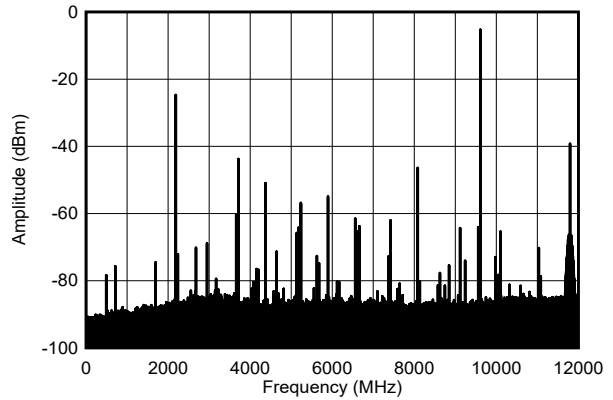


图 6-264. TX NSD vs DSA Setting at 9.61 GHz



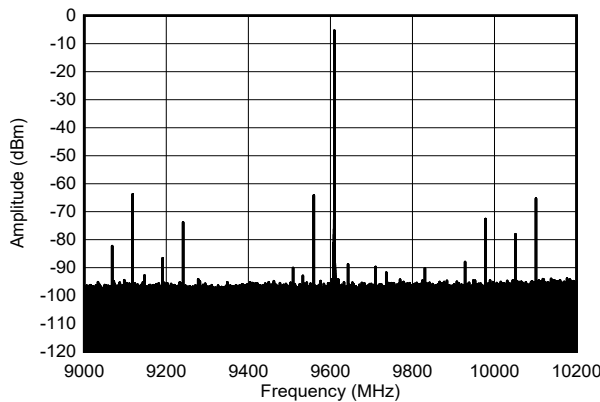
50-MHz tone spacing

图 6-265. TX 2-tone SFDR vs Digital Amplitude at 9.61 GHz



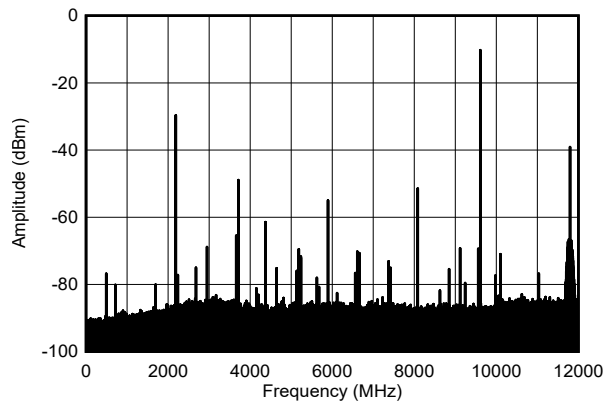
Includes PCB and cable losses.

图 6-266. TX Single Tone Spectrum at 9.61 GHz and -1dBFS (wideband)



Includes PCB and cable losses.

图 6-267. TX Single Tone Spectrum at 9.61 GHz and -1dBFS (1.2GHz BW)

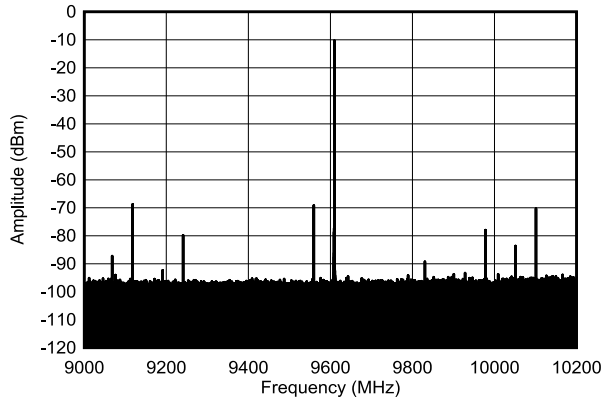


Includes PCB and cable losses.

图 6-268. TX Single Tone Spectrum at 9.61 GHz and -6dBFS (wideband)

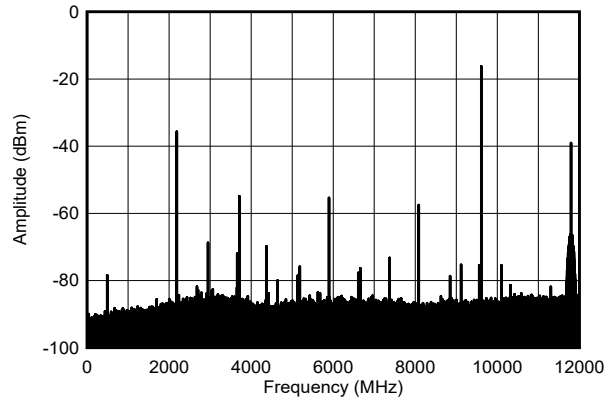
### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



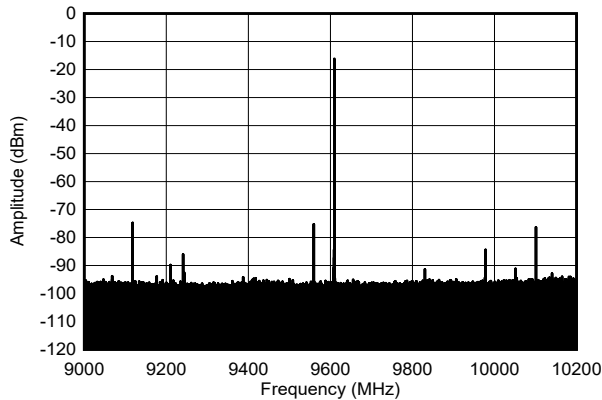
Includes PCB and cable losses.

**图 6-269. TX Single Tone Spectrum at 9.61 GHz and -6dBFS (1.2GHz BW)**



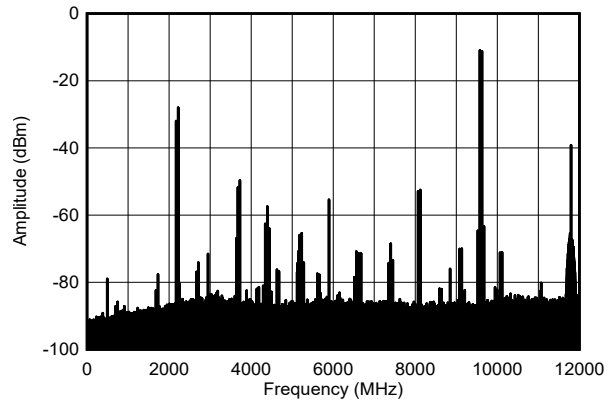
Includes PCB and cable losses.

**图 6-270. TX Single Tone Spectrum at 9.61 GHz and -12dBFS (wideband)**



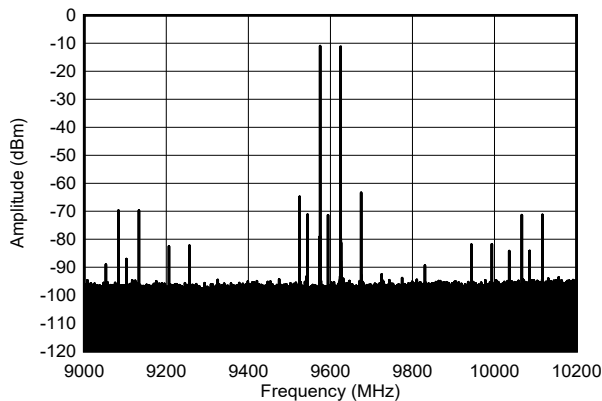
Includes PCB and cable losses.

**图 6-271. TX Single Tone Spectrum at 9.61 GHz and -12dBFS (1.2GHz BW)**



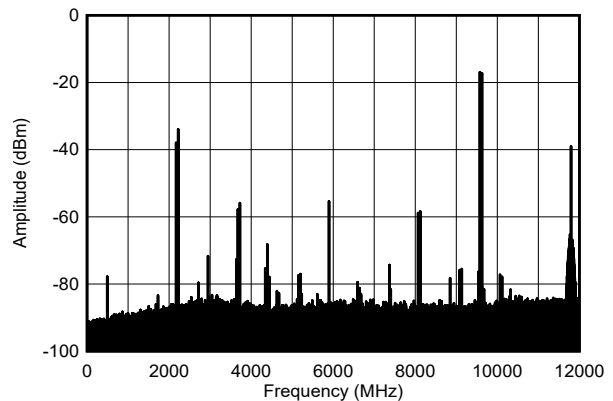
Includes PCB and cable losses, 50-MHz tone spacing.

**图 6-272. TX 2-Tone Spectrum at 9.61 GHz and -7dBFS (wideband)**



Includes PCB and cable losses, 50-MHz tone spacing.

**图 6-273. TX 2-Tone Spectrum at 9.61 GHz and -7dBFS (1.2GHz BW)**

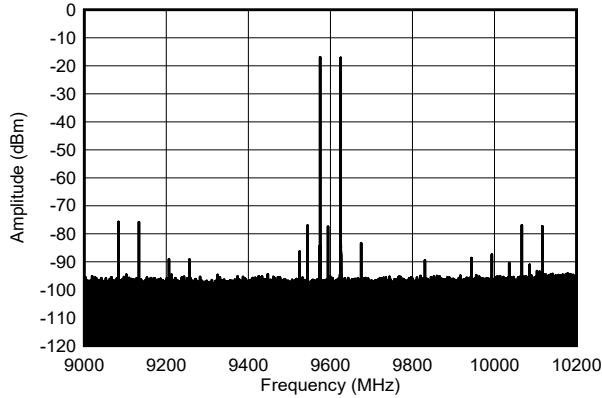


Includes PCB and cable losses, 50-MHz tone spacing.

**图 6-274. TX 2-Tone Spectrum at 9.61 GHz and -13dBFS (wideband)**

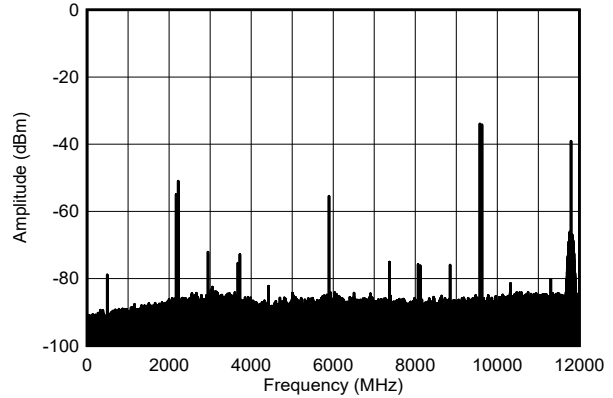
### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



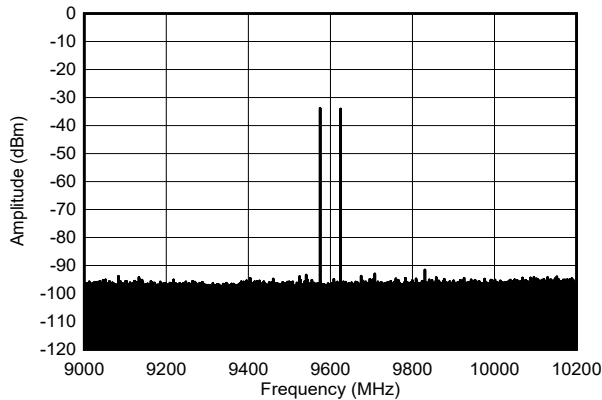
Includes PCB and cable losses, 50-MHz tone spacing.

**图 6-275. TX 2-Tone Spectrum at 9.61 GHz and -13dBFS (1.2GHz BW)**



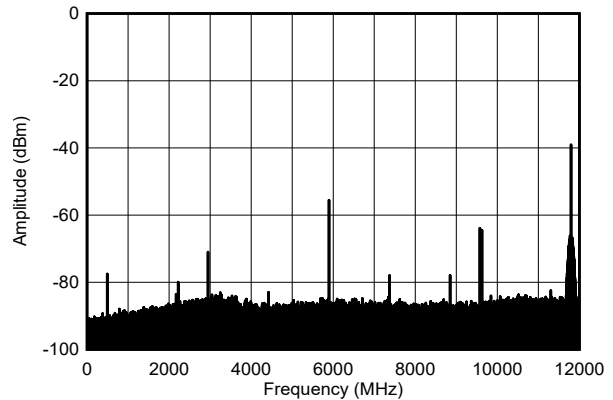
Includes PCB and cable losses, 50-MHz tone spacing.

**图 6-276. TX 2-Tone Spectrum at 9.61 GHz and -30dBFS Each (wideband)**



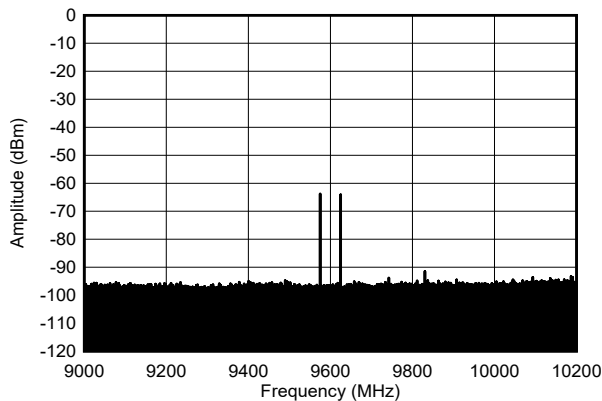
Includes PCB and cable losses, 50-MHz tone spacing.

**图 6-277. TX 2-Tone Spectrum at 9.61 GHz and -30dBFS Each (1.2GHz BW)**



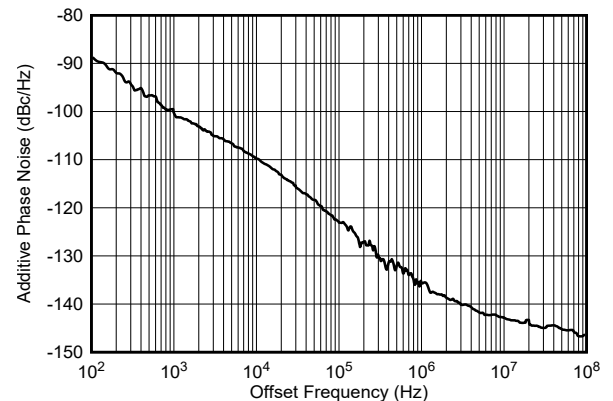
Includes PCB and cable losses, 50-MHz tone spacing.

**图 6-278. TX 2-Tone Spectrum at 9.61 GHz and -60dBFS Each (wideband)**



Includes PCB and cable losses, 50-MHz tone spacing.

**图 6-279. TX 2-Tone Spectrum at 9.61 GHz and -60dBFS Each (1.2GHz BW)**



Single sideband, external clock mode, input clock phase noise removed

**图 6-280. TX Additive Phase Noise vs Offset Frequency at 9.61 GHz**

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 1474.56\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

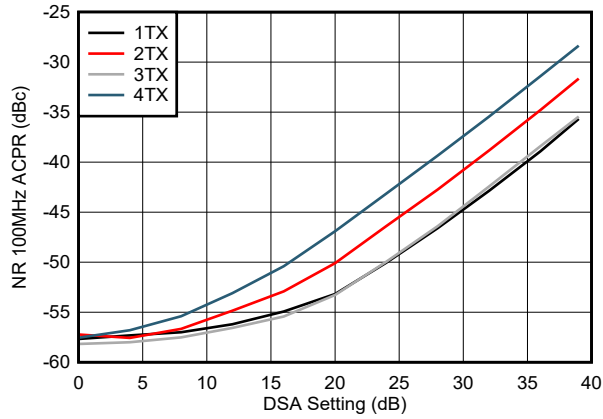


图 6-281. TX NR100MHz ACPR vs DSA Setting at 9.61 GHz

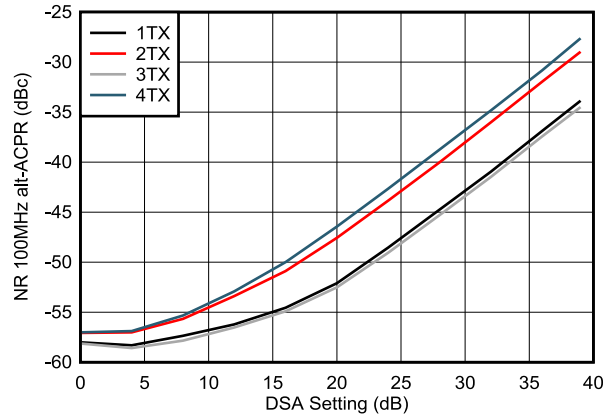


图 6-282. TX NR100MHz alt-ACPR vs DSA Setting at 9.61 GHz

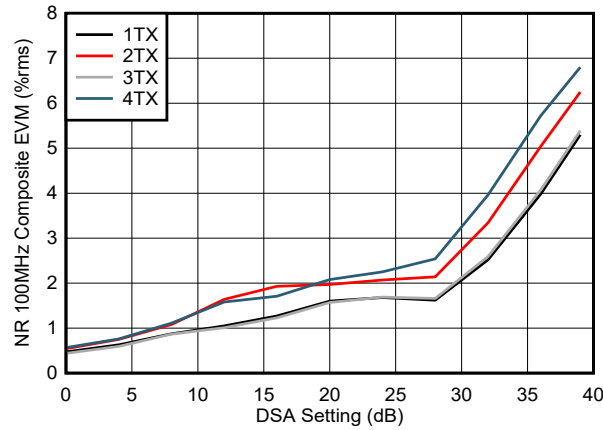
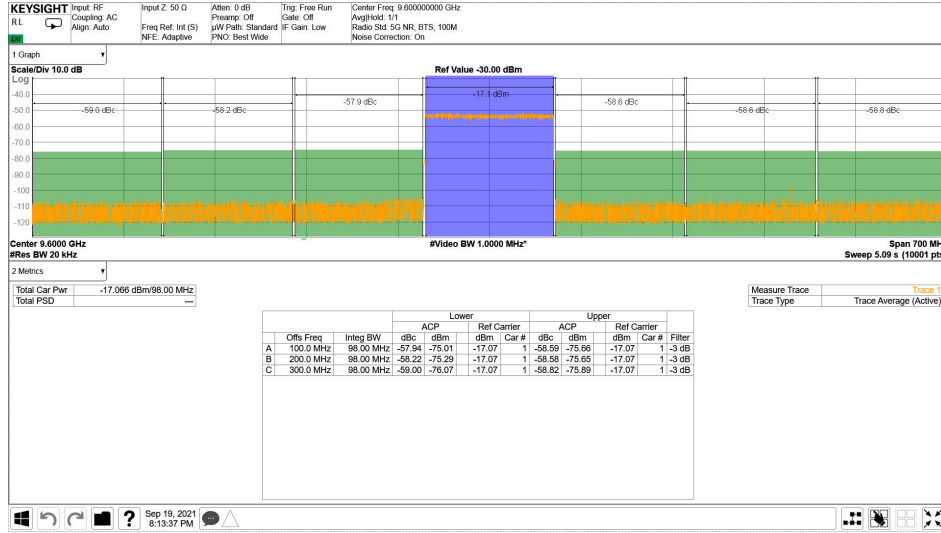


图 6-283. TX NR100MHz EVM vs DSA Setting at 9.61 GHz

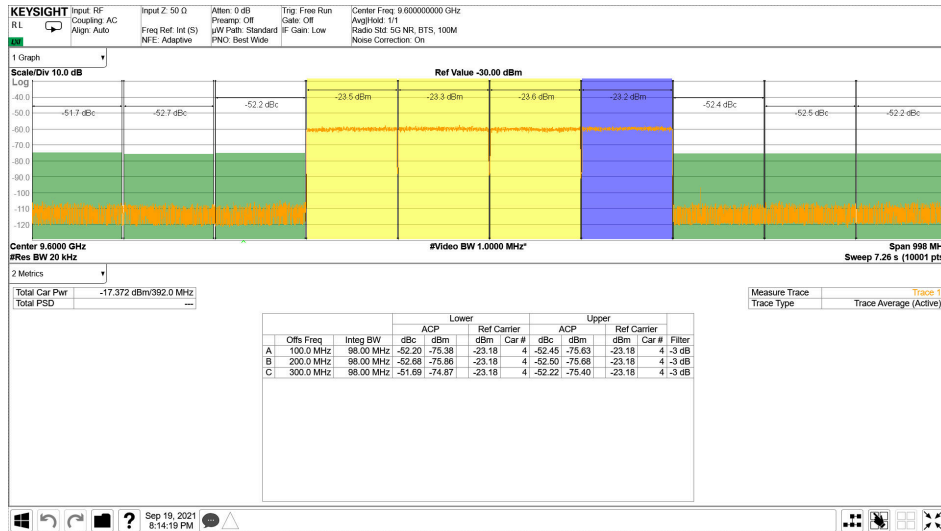
### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 1474.56\text{ MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



Includes PCB and cable losses.

图 6-284. TX NR100MHz Output Spectrum at 9.61 GHz

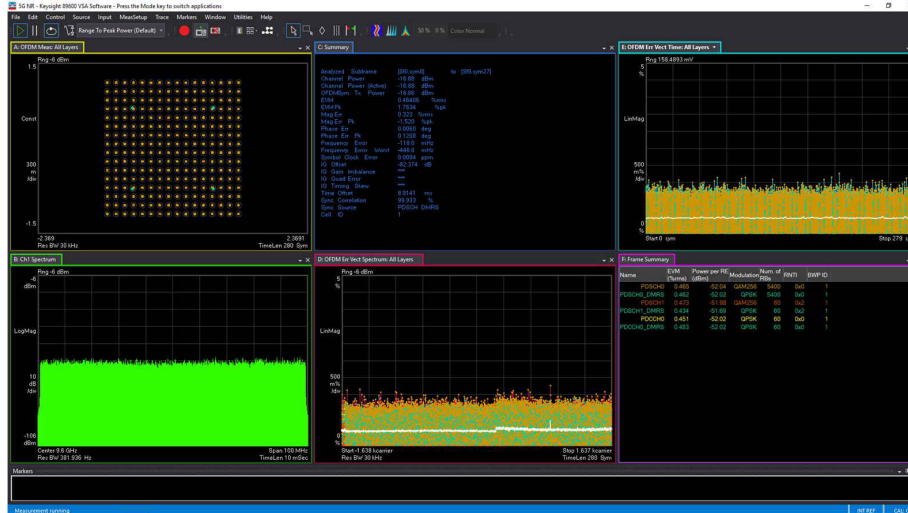


Includes PCB and cable losses.

图 6-285. TX 4xNR100MHz Output Spectrum at 9.61 GHz

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 1474.56\text{ MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



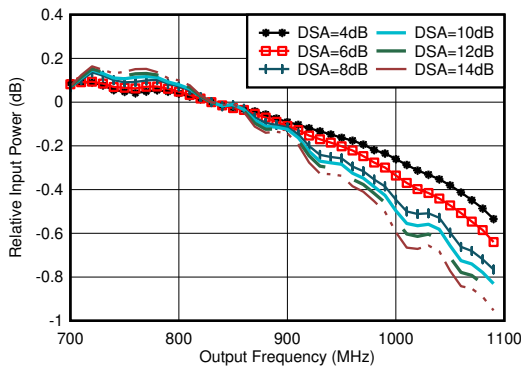
备注

Includes PCB and cable losses.

图 6-286. TX 100MHz NR EVM at 9.61 GHz

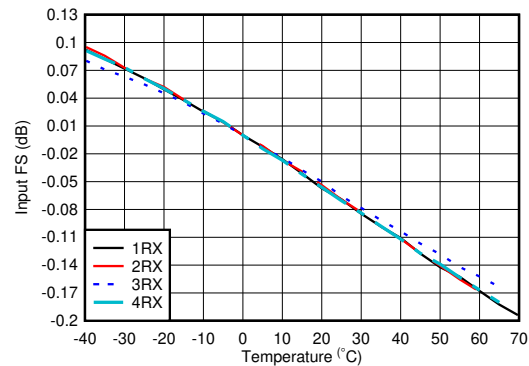
### 6.12.8 RX Typical Characteristics at 800 MHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 0.8 GHz matching, normalized to 830 MHz

图 6-287. RX In-Band Gain Flatness for Channel 1RX,  $f_{IN} = 830\text{ MHz}$

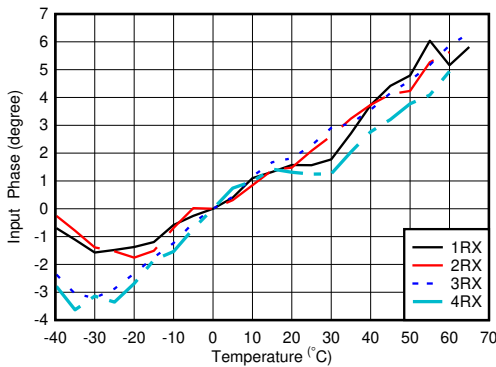


With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

图 6-288. RX Input Fullscale vs Temperature and Channel at 800MHz

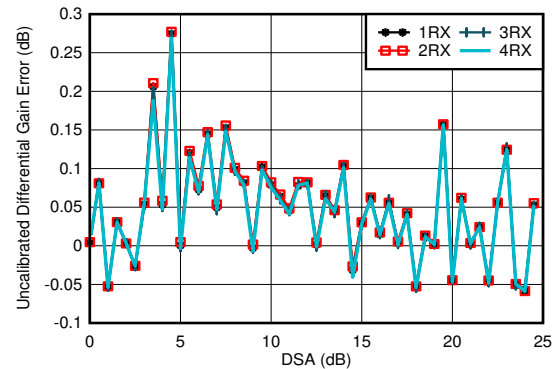
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 0.8 GHz matching, normalized to phase at  $25^\circ\text{C}$

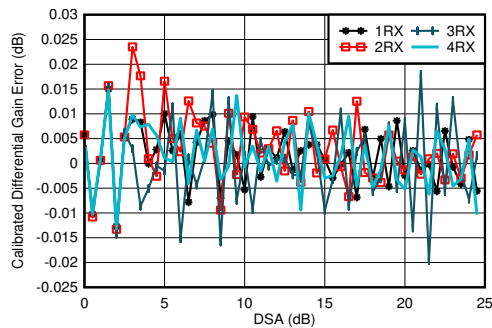
图 6-289. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 0.8\text{ GHz}$



With 0.8 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

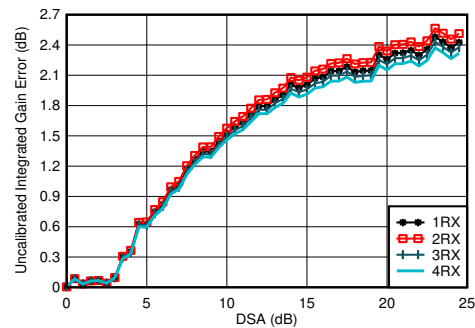
图 6-290. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

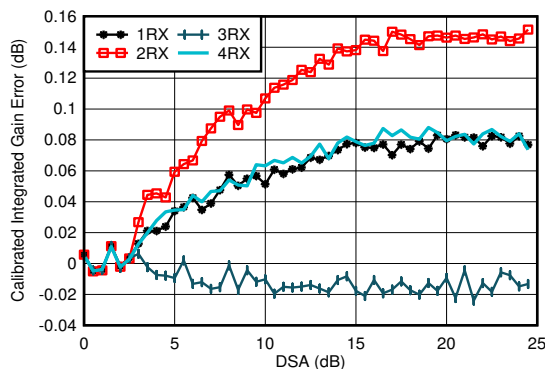
图 6-291. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

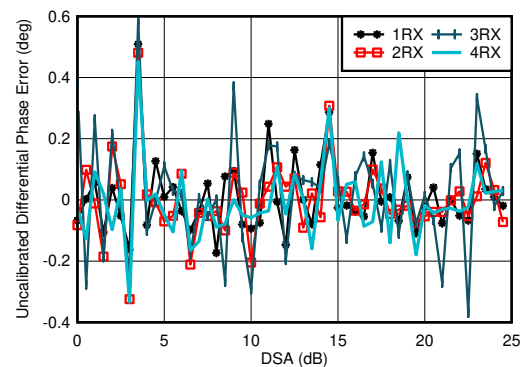
图 6-292. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-293. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



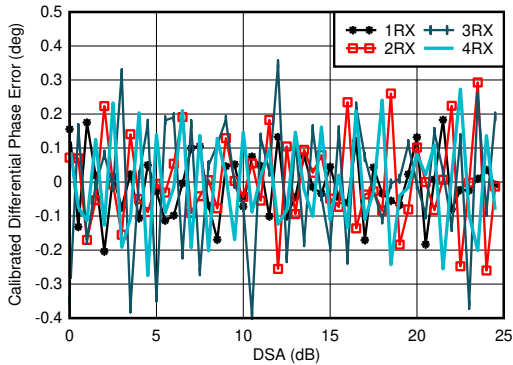
With 0.8 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$$

图 6-294. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz

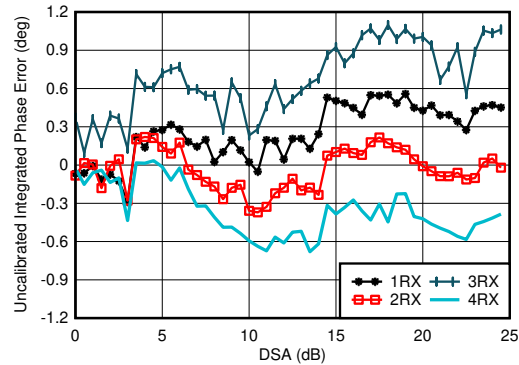
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



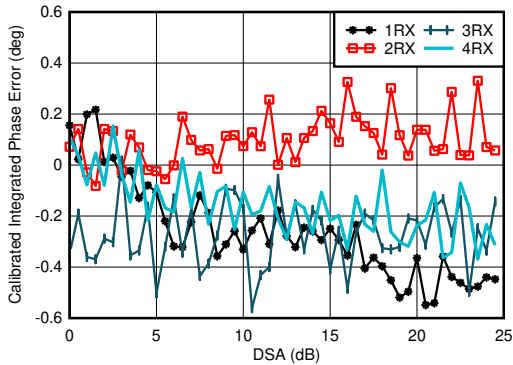
With 0.8 GHz matching  
 Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

图 6-295. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



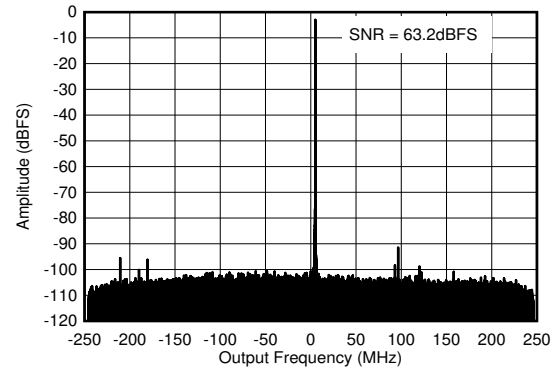
With 0.8 GHz matching  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-296. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



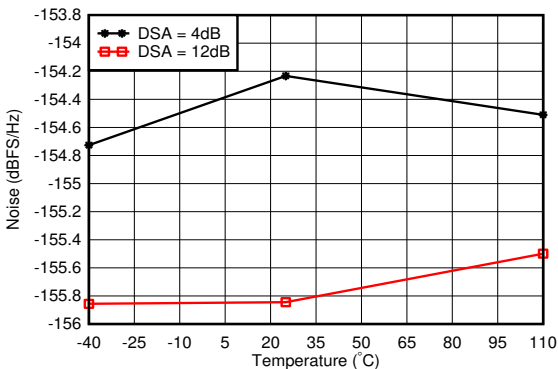
With 0.8 GHz matching  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-297. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



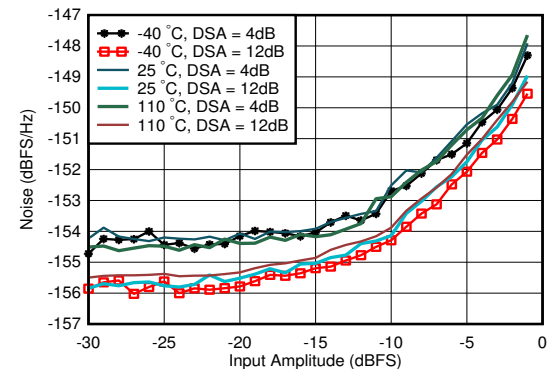
With 0.8 GHz matching,  $f_{IN} = 840\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

图 6-298. RX Output FFT at 0.8 GHz



With 0.8 GHz matching, 12.5-MHz offset from tone

图 6-299. RX Noise Spectral Density vs Temperature at 0.8 GHz



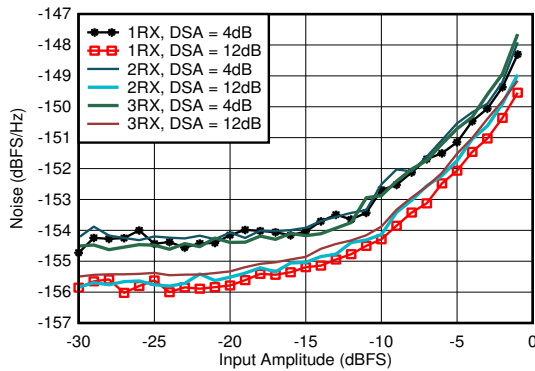
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

图 6-300. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz



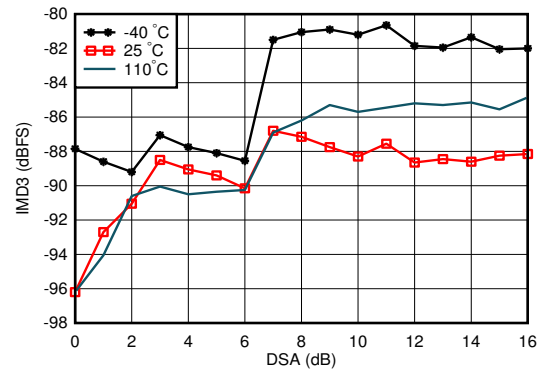
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



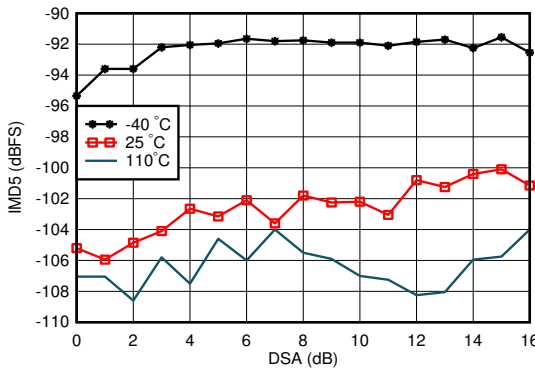
With 0.8 GHz matching, 12.5-MHz offset from tone

图 6-301. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz



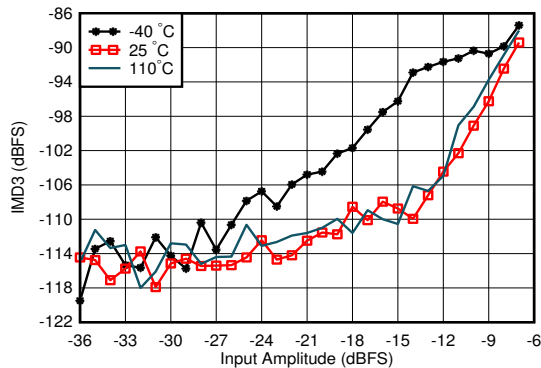
With 0.8 GHz matching, each tone - 7 dBFS, tone spacing = 20 MHz

图 6-302. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz



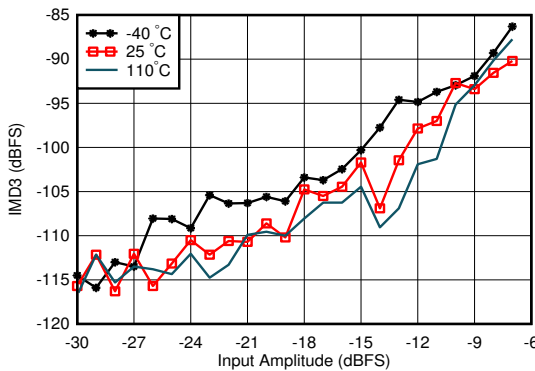
With 0.8 GHz matching, each tone - 7 dBFS, tone spacing = 20 MHz

图 6-303. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz



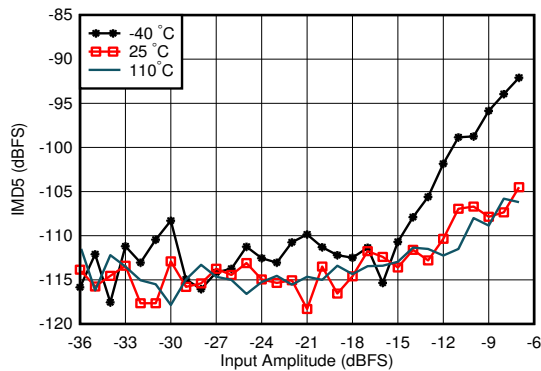
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

图 6-304. RX IMD3 vs Input Level and Temperature at 0.8 GHz



With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

图 6-305. RX IMD3 vs Input Level and Temperature at 0.8 GHz

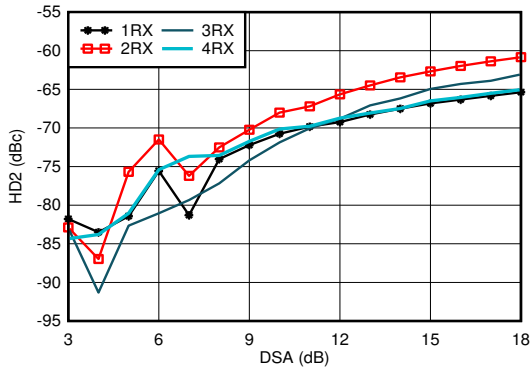


With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

图 6-306. RX IMD5 vs Input Level and Temperature at 0.8 GHz

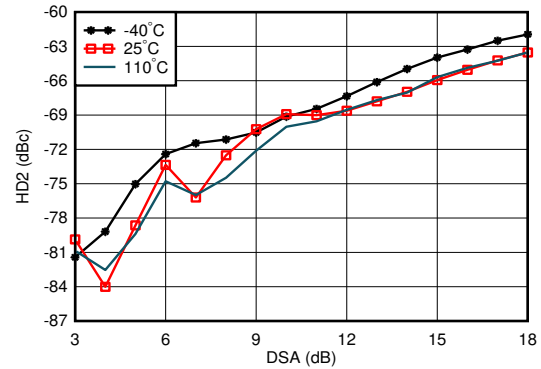
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



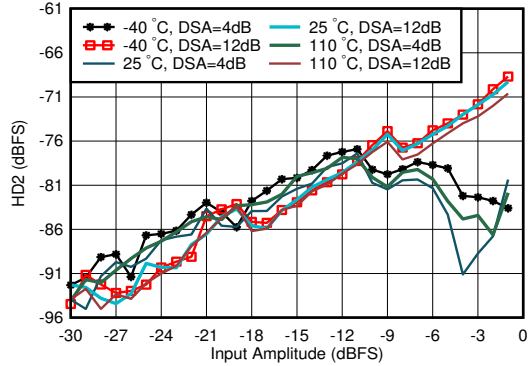
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-307. RX HD2 vs DSA Setting and Channel at 0.8 GHz



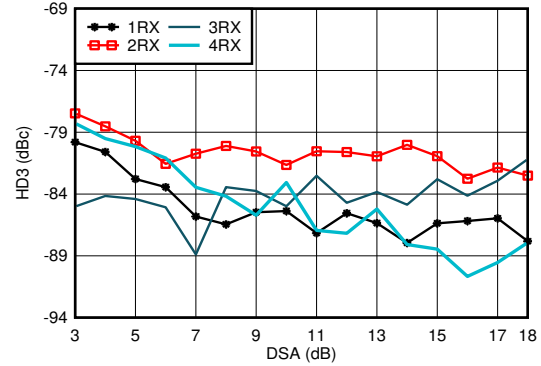
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-308. RX HD2 vs DSA Setting and Temperature at 0.8 GHz



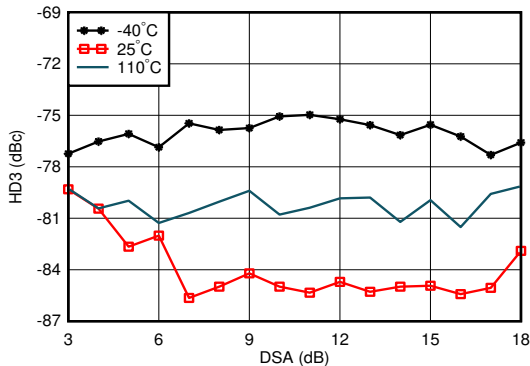
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-309. RX HD2 vs Input Level and Temperature at 0.8 GHz



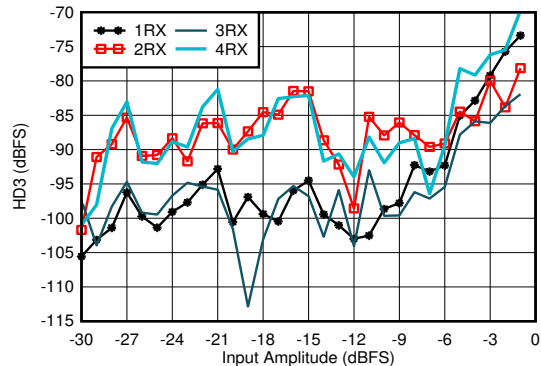
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-310. RX HD3 vs DSA Setting and Channel at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-311. RX HD3 vs DSA Setting and Temperature at 0.8 GHz

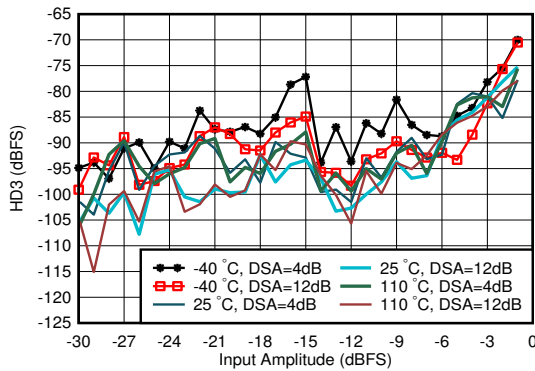


With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-312. RX HD3 vs Input Level and Channel at 0.8 GHz

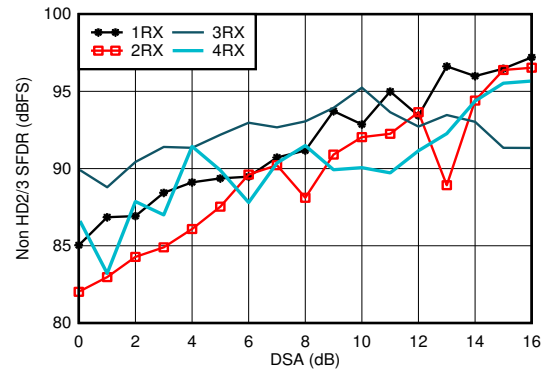
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



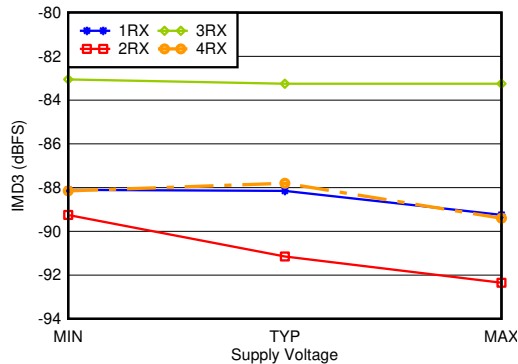
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-313. RX HD3 vs Input Level and Temperature at 0.8 GHz



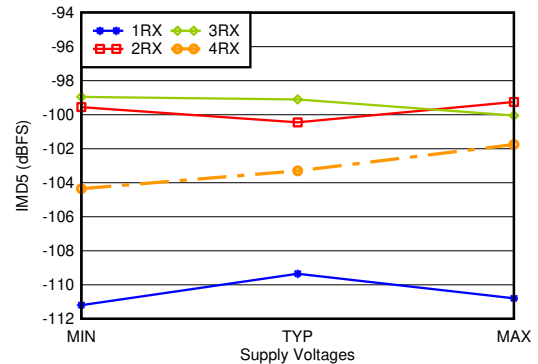
With 0.8 GHz matching

图 6-314. RX Non-HD2/3 vs DSA Setting at 0.8 GHz



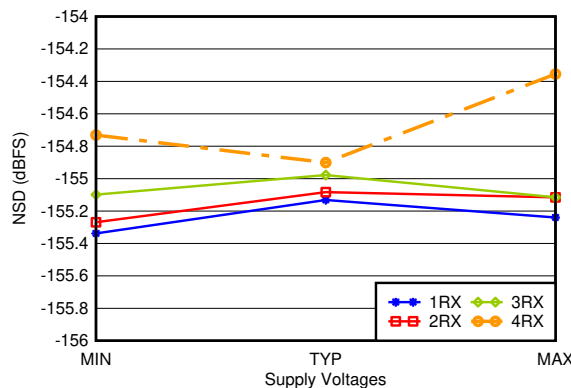
With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-315. RX IMD3 vs Supply and Channel at 0.8 GHz



With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-316. RX IMD5 vs Supply and Channel at 0.8 GHz

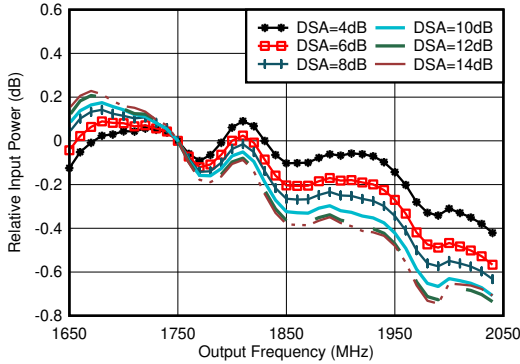


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-317. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

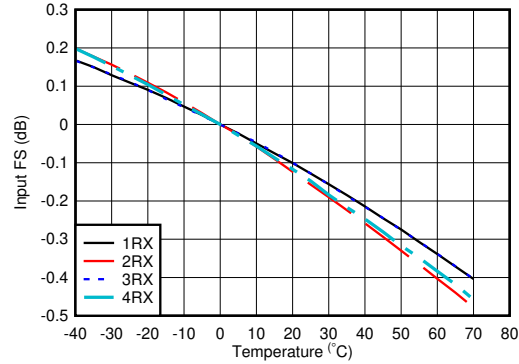
### 6.12.9 RX Typical Characteristics at 1.75 GHz - 1.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



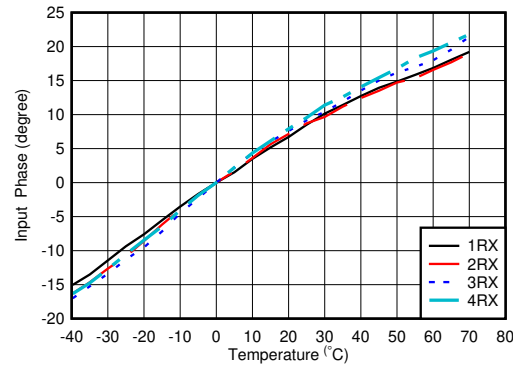
With 1.8 GHz matching, normalized to 1.75 GHz

图 6-318. RX In-Band Gain Flatness,  $f_{IN} = 1750\text{ MHz}$



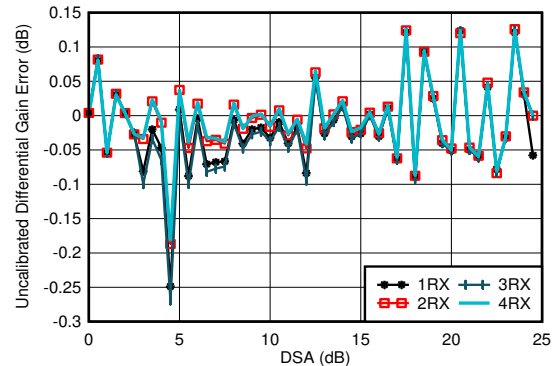
With 1.8 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

图 6-319. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at  $25^\circ\text{C}$

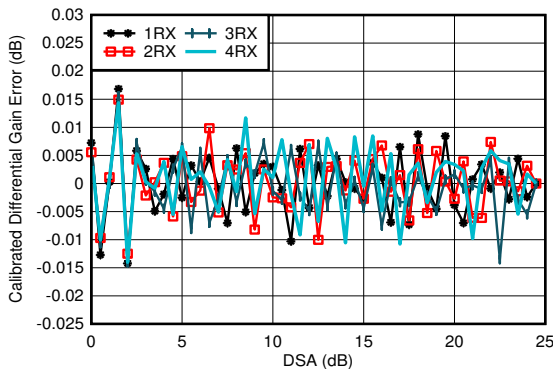
图 6-320. RX Input Phase vs Temperature and DSA at  $f_{IN} = 1.75\text{ GHz}$



With 1.8 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

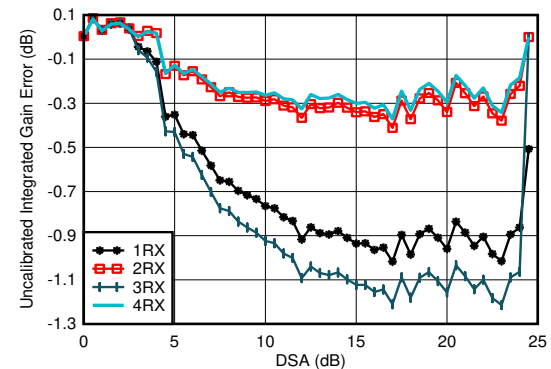
图 6-321. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

图 6-322. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



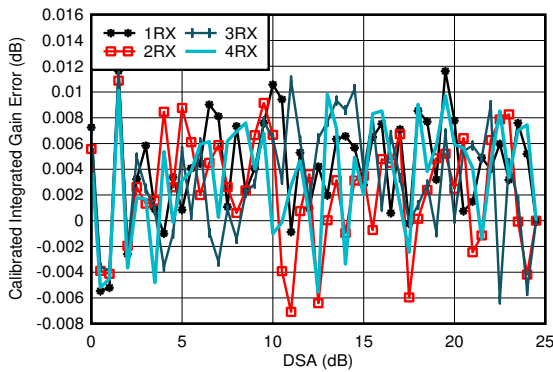
With 1.8 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-323. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

### 6.12.9 RX Typical Characteristics at 1.75 GHz - 1.9 GHz (continued)

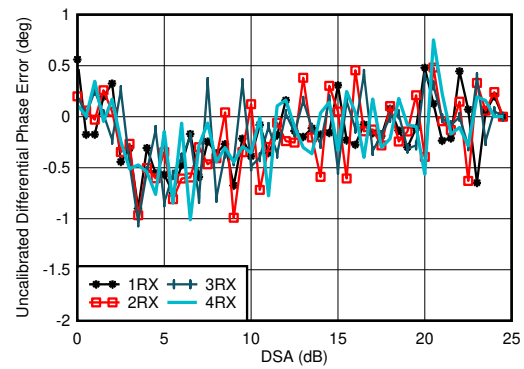
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 1.8 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

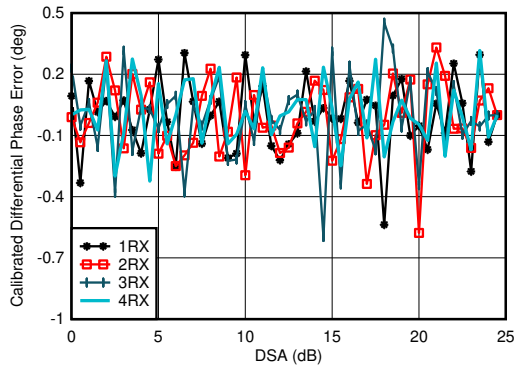
图 6-324. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$$

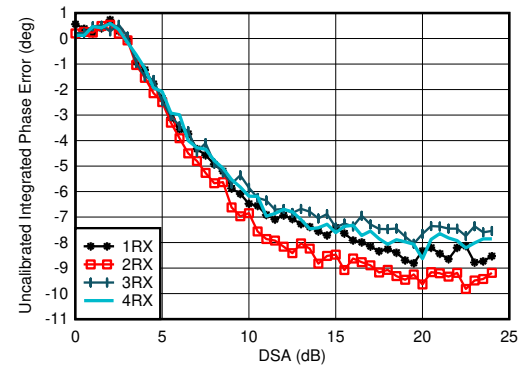
图 6-325. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$$

图 6-326. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



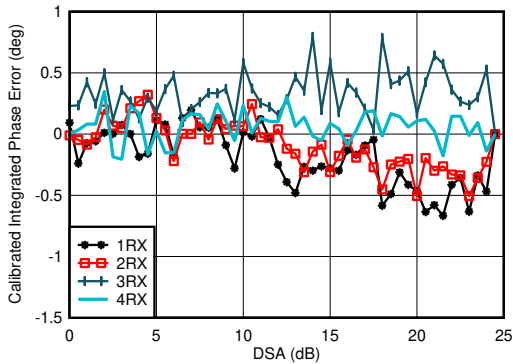
With 1.8 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

图 6-327. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

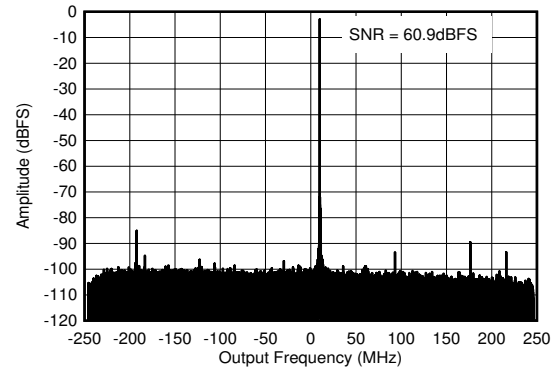
### 6.12.9 RX Typical Characteristics at 1.75 GHz - 1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



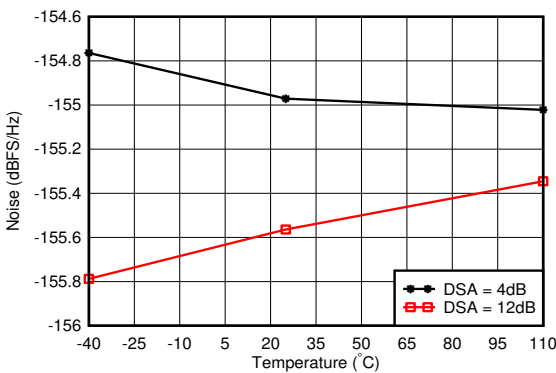
With 1.8 GHz matching  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-328. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



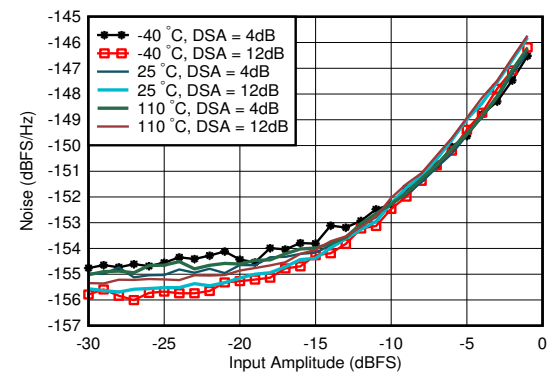
With 1.8 GHz matching,  $f_{IN} = 2610\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

图 6-329. RX Output FFT at 1.75 GHz



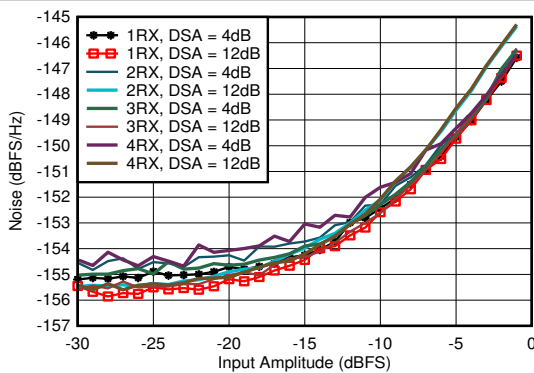
With 1.8 GHz matching, 12.5-MHz offset from tone

图 6-330. RX Noise Spectral Density vs Temperature at 1.75 GHz



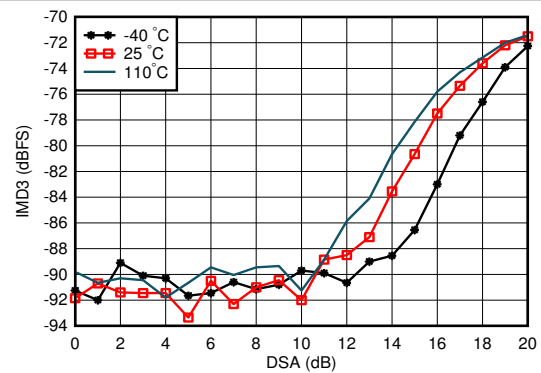
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

图 6-331. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



With 1.8 GHz matching, 12.5-MHz offset from tone

图 6-332. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz

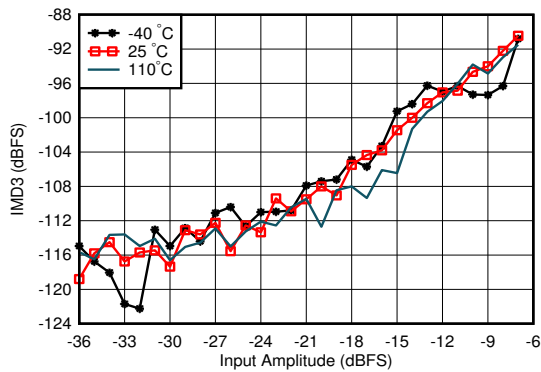


With 1.8 GHz matching, each tone -7 dBFS, tone spacing = 20 MHz

图 6-333. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz

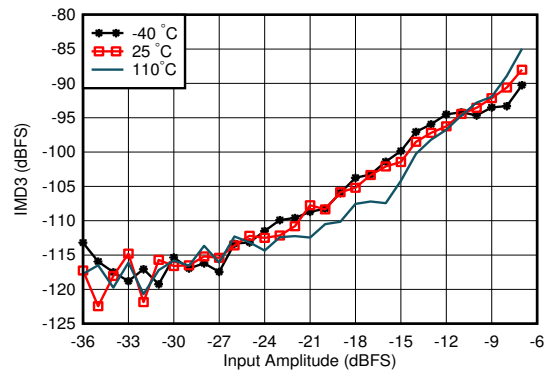
### 6.12.9 RX Typical Characteristics at 1.75 GHz - 1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



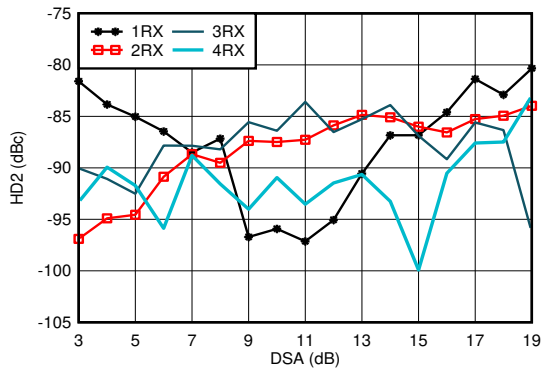
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

图 6-334. RX IMD3 vs Input Level and Temperature at 1.75 GHz



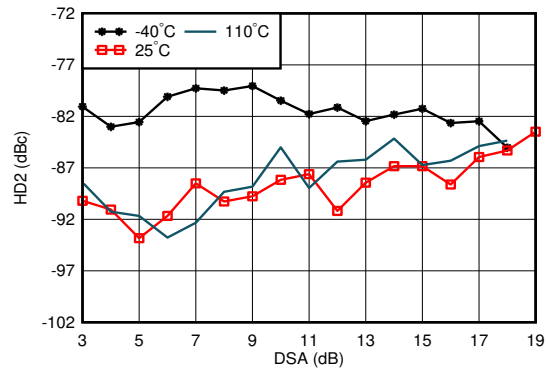
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

图 6-335. RX IMD3 vs Input Level and Temperature at 1.75 GHz



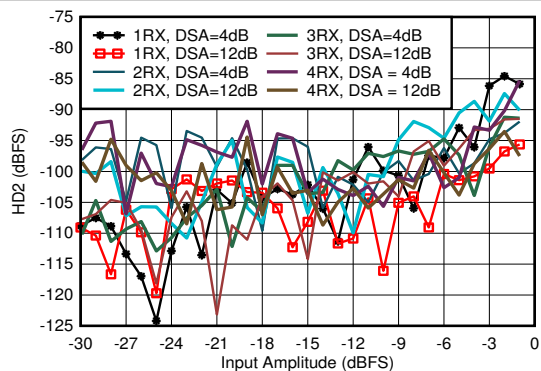
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-336. RX HD2 vs DSA Setting and Channel at 1.9 GHz



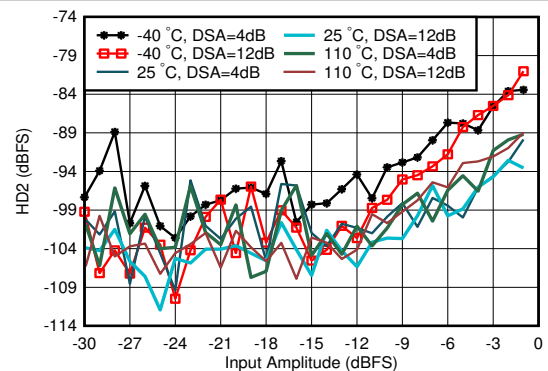
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-337. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-338. RX HD2 vs Input Amplitude and Channel at 1.9 GHz

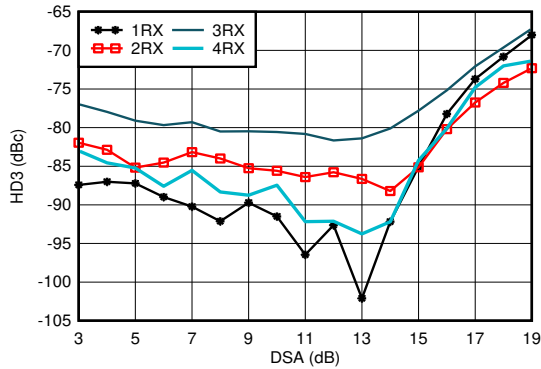


With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-339. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz

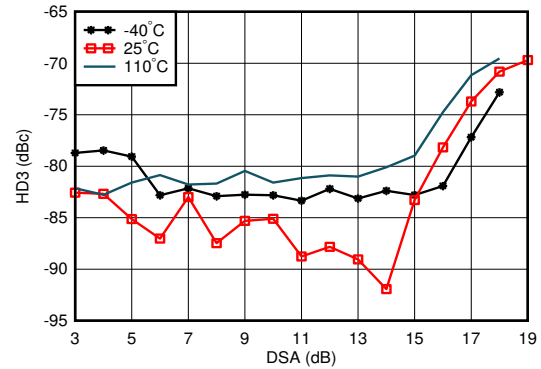
### 6.12.9 RX Typical Characteristics at 1.75 GHz - 1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



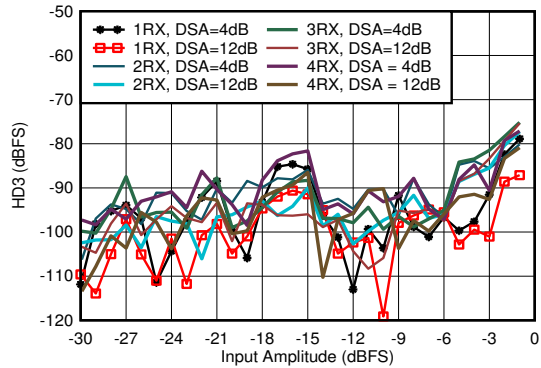
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

图 6-340. RX HD3 vs DSA Setting and Channel at 1.9 GHz



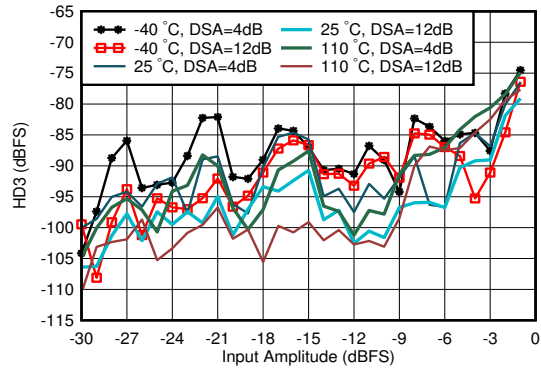
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

图 6-341. RX HD3 vs DSA Setting and Temperature at 1.9 GHz



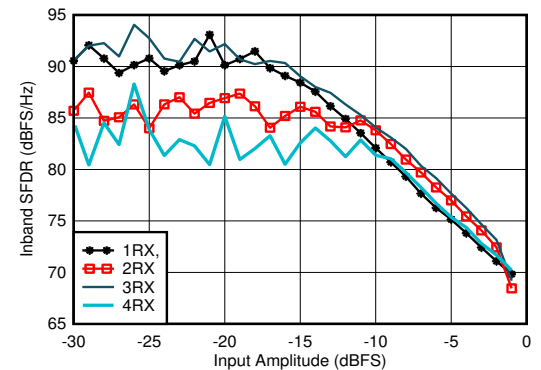
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

图 6-342. RX HD3 vs Input Level and Channel at 1.9 GHz



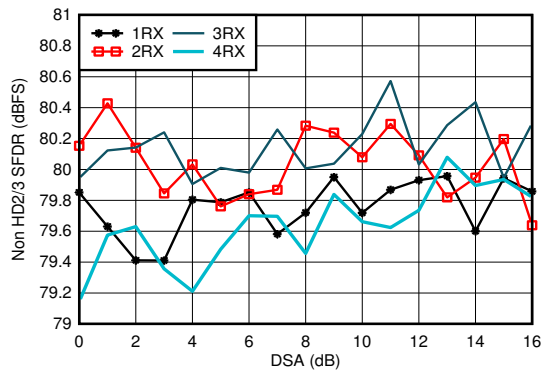
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

图 6-343. RX HD3 vs Input Level and Temperature at 1.9 GHz



With 1.8 GHz matching, decimated by 3

图 6-344. RX In-Band SFDR ( $\pm 400\text{ MHz}$ ) vs Input Amplitude at 1.75 GHz



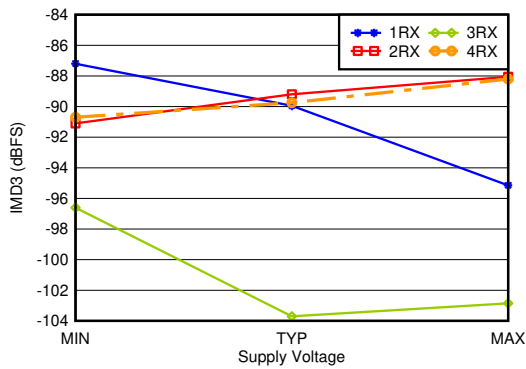
With 1.8 GHz matching

图 6-345. RX Non-HD2/3 vs DSA Setting at 1.75 GHz



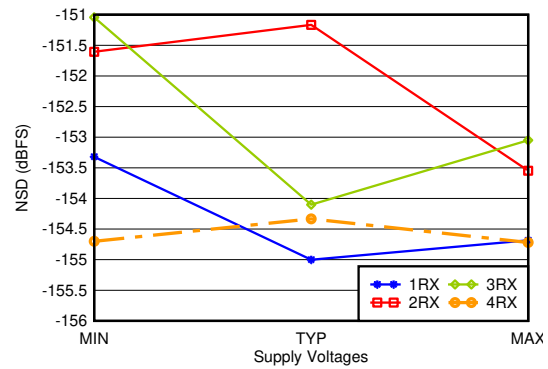
### 6.12.9 RX Typical Characteristics at 1.75 GHz - 1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{IN} = -3$  dBFS, DSA setting = 4 dB.



With 1.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-346. RX IMD3 vs Supply and Channel at 1.75 GHz

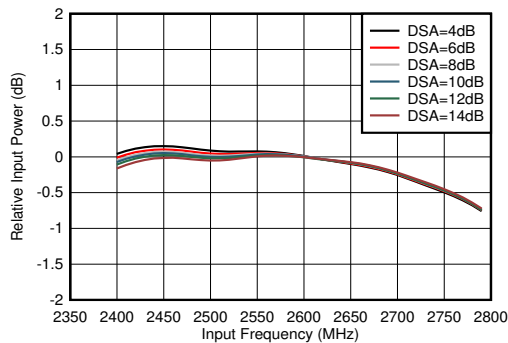


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-347. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

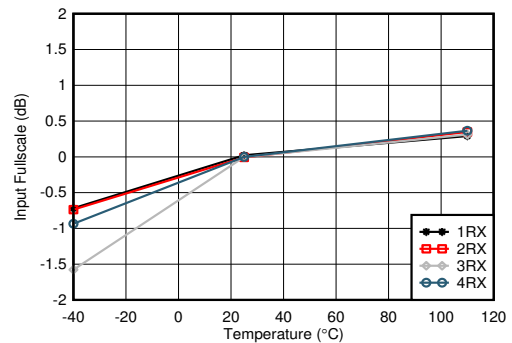
### 6.12.10 RX Typical Characteristics at 2.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{IN} = -3$  dBFS, DSA setting = 4 dB.



With matching, normalized to power at 2.6 GHz for each DSA setting

图 6-348. RX Inband Gain Flatness,  $f_{IN} = 2600$  MHz

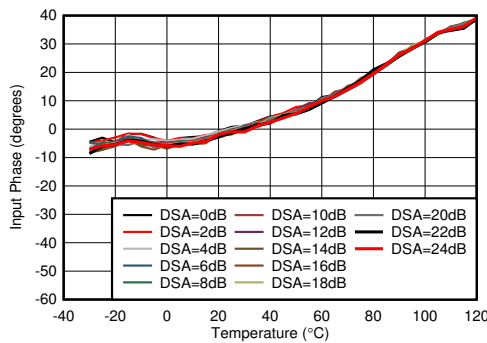


With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

图 6-349. RX Input Fullscale vs Temperature and Channel at 2.6 GHz

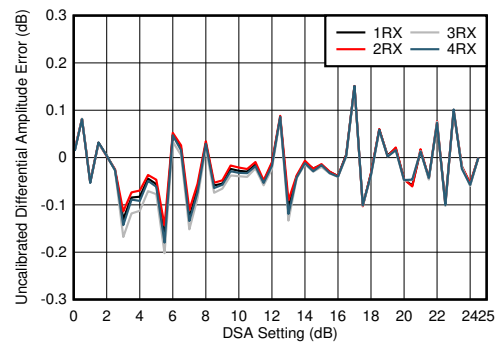
### 6.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 2.6 GHz matching, normalized to phase at  $25^\circ\text{C}$

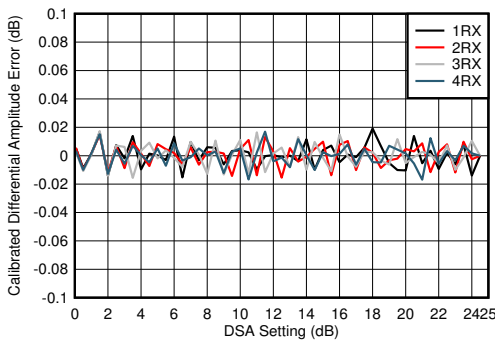
图 6-350. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 2.6\text{ GHz}$



With 2.6 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

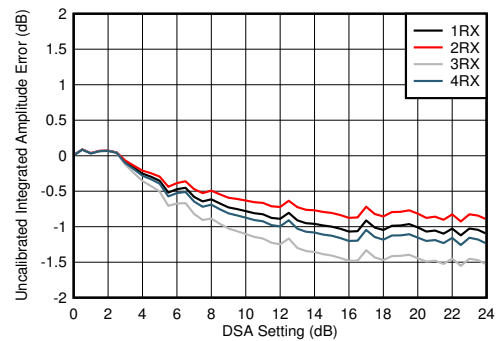
图 6-351. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

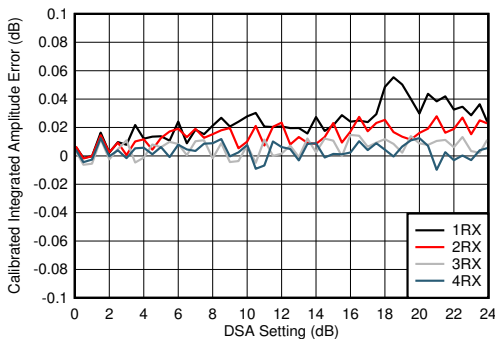
图 6-352. RX Calibrated Differential Amplitude Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

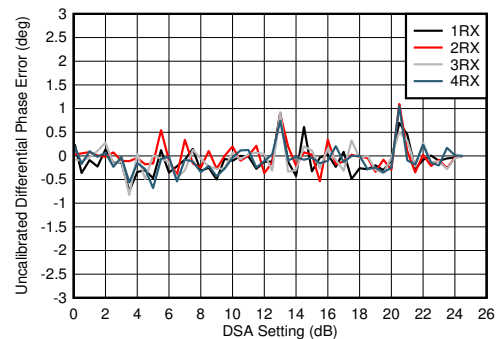
图 6-353. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 2.6 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-354. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



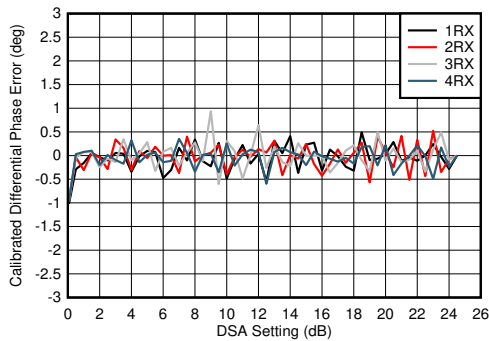
With 2.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$$

图 6-355. RX Uncalibrated Differential Phase Error vs DSA Setting at 2.6 GHz

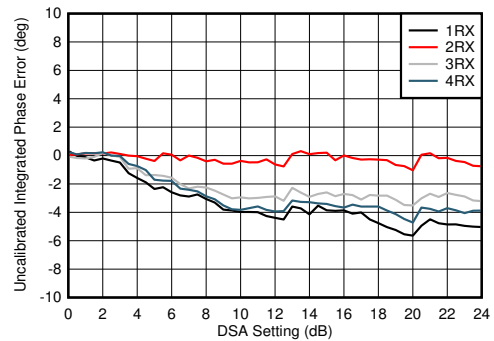
### 6.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



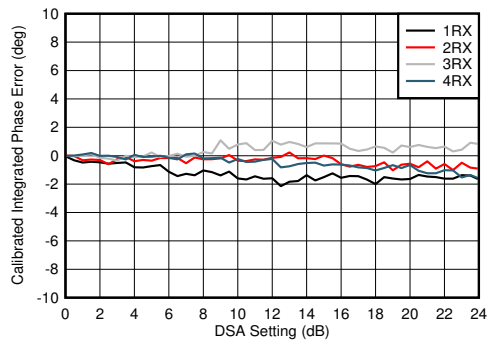
With 2.6 GHz matching  
Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

图 6-356. RX Calibrated Differential Phase Error vs DSA Setting at 2.6 GHz



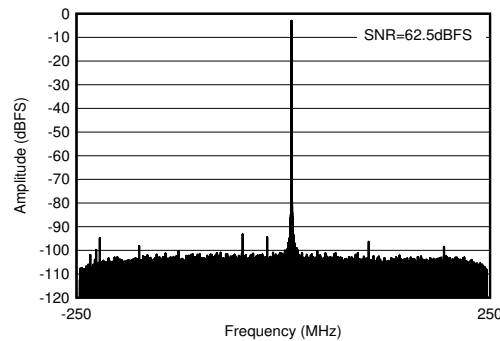
With 2.6 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-357. RX Uncalibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



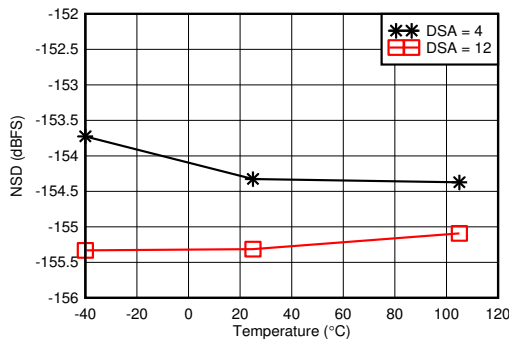
With 2.6 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-358. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



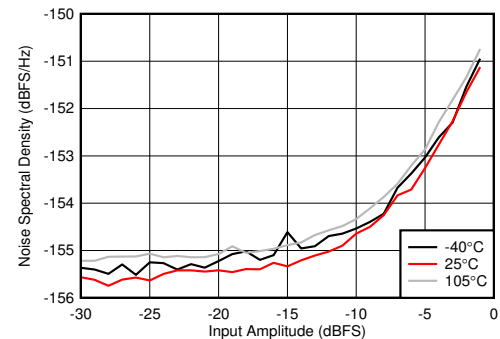
With 2.6 GHz matching,  $f_{\text{IN}} = 2610 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$

图 6-359. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

图 6-360. RX Noise Spectral Density vs Temperature at 2.6 GHz

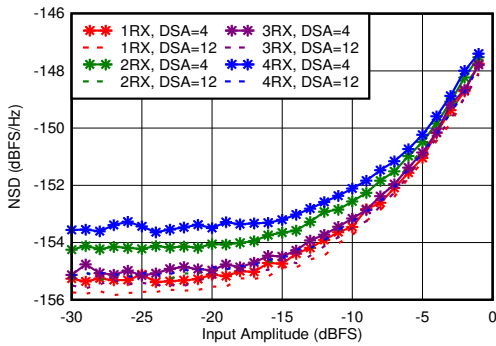


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

图 6-361. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

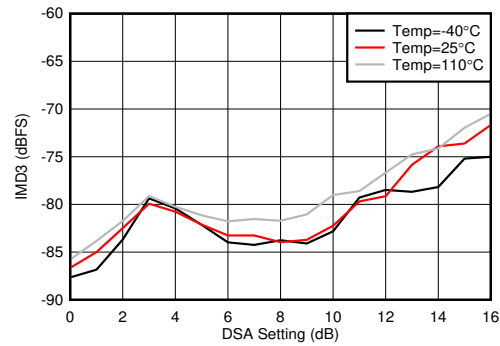
**6.12.10 RX Typical Characteristics at 2.6 GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



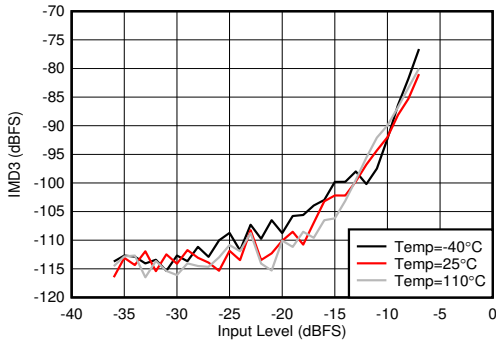
With 2.6 GHz matching, 12.5-MHz offset from tone

**图 6-362. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz**



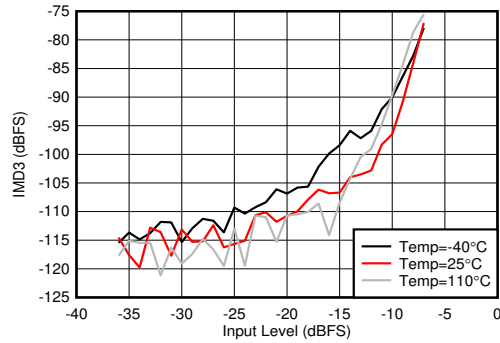
With 2.6 GHz matching, each tone -7 dBFS, tone spacing = 20 MHz

**图 6-363. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz**



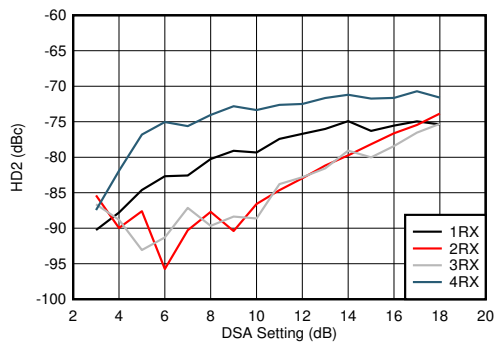
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**图 6-364. RX IMD3 vs Input Level and Temperature at 2.6 GHz**



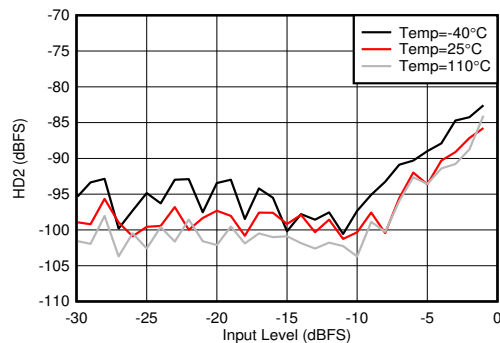
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**图 6-365. RX IMD3 vs Input Level and Temperature at 2.6 GHz**



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**图 6-366. RX HD2 vs DSA Setting and Channel at 2.6 GHz**

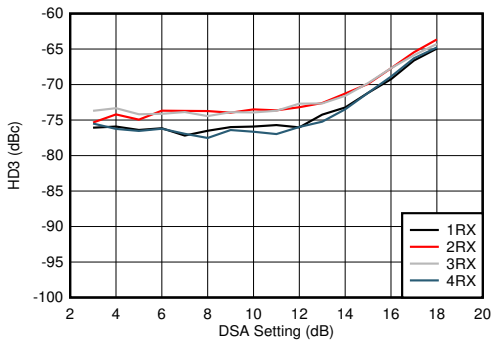


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**图 6-367. RX HD2 vs Input Level and Temperature at 2.6 GHz**

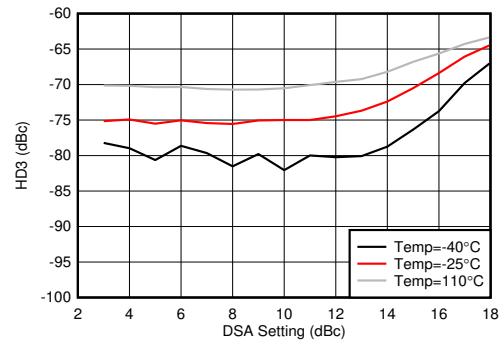
### 6.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



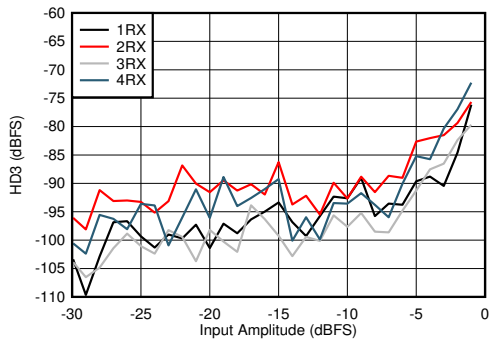
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-368. RX HD3 vs DSA Setting and Channel at 2.6 GHz



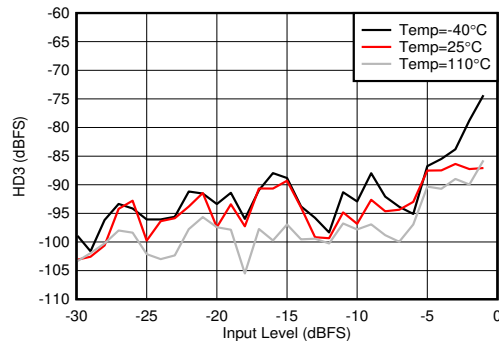
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-369. RX HD3 vs DSA Setting and Temperature at 2.6 GHz



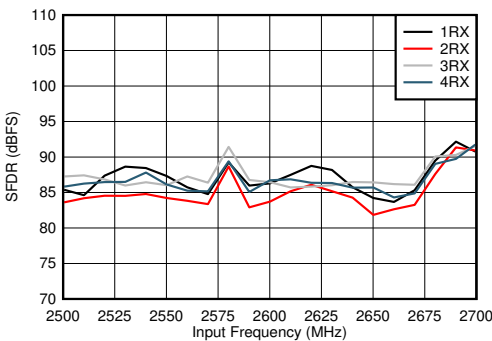
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-370. RX HD3 vs Input Level and Channel at 2.6 GHz



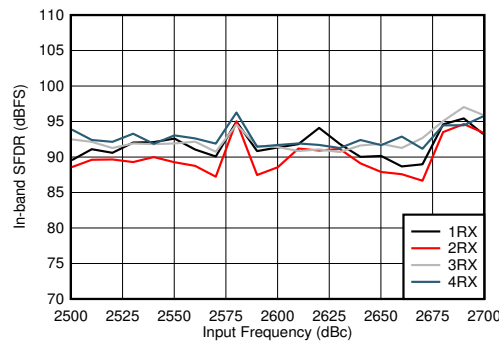
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-371. RX HD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching

图 6-372. RX In-Band SFDR ( $\pm 200\text{ MHz}$ ) vs Frequency With  $A_{IN} = -1\text{ dBFS}$  at 2.6 GHz

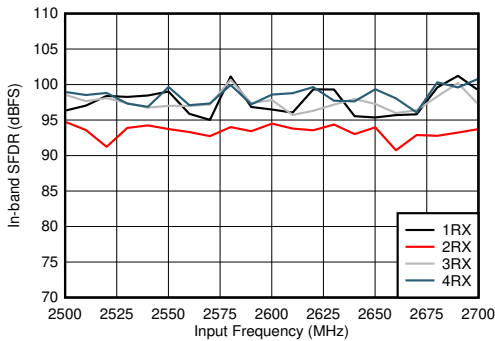


With 2.6 GHz matching

图 6-373. RX In-Band SFDR ( $\pm 200\text{ MHz}$ ) vs Frequency With  $A_{IN} = -6\text{ dBFS}$  at 2.6 GHz

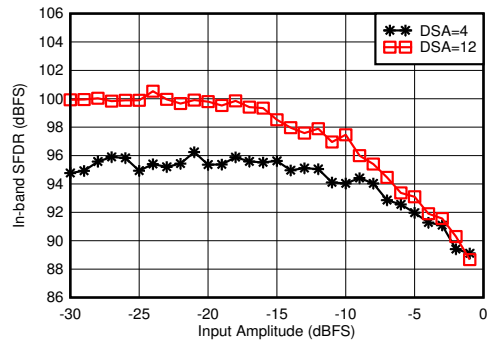
**6.12.10 RX Typical Characteristics at 2.6 GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



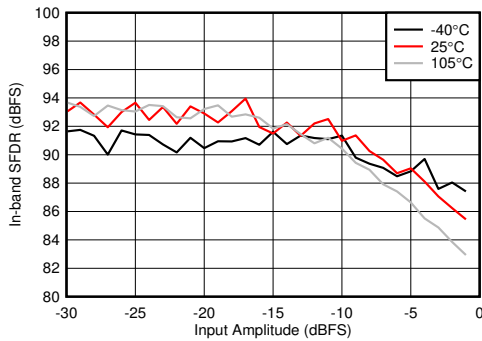
With 2.6 GHz matching

**图 6-374. RX In-Band SFDR ( $\pm 200\text{ MHz}$ ) vs Frequency With  $A_{IN} = -12\text{ dBFS}$  at 2.6 GHz**



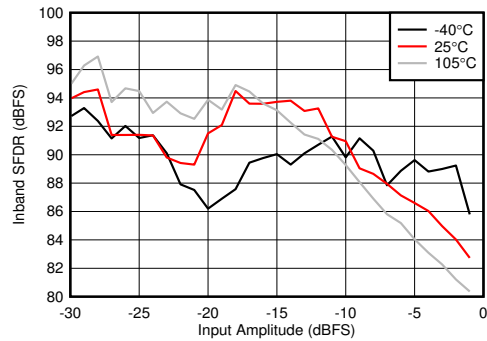
With 2.6 GHz matching

**图 6-375. RX In-Band SFDR ( $\pm 200\text{ MHz}$ ) vs Input Amplitude at 2.6 GHz**



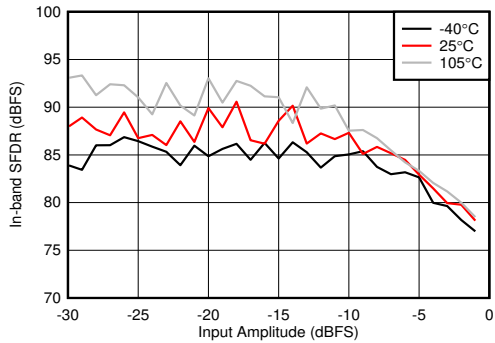
With 2.6 GHz matching

**图 6-376. RX In-Band SFDR ( $\pm 200\text{ MHz}$ ) vs Input Amplitude and Temperature at 2.6 GHz**



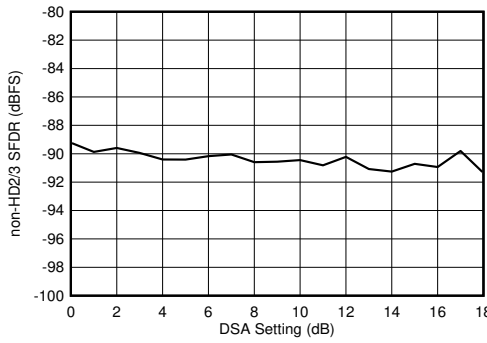
With 2.6 GHz matching, decimate by 8, DSA Setting = 12 dB

**图 6-377. RX Inband SFDR ( $\pm 150\text{ MHz}$ ) vs Input Amplitude and Temperature at 2.6 GHz**



With 2.6 GHz matching, decimate by 4

**图 6-378. RX In-Band SFDR ( $\pm 300\text{ MHz}$ ) vs Input Amplitude and Temperature at 2.6 GHz**

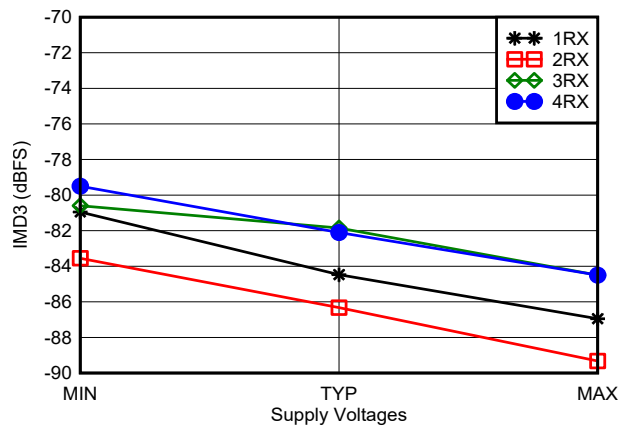


With 2.6 GHz matching

**图 6-379. RX Non-HD2/3 vs DSA Setting at 2.6 GHz**

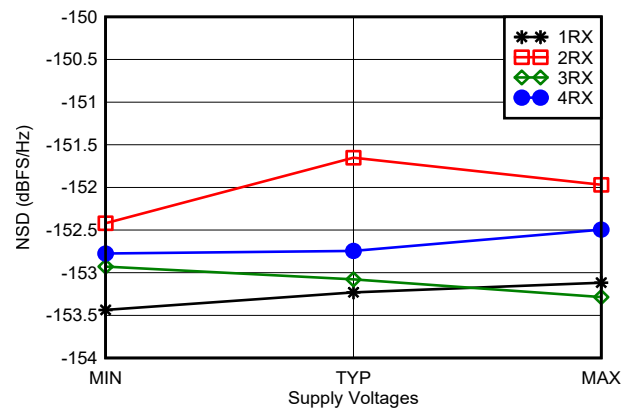
### 6.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 2.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-380. RX IMD3 vs Supply and Channel at 2.6 GHz

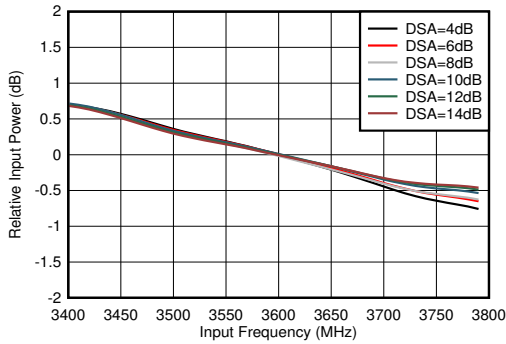


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-381. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

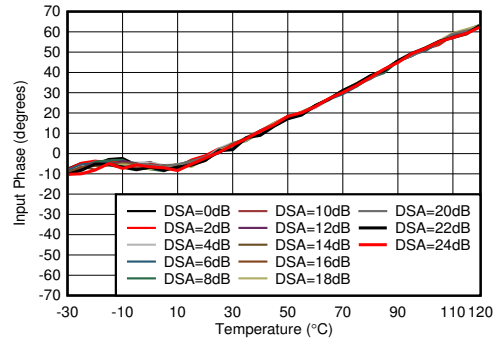
### 6.12.11 RX Typical Characteristics at 3.5 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



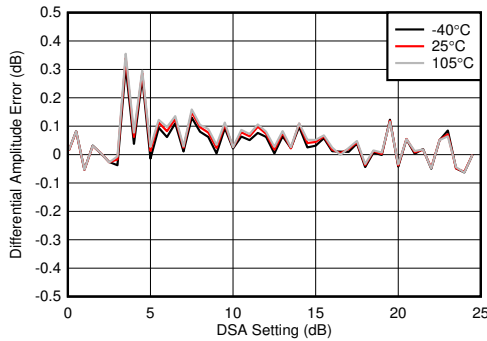
With 3.6 GHz matching, normalized to 3.6 GHz

图 6-382. RX In-Band Gain Flatness,  $f_{IN} = 3600\text{ MHz}$



With 3.6 GHz matching, normalized to phase at 25°C

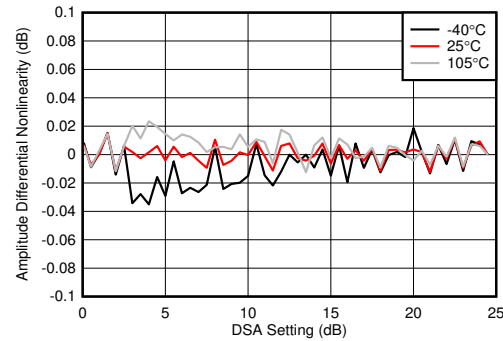
图 6-383. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

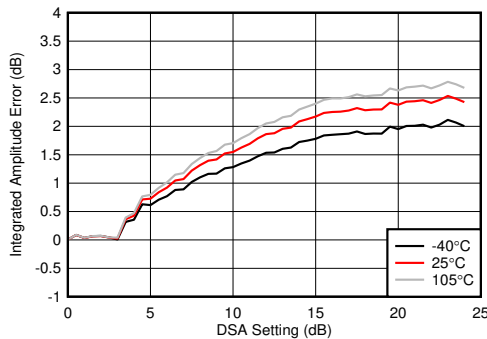
图 6-384. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

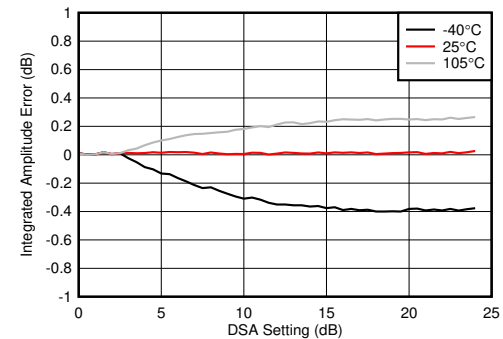
图 6-385. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-386. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

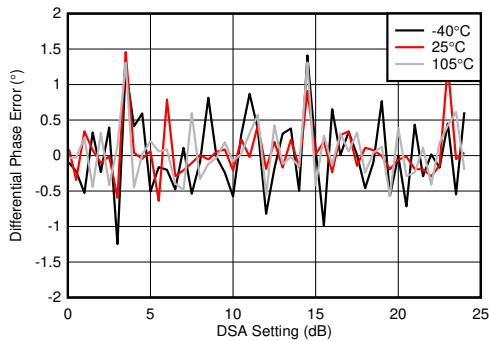
$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-387. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



### 6.12.11 RX Typical Characteristics at 3.5 GHz (continued)

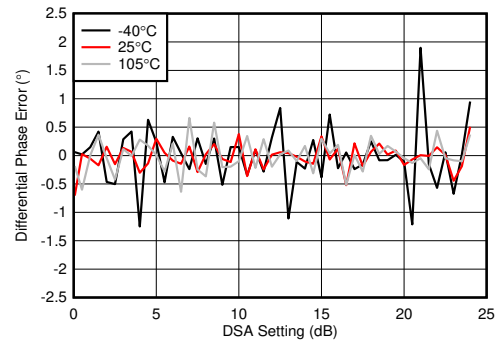
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

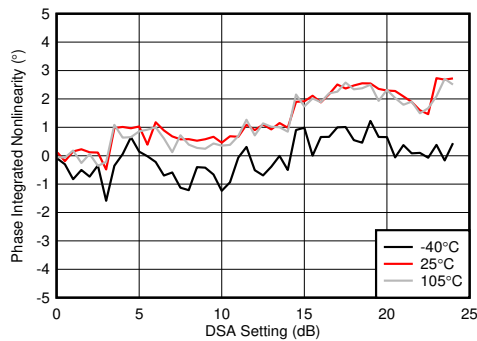
图 6-388. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

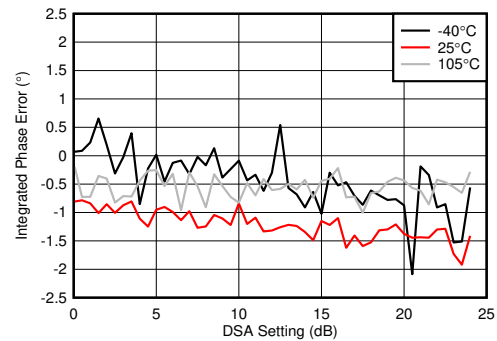
图 6-389. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

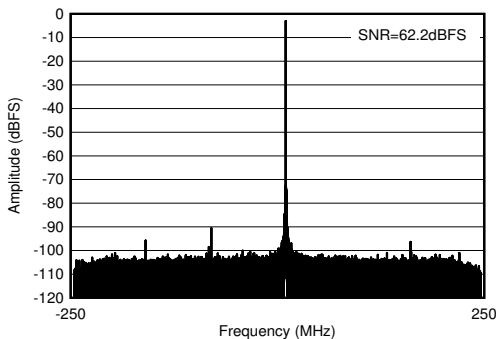
图 6-390. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

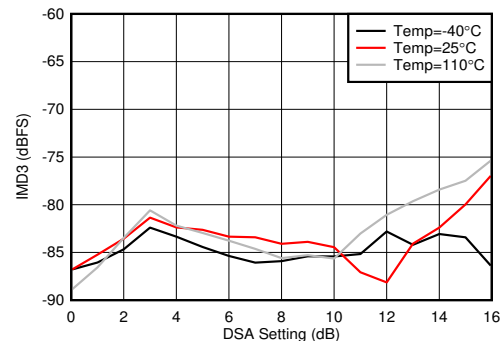
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

图 6-391. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching,  $f_{\text{IN}} = 3610 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$

图 6-392. RX Output FFT at 3.6 GHz

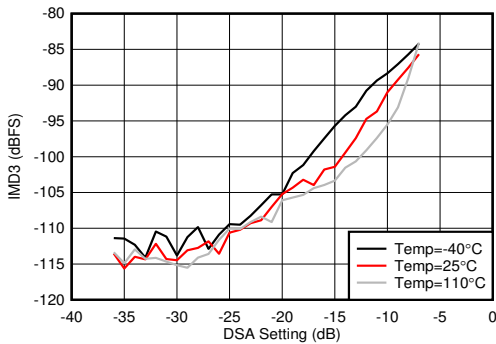


With 3.5 GHz matching, each tone at  $-7 \text{ dBFS}$ , 20-MHz tone spacing

图 6-393. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

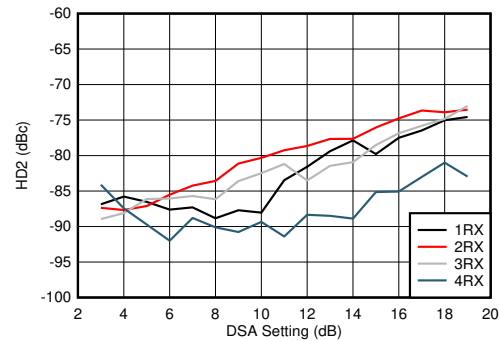
**6.12.11 RX Typical Characteristics at 3.5 GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



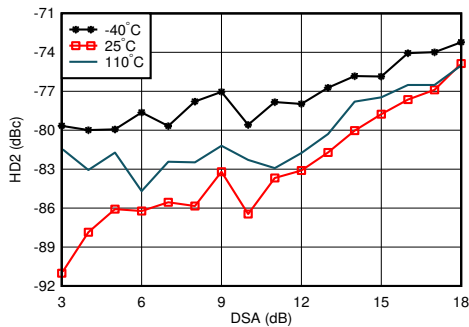
With 3.5 GHz matching, 20-MHz tone spacing

图 6-394. RX IMD3 vs Input Level and Temperature at 3.6 GHz



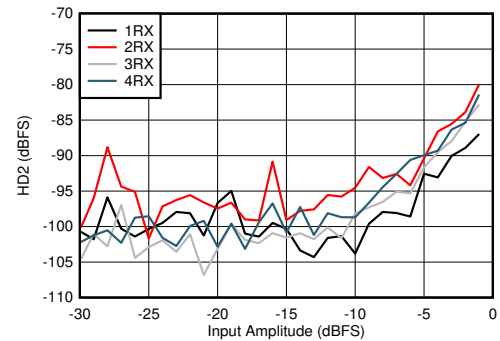
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-395. RX HD2 vs DSA Setting and Channel at 3.6 GHz



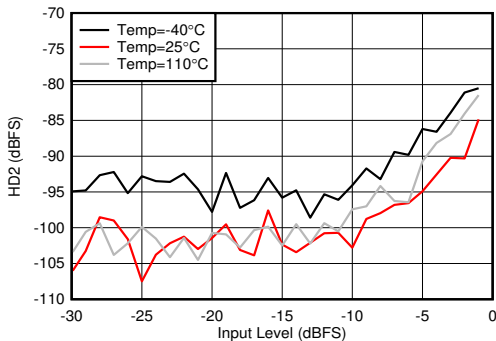
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-396. RX HD2 vs DSA Setting and Temperature at 3.6 GHz



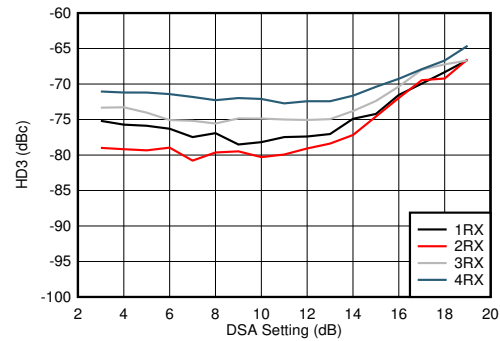
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-397. RX HD2 vs Input Level and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-398. RX HD2 vs Input Level and Temperature at 3.6 GHz

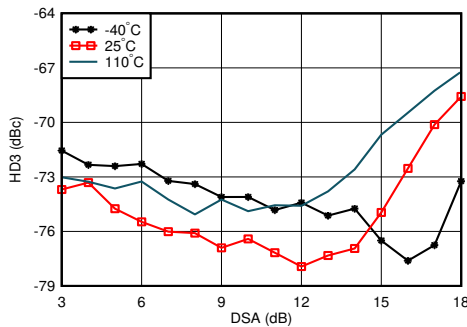


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-399. RX HD3 vs DSA Setting and Channel at 3.6 GHz

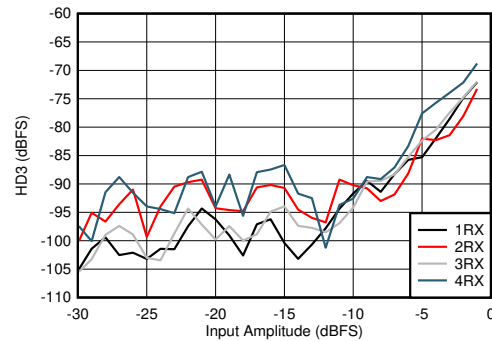
### 6.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



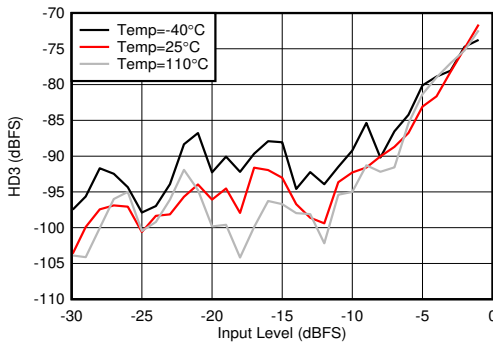
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-400. RX HD3 vs DSA Setting and Temperature at 3.6 GHz



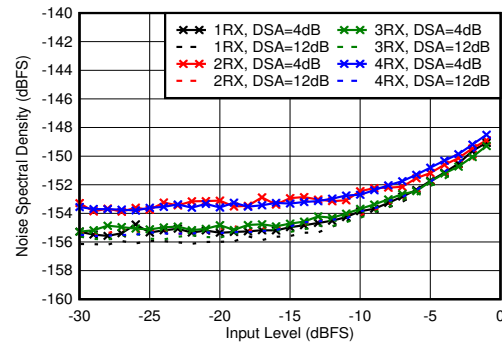
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-401. RX HD3 vs Input Level and Channel at 3.6 GHz



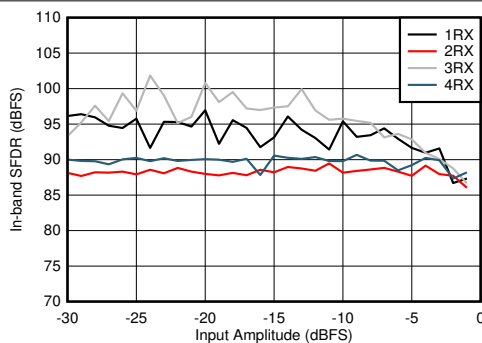
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-402. RX HD3 vs Input Level and Temperature at 3.6 GHz



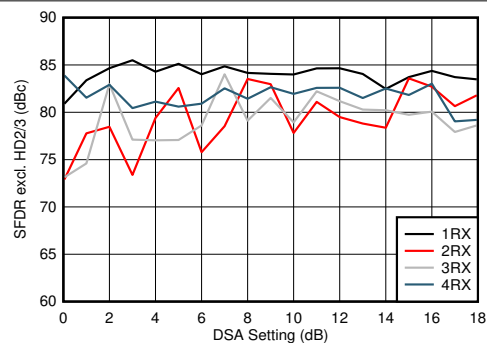
With 3.5 GHz matching, 12.5-MHz offset from tone

图 6-403. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



With 3.5 GHz matching

图 6-404. RX In-Band SFDR ( $\pm 200\text{ MHz}$ ) vs Input Level and Channel at 3.6 GHz

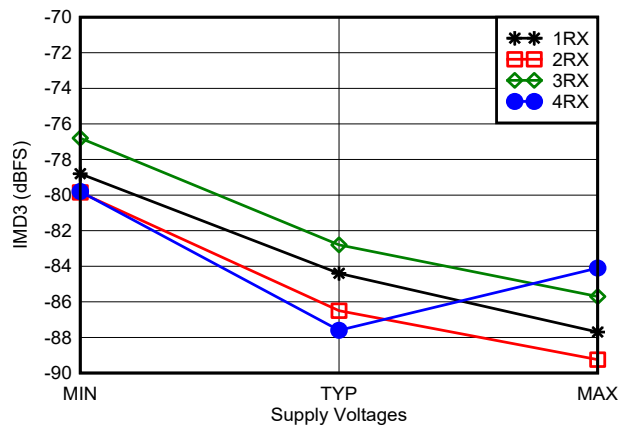


With 3.5 GHz matching

图 6-405. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz

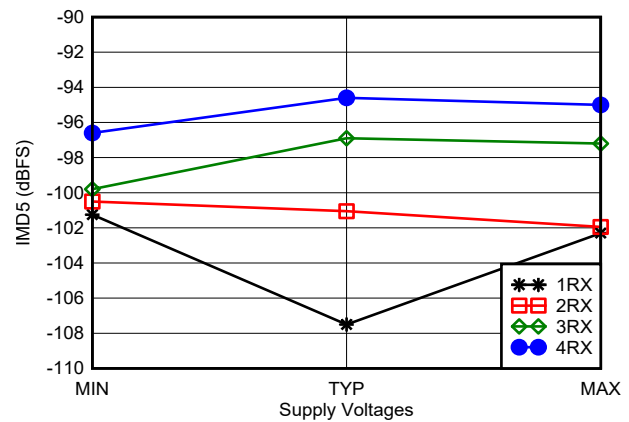
6.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



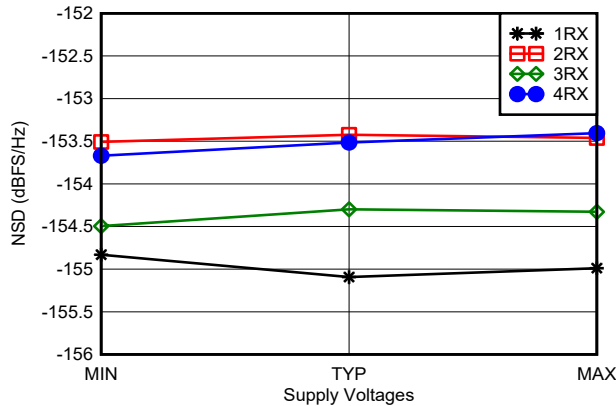
With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-406. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz



With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-407. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

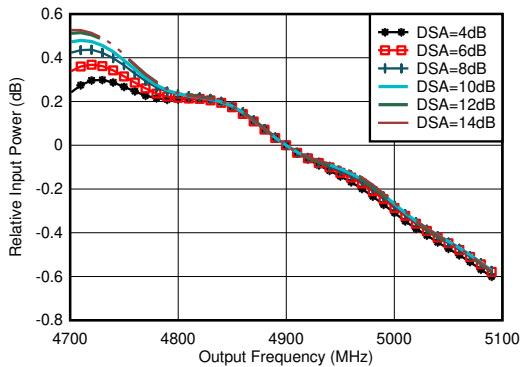


With 3.6 GHz matching, tone at -20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-408. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

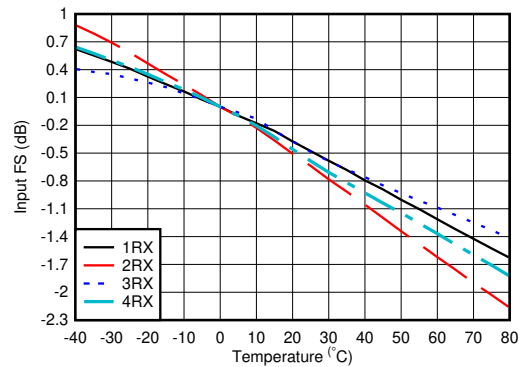
### 6.12.12 RX Typical Characteristics at 4.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



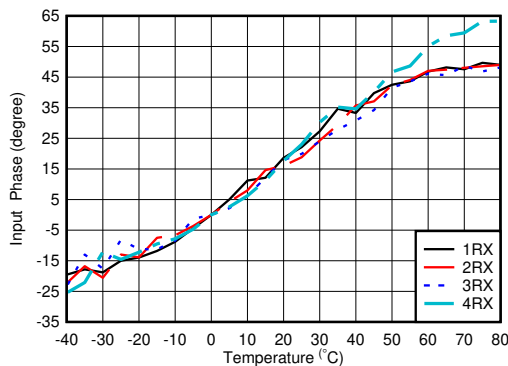
With matching, normalized to power at 4.9GHz for each DSA setting

图 6-409. RX Inband Gain Flatness,  $f_{IN} = 4900\text{ MHz}$



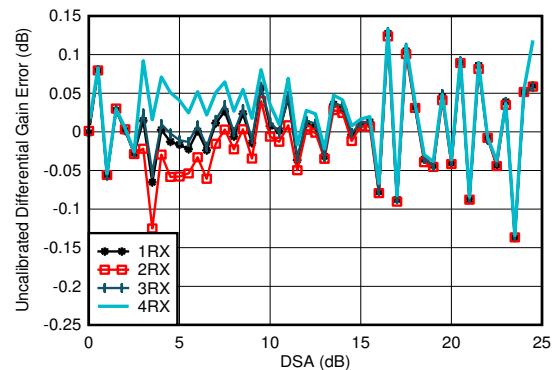
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

图 6-410. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

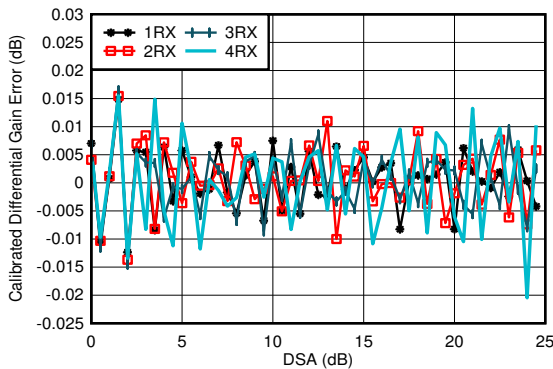
图 6-411. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 4.9\text{ GHz}$



With 4.9 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

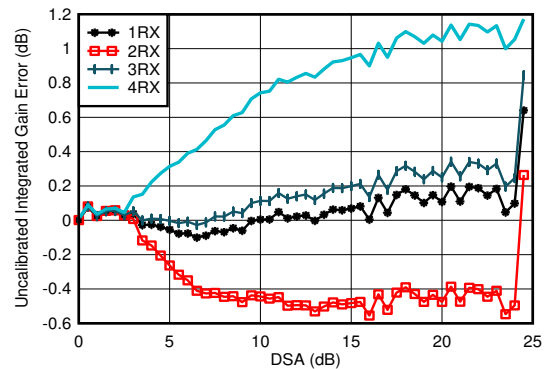
图 6-412. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

图 6-413. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



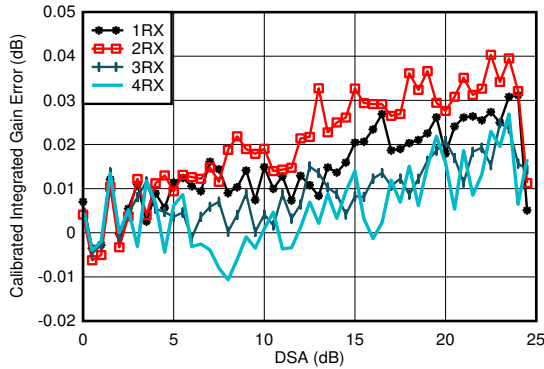
With 4.9 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-414. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

### 6.12.12 RX Typical Characteristics at 4.9 GHz (continued)

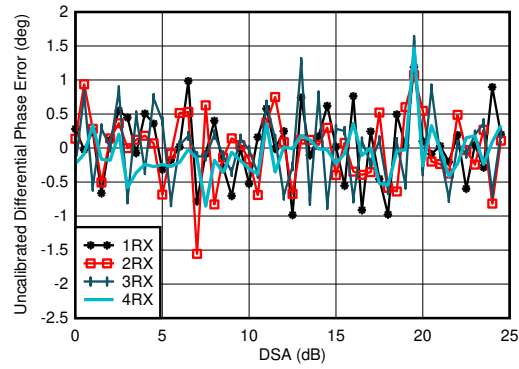
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 4.9 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

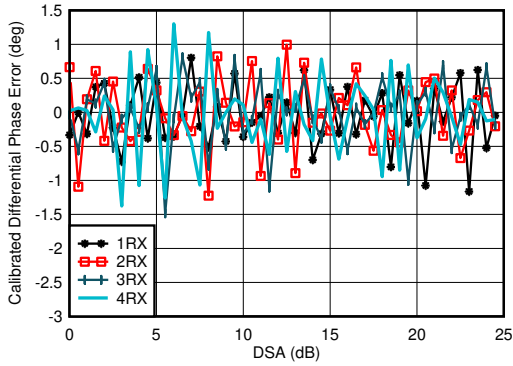
图 6-415. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$$

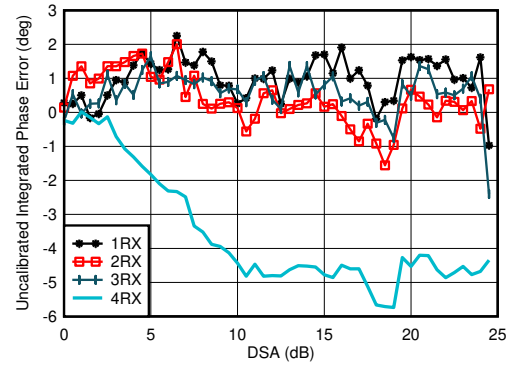
图 6-416. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$$

图 6-417. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



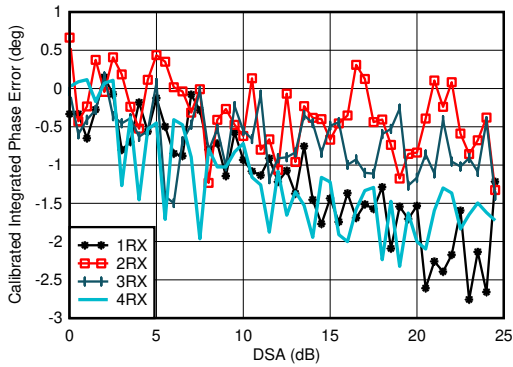
With 4.9 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

图 6-418. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

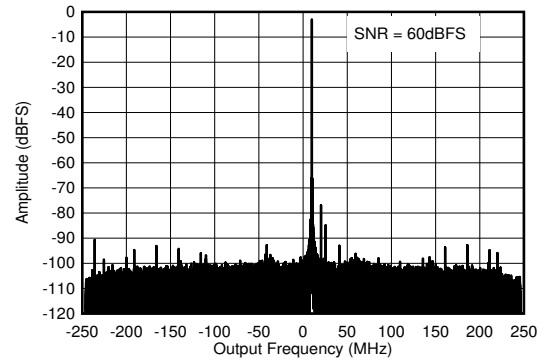
### 6.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



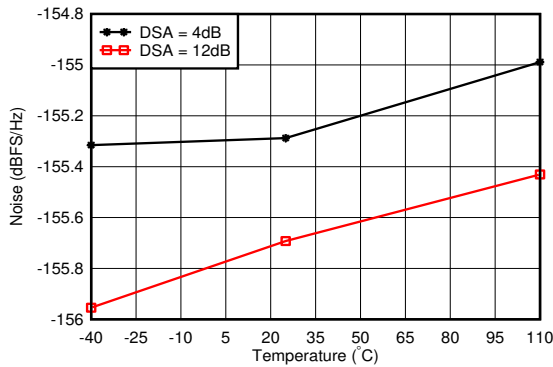
With 4.9 GHz matching  
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-419. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



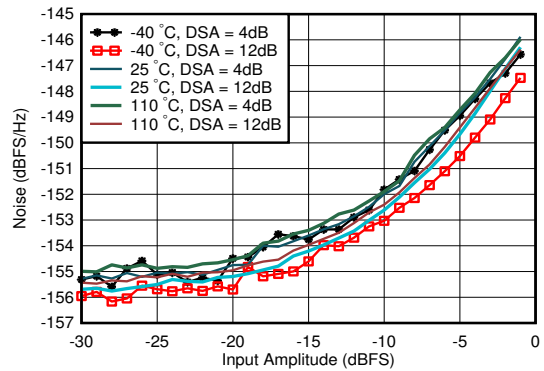
With 4.9 GHz matching,  $f_{\text{IN}} = 4910 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$

图 6-420. RX Output FFT at 4.9 GHz



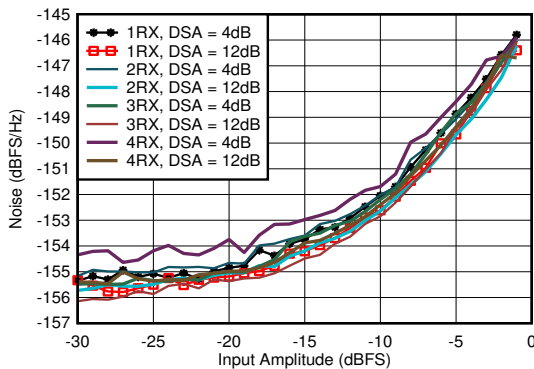
With 4.9 GHz matching, 12.5-MHz offset from tone

图 6-421. RX Noise Spectral Density vs Temperature at 4.9 GHz



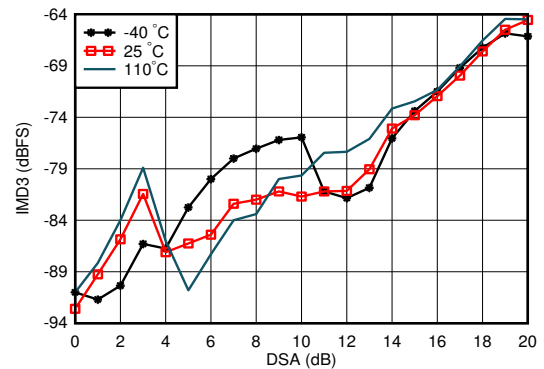
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

图 6-422. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



With 4.9 GHz matching, 12.5-MHz offset from tone

图 6-423. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz

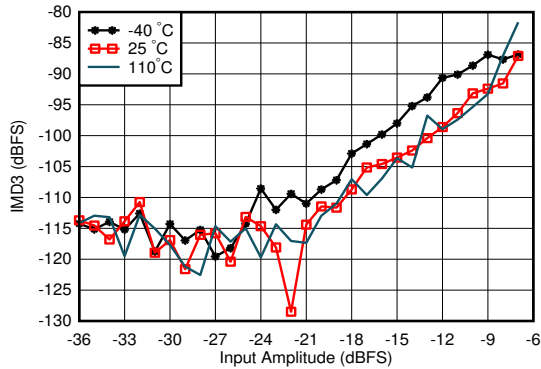


With 4.9 GHz matching, each tone  $-7 \text{ dBFS}$ , tone spacing = 20 MHz

图 6-424. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz

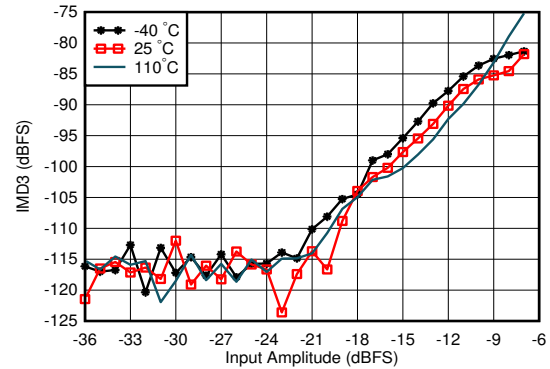
### 6.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



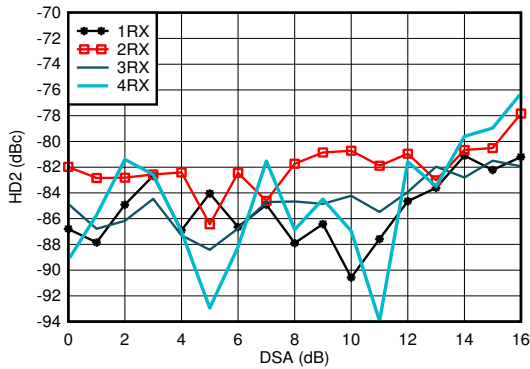
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

图 6-425. RX IMD3 vs Input Level and Temperature at 4.9 GHz



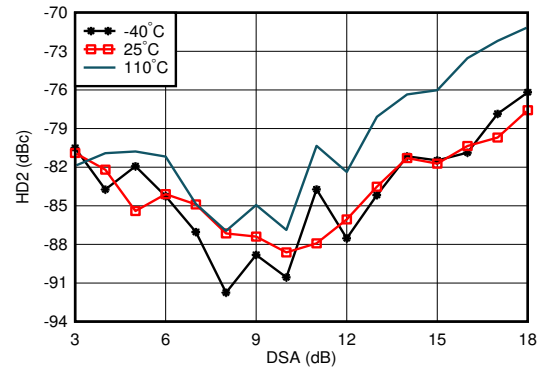
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

图 6-426. RX IMD3 vs Input Level and Temperature at 4.9 GHz



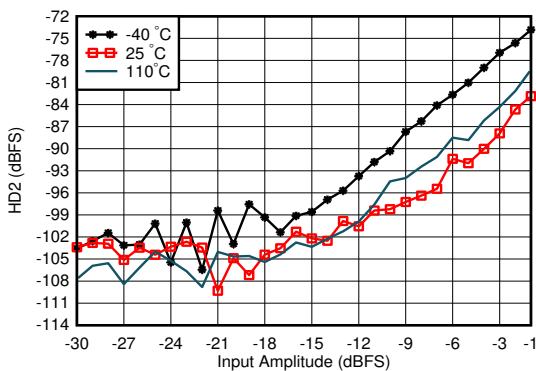
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-427. RX HD2 vs DSA Setting and Channel at 4.9 GHz



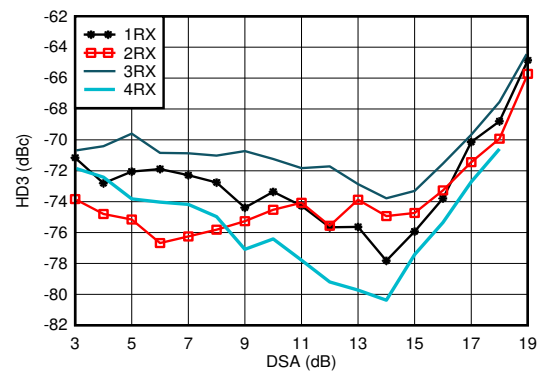
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-428. RX HD2 vs DSA and Temperature at 4.9 GHz



With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-429. RX HD2 vs Input Level and Temperature at 4.9 GHz



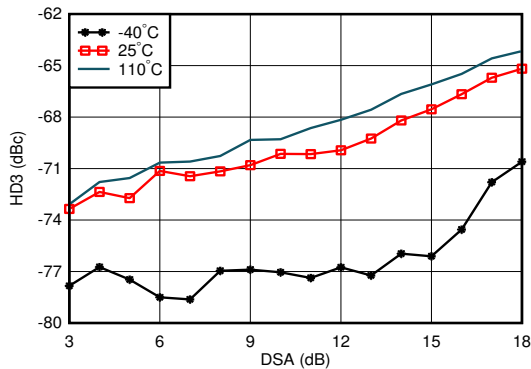
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-430. RX HD3 vs DSA Setting and Channel at 4.9 GHz



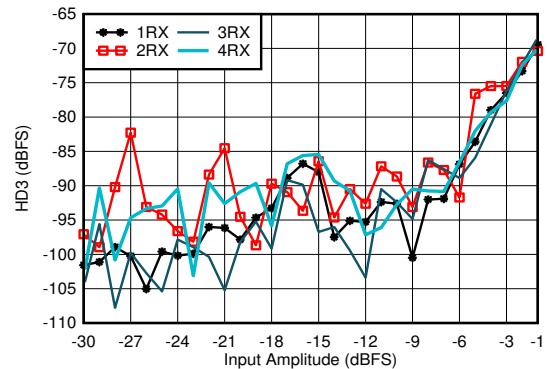
### 6.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



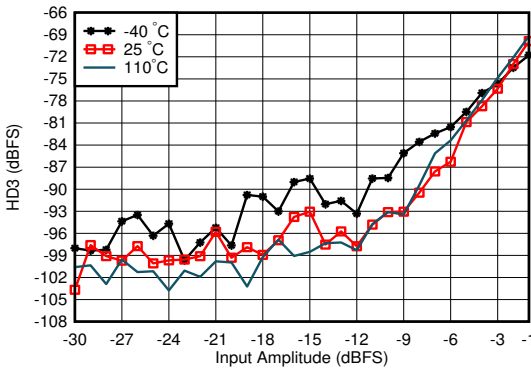
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-431. RX HD3 vs DSA Setting and Temperature at 4.9 GHz



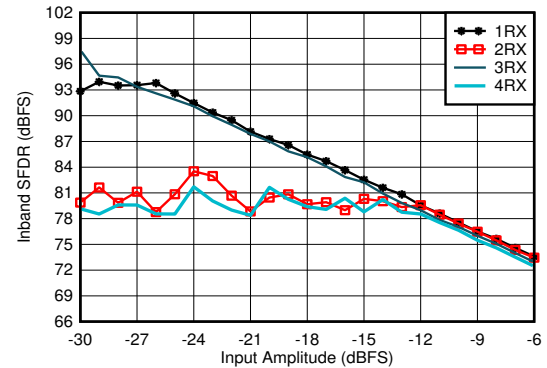
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-432. RX HD3 vs Input Level and Channel at 4.9 GHz



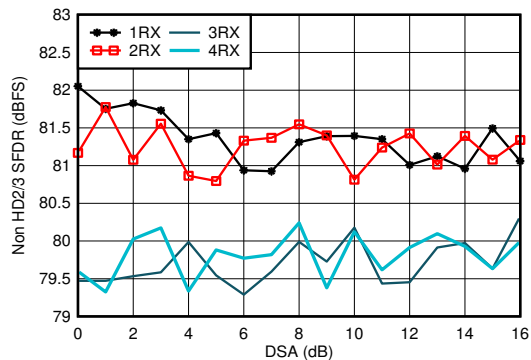
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-433. RX HD3 vs Input Level and Temperature at 4.9 GHz



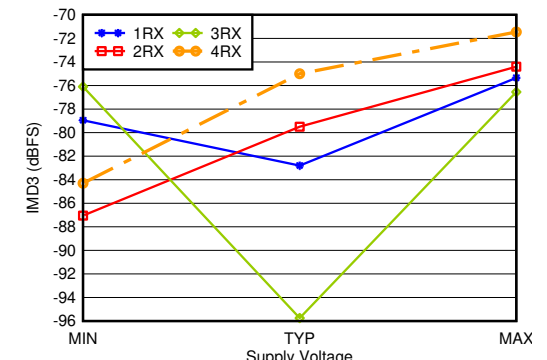
With 4.9 GHz matching, decimate by 3

图 6-434. RX In-Band SFDR ( $\pm 400 \text{ MHz}$ ) vs Input Amplitude and Channel at 4.9 GHz



With 4.9 GHz matching

图 6-435. RX Non-HD2/3 vs DSA Setting at 4.9 GHz

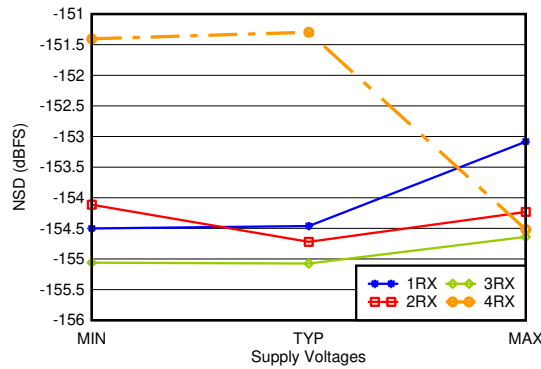


With 4.9 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-436. RX IMD3 vs Supply and Channel at 4.9 GHz

### 6.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.

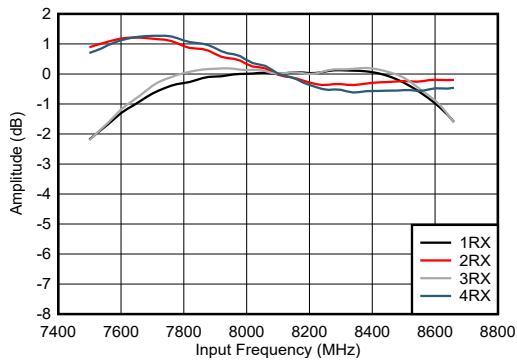


With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-437. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

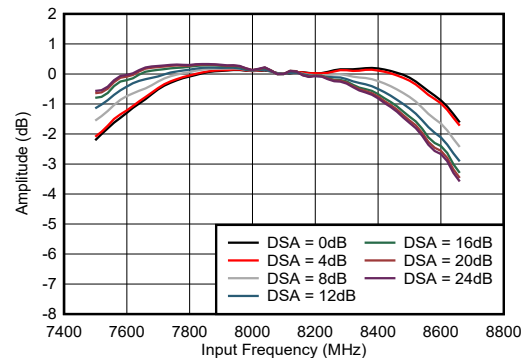
### 6.12.13 RX Typical Characteristics at 8.1GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{CLK} = 11796.48\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.



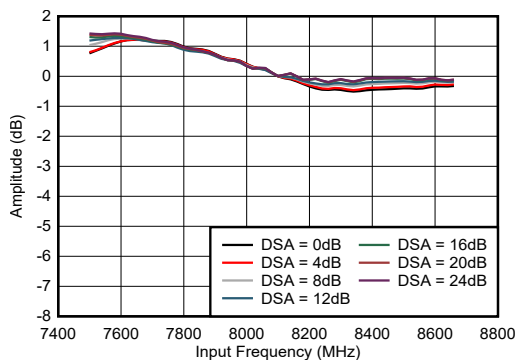
Normalized to 8.11GHz

图 6-438. RX Amplitude vs Frequency and Channel



1RX and 3RX, Normalized to 8.11GHz

图 6-439. RX Amplitude vs Frequency and DSA Setting



2RX and 4RX, Normalized to 8.11GHz

图 6-440. RX Amplitude vs Frequency and DSA Setting

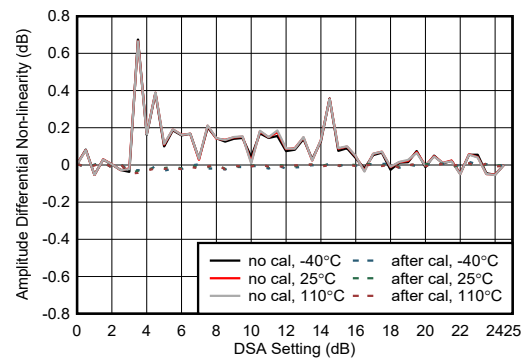


图 6-441. RX Amplitude Differential Nonlinearity at 8.11GHz

### 6.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

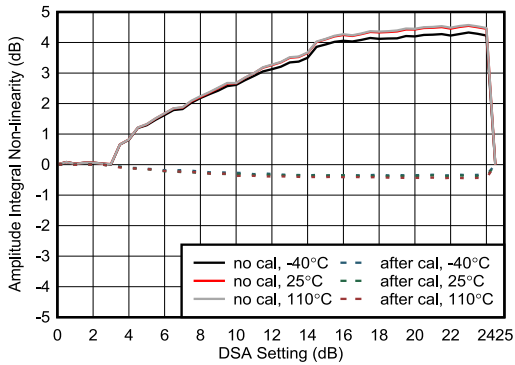


图 6-442. RX Amplitude Integrated Nonlinearity at 8.1GHz

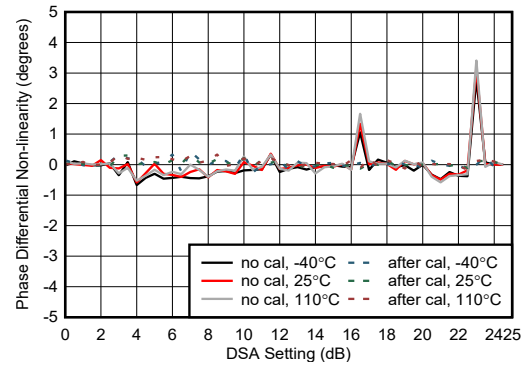


图 6-443. RX Phase Differential Nonlinearity at 8.1GHz

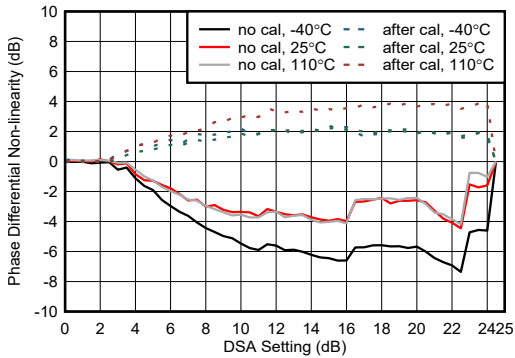


图 6-444. RX Phase Differential Nonlinearity at 8.1GHz

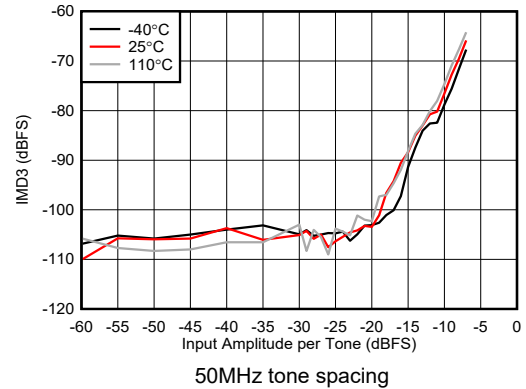


图 6-445. RX IMD3 vs Input Amplitude at 8.1GHz

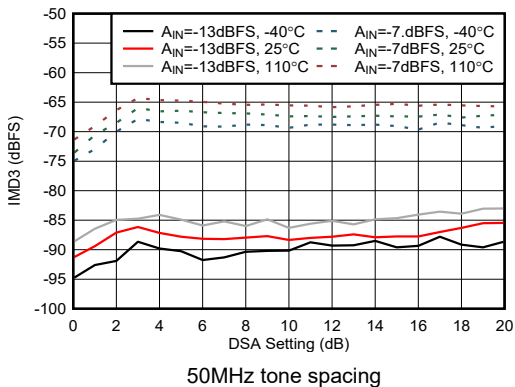


图 6-446. RX IMD3 vs DSA Setting at 8.1GHz

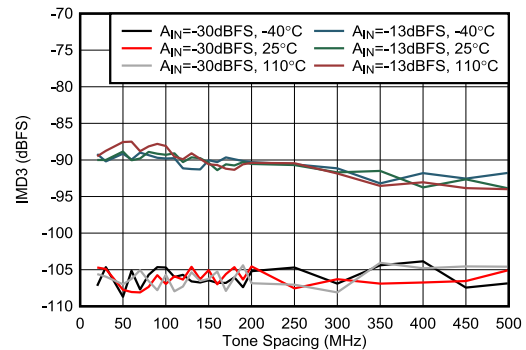


图 6-447. RX IMD3 vs Tone Spacing at 8.1GHz

**6.12.13 RX Typical Characteristics at 8.1GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

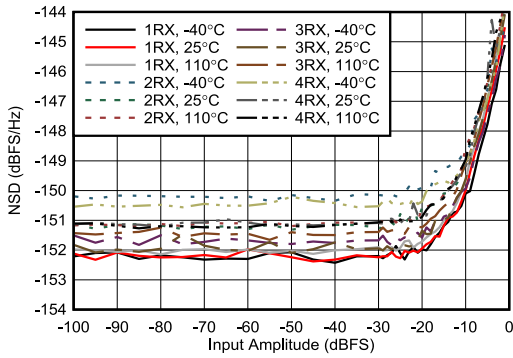


图 6-448. RX NSD vs Digital Amplitude at 8.1GHz

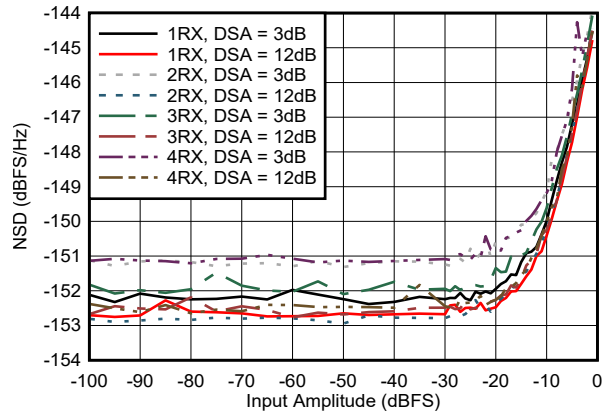


图 6-449. RX NSD vs Digital Amplitude at 8.1GHz

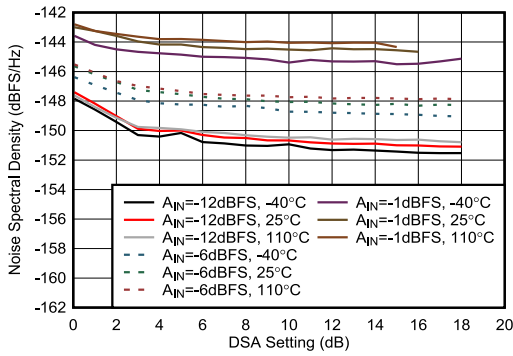


图 6-450. RX NSD vs DSA Setting at 8.1GHz

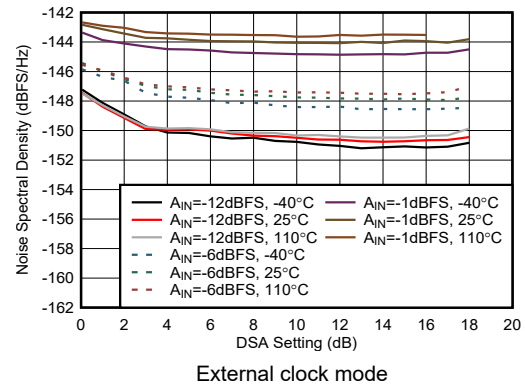


图 6-451. RX NSD vs DSA Setting at 8.1GHz

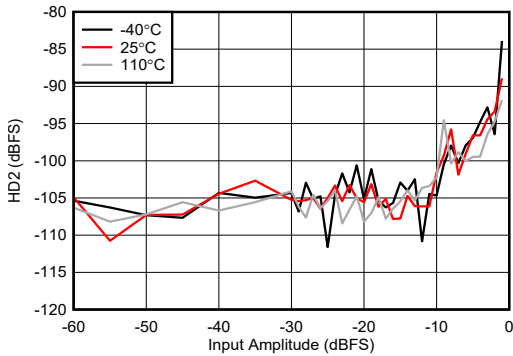


图 6-452. RX HD2 vs Digital Amplitude at 8.1GHz

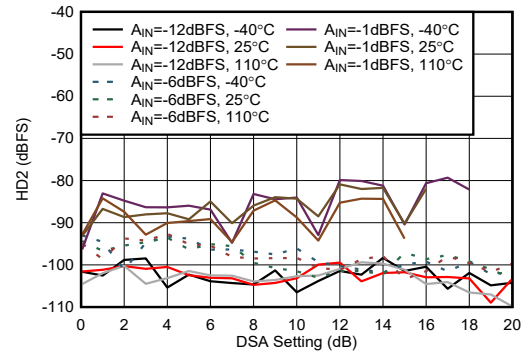


图 6-453. RX HD2 vs DSA Setting at 8.1GHz

### 6.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

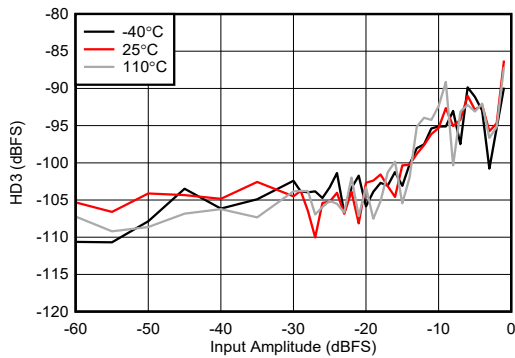


图 6-454. RX HD3 vs Digital Amplitude at 8.1GHz

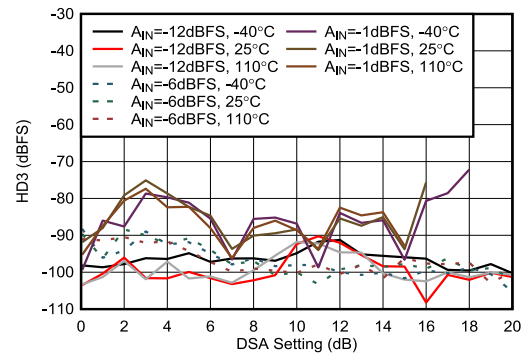


图 6-455. RX HD3 vs DSA Setting at 8.1GHz

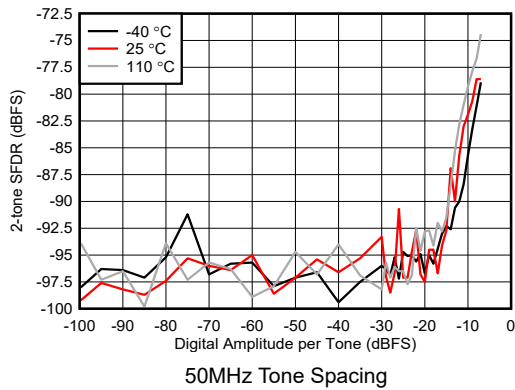


图 6-456. RX 2-tone SFDR vs Digital Amplitude at 8.1GHz

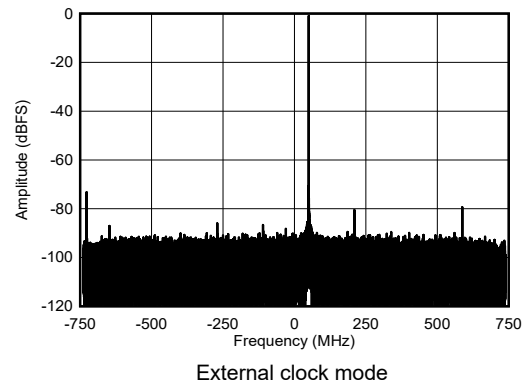


图 6-457. RX Single Tone Output FFT at 8.1GHz, -1dBFS

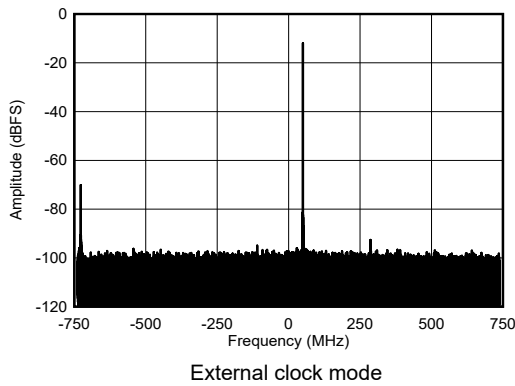


图 6-458. RX Single Tone Output FFT at 8.1GHz, -12dBFS

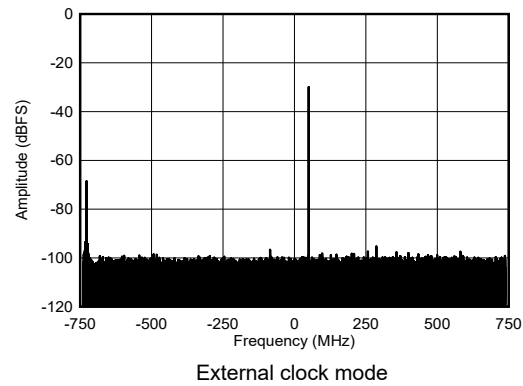


图 6-459. RX Single Tone Output FFT at 8.1GHz, -30dBFS

**6.12.13 RX Typical Characteristics at 8.1GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

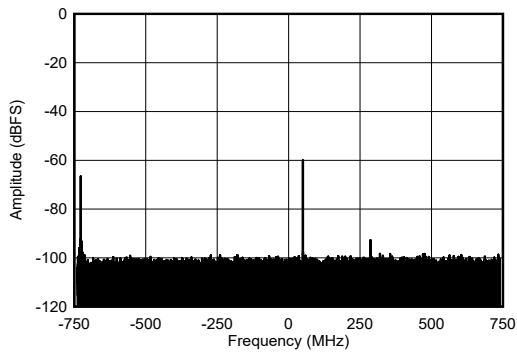


图 6-460. RX Single Tone Output FFT at 8.11GHz, -60dBFS

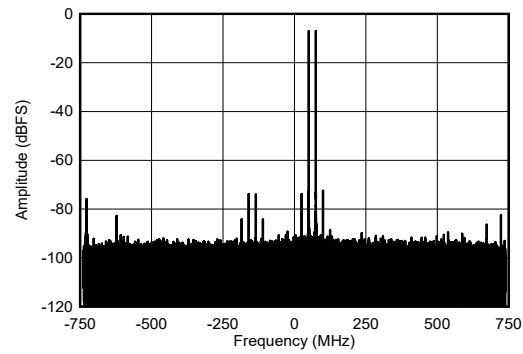


图 6-461. RX Dual Tone Output FFT at 8.11GHz

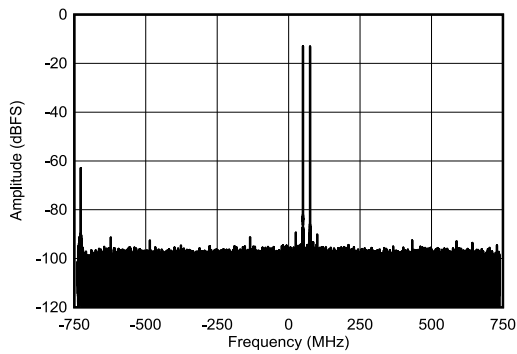


图 6-462. RX Dual Tone Output FFT at 8.11GHz

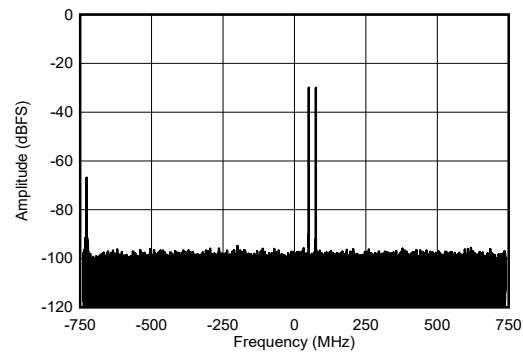


图 6-463. RX Dual Tone Output FFT at 8.11GHz

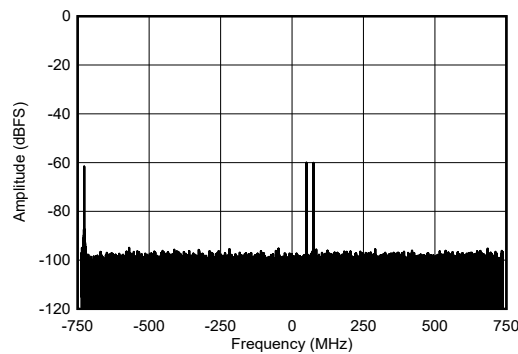


图 6-464. RX Dual Tone Output FFT at 8.11GHz

### 6.12.14 RX Typical Characteristics at 9.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

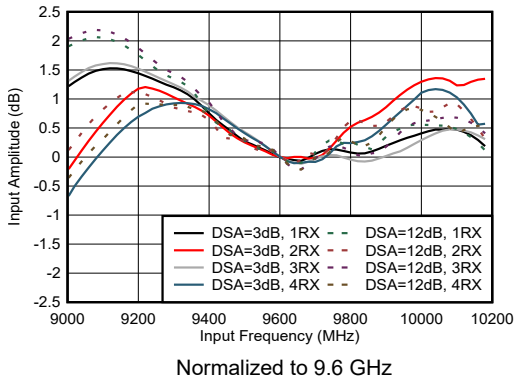


图 6-465. RX Input Amplitude vs Frequency

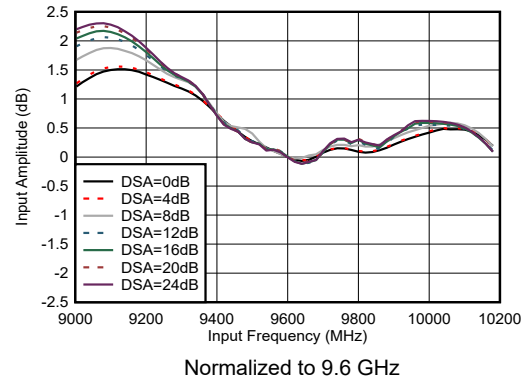


图 6-466. RX Input Amplitude vs Frequency at 9.6 GHz

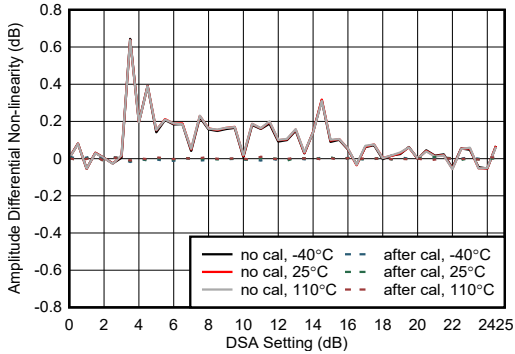


图 6-467. RX Amplitude Differential Non-Linearity at 9.6 GHz

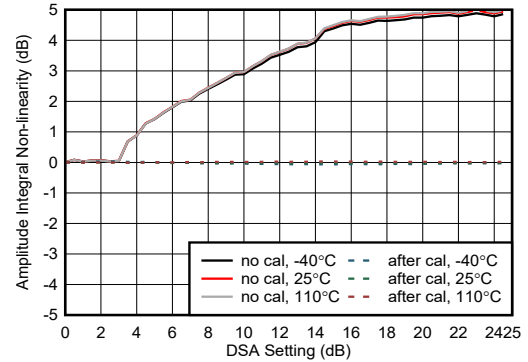


图 6-468. RX Amplitude Integrated Non-linearity at 9.6 GHz

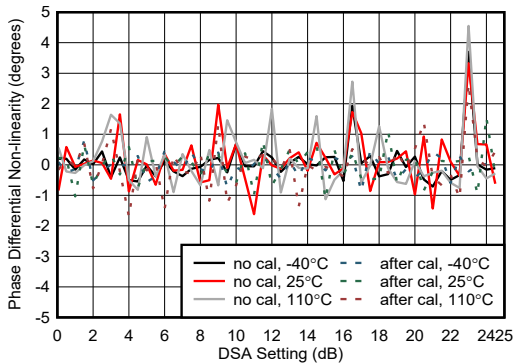


图 6-469. RX Phase Differential Non-linearity at 9.6 GHz

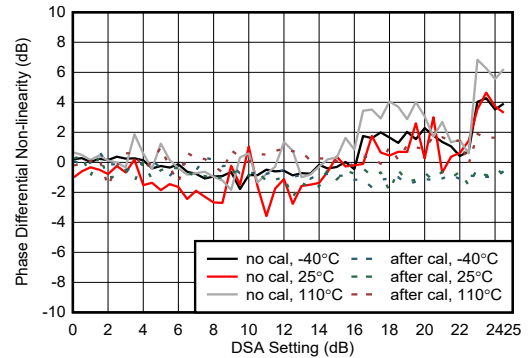


图 6-470. RX Phase Integrated Non-linearity at 9.6 GHz

**6.12.14 RX Typical Characteristics at 9.6 GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

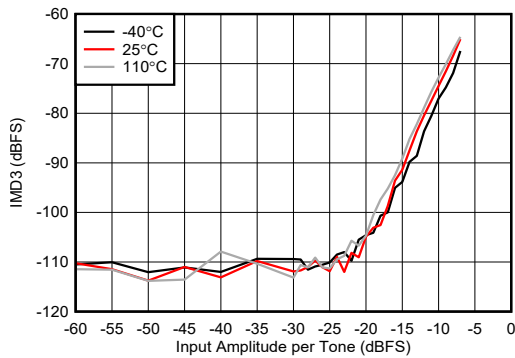


图 6-471. RX IMD3 vs Digital Amplitude at 9.6 GHz

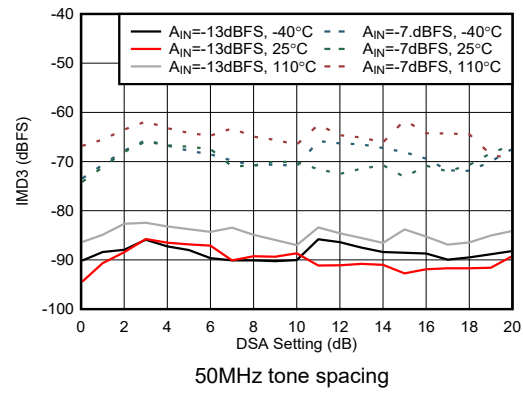


图 6-472. RX IMD3 vs DSA Setting at 9.6 GHz

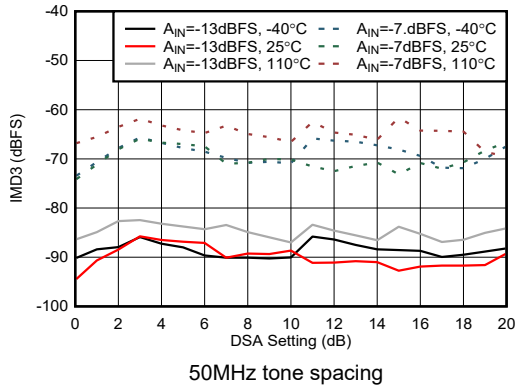


图 6-473. RX IMD3 vs DSA Setting at 9.6 GHz

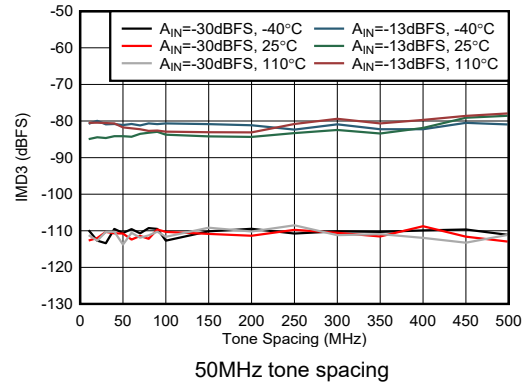


图 6-474. RX IMD3 vs Tone Spacing at 9.6 GHz

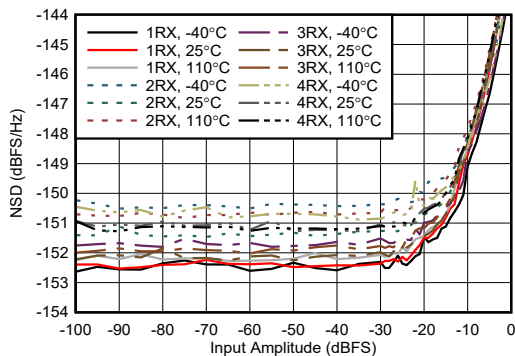


图 6-475. RX NSD vs Digital Amplitude at 9.6 GHz

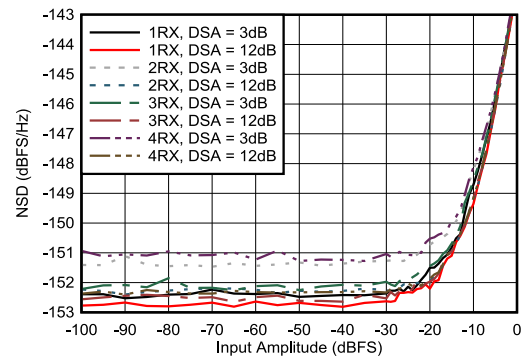


图 6-476. RX NSD vs Digital Amplitude at 9.6 GHz



### 6.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

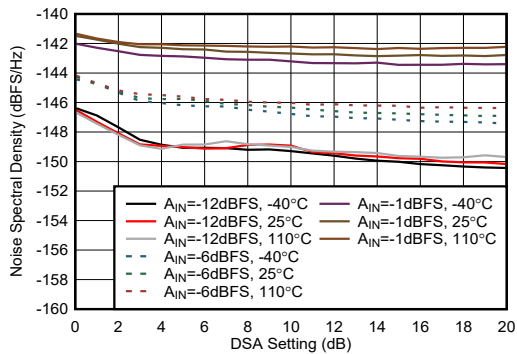


图 6-477. RX NSD vs DSA Setting at 9.6 GHz

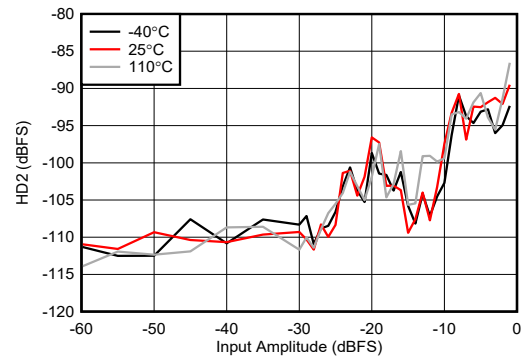


图 6-478. RX HD2 vs Digital Level at 9.6 GHz

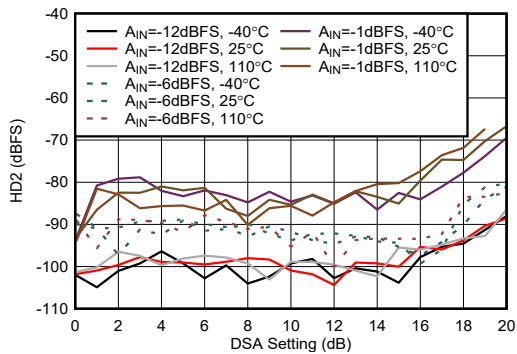


图 6-479. RX HD2 vs DSA Setting at 9.6 GHz

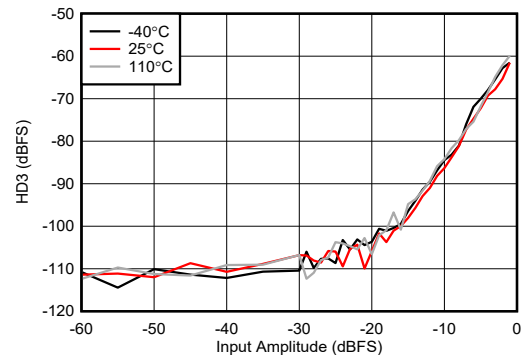


图 6-480. RX HD3 vs Digital Level at 9.6 GHz

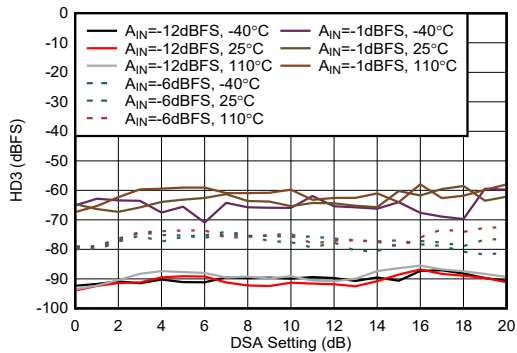
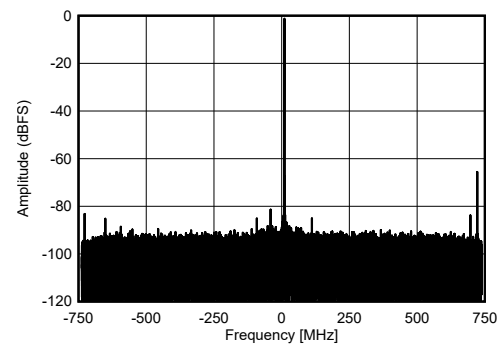


图 6-481. RX HD3 vs DSA Setting at 9.6 GHz

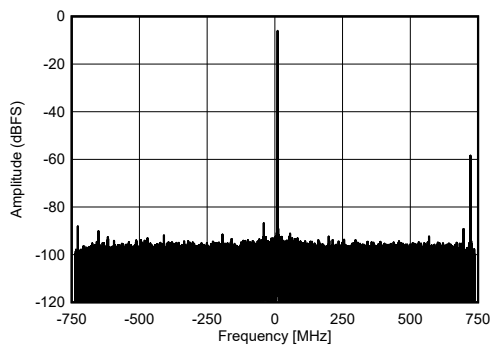


- 1 dBFS

图 6-482. RX Single Tone Output FFT at 9.61 GHz

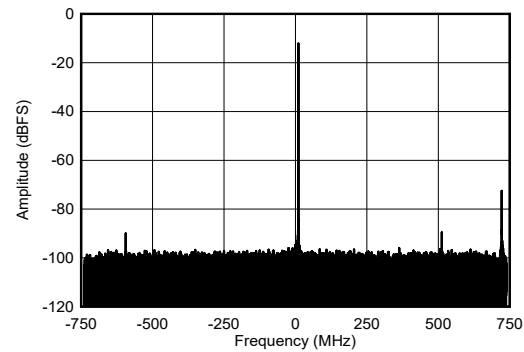
**6.12.14 RX Typical Characteristics at 9.6 GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.



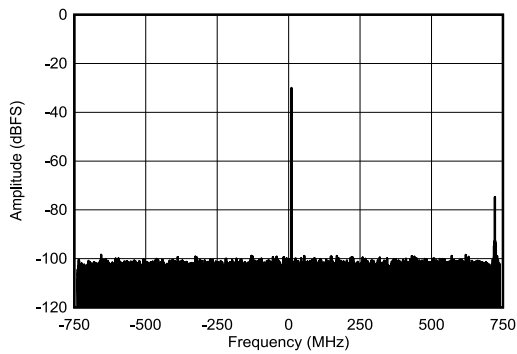
- 6 dBFS

图 6-483. RX Single Tone Output FFT at 9.61 GHz



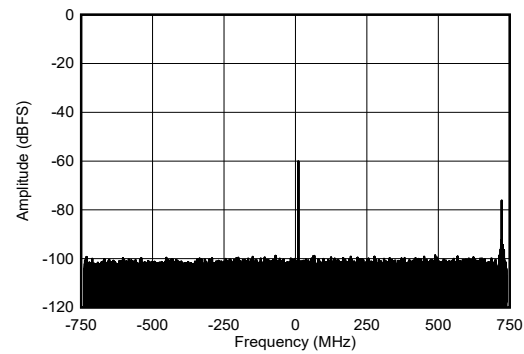
- 12 dBFS.

图 6-484. RX Single Tone Output FFT at 9.61 GHz



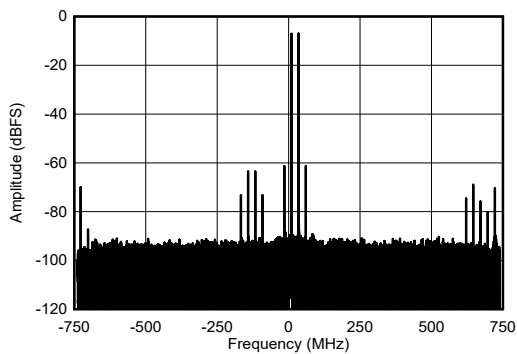
- 30 dBFS

图 6-485. RX Single Tone Output FFT at 9.61 GHz



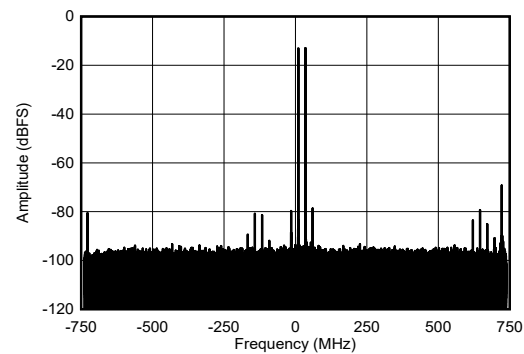
- 60 dBFS

图 6-486. RX Single Tone Output FFT at 9.61 GHz



9.61 GHz and 9.635 GHz, - 7 dBFS each tone

图 6-487. RX Two Tone Output FFT at 9.61 GHz

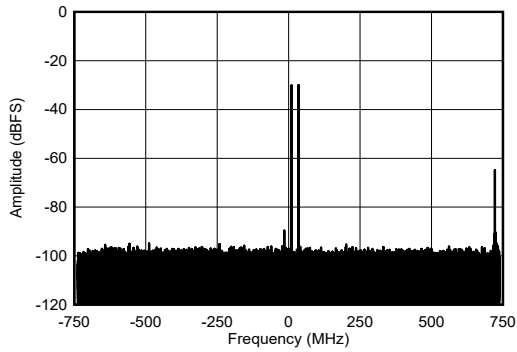


9.61 GHz and 9.635 GHz, - 13 dBFS each tone

图 6-488. RX Two Tone Output FFT at 9.61 GHz

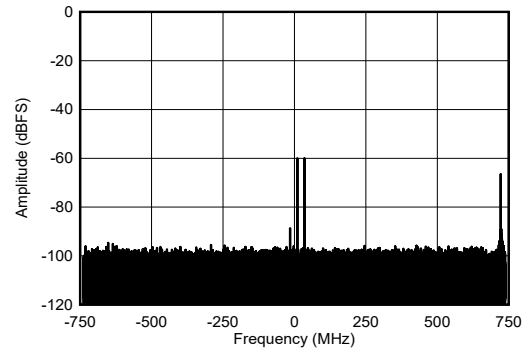
### 6.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.



9.61 GHz and 9.635 GHz, - 30 dBFS each tone

图 6-489. RX Two Tone Output FFT at 9.61 GHz

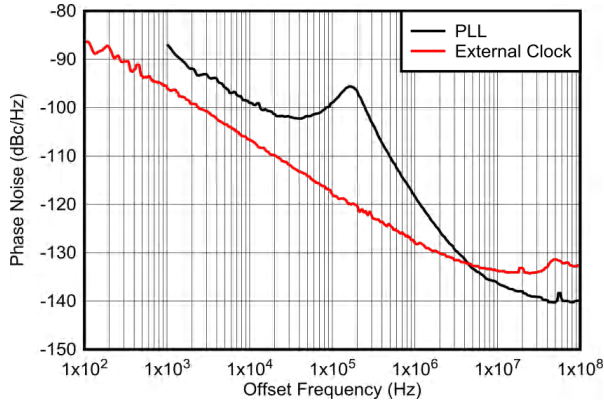


9.61 GHz and 9.635 GHz, - 60 dBFS each tone

图 6-490. RX Two Tone Output FFT at 9.61 GHz

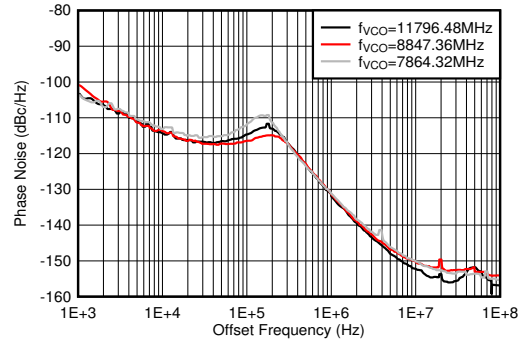
**6.12.15 PLL and Clock Typical Characteristics**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted,  $f_{REF} = 491.52\text{ MHz}$ , Phase noise measured at TX output



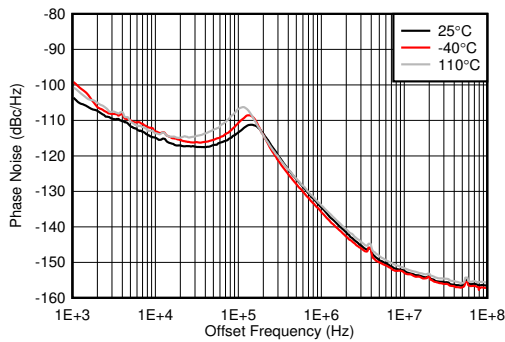
measured at TX output, normalized to 12GHz by  $20 \cdot \log_{10}(12\text{GHz}/F_{OUT})$

**图 6-491. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz**



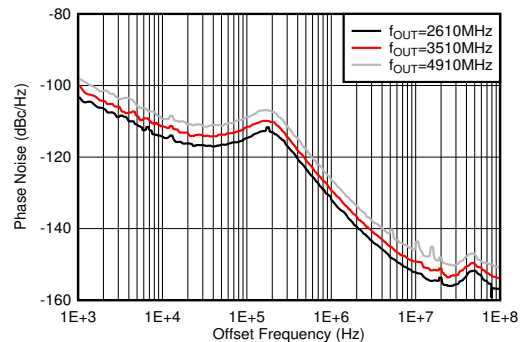
PLL enabled,  $f_{REF} = 491.52\text{MSPS}$ , measured at 2TXOUT

**图 6-492. Phase Noise vs Offset Frequency and  $f_{VCO}$  at  $f_{OUT} = 2610\text{ MHz}$**



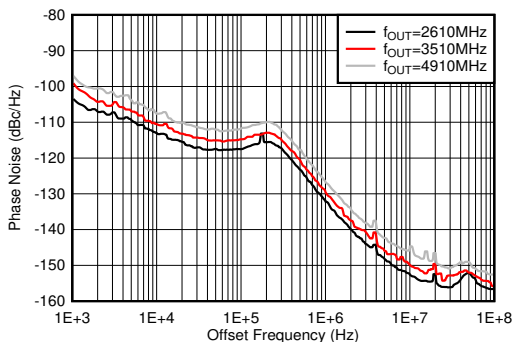
PLL enabled,  $f_{VCO} = 11796.48\text{ MHz}$ ,  $f_{REF} = 491.52\text{MSPS}$ , measured at 2TXOUT

**图 6-493. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910\text{ MHz}$**



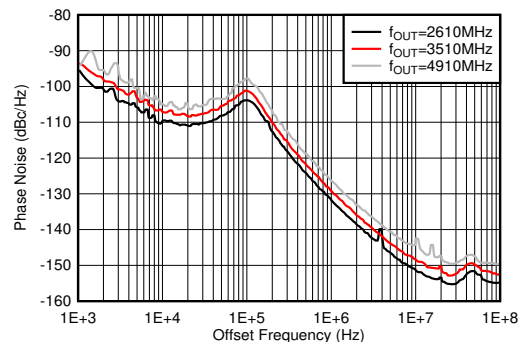
PLL enabled,  $f_{VCO} = 11796.48\text{ MHz}$ ,  $f_{REF} = 491.52\text{MSPS}$ , measured at 2TXOUT

**图 6-494. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $25^\circ\text{C}$**



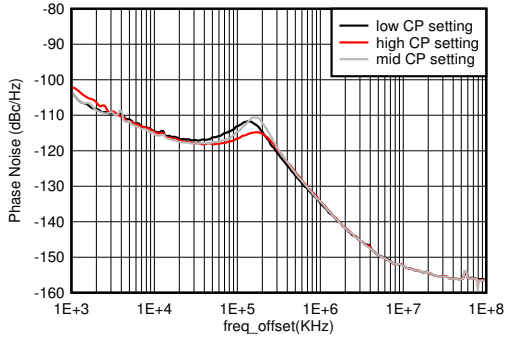
PLL enabled,  $f_{VCO} = 11796.48\text{ MHz}$ ,  $f_{REF} = 491.52\text{MSPS}$ , measured at 2TXOUT

**图 6-495. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $-40^\circ\text{C}$**



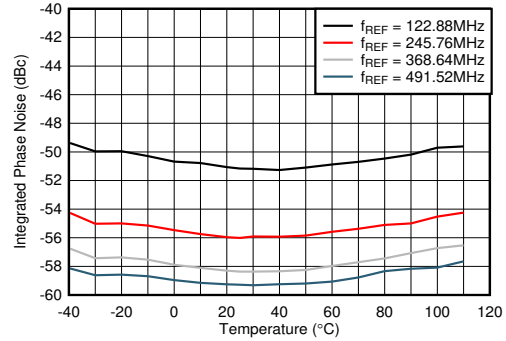
PLL enabled,  $f_{VCO} = 11796.48\text{ MHz}$ ,  $f_{REF} = 491.52\text{MSPS}$ , measured at 2TXOUT

**图 6-496. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $110^\circ\text{C}$**



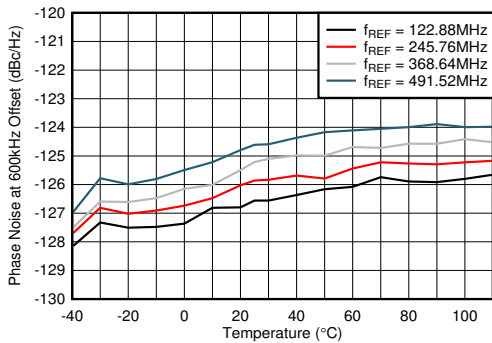
PLL enabled,  $f_{VCO} = 11796.48$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

图 6-497. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at  $f_{OUT} = 2.6$  GHz



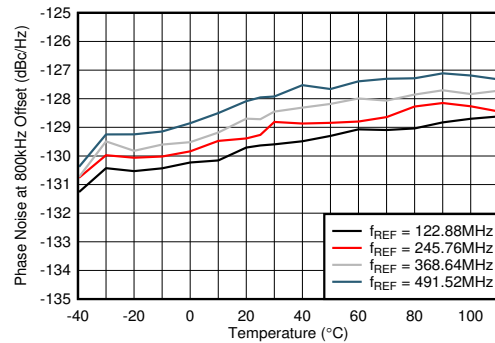
PLL enabled,  $f_{VCO} = 11796.48$  MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

图 6-498. Integrated Phase Noise for 12-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



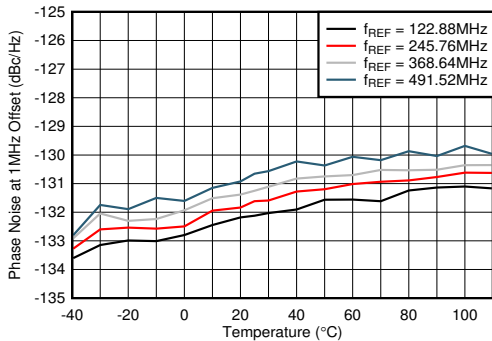
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

图 6-499. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



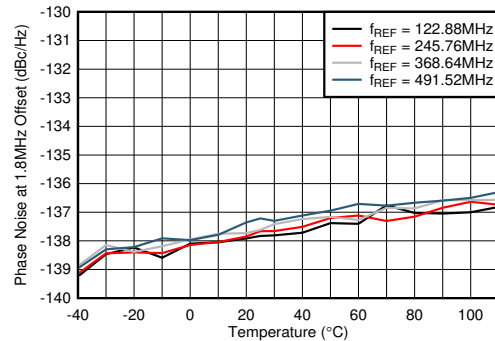
A. PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

图 6-500. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



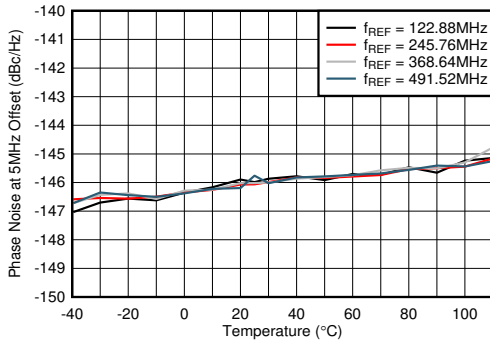
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

图 6-501. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



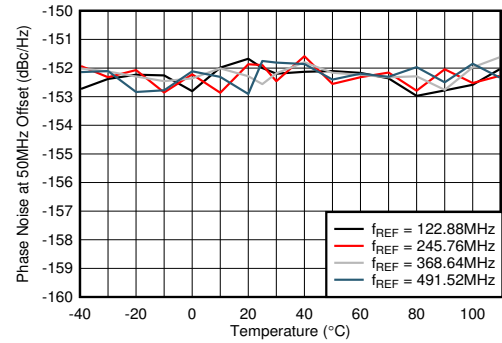
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

图 6-502. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



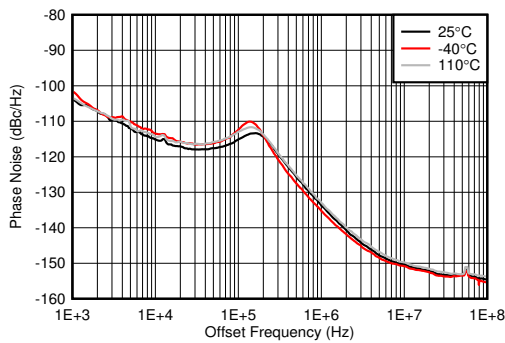
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**图 6-503. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



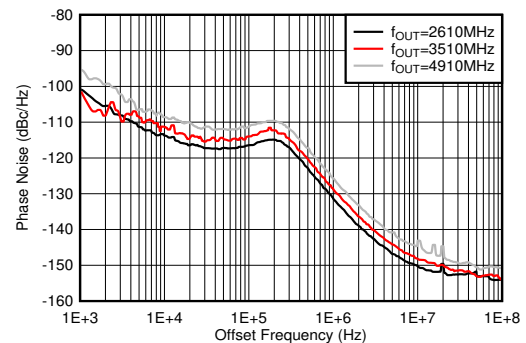
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**图 6-504. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



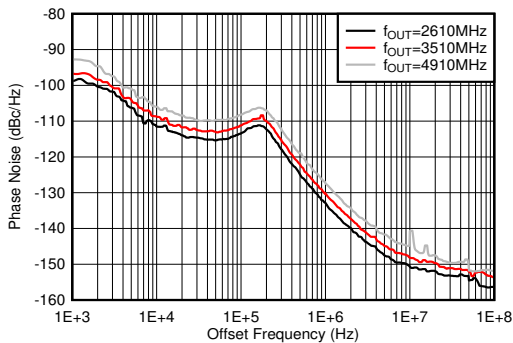
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-505. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**



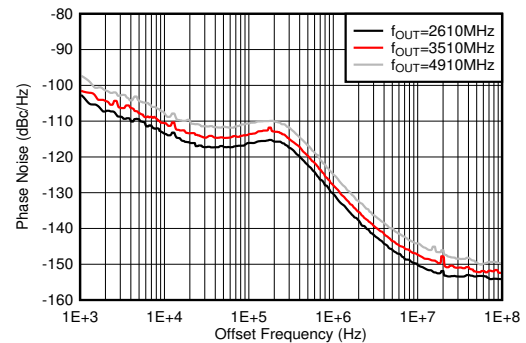
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-506. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 25°C**



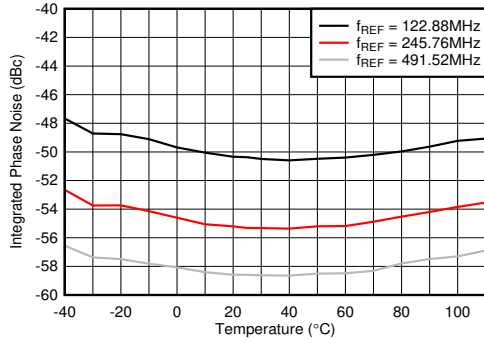
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-507. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at -40°C**



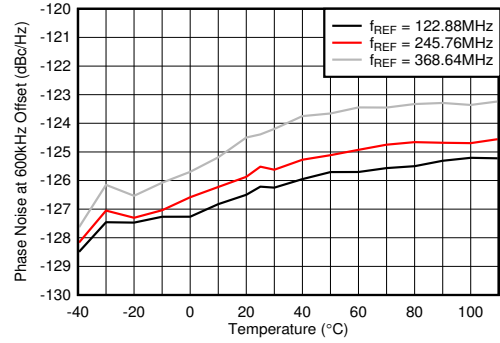
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-508. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 110°C**



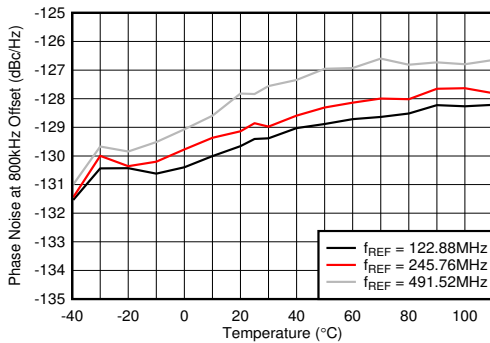
PLL enabled,  $f_{VCO} = 9830.4$  MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

图 6-509. Integrated Phase Noise for 10-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



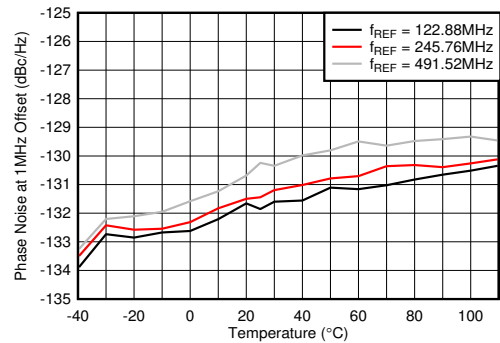
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

图 6-510. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



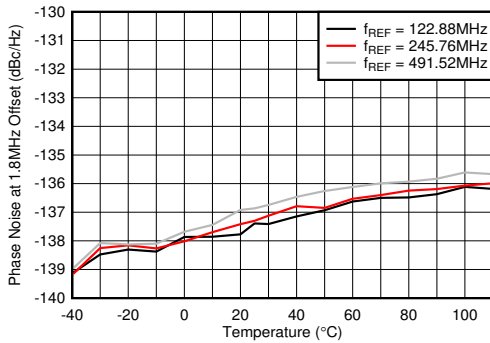
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

图 6-511. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



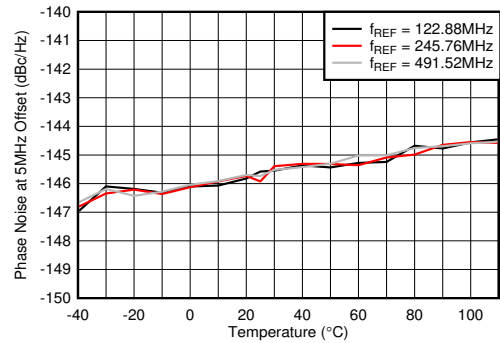
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

图 6-512. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



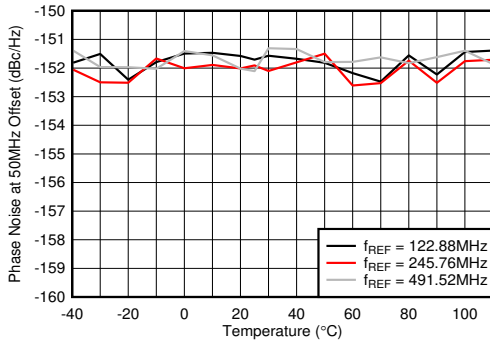
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

图 6-513. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



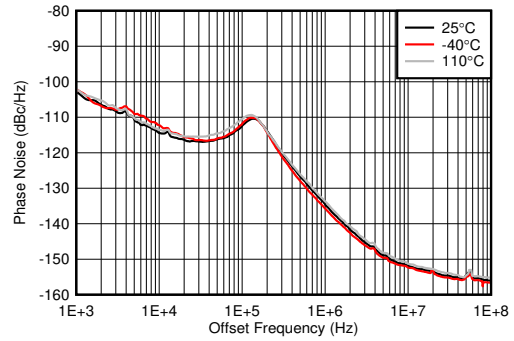
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

图 6-514. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



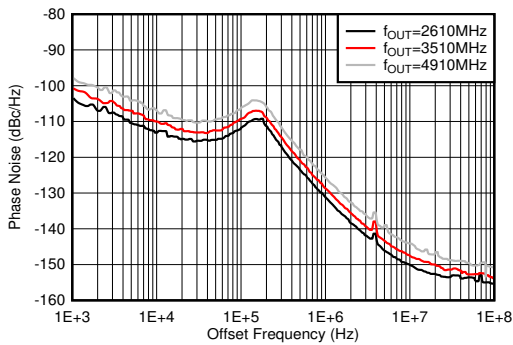
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**图 6-515. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



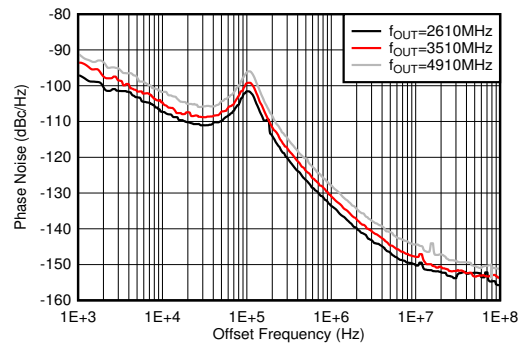
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

**图 6-516. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**



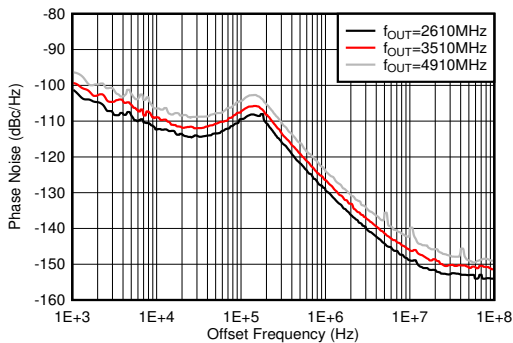
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

**图 6-517. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 25°C**



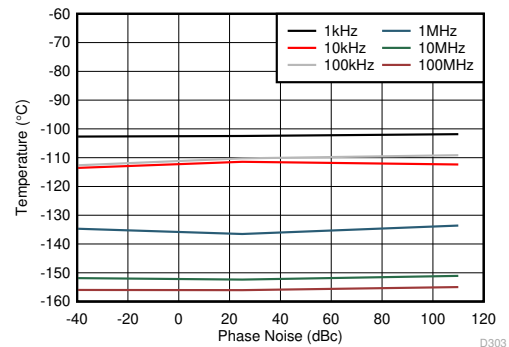
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

**图 6-518. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at -40°C**



PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

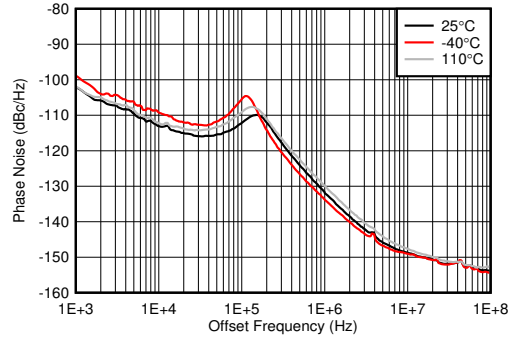
**图 6-519. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 110°C**



PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$ MSPS, minimum LPF BW, measured at 2TXOUT

**图 6-520. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at  $f_{OUT} = 2.6$  GHz**





PLL enabled,  $f_{VCO} = 7864.32$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-521. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**

## 7 Device and Documentation Support

### 7.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 7.2 支持资源

**TI E2E™ 支持论坛** 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 7.3 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 7.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 7.5 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7950IABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7950I	<a href="#">Samples</a>
AFE7950IALK	ACTIVE	FCBGA	ALK	400	90	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7950 SNPB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



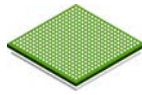
**TRAY**


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7950IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7950IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7950IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

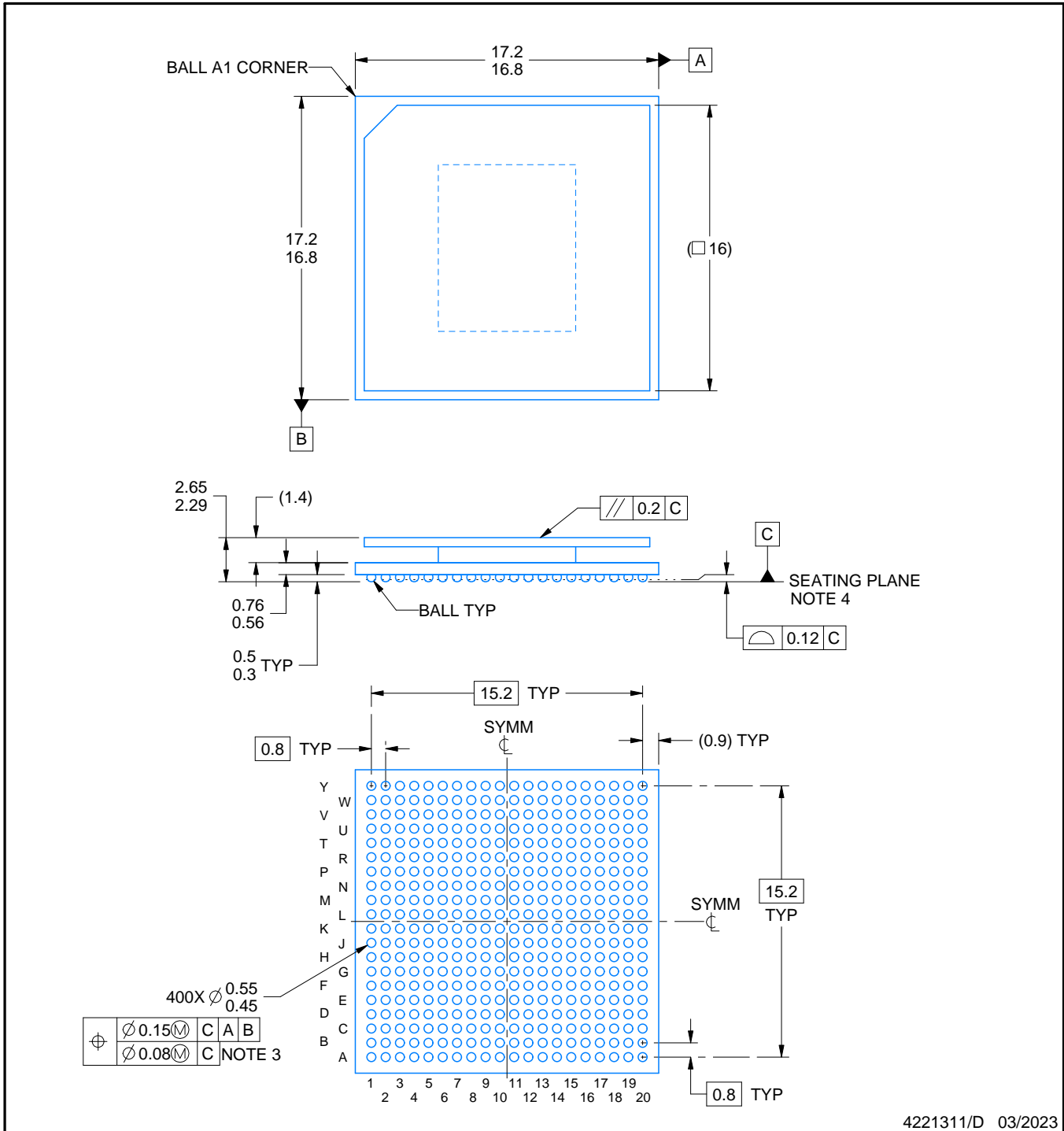
# ABJ0400A



# PACKAGE OUTLINE

FCBGA - 2.65 mm max height

BALL GRID ARRAY



## NOTES:

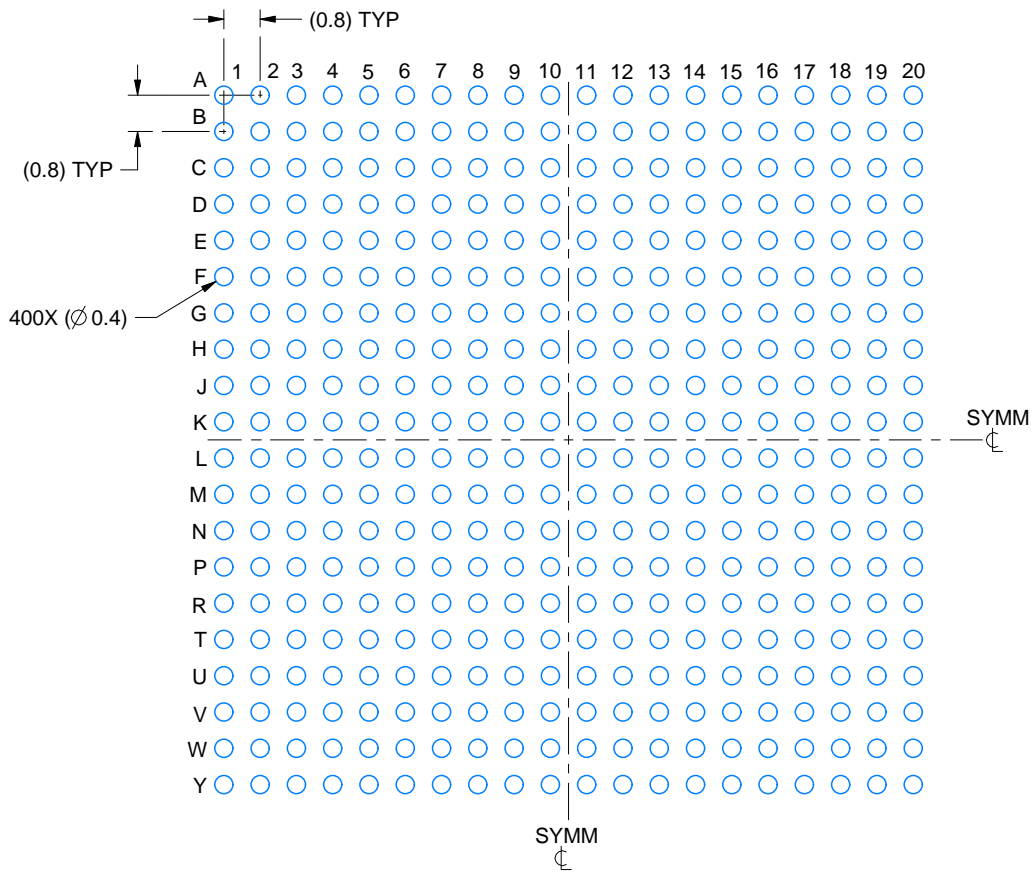
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

**ABJ0400A**

**FCBGA - 2.65 mm max height**

BALL GRID ARRAY



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:6X



**SOLDER MASK DETAILS**  
NOT TO SCALE

4221311/D 03/2023

NOTES: (continued)

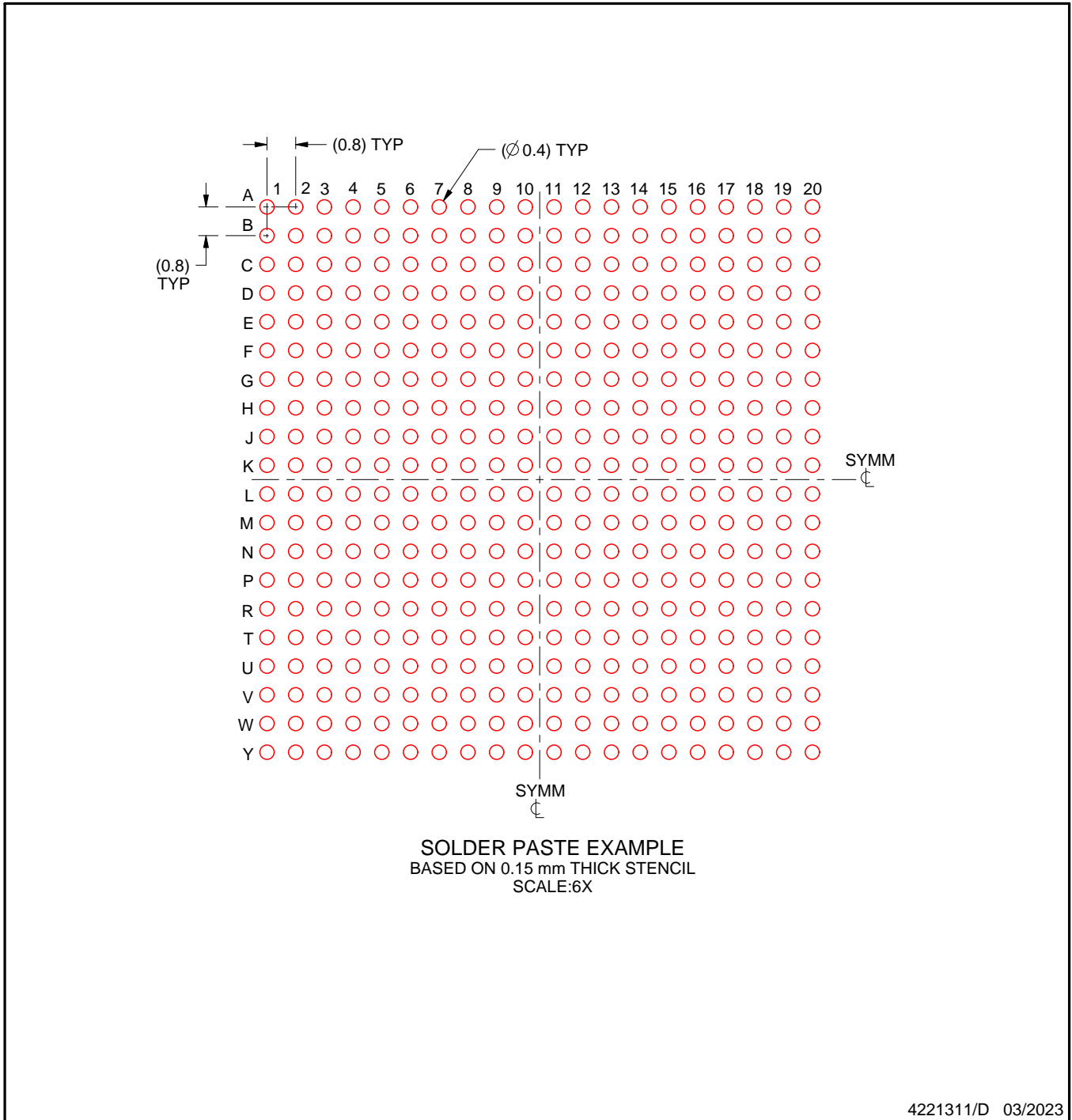
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:6X

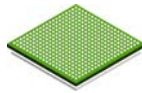
4221311/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



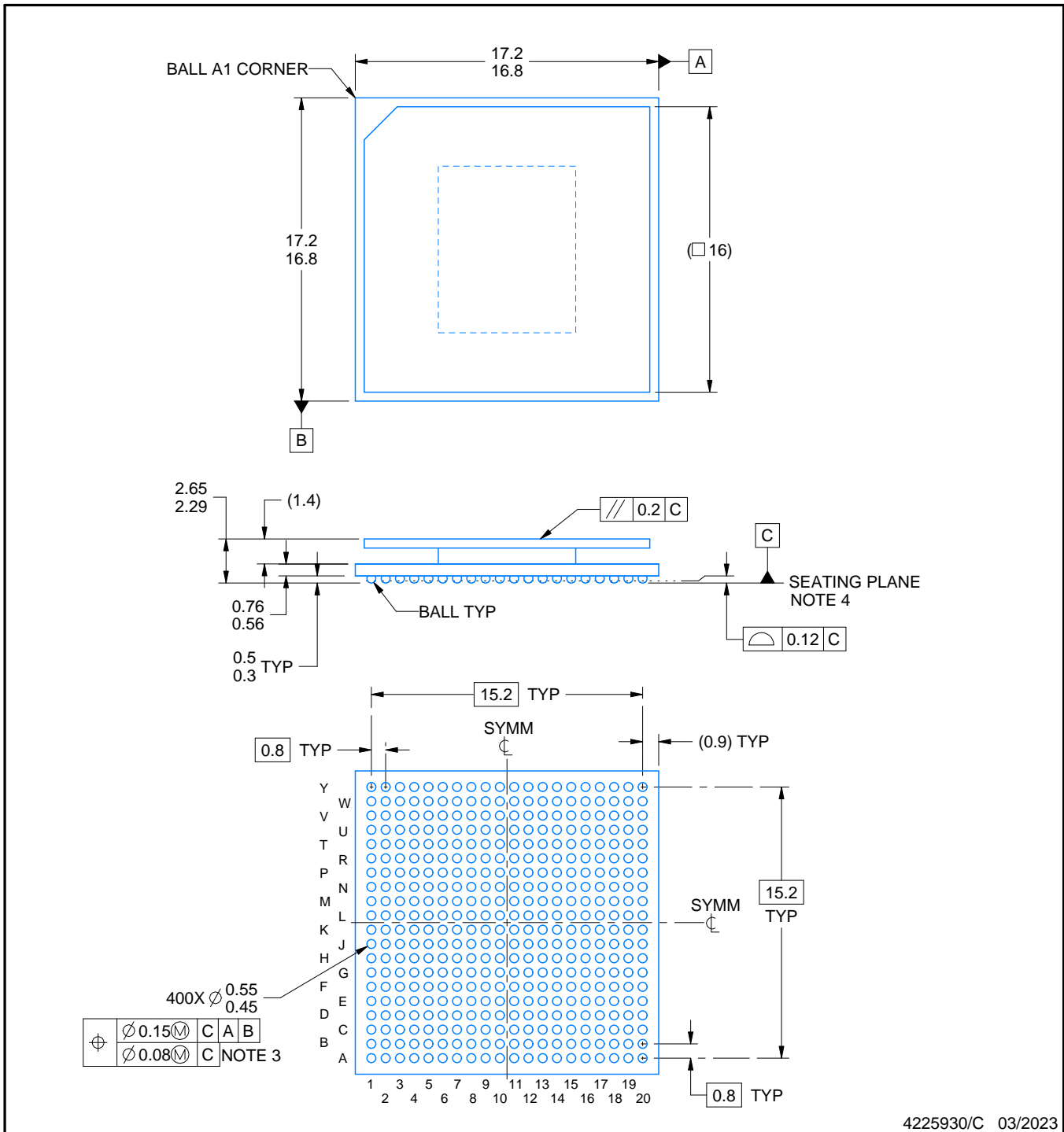
# ALK0400A



# PACKAGE OUTLINE

## FCBGA - 2.65 mm max height

BALL GRID ARRAY



4225930/C 03/2023

### NOTES:

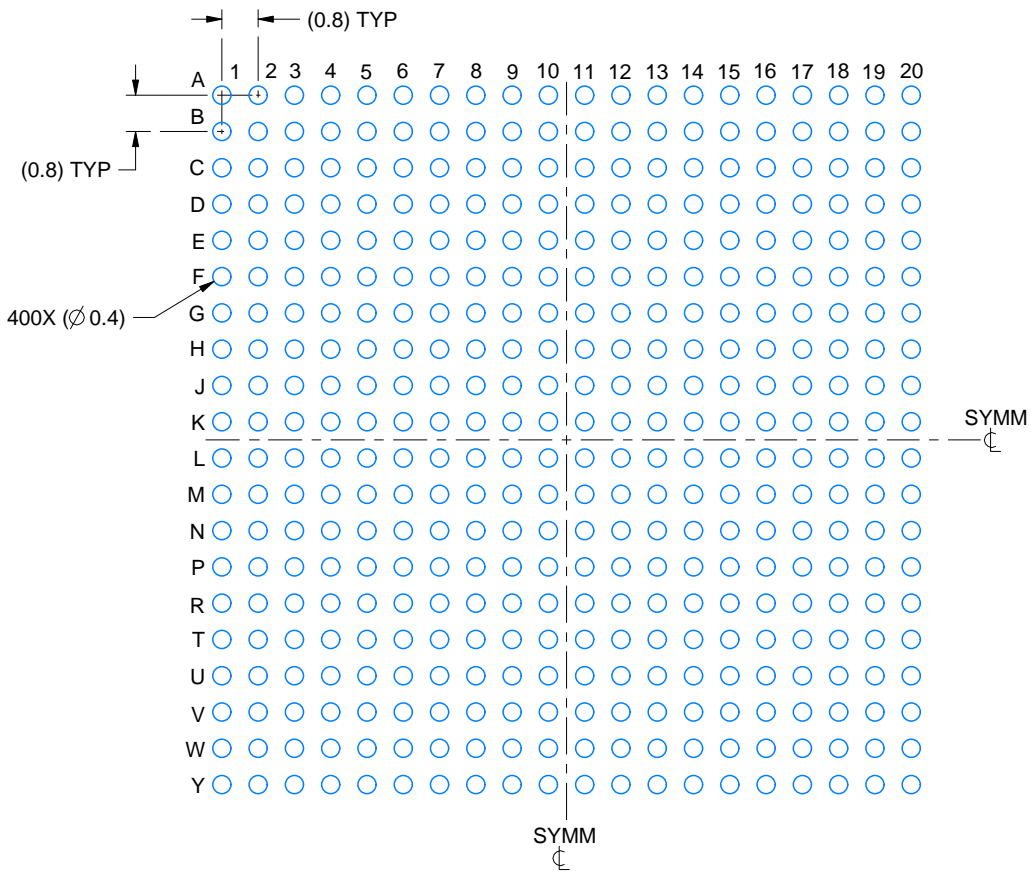
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

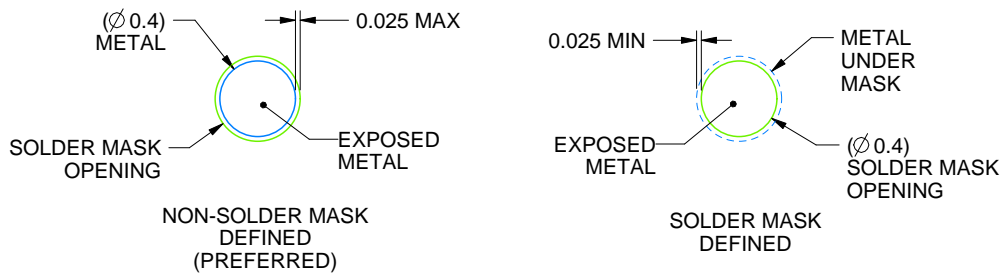
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

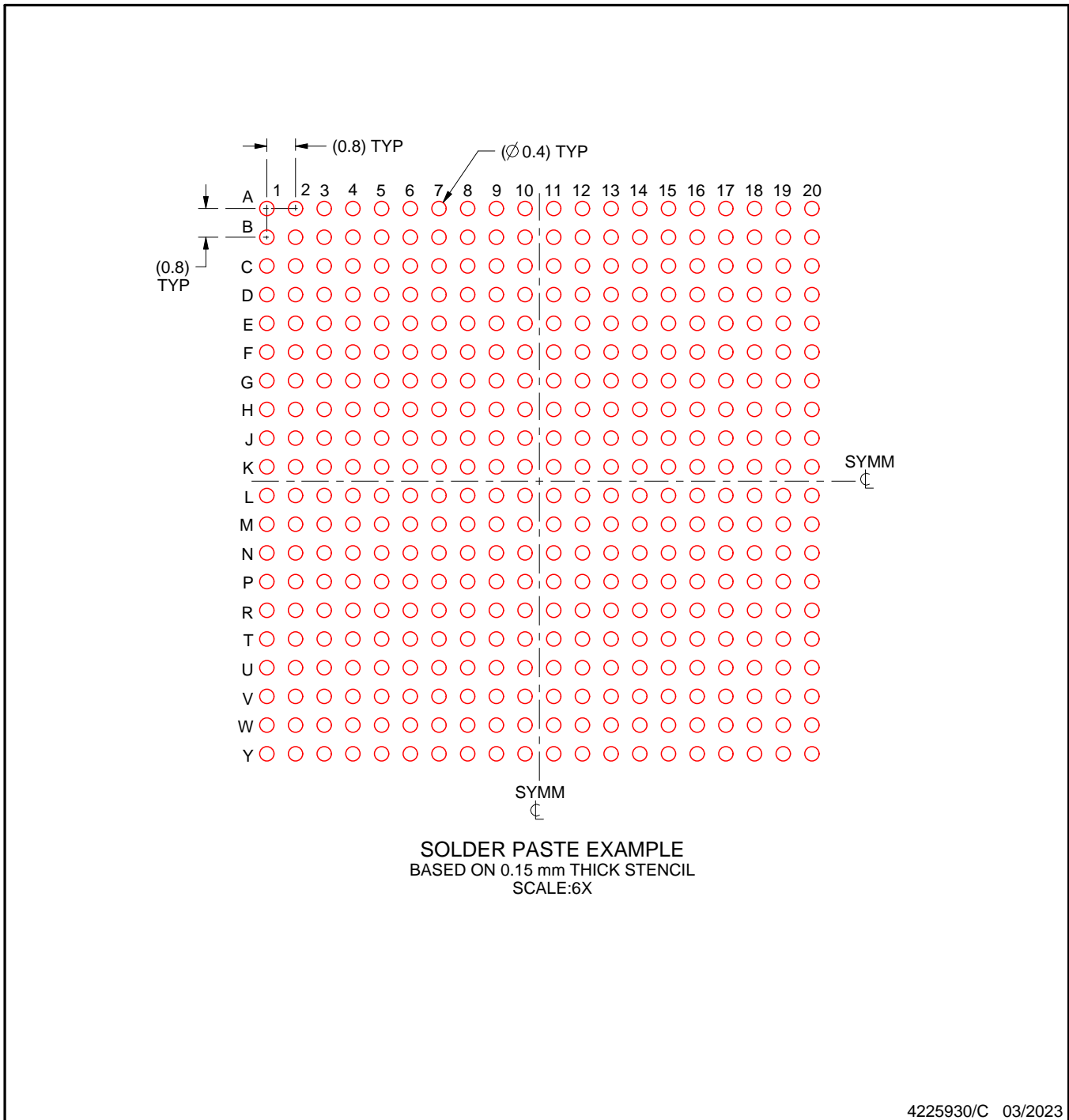
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

## ALK0400A

## FCBGA - 2.65 mm max height

BALL GRID ARRAY



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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