适用于 MCU 应用的具有共存选项的 CC3130 SimpleLink™ Wi-Fi® 无线网络处理器

1 特性

- 集成式 Wi-Fi® 和互联网协议
- 与 BLE 无线电共存 (CC13x2/CC26x2)
- 一组丰富的 IoT 安全特性，可帮助开发人员保护数据
- 低功耗模式适用于电池供电应用
- 网络辅助漫游
- 工业温度：–40°C 至 +85°C
- 可转让的 Wi-Fi 联盟®认证
- Wi-Fi 网络处理器子系统：
  - Wi-Fi 内核：
    - 802.11b/g/n 2.4GHz
    - 模式：
      - 接入点 (AP)
      - 基站 (STA)
      - Wi-Fi Direct®
    - 安全性：
      - WEP
      - WPA™/ WPA2™ PSK
      - WPA2 企业
      - WPA3™ 个人版
      - WPA3™ 企业版
  - 互联网和应用协议：
    - HTTP 服务器、mDNS、DNS-SD 和 DHCP
    - IPv4 和 IPv6 TCP/IP 堆栈
    - 16 BSD 套接字（完全安全的 TLS v1.2 和 SSL 3.0）
  - 内置的电源管理子系统：
    - 可配置的低功耗配置文件（始终、间歇性、标签）
    - 高级低功耗模式
    - 集成式直流/直流稳压器
- 多层安全特性：
  - 独立执行环境
  - 网络安全
  - 设备身份和密钥
  - 硬件加速器加密引擎（AES、DES、SHA/MD5 和 CRC）
  - 文件系统安全（加密、身份验证、访问控制）
  - 初始安全编程
  - 软件篡改检测
  - 证书注册请求 (CSR)
  - 每个设备具有唯一密钥对
- 应用吞吐量：
  - UDP：16Mbps，TCP：13Mbps
  - 峰值：72Mbps
- 电源管理子系统：
  - 集成式直流/直流转换器支持宽电源电压范围：
    - VBAT 宽电压模式：2.1 V 至 3.6 V
    - VIO 始终与 VBAT 关联
  - 高级低功耗模式：
    - 关断：1μA，休眠：4μA
    - 低功耗深度睡眠 (LPDS)：120μA
    - 空闲连接（MCU 处于 LPDS 状态）：710μA
    - RX 流量（MCU 处于活动模式）：53 mA
    - TX 流量（MCU 处于活动模式）：223 mA
- Wi-Fi TX 功率：
  - 1 DSSS 时为 18.0dBm
  - 54 OFDM 时为 14.5dBm
- Wi-Fi RX 灵敏度：
  - 1 DSSS 时为 -96dBm
  - 54 OFDM 时为 -74.5dBm
- 时钟源：
  - 具有内部振荡器的 40.0MHz 晶体
  - 32.768kHz 晶体或外部 RTC
- RGK 封装
  - 64 引脚 9mm × 9mm 极薄四方扁平无引线 (VQFN) 封装，0.5mm 间距
- 器件支持 SimpleLink™ MCU 平台开发人员生态系统

2 应用

- 对于物联网应用，例如：
  - 楼宇和住宅自动化：
    - HVAc 系统和恒温器
    - 视频监控、可视门铃和低功耗摄像头
    - 楼宇安防系统，电子智能锁
    - 烟雾探测器
    - 漏水检测器
  - 电器
    - 智能家庭远程控制
  - 资产跟踪
  - 工厂自动化
  - 医疗和保健
    - CPAP
  - 电网基础设施

3 说明

通过德州仪器 (TI) 的 CC3130 器件将任何微控制器 (MCU) 连接到物联网 (IoT)。SimpleLink™ Wi-Fi® CC3130 Internet-on-a chip™ 器件包含一个专用于 Wi-Fi® 和互联网协议的 Arm® Cortex®-M3 MCU，可减少主机 MCU 中的联网活动。该子系统包括 802.11b/g/n 无线电、基带以及具有强大加密引擎的 MAC，采用 256 位加密以实现快速、安全的互联网连接，并使用内置电源管理以实现出色的低功耗性能。

Wi-Fi CERTIFIED® CC3130 器件通过集成的 Wi-Fi Alliance® IoT 低功耗特性，极大地简化了低功耗功能的实施。

这一代引进了可进一步简化物联网连接的新功能。主要新特性包括：

- 低功耗 Bluetooth® 和 Wi-Fi 2.4-GHz 无线电共存 (CC13x2/CC26x2)
- 天线选择
- 可同时打开多达 16 个安全套接字
- 证书注册请求 (CSR)
- 在线证书状态协议 (OCSP)
- 经过 Wi-Fi® Alliance® 认证的 IoT 省电特性（例如 BSS 空闲上限、DMS 和代理 ARP）
- 降低模板包传输负载的无主机模式
- 网络辅助漫游

CC3130 器件随附一个占用空间小的用户友好型主机驱动程序，可简化网络应用的集成和开发。主机驱动程序可轻松移植到大多数平台和操作系统 (OS)。此驱动程序占用的内存很小，可在具有任何时钟速度的 8 位、16 位或 32 位微控制器上运行（无需使用高性能时钟或实时时钟）。

CC3130 器件是 SimpleLink™ MCU 平台的一部分，该平台是一个通用、简单易用的开发环境，基于一个单核软件开发套件 (SDK)、丰富的工具集、参考设计和 E2E™ 社区而构建，支持 Wi-Fi®、低功耗 Bluetooth®、Sub-1GHz 器件和主机 MCU。有关更多信息，请访问 *www.ti.com/simplelink*。

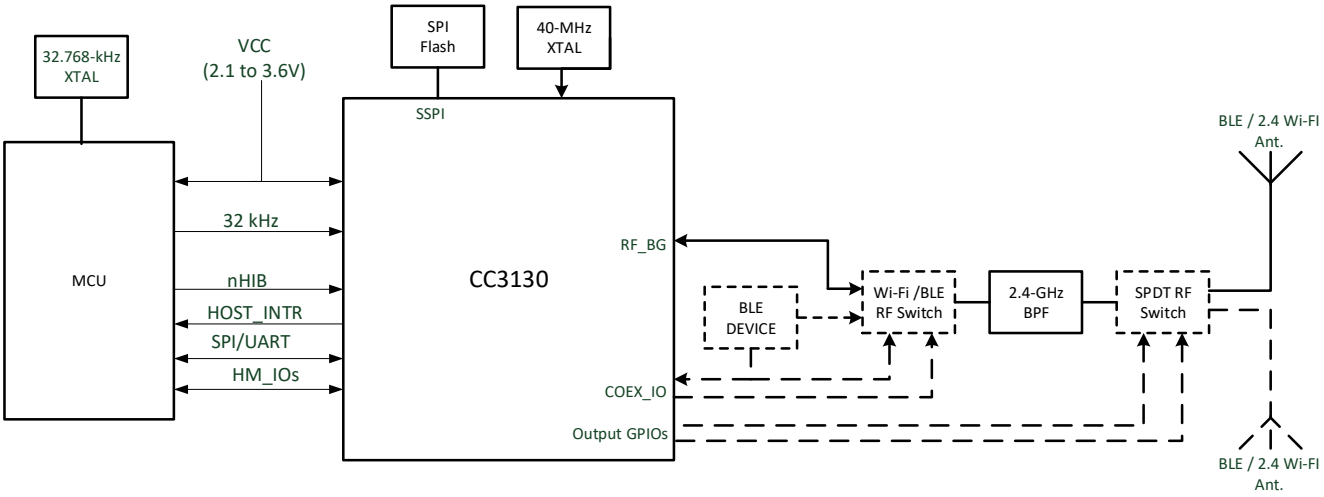
器件信息(1)

器件型号	封装	封装尺寸
CC3130RNMRGKR	VQFN (64)	9.00mm x 9.00mm（标称值）

(1) 如需更多信息，请参阅*机械、封装和可订购信息*部分。

4 功能方框图

图 4-1 显示了 CC3130 器件的功能方框图。



注意：双信器用于信号天线解决方案。使用天线选择功能（双天线）时，需要在双信器后应用 1 个 SPDT 开关和 2 条 GPIO 线路。

图 4-1. 功能方框图

图 4-2 显示了 CC3130 硬件概览。

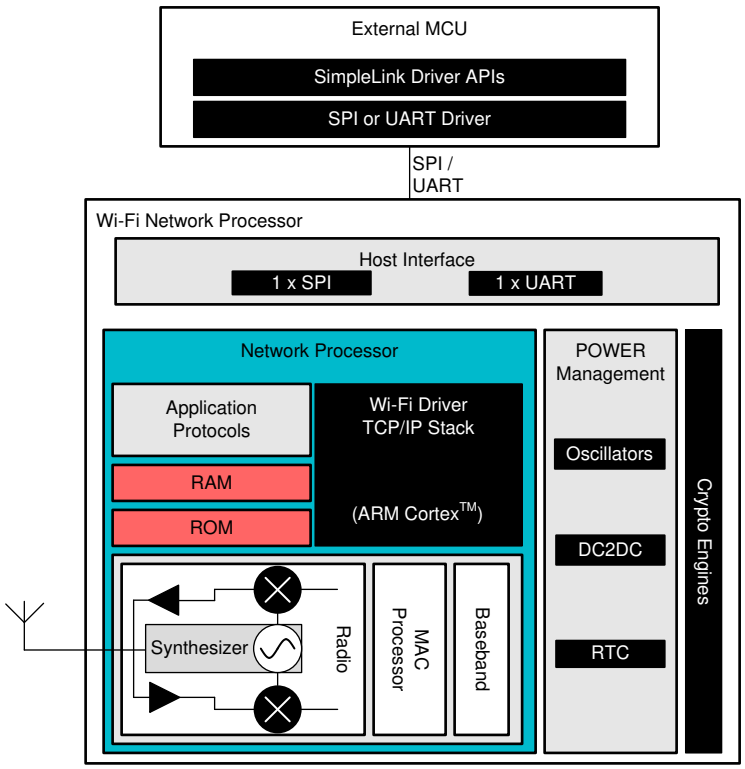


图 4-2. CC3130 硬件概览

图 4-3 显示了 CC3130 嵌入式软件概览。

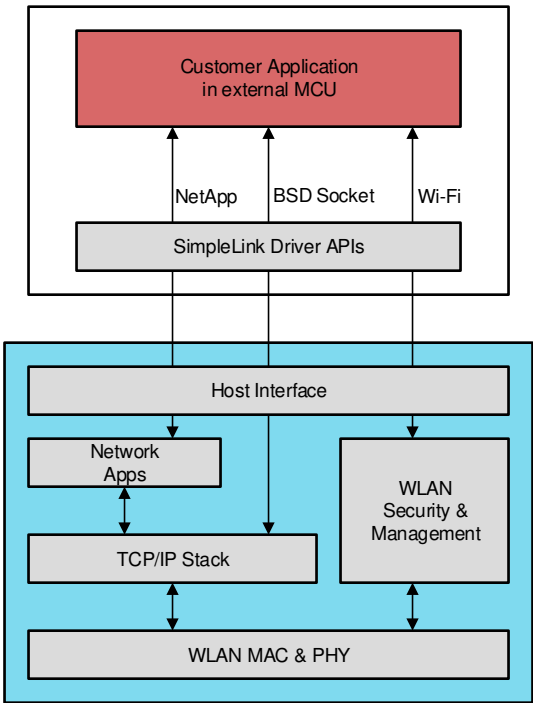


图 4-3. CC3130 软件概览

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5 Revision History

Changes from September 28, 2020 to May 13, 2021 (from Revision A (September 2020) to Revision B (May 2021)) **Page**

- 向节 1 中的 Wi-Fi 核心安全性添加了 “WPA3™ 企业版 “ 1
- Added "WPA3 personal and enterprise" to "Wi-Fi level of security" in 表 6-1. 6
- Added 节 8.16.3, *Host UART* 36
- Changed footnote in 节 9.1 38
- Added "WPA3™ personal and enterprise security" to 节 9.1. 38
- Added "WPA3™ enterprise" to 节 9.2.1. 38
- Changed tablenote for 表 9-1 39
- Added "WPA3™ enterprise" to "Wi-Fi security" in 表 9-1. 39

6 Device Comparison

表 6-1 lists the features supported across different CC3x3x devices.

表 6-1. Comparison of Device Features

FEATURE	DEVICE					
	CC3130	CC3135	CC3230S	CC3230SF	CC3235S	CC3235SF
Classification	Network Processor	Network Processor	Wireless microcontroller	Wireless microcontroller	Wireless microcontroller	Wireless microcontroller
Standard	802.11b/g/n	802.11a/b/g/n	802.11b/g/n	802.11b/g/n	802.11a/b/g/n	802.11a/b/g/n
TCP/IP stack	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6
Sockets	16	16	16	16	16	16
Package	9-mm × 9-mm VQFN	9-mm × 9-mm VQFN	9-mm × 9-mm VQFN	9-mm × 9-mm VQFN	9-mm × 9-mm VQFN	9-mm × 9-mm VQFN
ON-CHIP APPLICATION MEMORY						
Flash	—	—	—	1MB	—	1MB
RAM	—	—	256KB	256KB	256KB	256KB
RF FEATURES						
Frequency	2.4 GHz	2.4 GHz, 5 GHz	2.4 GHz	2.4 GHz	2.4 GHz, 5 GHz	2.4 GHz, 5 GHz
Coexistence with BLE Radio (CC13x2/ CC26x2)	Yes	Yes	Yes	Yes	Yes	Yes
SECURITY FEATURES						
Secure boot	—	—	Yes	Yes	Yes	Yes
FIPS 140-2 Level 1 Certification(1)	No	Yes	No	No	Yes	Yes
Enhanced application level security	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming
Wi-Fi level of security	WEP, WPS, WPA / WPA2 PSK, WPA2 (802.1x), WPA3 personal and enterprise					
Additional networking security	Unique device identity Trusted root-certificate catalog TI Root-of-trust public key Online certificate status protocol (OCSP) Certificate signing request (CSR) Unique per-device key pair					
Hardware acceleration	Hardware crypto engines					

(1) For exact status of FIPS certification for a specific part number, please refer to https://csrc.nist.gov/publications/fips.

6.1 Related Products

For information about other devices in this family of products or related products see the links below.

The SimpleLink™ MCU Portfolio	This portfolio offers a single development environment that delivers flexible hardware, software, and tool options for customers developing wired and wireless applications. With 100 percent code reuse across host MCUs, Wi-Fi®, Bluetooth® low energy, Sub-1 GHz devices and more, choose the MCU or connectivity standard that fits your design. A one-time investment with the SimpleLink™ software development kit (SDK) allows you to reuse often, opening the door to create unlimited applications.
SimpleLink™ Wi-Fi® Family	This device platform offers several Internet-on-a chip™ solutions, which address the need of battery-operated, security-enabled products. Texas Instruments offers a single-chip wireless microcontroller and a wireless network processor that can be paired with any MCU, allowing developers to design new Wi-Fi® products or upgrade existing products with Wi-Fi® capabilities.
MSP432™ Host MCU	features the Arm® Cortex®-M4 processor offering ample processing capability with floating point unit and memory footprint for advanced processing algorithm, communication protocols as well as application needs, while incorporating a 14-bit 1-msps ADC14 that provides a flexible and low-power analog with best-in-class performance to enable developers to add differentiated sensing and measurement capabilities to their Wi-Fi applications. For more information, visit www.ti.com/product/MSP432P401R.
Reference Designs	Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors. All designs include a schematic, test data and design files.
The SimpleLink™ Wi-Fi® SDK Plug-in	The SDK contains drivers, sample applications for Wi-Fi features and Internet, and documentation required to use the CC3130 solution.

7 Terminal Configuration and Functions

7.1 Pin Diagram

图 7-1 shows pin assignments for the 64-pin VQFN package.

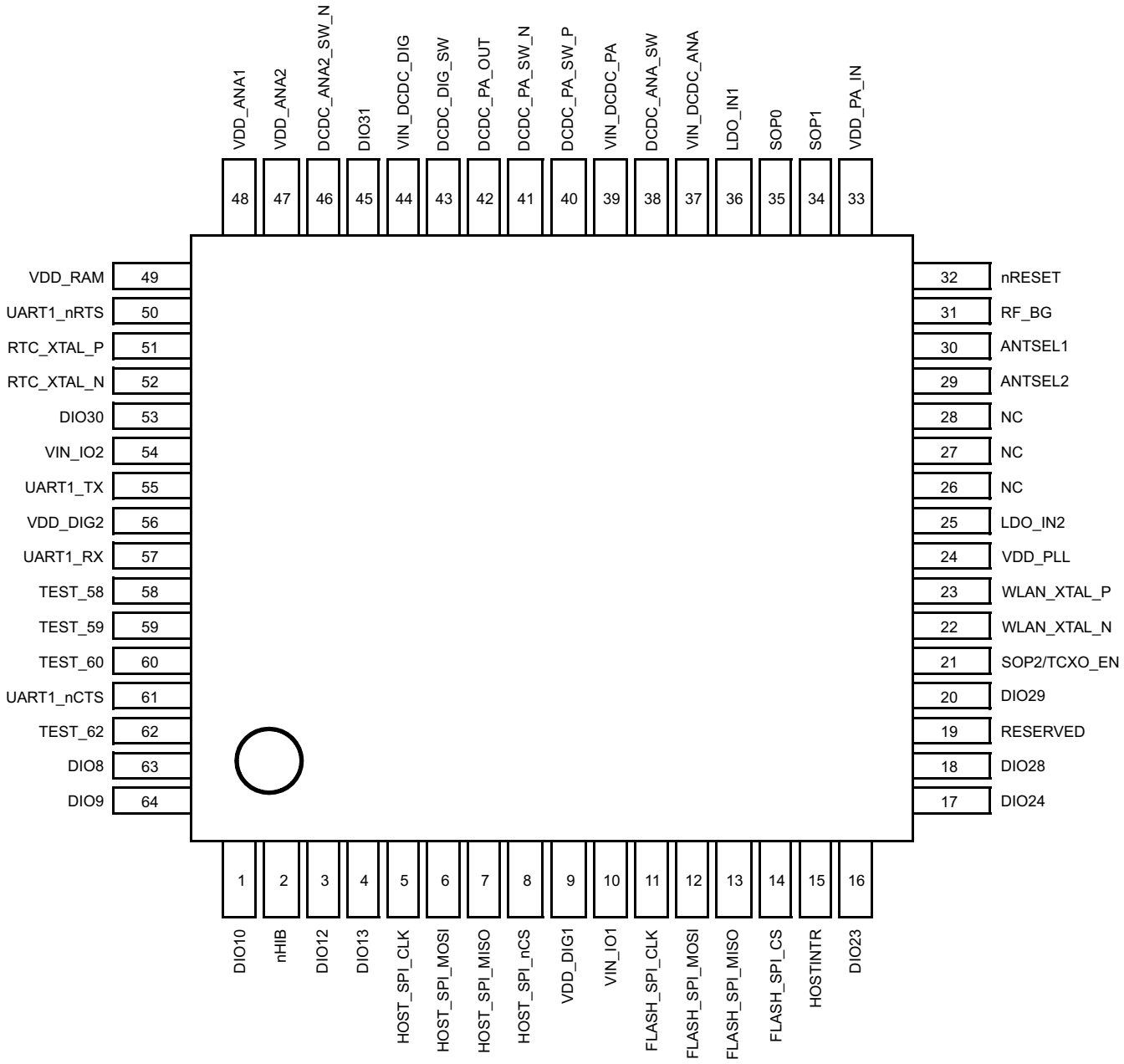


图 7-1. Top View Pin Assignment for 64-Pin VQFN

7.2 Pin Attributes

表 7-1 describes the CC3130 pins.

Note

Digital IOs on the CC3130 device refer to hostless mode, BLE/2.4 GHz coexistence, and antenna select IOs, not general-purpose IOs.

If an external device drives a positive voltage to signal pads when the CC3130 device is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3130 device can occur. To prevent current draw, TI recommends one of the following:

- All devices interfaced to the CC3130 device must be powered from the same power rail as the CC3130 device.
- Use level shifters between the CC3130 device and any external devices fed from other independent rails.
- The nRESET pin of the CC3130 device must be held low until the V_{BAT} supply to the device is driven and stable.

表 7-1. Pin Description and Attributes

PIN	DEFAULT FUNCTION	DIGITAL I/O				STATE AT RESET AND HIBERNATE	I/O TYPE(1)	DESCRIPTION
		PAD_CONFIG	HOSTLESS MODE	BLE COEX				
				CC_COEX_OUT	CC_COEX_IN			
1	DIO10	10	Y	Y	Y	–	I/O	Digital input or output
2	nHIB	11	-	-	-	Hi-Z	I	Hibernate signal input to the NWP subsystem (active low). This is connected to the MCU GPIO. If the GPIO from the MCU can float while the MCU enters low power, consider adding a pullup resistor on the board to avoid floating.
3	DIO12	12	Y	Y	Y	–	O	Digital input or output
4	DIO13	13	Y	Y	Y	–	–	Digital input or output
5	HOST_SPI_CLK	14	-	-	-	Hi-Z	I	Host interface SPI clock
6	HOST_SPI_MOSI	15	-	-	-	Hi-Z	I	Host interface SPI data input
7	HOST_SPI_MISO	16	-	-	-	Hi-Z	O	Host interface SPI data output
8	HOST_SPI_nCS	17	-	-	-	Hi-Z	I	Host interface SPI chip select (active low)
9	VDD_DIG1	-	N/A	N/A	N/A	Hi-Z	Power	Digital core supply (1.2 V)
10	VIN_IO1	-	N/A	N/A	N/A	Hi-Z	Power	I/O supply
11	FLASH_SPI_CLK	-	N/A	N/A	N/A	Hi-Z	O	Serial Flash interface: SPI clock
12	FLASH_SPI_MOSI	-	N/A	N/A	N/A	Hi-Z	O	Serial Flash interface: SPI data out
13	FLASH _SPI_MISO	-	N/A	N/A	N/A	Hi-Z	I	Serial Flash interface: SPI data in (active high)
14	FLASH _SPI_CS	-	N/A	N/A	N/A	Hi-Z	O	Serial Flash interface: SPI chip select (active low)
15	HOST_INTR	22	-	-	-	Hi-Z	O	Interrupt output (active high)
16	DIO23	23	Y	Y	Y	Hi-Z		Digital input or output
17	DIO24	24	Y	Y	Y	Hi-Z		Digital input or output
18	DIO28	40	Y	Y	Y	–	–	Digital input or output

表 7-1. Pin Description and Attributes (continued)

PIN	DEFAULT FUNCTION		DIGITAL I/O			STATE AT RESET AND HIBERNATE	I/O TYPE[1]	DESCRIPTION
		PAD_CONFIG	HOSTLESS MODE	BLE COEX				
				CC_COEX_OUT	CC_COEX_IN			
19	Reserved	28	-	-	-	Hi-Z	–	Connect a 100-kΩ pulldown resistor to ground.
20	DIO29	29	Y	Y	Y	Hi-Z		Digital input or output
21	SOP2/TCXO_EN[2]	25	Y[3]	Y	-	Hi-Z	O	Controls restore to default mode. Enable signal for external TCXO. Add a 10-kΩ pulldown resistor to ground.
22	WLAN_XTAL_N	-	N/A	N/A	N/A	Hi-Z	Analog	Connect the WLAN 40-MHz crystal here.
23	WLAN_XTAL_P	-	N/A	N/A	N/A	Hi-Z	Analog	Connect the WLAN 40-MHz crystal here.
24	VDD_PLL	-	N/A	N/A	N/A	Hi-Z	Power	Internal PLL power supply (1.4 V nominal)
25	LDO_IN2	-	N/A	N/A	N/A	Hi-Z	Power	Input to internal LDO
26	NC	-	N/A	N/A	N/A	–	–	No Connect
27	NC	-	N/A	N/A	N/A	–	–	No Connect
28	NC	-	N/A	N/A	N/A	–	–	No Connect
29	ANTSEL1[4]	-	N/A	N/A	N/A	Hi-Z	O	Reserved for future use
30	ANTSEL2[4]	-	N/A	N/A	N/A	Hi-Z	O	Reserved for future use
31	RF_BG	-	N/A	N/A	N/A	Hi-Z	RF	2.4 GHz RF TX, RX
32	nRESET	-	N/A	N/A	N/A	Hi-Z	I	RESET input for the device. Active low input. Use RC circuit (100 kΩ || 0.01 µF) for power on reset (POR).
33	VDD_PA_IN	-	N/A	N/A	N/A	Hi-Z	Power	Power supply for the RF power amplifier (PA)
34	SOP1	-	N/A	N/A	N/A	Hi-Z	–	SOP[2:0] used for factory restore. Add 100-kΩ pulldown to ground. See 节 9.6. SOP1 used for 5 GHz switch control
35	SOP0	-	N/A	N/A	N/A	Hi-Z	–	SOP[2:0] used for factory restore. Add 100-kΩ pulldown to ground. See 节 9.6. SOP0 used for 5GHz switch control
36	LDO_IN1	-	N/A	N/A	N/A	Hi-Z	Power	Input to internal LDO
37	VIN_DCDC_ANA	-	N/A	N/A	N/A	Hi-Z	Power	Power supply for the DC/DC converter for analog section
38	DCDC_ANA_SW	-	N/A	N/A	N/A	Hi-Z	Power	Analog DC/DC converter switch output
39	VIN_DCDC_PA	-	N/A	N/A	N/A	Hi-Z	Power	PA DC/DC converter input supply
40	DCDC_PA_SW_P	-	N/A	N/A	N/A	Hi-Z	Power	PA DC/DC converter switch output +ve
41	DCDC_PA_SW_N	-	N/A	N/A	N/A	Hi-Z	Power	PA DC/DC converter switch output – ve
42	DCDC_PA_OUT	-	N/A	N/A	N/A	Hi-Z	Power	PA DC/DC converter output. Connect the output capacitor for DC/DC here.
43	DCDC_DIG_SW	-	N/A	N/A	N/A	Hi-Z	Power	Digital DC/DC converter switch output
44	VIN_DCDC_DIG	-	N/A	N/A	N/A	Hi-Z	Power	Power supply input for the digital DC/DC converter
45	DIO31	31	Y	Y	Y	Hi-Z	–	Network Scripter I/O

表 7-1. Pin Description and Attributes (continued)

PIN	DEFAULT FUNCTION		DIGITAL I/O			STATE AT RESET AND HIBERNATE	I/O TYPE(1)	DESCRIPTION
		PAD_CONFIG	HOSTLESS MODE	BLE COEX				
				CC_COEX_OUT	CC_COEX_IN			
46	DCDC_ANA2_SW_N	-	N/A	N/A	N/A	Hi-Z	Power	Analog2 DC/DC converter switch output – ve
47	VDD_ANA2	-	N/A	N/A	N/A	Hi-Z	Power	Analog2 power supply input
48	VDD_ANA1	-	N/A	N/A	N/A	Hi-Z	Power	Analog1 power supply input
49	VDD_RAM	-	N/A	N/A	N/A	Hi-Z	Power	Power supply for the internal RAM
50	UART1_nRTS	0	-	-	-	Hi-Z	O	UART host interface (active low)
51	RTC_XTAL_P	-	N/A	N/A	N/A	Hi-Z	Analog	32.768-kHz XTAL_P or external CMOS level clock input
52	RTC_XTAL_N	32	Y	Y	Y	Hi-Z	Analog	32.768-kHz XTAL_N or 100-kΩ external pullup for external clock
53	DIO30	30	Y	Y	Y	Hi-Z	–	Network Scripter I/O
54	VIN_IO2		N/A	N/A	N/A	Hi-Z	Power	I/O power supply. Same as battery voltage.
55	UART1_TX	1	-	-	-	Hi-Z	O	UART host interface. Connect to test point on prototype for Flash programming.
56	VDD_DIG2	-	N/A			Hi-Z	Power	Digital power supply (1.2 V)
57	UART1_RX	2	-	-	-	Hi-Z	I	UART host interface; connect to test point on prototype for Flash programming.
58	TEST_58	3	Y	Y	Y	Hi-Z	O	Test signal; connect to an external test point.
59	TEST_60	4	Y	Y	Y	Hi-Z	O	Test signal; connect to an external test point.
60	TEST_60	5	Y	Y	Y	Hi-Z	O	Test signal; connect to an external test point.
61	UART1_nCTS	6	-	-	-	Hi-Z	I	UART host interface (active low)
62	TEST_62	7	-	-	-	Hi-Z	O	Test signal; connect to an external test point.
63	DIO8	8	Y	Y	Y	Hi-Z		Digital input or output
64	DIO9	9	Y	Y	Y	Hi-Z	–	Digital input or output
65	GND	-	N/A	N/A	N/A	–	Power	Ground tab used as thermal and electrical ground

(1) I = input
O = output
RF = radio frequency
I/O = bidirectional

(2) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

(3) Output Only

(4) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3130x device between two antennas. These pins must not be used for other functionalities.

7.3 Signal Descriptions

表 7-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Antenna selection	DIO10	1	I/O	O	Antenna selection control
	DIO12	3	I/O	O	
	DIO13	4	I/O	O	
	DIO23	16	I/O	O	
	DIO24	17	I/O	O	
	DIO28	18(1)	I/O	O	
	DIO29	20	I/O	O	
	DIO25	21	O	O	
	DIO31	45(1)	I/O	O	
	DIO32	52(1)	I/O	O	
	DIO30	53(1)	I/O	O	
	DIO3	58	I/O	O	
	DIO4	59	I/O	O	
	DIO5	60	I/O	O	
	DIO8	63	I/O	O	
	DIO9	64	I/O	O	
	ANTSEL1	29	O	O	Anatenna selection control 1
	ANTSEL2	30	O	O	Antenna selection control 2
BLE/2.4 GHz Radio coexistence	DIO10	1	I/O	I/O	Coexistence inputs and outputs
	DIO12	3	I/O	I/O	
	DIO13	4	I/O	I/O	
	DIO23	16	I/O	I/O	
	DIO24	17	I/O	I/O	
	DIO28	18(1)	I/O	I/O	
	DIO29	20	I/O	I/O	
	DIO25	21	O	O	
	DIO31	45(1)	I/O	I/O	
	DIO32	52(1)	I/O	I/O	
	DIO30	53(1)	I/O	I/O	
	DIO3	58	I/O	I/O	
	DIO4	59	I/O	I/O	
	DIO5	60	I/O	I/O	
	DIO8	63	I/O	I/O	
	DIO9	64	I/O	I/O	
Clock	WLAN_XTAL_N	22	—	—	40-MHz crystal; pull down if external TCXO is used
	WLAN_XTAL_P	23	—	—	40-MHz crystal or TCXO clock input
	RTC_XTAL_P	51	—	—	Connect 32.768-kHz crystal or force external CMOS level clock
	RTC_XTAL_N	52	—	—	Connect 32.768-kHz crystal or connect 100-kΩ resistor to supply voltage

表 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Hostless Mode	DIO10	1	I/O	I/O	Hostless mode inputs and outputs
	DIO12	3	I/O	I/O	
	DIO13	4	I/O	I/O	
	DIO23	16	I/O	I/O	
	DIO24	17	I/O	I/O	
	DIO28	18(1)	I/O	I/O	
	DIO29	20	I/O	I/O	
	DIO25	21	O	O	
	DIO31	45(1)	I/O	I/O	
	DIO32	52(1)	I/O	I/O	
	DIO30	53(1)	I/O	I/O	
	DIO3	58	I/O	I/O	
	DIO4	59	I/O	I/O	
	DIO5	60	I/O	I/O	
	DIO8	63	I/O	I/O	
	DIO9	64	I/O	I/O	
Power	VDD_DIG1	9	—	—	Internal digital core voltage
	VIN_IO1	10	—	—	Device supply voltage (V_{BAT})
	VDD_PLL	24	—	—	Internal analog voltage
	LDO_IN2	25	—	—	Internal analog RF supply from analog DC/DC output
	VDD_PA_IN	33	—	—	Internal PA supply voltage from PA DC/DC output
	LDO_IN1	36	—	—	Internal analog RF supply from analog DC/DC output
	VIN_DCDC_ANA	37	—	—	Analog DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_ANA_SW	38	—	—	Internal analog DC/DC switching node
	VIN_DCDC_PA	39	—	—	PA DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_PA_SW_P	40	—	—	Internal PA DC/DC switching node
	DCDC_PA_SW_N	41	—	—	Internal PA DC/DC switching node
	DCDC_PA_OUT	42	—	—	Internal PA buck converter output
	DCDC_DIG_SW	43	—	—	Internal digital DC/DC switching node
	VIN_DCDC_DIG	44	—	—	Digital DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_ANA2_SW_P	45	—	—	Analog to DC/DC converter +ve switching node
	DCDC_ANA2_SW_N	46	—	—	Internal analog to DC/DC converter – ve switching node
	VDD_ANA2	47	—	—	Internal analog to DC/DC output
	VDD_ANA1	48	—	—	Internal analog supply fed by ANA2 DC/DC output
	VDD_RAM	49	—	—	Internal SRAM LDO output
	VIN_IO2	54	—	—	Device supply voltage (V_{BAT})
	VDD_DIG2	56	—	—	Internal digital core voltage
HOST SPI	HOST_SPI_CLK	5	I/O	I	Host SPI clock input
	HOST_SPI_MOSI	6	I/O	I	Data from Host
	HOST_SPI_MISO	8	I/O	O	Data to Host
	HOST_SPI_nCS	7	I/O	I	Device select (active low)

表 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
FLASH SPI	FLASH_SPI_CLK	11	O	O	Clock to SPI serial flash (fixed default)
	FLASH_SPI_DOUT	12	O	O	Data to SPI serial flash (fixed default)
	FLASH_SPI_DIN	13	I	I	Data from SPI serial flash (fixed default)
	FLASH_SPI_CS	14	O	O	Device select to SPI serial flash (fixed default)
UART	UART1_nRTS	50	I/O	O	UART1 request-to-send (active low)
	UART1_TX	55	I/O	I	UART TX data
	UART1_RX	57	I/O	O	UART RX data
	UART1_nCTS	61	I/O	I	UART1 clear-to-send (active low)
Sense-On-Power	SOP2	21(2)	O	I	Sense-on-power 2
	SOP1	34	I	I	Configuration sense-on-power 1
	SOP0	35	I	I	Configuration sense-on-power 0
Reset	nRESET	32	I	I	Global master device reset (active low)
nHIB	nHIB	2	I	I	Hibernate signal input to the NWP subsystem (active low)
RF	RF_BG	31	I/O	I/O	WLAN analog RF 802.11b/g/n bands
Test Port	TEST_58	58	O	O	Test Signal
	TEST_59	59	I	I	Test Signal
	TEST_60	60	O	O	Test Signal
	TEST_62	62	O	O	Test Signal

(1) LPDS retention unavailable.
(2) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

7.4 Connections for Unused Pins

All unused pin should be configured as stated in 表 7-3.

表 7-3. Connections for Unused Pins

FUNCTION	SIGNAL DESCRIPTION	PIN NUMBER	ACCEPTABLE PRACTICE	PREFERRED PRACTICE
DIO	Digital input or output		Wake up I/O source should not be floating during hibernate. All the I/O pins will float while in Hibernate and Reset states. Ensure pullup and pulldown resistors are available on board to maintain the state of the I/O. Leave unused DIOs as NC	
No Connect	NC	26, 29, 30	Unused pin, leave as NC.	Unused pin, leave as NC
SOP	Configuration sense-on-power		Ensure pulldown resistors are available on unused SOP pins	100-kΩ Pull down resistor on SOP0 and SOP1. 2.7-kΩ pull down on SOP2
Reset	RESET input for the device		Never leave the reset pin floating	
Clock	RTC_XTAL_N		When using an external oscillator, add a 100-kΩ pullup resistor to VIO	
	WLAN_XTAL_N		When using an external oscillator, connect to ground if unused	

8 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

8.1 Absolute Maximum Ratings

All measurements are referenced at the device pins unless otherwise indicated. All specifications are over process and overvoltage unless otherwise indicated.
Over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
Supply voltage	V_{BAT} and V_{IO}	Pins: 37, 39, 44	–0.5	3.8	V
	V_{IO} – V_{BAT} (differential)	Pins: 10, 54	V_{BAT} and V_{IO} should be tied together		V
Digital inputs			–0.5	V_{IO} + 0.5	V
RF pins			–0.5	2.1	V
Analog pins, Crystal		Pins: 22, 23, 51, 52	–0.5	2.1	V
Operating temperature, T_A			–40	85	°C
Storage temperature, T_{stg}			–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

8.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Power-On Hours (POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

OPERATING CONDITION	POWER-ON HOURS [POH] (hours)
T_A up to 85°C(1)	87,600

(1) The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

8.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

				MIN	TYP	MAX	UNIT
Supply voltage	V_{BAT}, V_{IO} (shorted to V_{BAT})	Pins: 10, 37, 39, 44, 54	Direct battery connection(3)	2.1(4)	3.3	3.6	V
Ambient thermal slew				–20		20	°C/minute

(1) Operating temperature is limited by crystal frequency variation.
(2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
(3) To ensure WLAN performance, ripple on the supply must be less than ±300 mV.
(4) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1 V, and care must be taken when operating at the minimum specified voltage.

8.5 Current Consumption Summary

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER	TEST CONDITIONS[1] [2]		MIN	TYP	MAX	UNIT
TX	1 DSSS	TX power level = 0		272		mA
		TX power level = 4		188		
	6 OFDM	TX power level = 0		248		
		TX power level = 4		179		
	54 OFDM	TX power level = 0		223		
		TX power level = 4		160		
RX[5]	1 DSSS			53		mA
	54 OFDM			53		
Idle connected[3]				690		µA
LPDS				115		µA
Hibernate				4		µA
Shutdown				1		µA
Peak calibration current[4] [5]	V_{BAT} = 3.6 V			420		mA
	V_{BAT} = 3.3 V			450		
	V_{BAT} = 2.1 V			670		

(1) TX power level = 0 implies maximum power (see 图 8-1, 图 8-2, and 图 8-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) The CC3130 system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.
(3) DTIM = 1
(4) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see *CC3x20, CC3x35 SimpleLink™ Wi-Fi® and Internet of Things Network Processor Programmer's Guide*.
(5) The RX current is measured with a 1-Mbps throughput rate.

8.6 TX Power Control

The CC3130 has several options for modifying the output power of the device when required. It is possible to lower the overall output power at a global level using the global TX power level setting. In addition, the 2.4 GHz band allows the user to enter additional back-offs [1], per channel, region [2]and modulation rates [3], via Image creator (see the *UniFlash CC3x20, CC3x35 SimpleLink™ Wi-Fi® and Internet-on-a chip™ Solution ImageCreator and Programming Tool User's Guide* for more details).

图 8-1, 图 8-2, and 图 8-3 show TX power and IBAT versus TX power level settings for the CC3130 device at modulations of 1 DSSS, 6 OFDM, and 54 OFDM, respectively.

In 图 8-1, the area enclosed in the circle represents a significant reduction in current during transition from TX power level 3 to level 4. In the case of lower range requirements (14-dBm output power), TI recommends using TX power level 4 to reduce the current.

[1] The back-off range is between -6 dB to +6 dB in 0.25dB increments.
[2] FCC/ISED, ETSI (Europe), and Japan are supported.
[3] Back-off rates are grouped into 11b rates, high modulation rates (MCS7, 54 OFDM and 48 OFDM), and lower modulation rates (all other rates).

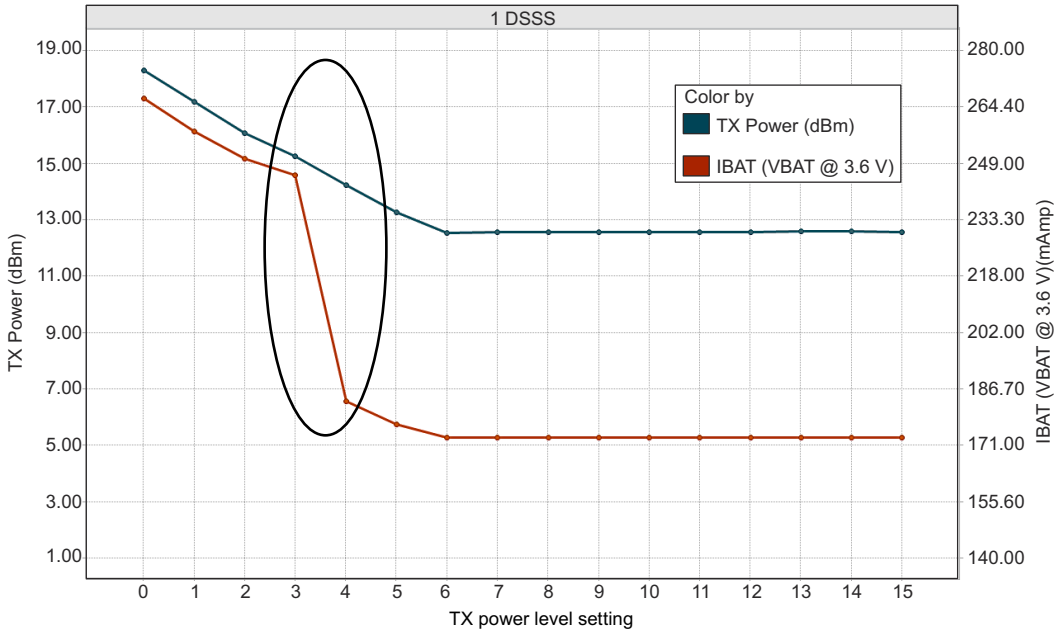


图 8-1. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

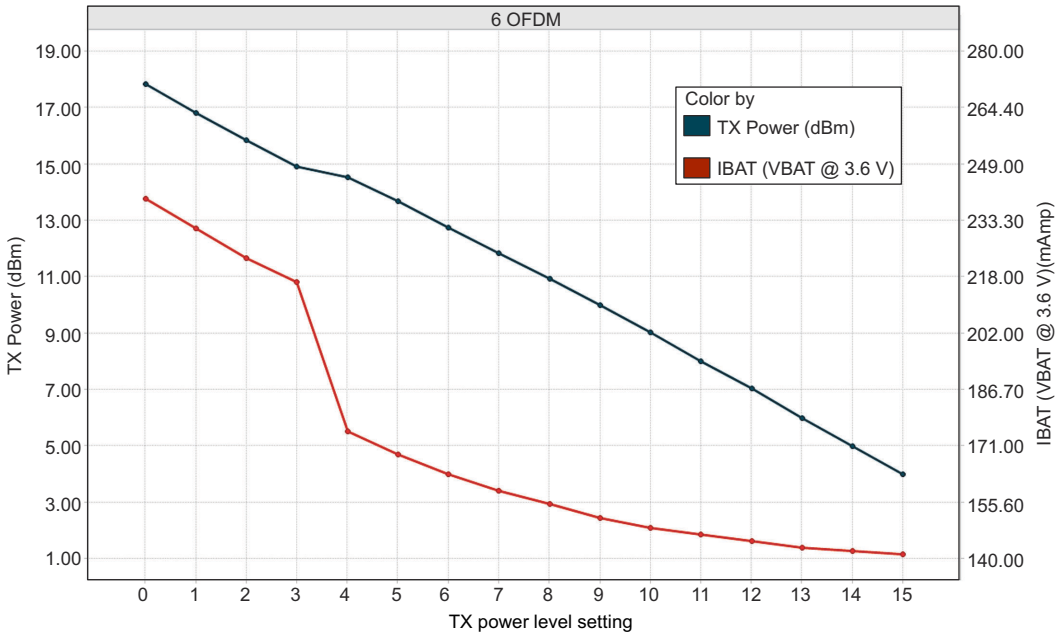


图 8-2. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

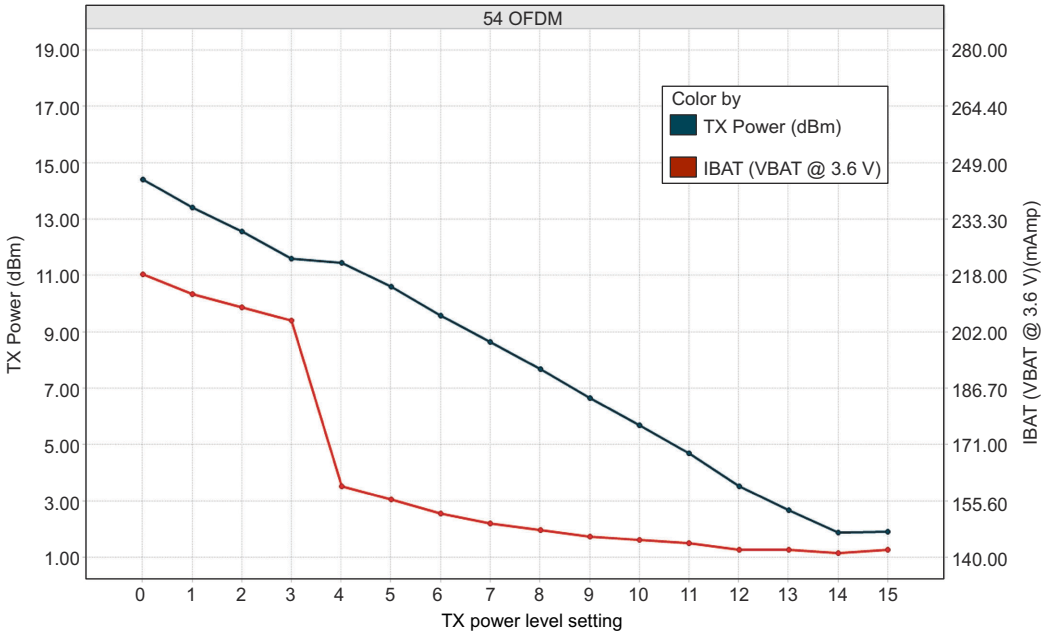


图 8-3. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

8.7 Brownout and Blackout Conditions

The device enters a brownout condition when the input voltage drops below $V_{brownout}$ (see 图 8-4 and 图 8-5). This condition must be considered during design of the power supply routing, especially when operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout condition. The resistance includes the internal resistance of the battery, the contact resistance of the battery holder (four contacts for 2× AA batteries), and the wiring and PCB routing resistance.

Note

When the device is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

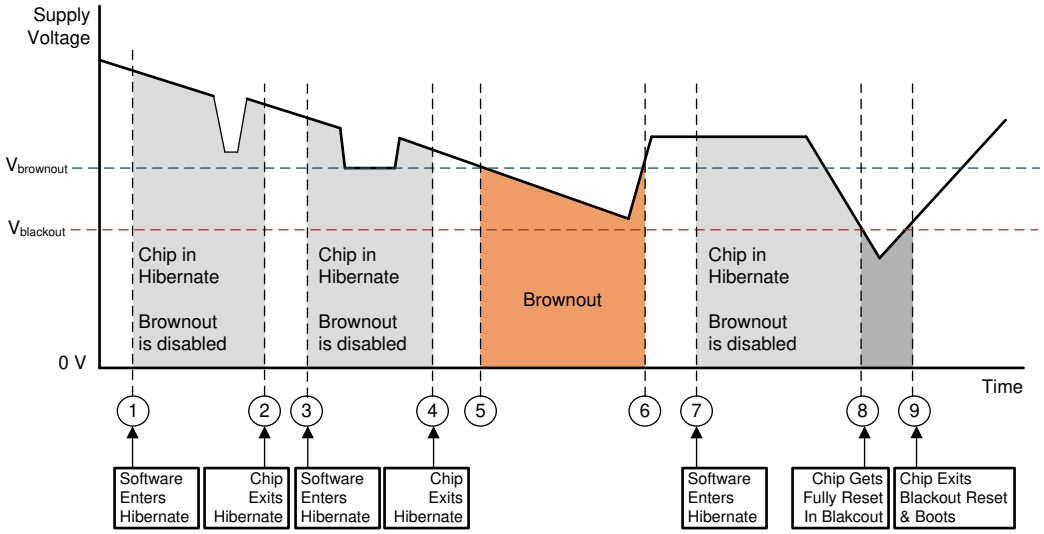


图 8-4. Brownout and Blackout Levels (1 of 2)

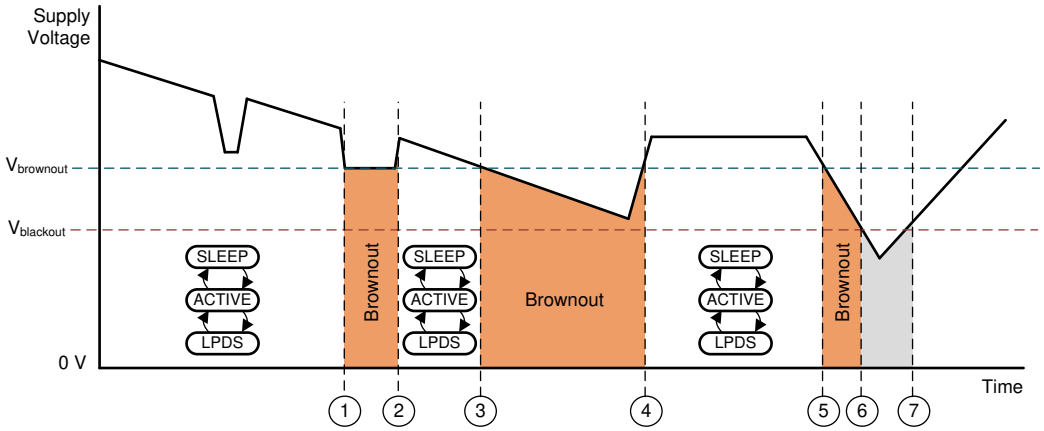


图 8-5. Brownout and Blackout Levels (2 of 2)

In the brownout condition, all sections of the device (including the 32-kHz RTC) shut down except for the Hibernate module, which remains on. The current in this state can reach approximately 400 µA. The blackout condition is equivalent to a hardware reset event in which all states within the device are lost.

节 8.7.1 lists the brownout and blackout voltage levels.

8.7.1 Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

8.8 Electrical Characteristics for DIO Pins

8.8.1 Electrical Characteristics: DIO Pins Except 52 and 53

T_A = 25°C, V_{BAT} = 2.1 V to 3.3 V.(1)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V			V_{DD} × 0.75	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V	V_{DD} × 0.25			
I_{OH}	High-level source current	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			

T_A = 25°C, V_{BAT} = 2.1 V to 3.3 V.(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Low-level sink current	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

8.8.2 Electrical Characteristics: DIO Pins 52 and 53

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V.(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Pin capacitance				7		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			– 0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				50		nA
I_{IL}	Low-level input current				50		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ⩽ V_{DD} < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ⩽ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ⩽ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ⩽ V_{DD} < 2.4 V			V_{DD} × 0.75	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ⩽ V_{DD} < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ⩽ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ⩽ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ⩽ V_{DD} < 2.4 V	V_{DD} × 0.25			
I_{OH}	High-level source current, V_{OH} = 2.4	2-mA drive		1.5			mA
		4-mA drive		2.5			
		6-mA drive		3.5			
I_{OL}	Low-level sink current	2-mA drive		1.5			mA
		4-mA drive		2.5			
		6-mA drive		3.5			

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V.(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	nRESET				0.6		V

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

8.9 Electrical Characteristics for Pin Internal Pullup and Pulldown

T_A = 25°C, V_{BAT} = 3.0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	Pullup current, V_{OH} = 2.4 (V_{DD} = 3.0 V)		5		10	µA
I_{OL}	Pulldown current, V_{OL} = 0.4 (V_{DD} = 3.0 V)		5			µA

8.10 WLAN Receiver Characteristics

表 8-1. WLAN Receiver Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters are measured at the SoC pin on channel 6 (2437 MHz).

PARAMETER	TEST CONDITIONS (Mbps)	MIN	TYP	MAX	UNIT
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)(2)	1 DSSS		–96.0		dBm
	2 DSSS		–94.0		
	11 CCK		–88.0		
	6 OFDM		–90.5		
	9 OFDM		–90.0		
	18 OFDM		–86.5		
	36 OFDM		–80.5		
	54 OFDM		–74.5		
	MCS7 (GF)(1)		–71.5		
Maximum input level (10% PER)	802.11b		–4.0		dBm
	802.11g		–10.0		

(1) Sensitivity for mixed mode is 1-dB worse.
(2) Sensitivity is 1-dB worse on channel 13 (2472 MHz).

8.11 WLAN Transmitter Characteristics

表 8-2. WLAN Transmitter Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters measured at SoC pin on channel 6 (2437 MHz).(1) (2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating frequency range(3) (4)		2412		2472	MHz
Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		18.0		dBm
	2 DSSS		18.0		
	11 CCK		18.3		
	6 OFDM		17.3		
	9 OFDM		17.3		
	18 OFDM		17.0		
	36 OFDM		16.0		
	54 OFDM		14.5		
	MCS7		13.0		
Transmit center frequency accuracy		–25		25	ppm

(1) The OFDM and MCS7 edge channels (2412 and 2462 MHz) have reduced TX power to meet FCC emission limits.
(2) Power of 802.11b rates are reduced to meet ETSI requirements in Europe.
(3) Channels 1 (2142 MHz) through 11 (2462 MHz) are supported for FCC.
(4) Channels 1 (2142 MHz) through 13 (2472MHz) are supported for Europe and Japan. Note that channel 14 is not supported for Japan.

8.12 WLAN Transmitter Out-of-Band Emissions

The device requires an external band-pass filter to meet the various emission standards, including FCC. 节 8.12.1 presents the minimum attenuation requirements for the band-pass filter. TI recommends using the same filter used in the reference design to ease the process of certification.

8.12.1 WLAN 2.4 GHz Filter Requirements

PARAMETER	FREQUENCY (MHz)	MIN	TYP	MAX	UNIT
Return loss	2412 to 2484	10			dB
Insertion loss(1)	2412 to 2484		1	1.5	dB
Attenuation	804 to 828	30	42		dB
	1608 to 1656	20	23		
	3216 to 3312	30	49		
	4020 to 4140	40	52		
	4824 to 4968	20	30		
	5628 to 5796	20	27		
	6432 to 6624	20	42		
	7200 to 7500	35	44		
	7500 to 10000	20	30		
Reference impendence	2412 to 2484		50		Ω
Filter type	Bandpass				

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

8.13 BLE/2.4 GHz Radio Coexistence and WLAN Coexistence Requirements

For proper BLE/2.4 GHz radio coexistence, the following requirements needs to met:

表 8-3. COEX Isolation Requirement

PARAMETER	Band	MIN	TYP	MAX	UNIT
Port-to-port isolation	Single antenna	20(1)			dB
	Dual antenna Configuration	20(2)			

(1) WLAN/BLE switch used must provide a minimum of 20 dB isolation between ports.
(2) For dual antenna configuration antenna placement must be such that isolation between the BLE and WLAN ports is at least 20 dB.

8.14 Thermal Resistance Characteristics for RGK Package

THERMAL METRICS(1)		°C/W(2) (3)	AIR FLOW (m/s)(4)
$R_{\Theta JC}$	Junction-to-case	6.3	0.0051
$R_{\Theta JB}$	Junction-to-board	2.4	0.0051
$R_{\Theta JA}$	Junction-to-free air	23	0.0051
$R_{\Theta JMA}$	Junction-to-moving air	14.6	0.765
		12.4	1.275
		10.8	2.55
Psi_{JT}	Junction-to-package top	0.2	0.0051
		0.2	0.765
		0.3	1.275
		0.1	2.55
Psi_{JB}	Junction-to-board	2.3	0.0051
		2.3	0.765
		2.2	1.275
		2.4	2.55

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R_{\Theta JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.
(4) m/s = meters per second.

8.15 Timing and Switching Characteristics

8.15.1 Power Supply Sequencing

For proper operation of the CC3130 device, perform the recommended power-up sequencing as follows:

1. Tie the following pins together on the board:
   - V_{BAT} (pins 37, 39, and 44)
   - V_{IO} (pins 54 and 10)
2. Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100 K ||, 0.01 µF, RC = 1 ms).
3. For an external RTC, ensure that the clock is stable before RESET is deasserted (high).

For timing diagrams, see 节 8.15.3.

8.15.2 Device Reset

When a device restart is required, the user may issue a negative pulse to the nRESET pin. The user must follow one of the following alternatives to ensure the reset is properly applied:

- A negative reset pulse (on pin 32) of at least 200-ms duration
- If the 200-ms pulse duration cannot be ensured, a pulldown resistor of 2 MΩ must be connected to pin 52 (RTC_XTAL_N). If implemented, a shorter pulse of at least 100 µs can be used.

To ensure a proper reset sequence, the user must call the sl_stop function prior to toggling the reset. When a reset is required, it is preferable to use the software reset instead of an external trigger.

8.15.3 Reset Timing

8.15.3.1 nRESET (32-kHz Crystal)

图 8-6 shows the reset timing diagram for the 32-kHz crystal first-time power-up and reset removal.

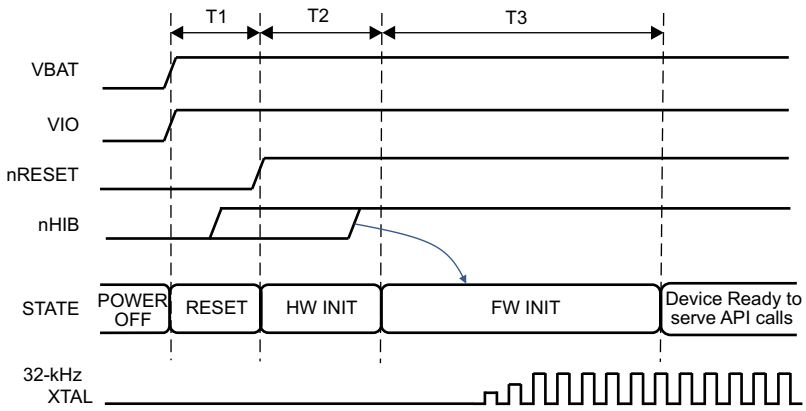


图 8-6. First-Time Power-Up and Reset Removal Timing Diagram (32-kHz Crystal)

节 8.15.3.2 describes the timing requirements for the 32-kHz crystal first-time power-up and reset removal.

8.15.3.2 First-Time Power-Up and Reset Removal Timing Requirements (32-kHz Crystal)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	nReset time	nReset timing after VBAT and VIO supply are stable		1		ms
T2	Hardware wake-up time			25		ms
T3	Initialization time	32-kHz crystal settling plus firmware initialization time plus radio calibration		1.35		s

8.15.3.3 nRESET (External 32-kHz Crystal)

图 8-7 shows the reset timing diagram for the external 32-kHz crystal first-time power-up and reset removal.

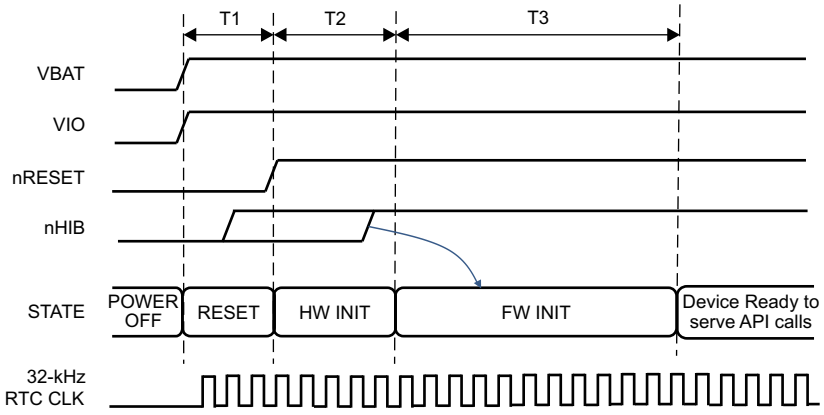


图 8-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32-kHz Crystal)

节 8.15.3.3.1 describes the timing requirements for the external first-time power-up and reset removal.

8.15.3.3.1 First-Time Power-Up and Reset Removal Timing Requirements (External 32-kHz Crystal)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	nReset time	nReset timing after VBAT and VIO supply are stable		1		ms
T2	Hardware wake-up time			25		ms
T3	Initialization time	Firmware initialization time plus radio calibration		250		ms

8.15.4 Wakeup From HIBERNATE Mode

Note

The 32.768-kHz crystal is kept enabled by default when the chip goes into HIBERNATE mode in response to nHIB being pulled low.

图 8-8 shows the timing diagram for wakeup from HIBERNATE mode.

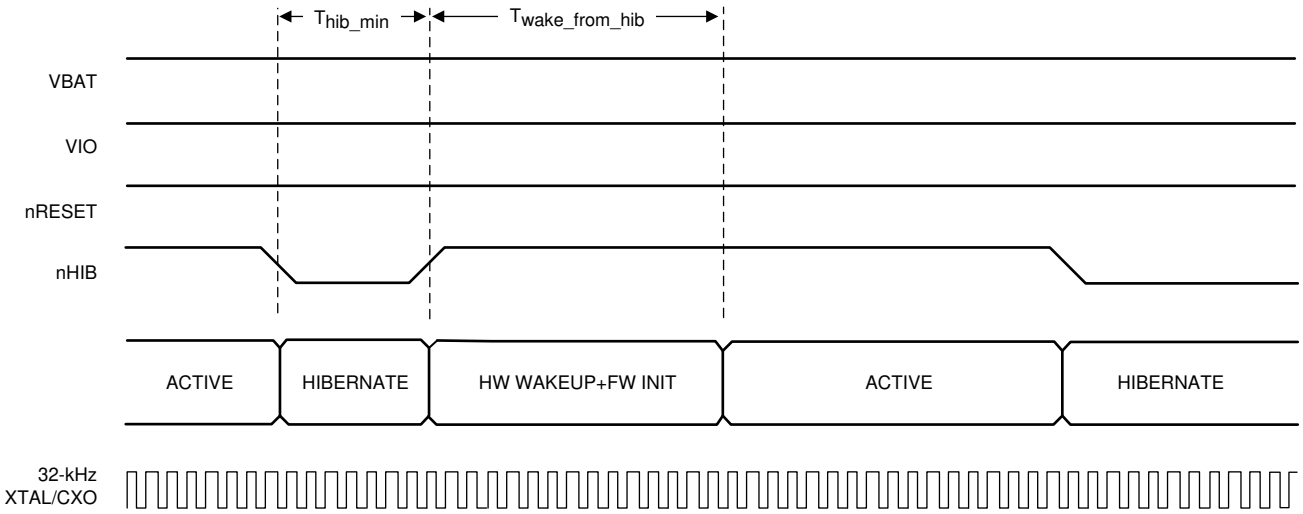


图 8-8. nHIB Timing Diagram

节 8.15.4.1 describes the timing requirements for nHIB.

8.15.4.1 nHIB Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{hib_min}	Minimum hibernate time	Minimum pulse width of nHIB being low(2)	10			ms
$T_{wake\_from\_hib}$	Hardware wakeup time plus firmware initialization time	See(1)		50		ms

(1) If temperature changes by more than 20°C, initialization time from HIB can increase by 200 ms due to radio calibration.
(2) Ensure that the nHIB pulse width is kept above the minimum requirement under all conditions (such as power up, MCU reset, and so on).

8.15.5 Clock Specifications

The CC3130 device requires two separate clocks for its operation:

- A slow clock running at 32.768 kHz is used for the RTC.
- A fast clock running at 40 MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators that enable the use of less-expensive crystals rather than dedicated TCXOs for these clocks. The RTC can also be fed externally to provide reuse of an existing clock on the system and to reduce overall cost.

8.15.5.1 Slow Clock Using Internal Oscillator

The RTC crystal connected on the device supplies the free-running slow clock. The accuracy of the slow clock frequency must be 32.768 kHz ±150 ppm. In this mode of operation, the crystal is tied between RTC_XTAL_P (pin 51) and RTC_XTAL_N (pin 52) with a suitable load capacitance to meet the ppm requirement.

图 8-9 shows the crystal connections for the slow clock.

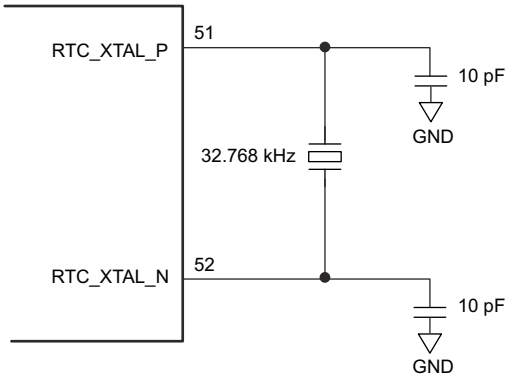


图 8-9. RTC Crystal Connections

节 8.15.5.1.1 lists the RTC crystal requirements.

8.15.5.1.1 RTC Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			32.768		kHz
Frequency accuracy	Initial plus temperature plus aging			±150	ppm
Crystal ESR	32.768 kHz			70	kΩ

8.15.5.2 Slow Clock Using an External Clock

When an RTC oscillator is present in the system, the CC3130 device can accept this clock directly as an input. The clock is fed on the RTC_XTAL_P line, and the RTC_XTAL_N line is held to V_{IO}. The clock must be a CMOS-level clock compatible with V_{IO} fed to the device.

图 8-10 shows the external RTC input connection.

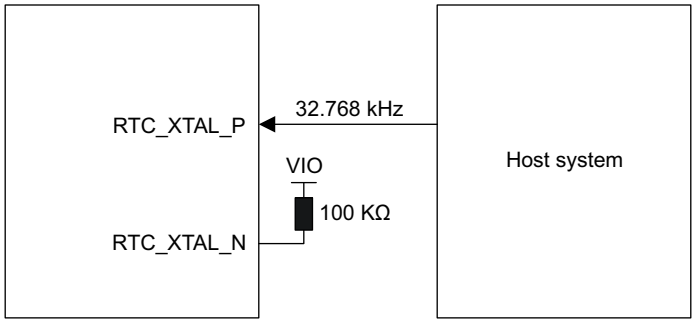


图 8-10. External RTC Input

节 8.15.5.2.1 lists the external RTC digital clock requirements.

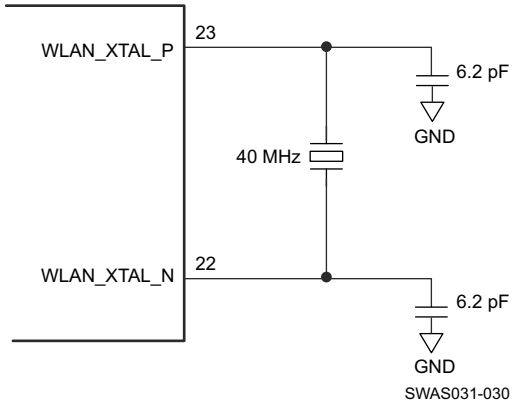
8.15.5.2.1 External RTC Digital Clock Requirements

CHARACTERISTICS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency				32768		Hz
	Frequency accuracy (Initial plus temperature plus aging)				±150		ppm
t_r, t_f	Input transition time t_r, t_f (10% to 90%)					100	ns
	Frequency input duty cycle			20%	50%	80%	
V_{ih}	Slow clock input voltage limits		Square wave, DC coupled	0.65 × V_{IO}		V_{IO}	V
V_{il}				0		0.35 × V_{IO}	V_{peak}
	Input impedance	Resistance		1			MΩ
		Capacitance				5	pF

8.15.5.3 Fast Clock (F_{ref}) Using an External Crystal

The CC3130 device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The crystal is fed directly between WLAN_XTAL_P (pin 23) and WLAN_XTAL_N (pin 22) with suitable loading capacitors.

图 8-11 shows the crystal connections for the fast clock.



A. The crystal capacitance must be tuned to ensure that the PPM requirement is met. See *CC31xx & CC32xx Frequency Tuning* for information on frequency tuning.

图 8-11. Fast Clock Crystal Connections

节 8.15.5.3.1 lists the WLAN fast-clock crystal requirements.

8.15.5.3.1 WLAN Fast-Clock Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			40		MHz
Frequency accuracy	Initial plus temperature plus aging			±20	ppm
Crystal ESR	40 MHz			60	Ω

8.15.5.4 Fast Clock (F_{ref}) Using an External Oscillator

The CC3130 device can accept an external TCXO/XO for the 40-MHz clock. In this mode of operation, the clock is connected to WLAN_XTAL_P (pin 23). WLAN_XTAL_N (pin 22) is connected to GND. The external TCXO/XO can be enabled by TCXO_EN (pin 21) from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

图 8-12 shows the connection.

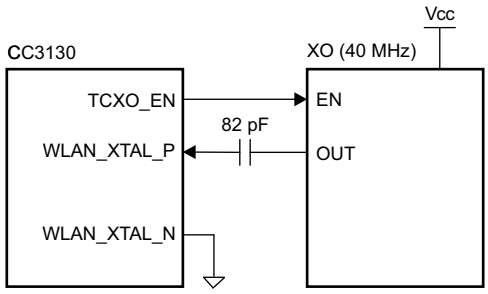


图 8-12. External TCXO Input

节 8.15.5.4.1 lists the external F_{ref} clock requirements.

8.15.5.4.1 External F_{ref} Clock Requirements (– 40°C to +85°C)

CHARACTERISTICS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency				40.00		MHz
	Frequency accuracy (Initial plus temperature plus aging)					±20	ppm
	Frequency input duty cycle			45%	50%	55%	
V_{pp}	Clock voltage limits		Sine or clipped sine wave, AC coupled	0.7		1.2	V_{pp}
	Phase noise at 40 MHz		at 1 kHz			– 125	dBc/Hz
			at 10 kHz			– 138.5	
			at 100 kHz			– 143	
	Input impedance	Resistance		12			kΩ
		Capacitance				7	pF

8.15.6 Interfaces

This section describes the interfaces that are supported by the CC3130 device:

- Host SPI
- Flash SPI
- Digital IO

8.15.6.1 Host SPI Interface Timing

图 8-13 shows the Host SPI interface timing diagram.

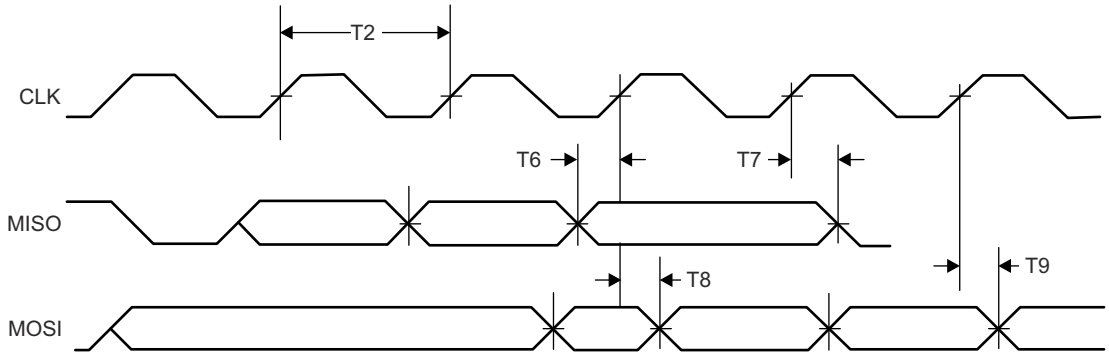


图 8-13. Host SPI Interface Timing

节 8.15.6.1.1 lists the Host SPI interface timing parameters.

8.15.6.1.1 Host SPI Interface Timing Parameters

PARAMETER NUMBER	DESCRIPTION		MIN	MAX	UNIT
T1	F(1)	Clock frequency at V_{BAT} = 3.3 V		20	MHz
		Clock frequency at V_{BAT} ⩽ 2.1 V		12	
T2	t_{clk} (1) (2)	Clock period	50		ns
T3	t_{LP} (1)	Clock low period		25	ns
T4	t_{HT} (1)	Clock high period		25	ns
T5	D(1)	Duty cycle	45%	55%	
T6	t_{IS} (1)	RX data setup time	4		ns
T7	t_{IH} (1)	RX data hold time	4		ns
T8	t_{OD} (1)	TX data output delay		20	ns
T9	t_{OH} (1)	TX data hold time		24	ns

(1) The timing parameter has a maximum load of 20 pF at 3.3 V.
(2) Ensure that nCS (active-low signal) is asserted 10 ns before the clock is toggled. nCS can be deasserted 10 ns after the clock edge.

8.15.6.2 Flash SPI Interface Timing

图 8-14 shows the Flash SPI interface timing diagram.

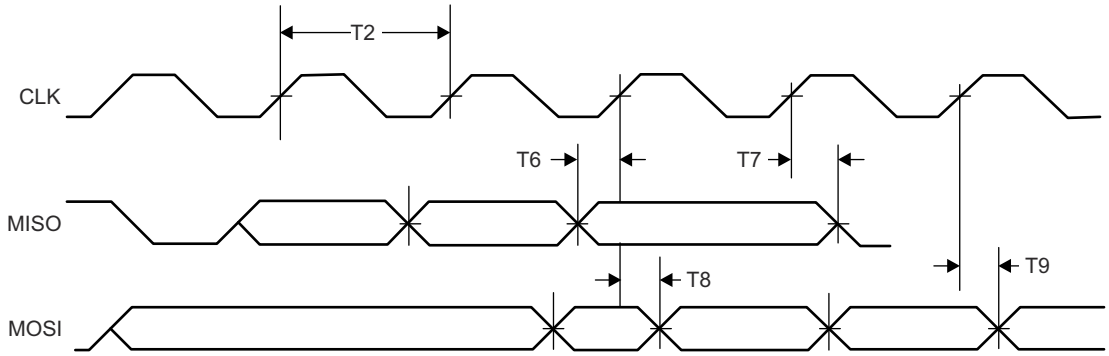


图 8-14. Flash SPI Interface Timing

节 8.15.6.2.1 lists the Flash SPI interface timing parameters.

8.15.6.2.1 Flash SPI Interface Timing Parameters

PARAMETER NUMBER	DESCRIPTION		MIN	MAX	UNIT
T1	F	Clock frequency		20	MHz
T2	t_{clk}	Clock period	50		ns
T3	t_{LP}	Clock low period		25	ns
T4	t_{HT}	Clock high period		25	ns
T5	D	Duty cycle	45%	55%	
T6	t_{IS}	RX data setup time	1		ns
T7	t_{IH}	RX data hold time	2		ns
T8	t_{OD}	TX data output delay		8.5	ns
T9	t_{OH}	TX data hold time		8	ns

8.15.6.3 DIO Interface Timing

Note

Digital IOs on CC3130 refers to antenna select, hostless mode, and BLE/2.4 GHz coexistence IOs not general purpose IOs

图 8-15 shows the DIO timing diagram.

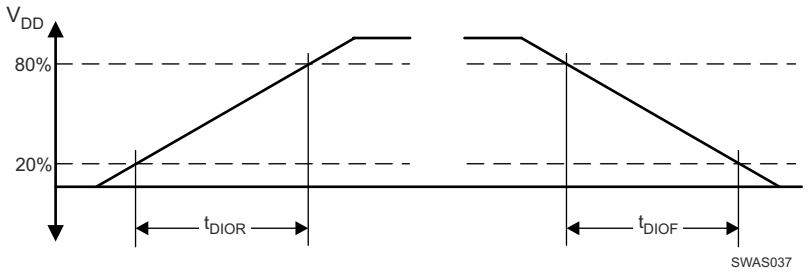


图 8-15. DIO Timing Diagram

8.15.6.3.1 DIO Output Transition Time Parameters (V_{supply} = 3.3 V)

节 8.15.6.3.1.1 lists the DIO output transition times for V_{supply} = 3.3 V.

8.15.6.3.1.1 DIO Output Transition Times (V_{supply} = 3.3 V)[1]

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	t_r			t_f			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
2[2]	2MA_EN=1	8.0	9.3	10.7	8.2	9.5	11.0	ns
	4MA_EN=0							
4[2]	2MA_EN=0	6.6	7.1	7.6	4.7	5.2	5.8	ns
	4MA_EN=1							
6	2MA_EN=1	3.2	3.5	3.7	2.3	2.6	2.9	ns
	4MA_EN=1							

(1) V_{supply} = 3.3 V, T = 25°C, total pin load = 30 pF
(2) The 2-mA and 4-mA drive strength does not apply to the COEX I/O pins. Pins configured as COEX lines are invariably driven at 6 mA.

8.15.6.3.2 DIO Input Transition Time Parameters

节 8.15.6.3.2.1 lists the input transition time parameters.

8.15.6.3.2.1 DIO Input Transition Time Parameters

PARAMETERS		MIN	MAX	UNIT
t_r	Input transition time (t_r, t_f), 10% to 90%	1	3	ns
t_f		1	3	ns

8.16 External Interfaces

8.16.1 SPI Flash Interface

The external serial Flash stores the user profiles and firmware patch updates. The CC3130 device acts as a master in this case; the SPI serial Flash acts as the slave device. This interface can work up to a speed of 20 MHz.

图 8-16 shows the SPI Flash interface.

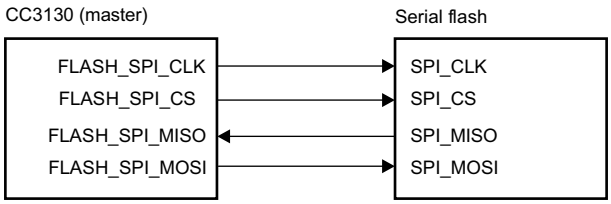


图 8-16. SPI Flash Interface

表 8-4 lists the SPI Flash interface pins.

表 8-4. SPI Flash Interface

PIN NAME	DESCRIPTION
FLASH_SPI_CLK	Clock (up to 20 MHz) CC3130 device to serial Flash
FLASH_SPI_CS	CS signal from CC3130 device to serial Flash
FLASH_SPI_MISO	Data from serial Flash to CC3130 device
FLASH_SPI_MOSI	Data from CC3130 device to serial Flash

8.16.2 SPI Host Interface

The device interfaces to an external host using the SPI interface. The CC3130 device can interrupt the host using the HOST_INTR line to initiate the data transfer over the interface. The SPI host interface can work up to a speed of 20 MHz.

图 8-17 shows the SPI host interface.

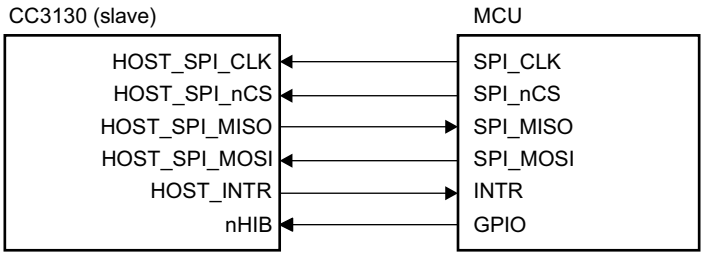


图 8-17. SPI Host Interface

表 8-5 lists the SPI host interface pins.

表 8-5. SPI Host Interface

PIN NAME	DESCRIPTION
HOST_SPI_CLK	Clock (up to 20 MHz) from MCU host to CC3130 device
HOST_SPI_nCS	CS (active low) signal from MCU host to CC3130 device
HOST_SPI_MOSI	Data from MCU host to CC3130 device
HOST_INTR	Interrupt from CC3130 device to MCU host
HOST_SPI_MISO	Data from CC3130 device to MCU host
nHIB	Active-low signal that commands the CC3130 device to enter hibernate mode (lowest power state)

8.16.3 Host UART Interface

The SimpleLink device requires the UART configuration described in 表 8-6.

表 8-6. SimpleLink™ UART Configuration

PROPERTY	SUPPORTED CC3130 CONFIGURATION
Baud rate	115200 bps, no auto-baud rate detection, can be changed by the host up to 3 Mbps using a special command
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	LSBit first
Host interrupt polarity	Active high
Host interrupt mode	Rising edge or level 1
Endianness	Little-endian only(1)

(1) The SimpleLink device does not support automatic detection of the host length while using the UART interface.

8.16.3.1 5-Wire UART Topology

图 8-18 shows the typical 5-wire UART topology comprised of four standard UART lines plus one IRQ line from the device to the host controller to allow efficient low-power mode.

This topology is recommended because the configuration offers the maximum communication reliability and flexibility between the host and the SimpleLink device.

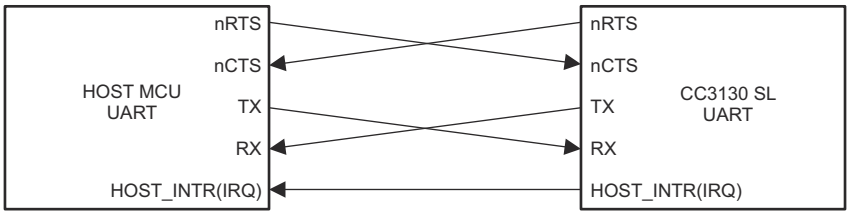


图 8-18. 5-Wire UART Topology

8.16.3.2 4-Wire UART Topology

The 4-wire UART topology eliminates the host IRQ line (see 图 8-19). Using this topology requires meeting one of the following conditions:

- The host is always awake or active.
- The host goes to sleep, but the UART module has receiver start-edge detection for auto wakeup and does not lose data.

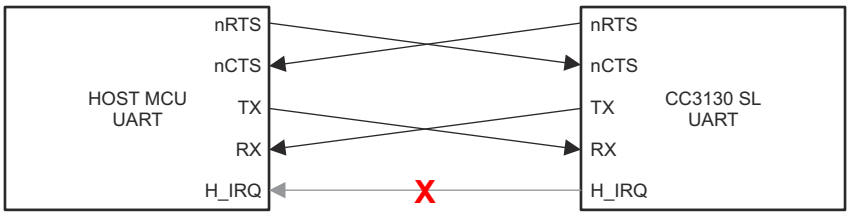


图 8-19. 4-Wire UART Configuration

8.16.3.3 3-Wire UART Topology

The 3-wire UART topology requires only the following lines (see 图 8-20):

- RX
- TX
- CTS

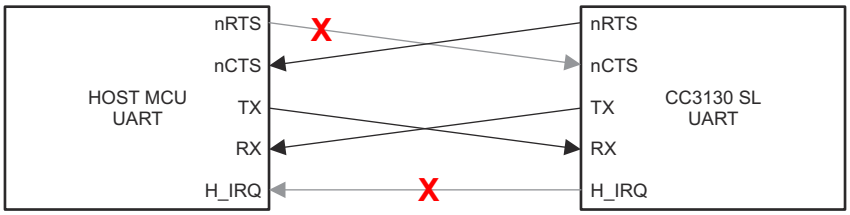


图 8-20. 3-Wire UART Topology

Using this topology requires meeting one of the following conditions:

- The host always stays awake or active.
- The host goes to sleep but the UART module has receiver start-edge detection for auto-wake-up and does not lose data.
- The host can always receive any amount of data transmitted by the SimpleLink™ device because there is no flow control in this direction.

Because there is no full flow control, the host cannot stop the SimpleLink™ device to send its data; thus, the following parameters must be carefully considered:

- Maximum baud rate
- RX character interrupt latency and low-level driver jitter buffer
- Time consumed by the user's application

9 Detailed Description

9.1 Overview

Connect any microcontroller (MCU) to the Internet of Things (IoT) with the CC3130 device from Texas Instruments™. The CC3130 Wi-Fi® Internet-on-a chip™ device contains an Arm® Cortex®-M3 MCU dedicated to wi-fi and internet protocols, in order to offload networking activities from the host MCU. The subsystem includes an 802.11b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure Internet connections with 256-bit encryption and a built in power management for best in class low power performance. The CC3130 device supports station, AP, and Wi-Fi Direct® modes. The device also supports WPA2™ personal and enterprise security, WPS 2.0, and WPA3™ personal and enterprise security [4]. The Wi-Fi network processor includes an embedded IPv6 and IPv4 TCP/IP stack.

9.2 Device Features

9.2.1 WLAN

The WLAN features are as follows:

- 802.11b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, Wi-Fi Direct client, and group owner with CCK and OFDM rates in the 2.4 GHz band (channels 1 through 13).

  Note

  802.11n is supported only in Wi-Fi® station and Wi-Fi Direct®.

- The automatically calibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in serial flash allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators, including: WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x), WPA3 Personal and WPA3 Enterprise.
- Smart provisioning options deeply integrated within the device providing a comprehensive end-to-end solution. With elaborate events notification to the host, enabling the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point with HTTP server
  - WPS - Wi-Fi Protected Setup, supporting both push button and pin code options.
  - SmartConfig™ Technology: TI proprietary, easy to use, one-step, one-time process used to connect a CC3130-enabled device to the home wireless network.
- 802.11 transceiver mode allows transmitting and receiving of proprietary data through a socket The 802.11 transceiver mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works with the filtering options.
- Antenna selection for best connection
- BLE/2.4 GHz radio coexistence mechanism to avoid interference

[4] Supported from Service Pack v4.5.0.11-3.1.0.5-3.1.0.25. Limited to STA mode only.

9.2.2 Network Stack

The Network Stack features are as follows:

- Integrated IPv4, IPv6 TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

Note

Not all APIs are 100% BSD compliant. Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, RAW, SSL\TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 with DAD and stateless autoconfiguration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet
- Built-in network applications and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial flash
    - RESTful APIs for setting and configuring application content
    - Dynamic user callbacks
  - Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3130 device provides critical information, such as device name, IP, vendor, and port number.
  - DHCP server
  - Ping

表 9-1 describes the NWP features.

表 9-1. NWP Features

Feature	Description
Wi-Fi standards	802.11b/g/n station 802.11b/g AP supporting up to four stations Wi-Fi Direct client and group owner
Wi-Fi channels	2.4 GHz ISM
Channel Bandwidth	20 MHz
Wi-Fi security	WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x), WPA3 personal and enterprise (1)
Wi-Fi provisioning	SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP web server
IP protocols	IPv4/IPv6
IP addressing	Static IP, LLA, DHCPv4, DHCPv6 with DAD
Cross layer	ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP
Transport	UDP, TCP SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2 RAW
Network applications and utilities	Ping HTTP/HTTPS web server mDNS DNS-SD DHCP server
Host interface	UART/SPI

表 9-1. NWP Features (continued)

Feature	Description
Security	Device identity Trusted root-certificate catalog TI root-of-trust public key
Power management	Enhanced power policy management uses 802.11 power save and deep-sleep power modes
Other	Transceiver Programmable RX filters with event-trigger mechanism Rx Metrics for tracking the surrounding RF environment

(1) Supported from Service Pack v4.5.0.11-3.1.0.5-3.1.0.25. Limited to STA mode only.

9.2.3 Security

The SimpleLink Wi-Fi CC3130 Internet-on-a chip device enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

Code and Data Security:

- Secured network information: Network passwords and certificates are encrypted
- Secured and authenticated service pack: SP is signed based on TI certificate

Wi-Fi and Internet Security:

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0 MSCHAPv2
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2
- Secure HTTP server (HTTPS)
- The Trusted root-certificate catalog verifies that the CA used by the application is trusted and known secure content delivery
- The TI root-of-trust public key is a hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery allows file transfer to the system in a secure way on any unsecured tunnel
- Secure sockets
  - Protocol versions: SSL v3/TLS 1.0/TLS 1.1/TLS 1.2
  - On-chip powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA

- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
- SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256
- SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA
- SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
- SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384
- SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
- SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
- SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256

– Server authentication
– Client authentication
– Domain name verification
– Socket upgrade to secure socket – STARTTLS

9.2.4 Host Interface and Driver

- Interfaces over a 4-wire serial peripheral interface (SPI) with any MCU or a processor at a clock speed of 20 MHz.
- Interfaces over UART with any MCU with a baud rate up to 3 Mbps. A low footprint driver is provided for TI MCUs and is easily ported to any processor or ASIC.
- Simple APIs enable easy integration with any single-threaded or multithreaded application.

9.2.5 System

- Works from a single preregulated power supply or connects directly to a battery
- Ultra-low leakage when disabled (hibernate mode) with a current of less than 4 µA with the RTC running
- Integrated clock sources

9.3 Power-Management Subsystem

The CC3130 power-management subsystem contains DC/DC converters to accommodate the different voltage or current requirements of the system.

- Digital DC/DC (Pin 44): Input: V_{BAT} wide voltage (2.1 to 3.6 V)
- ANA1 DC/DC (Pin 38): Input: V_{BAT} wide voltage (2.1 to 3.6 V)
- PA DC/DC (Pin 39): Input: V_{BAT} wide voltage (2.1 to 3.6 V)

The CC3130 device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the device to operate from a wide variety of input sources. For maximum flexibility, the device can operate in the modes described in 节 9.3.1.

9.3.1 V_{BAT} Wide-Voltage Connection

In the wide-voltage battery connection, the device is powered directly by the battery or preregulated 3.3-V supply. All other voltages required to operate the device are generated internally by the DC/DC converters. This scheme supports wide-voltage operation from 2.1 to 3.6 V and is thus the most common mode for the device.

9.4 Low-Power Operating Modes

This section describes the low-power modes supported by the device to optimize battery life.

9.4.1 Low-Power Deep Sleep

The low-power deep-sleep (LPDS) mode is an energy-efficient and transparent sleep mode that is entered automatically during periods of inactivity based on internal power optimization algorithms. The device can wake up in less than 3 ms from the internal timer or from any incoming host command. Typical battery drain in this mode is 115 µA. During LPDS mode, the device retains the software state and certain configuration information. The operation is transparent to the external host; thus, no additional handshake is required to enter or exit LPDS mode. Advanced features of long sleep interval and IoT low power for extending LPDS time for up to 22 seconds while maintaining Wi-Fi connection is also supported

9.4.2 Hibernate

The hibernate mode is the lowest power mode in which all of the digital logic is power-gated. Only a small section of the logic powered directly by the main input supply is retained. The RTC is kept running and the device wakes up once the nHIB line is asserted by the host driver. The wake-up time is longer than LPDS mode at approximately 50 ms. The typical battery drain in this mode is 4.5 µA.

Note

Wake-up time can be extended depending on the service-pack size.

9.4.3 Shutdown

The shutdown mode is the lowest power-mode system-wise. All device logics are off, including the real-time clock (RTC). The wake-up time in this mode is longer than hibernate at approximately 1.1 s. The typical battery drain in this mode is 1 µA.

9.5 Memory

9.5.1 External Memory Requirements

The CC3130 device maintains a proprietary file system on the sFLASH. The CC3130 file system stores the service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always at the beginning of the sFLASH. The applications microcontroller must access the sFLASH memory area allocated to the file system directly through the CC3130 file system. The applications microcontroller must not access the sFLASH memory area directly.

The file system manages the allocation of sFLASH blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on sFLASH using human-readable filenames rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system.

All file types can have a maximum of 100 supported files in the file system. All files are stored in 4-KB blocks and thus use a minimum of 4KB of Flash space. Fail-safe files require twice the original size and use a minimum of 8KB. Encrypted files are counted as fail-safe in terms of space. The maximum file size is 1MB.

表 9-2 lists the minimum required memory consumption under the following assumptions:

- System files in use consume 64 blocks (256KB).
- Vendor files are not taken into account.
- Gang image:
  - Storage for the gang image is rounded up to 32 blocks (meaning 128-KB resolution).
  - Gang image size depends on the actual content size of all components. Additionally, the image should be 128-KB aligned so unaligned memory is considered lost. Service pack, system files, and the 128-KB aligned memory are assumed to occupy 256KB.
- All calculations consider that the restore-to-default is enabled.

表 9-2. Recommended Flash Size

ITEM	CC3130 [KB]
File system allocation table	20
System and configuration files	256
Service Pack	264
Gang image size	256
Total	796
Minimal Flash size	8MBit
Recommended Flash size	16MBit

Note

The maximum supported serial flash size is 32MB (256Mb) (see the *Using Serial Flash on CC3135 and CC3235x SimpleLink™ Wi-Fi® and Internet-of-Things Devices application report*).

9.6 Restoring Factory Default Configuration

The device has an internal recovery mechanism that allows rolling back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the sFLASH in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None – no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by pulling or forcing SOP[2:0] = 110 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial Flash vendor.

9.7 Hostless Mode

The SimpleLink™ Wi-Fi® CC3130 device incorporates a scripting ability that enables offloading of simple tasks from the host processor. Using simple and conditional scripts, repetitive tasks can be handled internally, which allows the host processor to remain in a low-power state. In some cases where the scripter is being used to send packets, it reduces code footprint and memory consumption. The *if-this-then-that* style conditioning can include anything from GPIO toggling to transmitting packets.

The conditional scripting abilities can be divided into conditions and actions. The conditions define when to trigger actions. Only one action can be defined per condition, but multiple instances of the same condition may be used, so in effect multiple actions can be defined for a single condition. In total, 16 condition and action pairs can be defined. The conditions can be simple, or complex using sub-conditions (using a combinatorial AND condition between them). The actions are divided into two types, those that can occur during runtime and those that can occur only during the initialization phase.

The following actions can only be performed when triggered by the pre-initialization condition:

- Set roles AP, station, P2P, and Tag modes
- Delete all stored profiles
- Set connection policy
- Hardware GPIO indication allows an I/O to be driven directly from the WLAN core hardware to indicate internal signaling

The following actions may be activated during runtime:

- Send transceiver packet
- Send UDP packet
- Send TCP packet
- Increment counter increments one of the user counters by 1
- Set counter allows setting a specific value to a counter
- Timer control
- Set GPIO allows GPIO output from the device using the internal networking core
- Enter Hibernate state

Note

Consider the following limitations:

- Timing cannot be ensured when using the network scripter because some variable latency will apply depending on the utilization of the networking core.
- The scripter is limited to 16 pairs of conditions and reactions.
- Both timers and counters are limited to 8 instances each. Timers are limited to a resolution of 1 second. Counters are 32 bits wide.
- Packet length is limited to the size of one packet and the number of possible packet tokens is limited to 8.

10 Applications, Implementation, and Layout

Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 BLE/2.4 GHz Radio Coexistence

The CC3130 device is designed to support BLE/2.4 GHz radio coexistence. Because WLAN is inherently more tolerant to time-domain disturbances, the coexistence mechanism gives priority to the Bluetooth® low energy entity over the WLAN.

The following coexistence modes can be configured by the user:

- Off mode or intrinsic mode
  - No BLE/2.4 GHz radio coexistence, or no synchronization between WLAN and Bluetooth® low energy—in case Bluetooth® low energy exists in this mode, collisions can randomly occur.
- Time division multiplexing (TDM, single antenna)
  - In this mode, (see 图 10-1) the two entities share the antenna through an RF switch using two GPIOs (one input and one output from the WLAN perspective).
- Time division multiplexing (TDM, dual antenna)
  - in this mode, (see 图 10-2) the two entities have separate antennas, No RF switch is required and only a single GPIO (on input from the WLAN persective).

图 10-1 shows the single antenna implementation of a complete Bluetooth® low energy and WLAN coexistence network. The Coex switch is controlled by a GPIO signal from the BLE device and a GPIO signal from the CC3130 device.

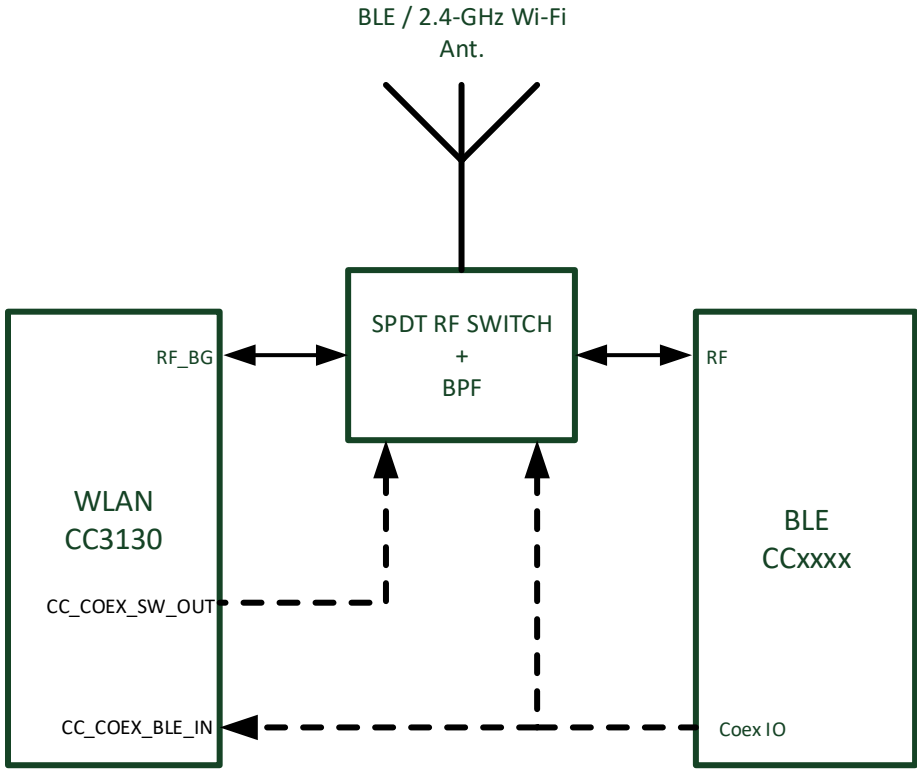


图 10-1. Single-Antenna Coexistence Mode Block Diagram

图 10-2 shows the dual antenna implementation of a complete Bluetooth low energy and WLAN coexistence network. Note in this implementation no Coex switch is required and only a single GPIO from the BLE device to the CC3130 device is required.

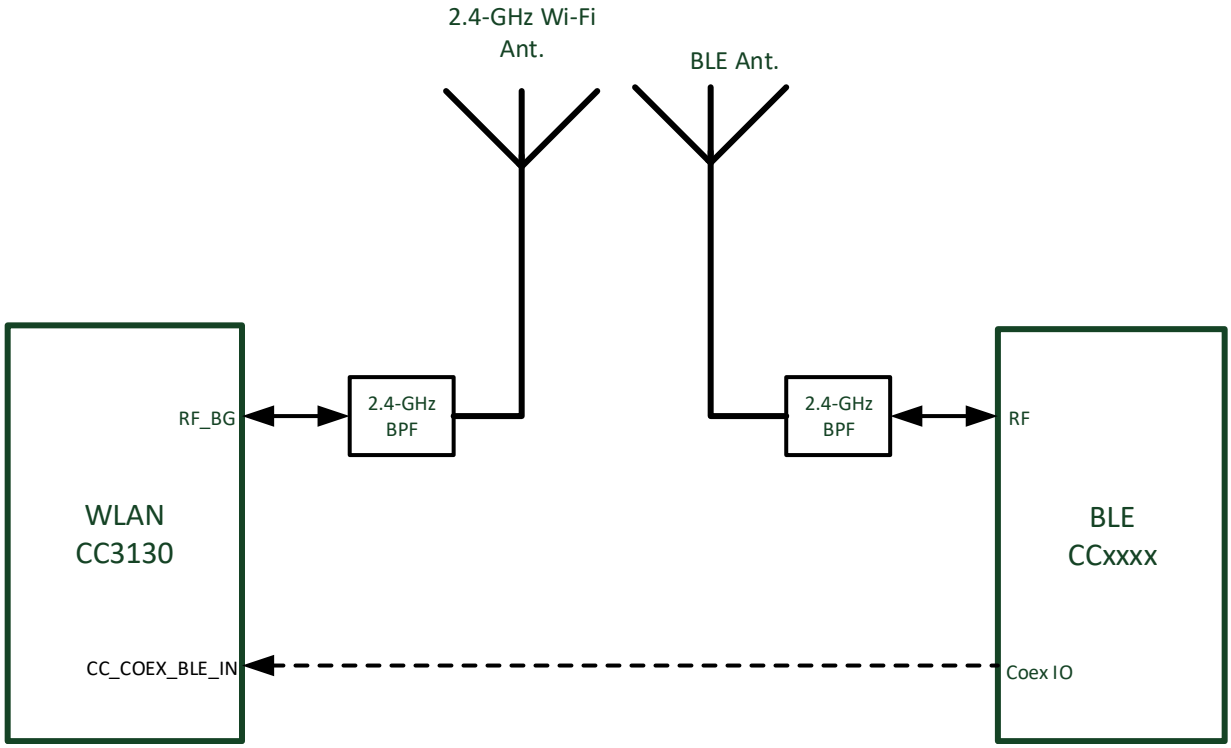


图 10-2. Dual-Antenna Coexistence Mode Block Diagram

10.1.2 Antenna Selection

The CC3130 device is designed to also support antenna selection and is controlled from Image Creator. When enabled, there are 3 options possible options:

- ANT 1: When selected, the GPIOs that are defined for antenna selection with set the RF path for antenna 1.
- ANT 2: When selected, the GPIOs that are defined for antenna selection will set the RF path for antenna 2.
- Autoselect: When selected, during a scan and prior to connecting to an AP, CC3130 device will determine the best RF path and select the appropriate antenna [5] [6]. The result is the saved as port of the profile.

图 10-3 shows the implementation of a complete Bluetooth® low energy and WLAN coexistence network with WLAN and antenna selection. The Coex switch is controlled by a GPIO signal from the BLE device and a GPIO signal from the CC3130 device. The antenna switch is controlled by 2 GPIO lines from the CC3130 device.

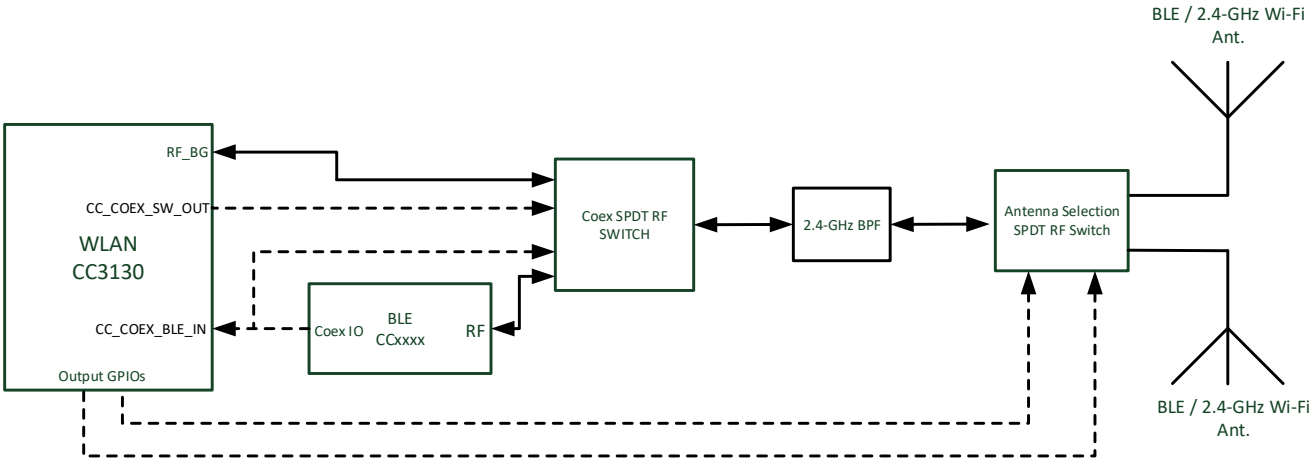


图 10-3. Antenna Selection Solution With Coexistence

[5] When selecting Autoselect via the API, a reset is required in order for the CC3230x device to determine the best antenna for use.
[6] Refer to the *UniFlash CC3x20, CC3x35 SimpleLink™ Wi-Fi® and Internet-on-a chip™ Solution ImageCreator and Programming Tool User's Guide* for more information.

图 10-4 shows the antenna selection implementation for Wi-Fi, with BLE operating on it's own antenna. Note in this implementation no Coex switch is required and only a single GPIO from the BLE device to the CC3130 device is required. The antenna switch is controlled by 2 GPIO lines from the CC3130 device.

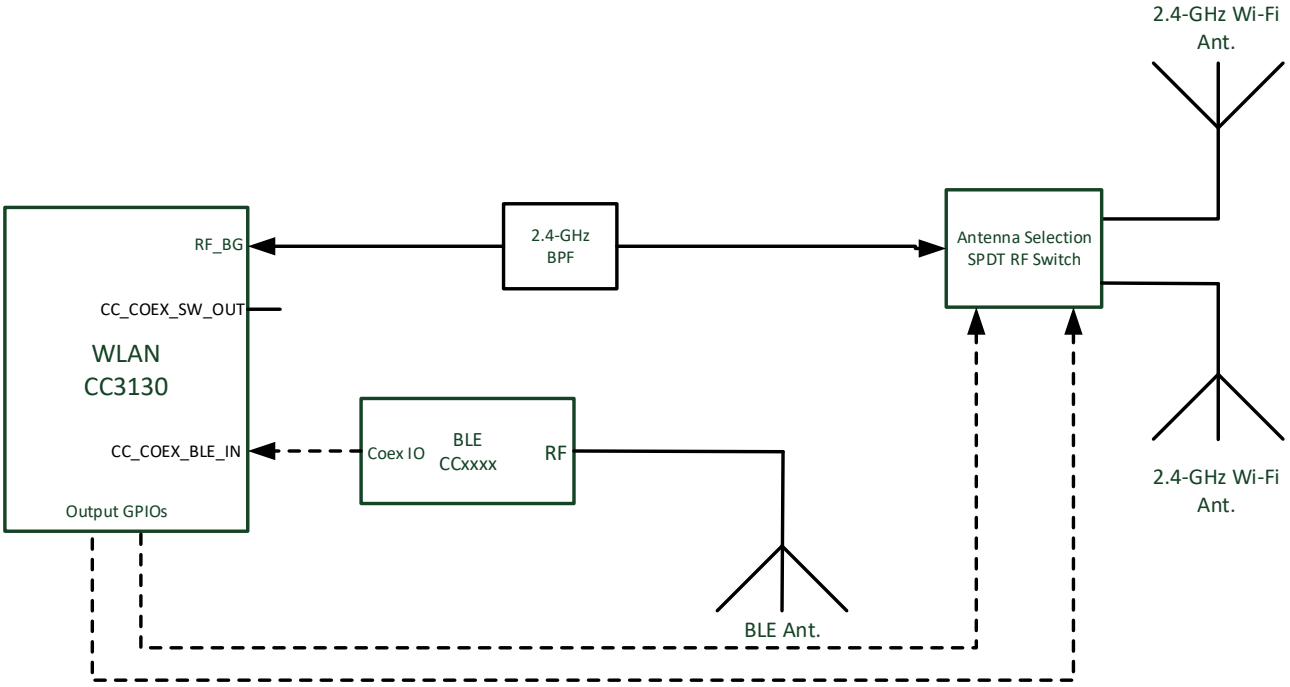


图 10-4. Coexistence Solution With Wi-Fi Antenna Selection and Dedicated BLE Antenna

10.1.3 Typical Application

图 10-5 shows the schematic of the engine area for the CC3130 device in the wide-voltage mode of operation, and the optional RF implementations with BLE/2.4GHz coexistence. The corresponding Bill-of-Materials show in 表 10-1. For a full operation reference design, see the *CC3235x SimpleLink™ and Internet of Things Hardware Design Files*.

Note

The Following guidelines are recommended for implementation of the RF design:

- Ensure an RF path is designed with an impedance of 50 Ω
- Tuning of the antenna impedance π matching network is recommended after manufacturing of the PCB to account for PCB parasitics
- π or L matching and tuning may be required between cascaded passive components on the RF path

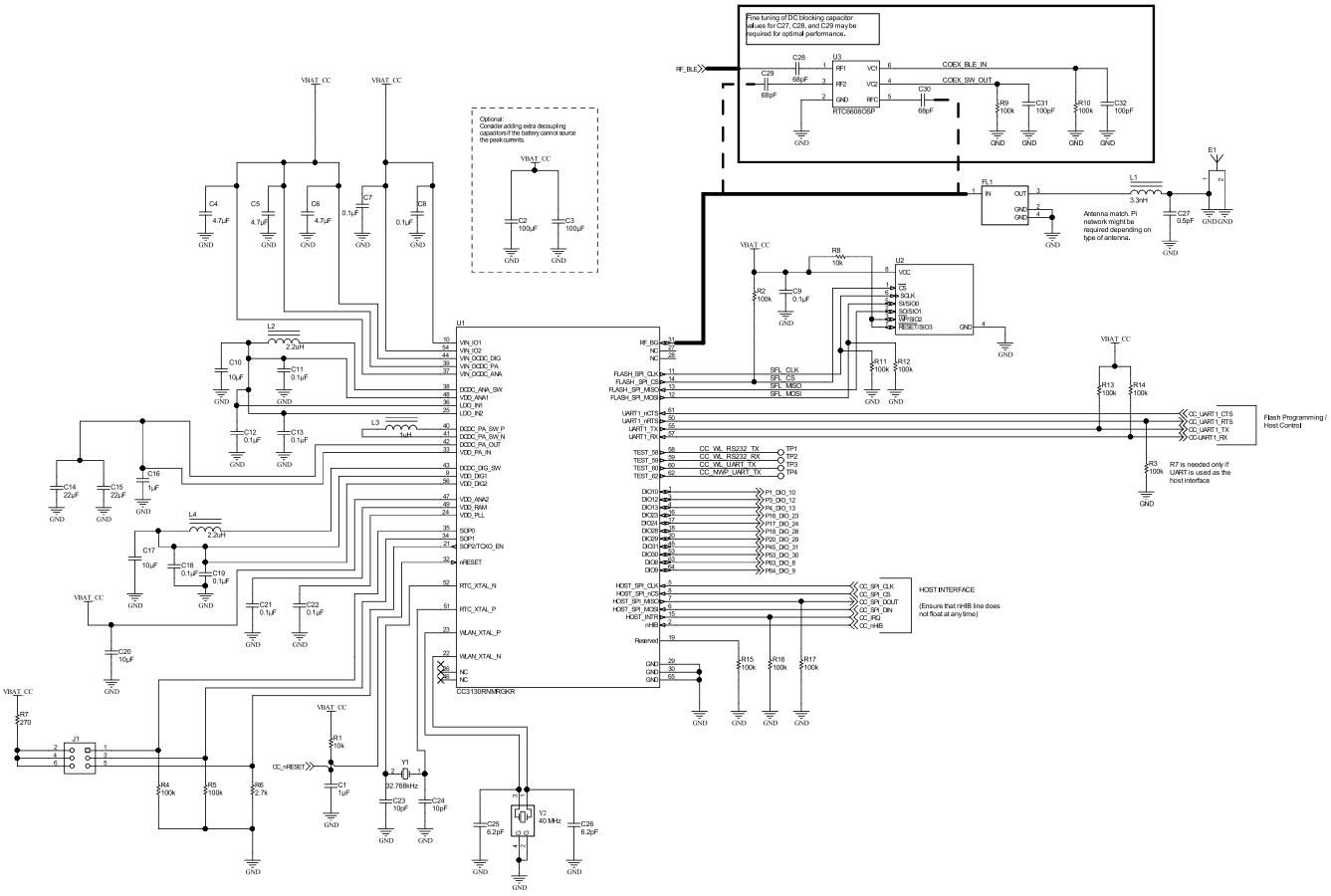


图 10-5. CC3130 Engine Area and Optional BLE Coexistence

表 10-1. Bill-of-Materials for CC3130 Engine Area and Optional Coexistence

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	C1	1 µF	MuRata	GRM155R61A105KE15D	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
2	C2, C3	100 µF	Taiyo Yuden	LMK325ABJ107MMHT	Capacitor, Ceramic, 100 µF, 10 V, ±20%, X5R, 1210
3	C4, C5, C6	4.7 µF	TDK	C1005X5R0J475M050BC	Capacitor, Ceramic, 4.7 µF, 6.3 V, ±20%, X5R, 0402
10	C7, C8, C9, C11, C12, C13, C18, C19, C21, C22	0.1 µF	TDK	C1005X5R1A104K050BA	Capacitor, Ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402
3	C10, C17, C20	10 µF	MuRata	GRM188R60J106ME47D	Capacitor, Ceramic, 10 µF, 6.3 V, ±20%, X5R, 0603
2	C14, C15	22 µF	TDK	C1608X5R0G226M080AA	Capacitor, Ceramic, 22 µF, 4 V, ±20%, X5R, 0603
1	C16	1 µF	TDK	C1005X5R1A105K050BB	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
2	C23, C24	10 pF	MuRata	GRM1555C1H100JA01D	Capacitor, Ceramic, 10 pF, 50 V, ±5%, C0G/NP0, 0402
2	C25, C26	6.2 pF	MuRata	GRM1555C1H6R2CA01D	Capacitor, Ceramic, 6.2 pF, 50 V, ±5%, C0G/NP0, 0402
1	C27	0.5 pF	MuRata	GRM1555C1HR50BA01D	Capacitor, Ceramic, 0.5 pF, 50 V, ±20%, C0G/NP0, 0402

表 10-1. Bill-of-Materials for CC3130 Engine Area and Optional Coexistence (continued)

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
3	C28(1), C29(1), C30(1)	68 pF	MuRata	GRM0335C1H680JA1D	CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0201
2	C31(1), C32(1)	100 pF	Yageo	CC0201JRNPO8BN101	CAP, CERM, 100 pF, 25 V, +/- 5%, C0G/NP0, 0201
1	E1	2.45-GHz Antenna	Taiyo Yuden	AH316M245001-T	ANT Bluetooth W-LAN Zigbee®, SMD
1	FL1	1.02 dB	TDK	DEA202450BT-1294C1-H	Multilayer Chip Band Pass Filter For 2.4 GHz W-LAN/Bluetooth, SMD
1	L1	3.3 nH	MuRata	LQG15HS3N3S02D	Inductor, Multilayer, Air Core, 3.3 nH, 0.3 A, 0.17 ohm, SMD
2	L2, L4	2.2 µH	MuRata	LQM2HPN2R2MG0L	Inductor, Multilayer, Ferrite, 2.2 µH, 1.3 A, 0.08 ohm, SMD
1	L3	1 µH	MuRata	LQM2HPN1R0MG0L	Inductor, Multilayer, Ferrite, 1 µH, 1.6 A, 0.055 ohm, SMD
1	R1, R8	10 k	Vishay-Dale	CRCW040210K0JNED	Resistor, 10 k, 5%, 0.063 W, 0402
13	R2, R3, R4, R5, R9(1), R10(1), R11, R12, R13, R14, R15, R16, R17	100 k	Vishay-Dale	CRCW0402100KJNED	Resistor, 100 k, 5%, 0.063 W, 0402
1	R6	2.7 k	Vishay-Dale	CRCW04022K70JNED	Resistor, 2.7 k, 5%, 0.063 W, 0402
1	R7	270	Vishay-Dale	CRCW0402270RJNED	Resistor, 270, 5%, 0.063 W, 0402
1	U1	MX25R	Macronix International Co., LTD	MX25R3235FM1IL0	Ultra-Low Power, 32-Mbit [x 1/x 2/x 4] CMOS MXSMIO (Serial Multi I/O) Flash Memory, SOP-8
1	U2	CC3130	Texas Instruments	CC3130RNMRGKR	SimpleLink™ Wi-Fi® Wireless Ntework Processor, RGK0064B
1	U3(1)	SPDT Switch	Richwave	RTC6608OSP	0.03 GHz-6 GHz SPDT Switch
1	Y1	Crystal	Abracon Corportation	ABS07-32.768KHZ-9-T	Crystal, 32.768 KHz, 9PF, SMD
1	Y2	Crystal	Epson	Q24FA20H0039600	Crystal, 40 MHz, 8pF, SMD

(1) If the BLE/2.4 GHz Coexistence features is not used, these components are not required.

10.2 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC3130 VQFN device. Follow these guidelines ensures that the design will minimize the risk with regulatory certifications including FCC, ETSI, and CE. For more information, see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.

10.2.1 General PCB Guidelines

Use the following PCB guidelines:

- Verify the recommended PCB stackup in the PCB design guidelines, as well as the recommended layers for signals and ground.
- Ensure that the VQFN PCB footprint follows the information in .
- Ensure that the VQFN PCB GND and solder paste follow the recommendations provided in *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.
- Decoupling capacitors must be as close as possible to the VQFN device.

10.2.2 Power Layout and Routing

Three critical DC/DC converters must be considered for the CC3130 device.

- Analog DC/DC converter
- PA DC/DC converter
- Digital DC/DC converter

Each converter requires an external inductor and capacitor that must be laid out with care. DC current loops are formed when laying out the power components.

10.2.2.1 Design Considerations

The following design guidelines must be followed when laying out the CC3130 device:

- Ground returns of the input decoupling capacitors (C11, C13, and C19) should be routed on Layer 2 using thick traces to isolate the RF ground from the noisy supply ground. This step is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be greater than 12 mils. Take special consideration for power amplifier supply lines (pin 33, 40, 41, and 42), and all input supply pins (pin 37, 39, and 44).
- Ensure the shortest grounding loop for the PLL supply decoupling capacitor (pin 24).
- Place all decoupling capacitors as close to the respective pins as possible.
- Power budget—the CC3130 device can consume up to 450 mA for 3.3 V, 670 mA for 2.1 V, for 24 ms during the calibration cycle.
- Ensure the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.
- The CC3130 device contains many high-current input pins. Ensure the trace feeding these pins can handle the following currents:
  - VIN_DCDC_PA input (pin 39) maximum 1 A
  - VIN_DCDC_ANA input (pin 37) maximum 600 mA
  - VIN_DCDC_DIG input (pin 44) maximum 500 mA
  - DCDC_PA_SW_P (pin 40) and DCDC_PA_SW_N (pin 41) switching nodes maximum 1 A
  - DCDC_PA_OUT output node (pin 42) maximum 1 A
  - DCDC_ANA_SW switching node (pin 38) maximum 600 mA
  - DCDC_DIG_SW switching node (pin 43) maximum 500 mA
  - VDD_PA_IN supply (pin 33) maximum 500 mA

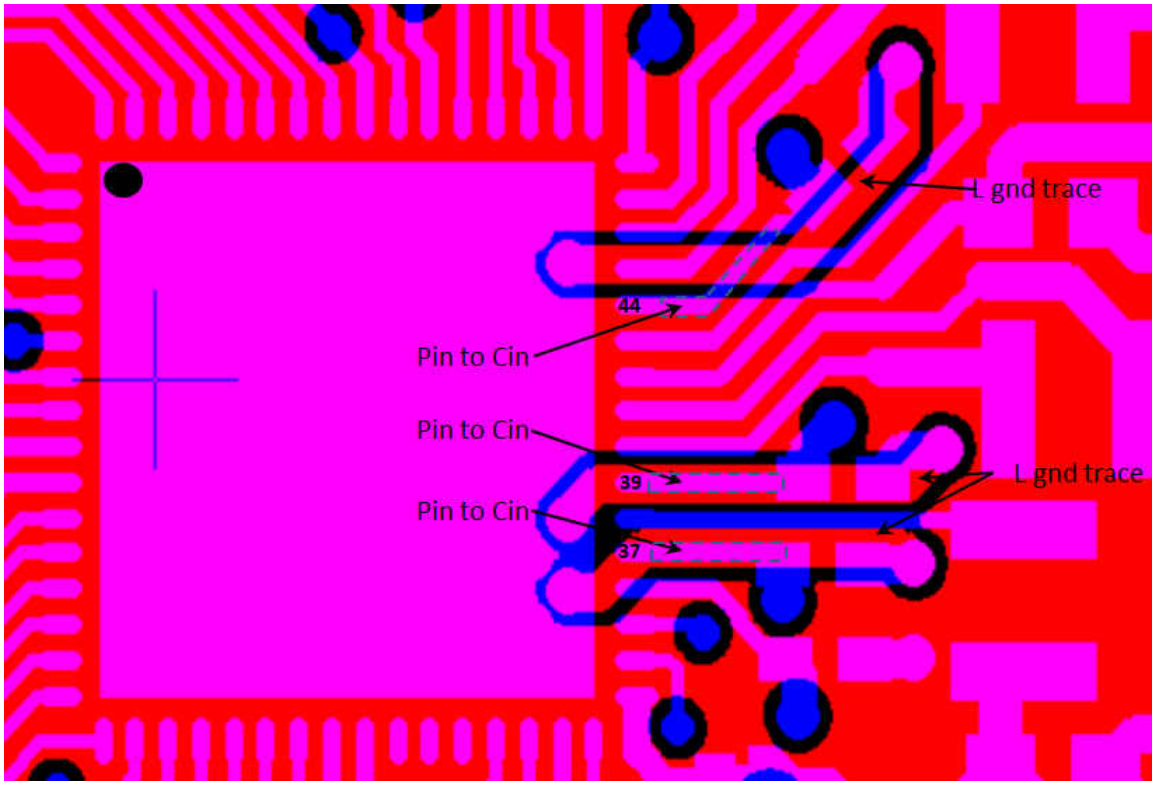


图 10-6. Ground Returns for Input Capacitors

10.2.3 Clock Interface Guidelines

The following guidelines are for the slow clock:

- The 32.768-kHz crystal must be placed close to the VQFN package.
- Ensure that the load capacitance is tuned according to the board parasitics to the frequency tolerance within ±150 ppm.
- The ground plane on layer two is solid below the trace lanes, and there is ground around these traces on the top layer.

The following guidelines are for the fast clock:

- The 40-MHz crystal must be placed close to the VQFN package.
- Ensure that the load capacitance is tuned according to the board parasitics to the frequency tolerance within ±10 ppm at room temperature. The total frequency across parts, temperature, and with aging must be ±25 ppm to meet the WLAN specification.
- To avoid noise degradation, ensure that no high-frequency lines are routed close to the routing of the crystal pins.
- Ensure that crystal tuning capacitors are close to the crystal pads.
- Both traces (XTAL_N and XTAL_P) should be as close as possible to parallel and approximately the same length.
- The ground plane on layer two is solid below the trace lines, and there should be ground around these traces on the top layer.
- For frequency tuning, see *CC31xx & CC32xx Frequency Tuning*.

10.2.4 Digital Input and Output Guidelines

The following guidelines are for the digital I/Os:

- Route SPI and UART lines away from any RF traces.
- Keep the length of the high-speed lines as short as possible to avoid transmission line effects.
- Keep the line lower than 1/10 of the rise time of the signal to ignore transmission line effects (required if the traces cannot be kept short). Place the resistor at the source end closer to the device that is driving the signal.
- Add a series-terminating resistor for each high-speed line (for example, SPI_CLK or SPI_DATA) to match the driver impedance to the line. Typical terminating-resistor values range from 27 to 36 Ω for a 50-Ω line impedance.
- Route high-speed lines with a continuous ground reference plane below it to offer good impedance throughout. This routing also helps shield the trace against EMI.
- Avoid stubs on high-speed lines to minimize the reflections. If the line must be routed to multiple locations, use a separate line driver for each line.
- If the lines are longer compared to the rise time, add series-terminating resistors near the driver for each high-speed line to match the driver impedance to the line. Typical terminating-resistor values range from 27 to 36 Ω for a 50-Ω line impedance.

10.2.5 RF Interface Guidelines

The following guidelines are for the RF interface. Follow guidelines specified in the vendor-specific antenna design guides (including placement of the antenna). Also see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines* for general antenna guidelines.

- Ensure that the antenna is matched for 50-Ω. A π-matching network is recommended. Ensure that the π pad is available for tuning the matching network after PCB manufacture.
- Ensure that the area underneath the BPFs pads have a solid plane on layer 2 and that the minimum filter requirements are met.
- Verify that the Wi-Fi RF trace is a 50-Ω, impedance-controlled trace with a reference to solid ground.
- The RF trace bends must be made with gradual curves. Avoid 90-degree bends.
- The RF traces must not have sharp corners.
- There must be no traces or ground under the antenna section.
- The RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- For optimal antenna performance, ensure adequate ground plane around the antenna on all layers.
- Ensure RF connectors for conducted testing are isolated from the top layer ground using vias.
- Maintain a controlled pad to trace shapes using filleted edges if necessary to avoid mismatch.

11 Device and Documentation Support

11.1 Tools and Software

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

For the most up-to-date list of development tools and software, see the CC3130 Design & development page. Users can also click the "Alert Me" button on the top right corner of the CC3130 Design & development page to stay informed about updates related to the CC3130 device.

Development Tools

SimpleLink™ Wi-Fi® Starter Pro	The supported devices are: CC3100, CC3200, CC3120R, CC3220x, CC3130, and CC3235x. The SimpleLink™ Wi-Fi® Starter Pro mobile App is a new mobile application for SimpleLink™ provisioning. The app goes along with the embedded provisioning library and example that runs on the device side (see *SimpleLink™ Wi-Fi® SDK plugin* and *TI SimpleLink™ CC32XX Software Development Kit (SDK)*). The new provisioning release is a TI recommendation for Wi-Fi provisioning using SimpleLink™ Wi-Fi® products. The provisioning release implements advanced AP mode and SmartConfig™ technology provisioning with feedback and fallback options to ensure successful process has been accomplished. Customers can use both embedded library and the mobile library for integration to their end products.
SimpleLink™ Wi-Fi® SDK plugin	The CC3130 device is supported. The CC3130 SDK contains drivers, many sample applications for Wi-Fi® features and internet, and documentation needed to use the CC3130 Internet-on-a chip™ solution. This SDK can be used with TI’s MSP432P401R LaunchPad™, or SimpleLink™ Studio, a PC tool that allows MCU development with the CC3130 device. You can also use the SDK as example code for any platform. All sample applications in the SDK are supported on TI’s MSP432P401R ultra-low power MCUs with Code Composer Studio™ IDE and TI RTOS. In addition, many of the applications support IAR.
SimpleLink™ Studio for CC31xx	The CC31xx device is supported. SimpleLink™ Studio for CC31xx is a Windows®-based software tool used to aid in the development of embedded networking applications and software for microcontrollers. Using SimpleLink™ Studio for CC31xx, embedded software developers can develop and test applications using any desktop IDE, such as Visual Studio or Eclipse, and connect their applications to the cloud using the CC31xx BoosterPack™ Plug-in Module. The application can then be easily ported to any microcontroller. With the SimpleLink™ Wi-Fi® CC31xx solution, customers now have the flexibility to add Wi-Fi® to any microcontroller (MCU). This Internet-on-a-chip solution contains all you need to easily create IoT solutions: security, quick connection, cloud support, and more. For more information on CC31xx devices, visit SimpleLink™ Wi-Fi® solutions.

SimpleLink™ Wi-Fi® Radio Testing Tool	The supported devices are: CC3100, CC3200, CC3120R, CC3220, CC3130, CC3135, CC3230x, and CC3235x. The SimpleLink™ Wi-Fi® Radio Testing Tool is a Windows-based software tool for RF evaluation and testing of SimpleLink™ Wi-Fi® CC3x20 and CC3x35 designs during development and certification. The tool enables low-level radio testing capabilities by manually setting the radio into transmit or receive modes. Using the tool requires familiarity and knowledge of radio circuit theory and radio test methods. Created for the internet-of-things (IoT), the SimpleLink™ Wi-Fi® CC31xx and CC32xx family of devices include on-chip Wi-Fi®, Internet, and robust security protocols with no prior Wi-Fi® experience needed for faster development. For more information on these devices, visit SimpleLink™ Wi-Fi® family, Internet-on-a chip™ solutions.
UniFlash Standalone Flash Tool for TI Microcontrollers (MCU), Sitara™ Processors and SimpleLink™ Devices	CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara™ processors. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

TI Designs and Reference Designs

The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jumpstart your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

11.2 Firmware Updates

TI updates features in the service pack for this module with no published schedule. Due to the ongoing changes, TI recommends that the user has the latest service pack in their module for production.

To stay informed, click the SDK “Alert me” button the top right corner of the product page, or visit *SimpleLink ™ Wi-Fi® SDK plugin*.

11.3 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3130 device and support tools (see 图 11-1).

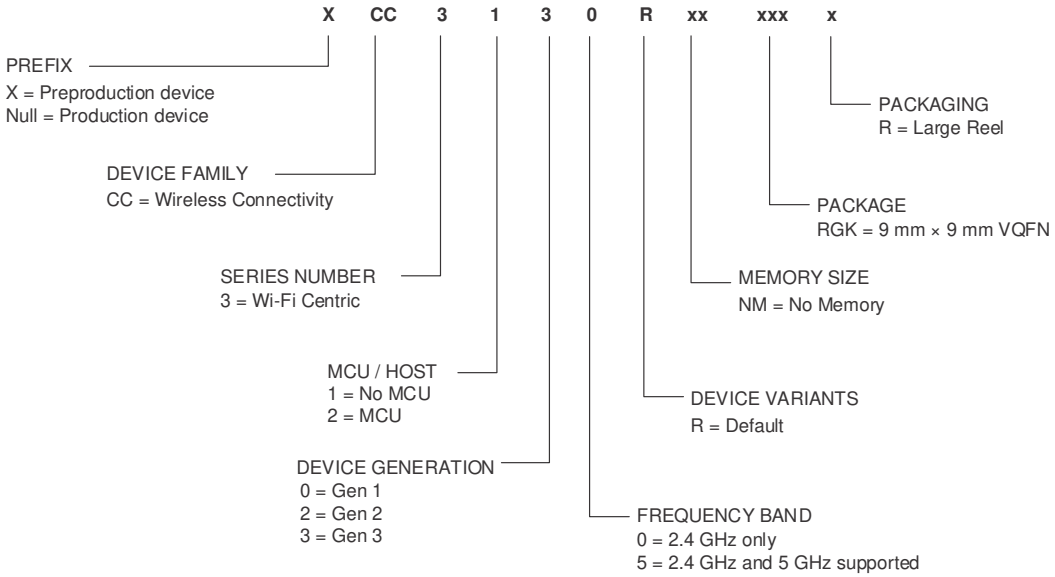


图 11-1. CC3130 Device Nomenclature

11.4 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (CC3130). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document. The current documentation that describes the processor, related peripherals, and other technical collateral follows.

The following documents provide support for the CC3130 device.

Application Reports

CC3135 and CC3235 SimpleLink™ Wi-Fi® Embedded Programming User Guide	CC3135 and CC3235 SimpleLink Wi-Fi Embedded Programming User Guide
SimpleLink™ CC3135, CC3235 Wi-Fi® Internet-on-a chip™ Networking Sub-System Power Management	This application report describes the best practices for power management and extended battery life for embedded low-power Wi-Fi devices such as the SimpleLink Wi-Fi Internet-on-a chip solution from Texas Instruments.
SimpleLink™ CC31xx, CC32xx Wi-Fi® Internet-on-a chip™ Solution Built-In Security Features	The SimpleLink Wi-Fi CC31xx and CC32xx Internet-on-a chip family of devices from Texas Instruments offer a wide range of built-in security features to help developers address a variety of security needs, which is achieved without any processing burden on the main microcontroller (MCU). This document describes these security-related features and provides recommendations for leveraging each in the context of practical system implementation.
SimpleLink™ CC3135, CC3235 Wi-Fi® and Internet-of-Things Over-the-Air Update	This document describes the OTA library for the SimpleLink Wi-Fi CC3x35 family of devices from Texas Instruments and explains how to prepare a new cloud-ready update to be downloaded by the OTA library.
SimpleLink™ CC3135, CC3235 Wi-Fi® Internet-on-a chip™ Solution Device Provisioning	This guide describes the provisioning process, which provides the SimpleLink Wi-Fi device with the information (network name, password, and so forth) needed to connect to a wireless network.
Transfer of TI's Wi-Fi® Alliance Certifications to Products Based on SimpleLink™	This document explains how to employ the Wi-Fi® Alliance (WFA) derivative certification transfer policy to transfer a WFA certification, already obtained by Texas Instruments, to a system you have developed.
Using Serial Flash on SimpleLink™ CC3135 and CC3235 Wi-Fi® and Internet-of-Things Devices	This application note is divided into two parts. The first part provides important guidelines and best- practice design techniques to consider when choosing and embedding a serial Flash paired with the CC3135 and CC3235 (CC3x35) devices. The second part describes the file system, along with guidelines and considerations for system designers working with the CC3x35 devices.

User's Guides

SimpleLink ™ Wi-Fi® and Internet-of-Things CC31xx and CC32xx Network Processor	This document provides software (SW) programmers with all of the required knowledge for working with the networking subsystem of the SimpleLink Wi-Fi devices. This guide provides basic guidelines for writing robust, optimized networking host applications, and describes the capabilities of the networking subsystem. The guide contains some example code snapshots, to give users an idea of how to work with the host driver. More comprehensive code examples can be found in the formal software development kit (SDK). This guide does not provide a detailed description of the host driver APIs.

SimpleLink™ Wi-Fi® CC3135 and CC3235 and IoT Solution Layout Guidelines	This document provides the design guidelines of the 4-layer PCB used for the CC3135 and CC3235 SimpleLink Wi-Fi family of devices from Texas Instruments. The CC3135 and CC3235 devices are easy to lay out and are available in quad flat no-leads (QFNS) packages. When designing the board, follow the suggestions in this document to optimize performance of the board.
SimpleLink™ Wi-Fi® CC3130 BoosterPack™ Development Kit (BOOSTXL-CC3130)	The SimpleLink Wi-Fi CC3130 wireless network processor from Texas Instruments™ provides users the flexibility to add Wi-Fi to any MCU. This user's guide explains the various configurations of the CC3130 BoosterPack™ Plug-In Module.
SimpleLink™ Wi-Fi® and Internet-on-a chip™ CC3135 and CC3235 Solution Radio Tool	The Radio Tool serves as a control panel for direct access to the radio, and can be used for both the radio frequency (RF) evaluation and for certification purposes. This guide describes how to have the tool work seamlessly on Texas Instruments evaluation platforms such as the BoosterPack plus FTDI emulation board for CC3235 devices, and the LaunchPad for CC3235 devices.
SimpleLink™ Wi-Fi® CC3135 and CC3235 Provisioning for Mobile Applications	This guide describes TI's SimpleLink Wi-Fi provisioning solution for mobile applications, specifically on the usage of the Android™ and IOS® building blocks for UI requirements, networking, and provisioning APIs required for building the mobile application.

More Literature

CC3x35 SimpleLink™ Wi-Fi® Hardware Design Checklist

CC3130 SimpleLink™ WI-Fi® BoosterPack™ Design Files

11.5 Trademarks

WPA3™, WPA™, WPA2™, are trademarks of Wi-Fi Alliance.
E2E™, Internet-on-a chip™, Texas Instruments™, SmartConfig™, LaunchPad™, Code Composer Studio™, BoosterPack™, and Sitara™ are trademarks of Texas Instruments.
Android™ is a trademark of Google LLC.
Wi-Fi®, Wi-Fi 联盟®, and Wi-Fi Direct® are registered trademarks of Wi-Fi Alliance.
Arm® and Cortex® are registered trademarks of Arm Limited.
Zigbee® is a registered trademark of Zigbee Alliance.
Windows® is a registered trademark of Microsoft Inc.
IOS® is a registered trademark of Cisco.
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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking(5) (6)
CC3130RNMRGKR	PREVIEW	VQFN	RGK	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3130RNM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC3130RNMRGKR	ACTIVE	VQFN	RGK	64	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3130R NM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

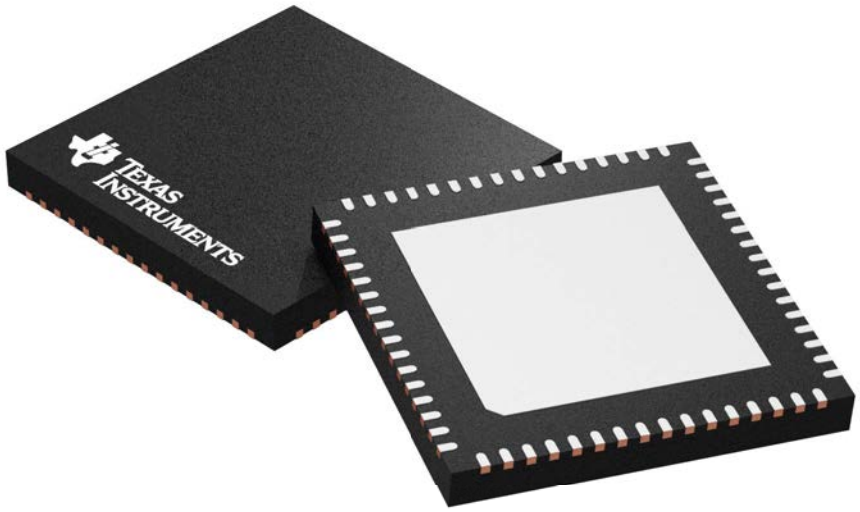
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RGK 64

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



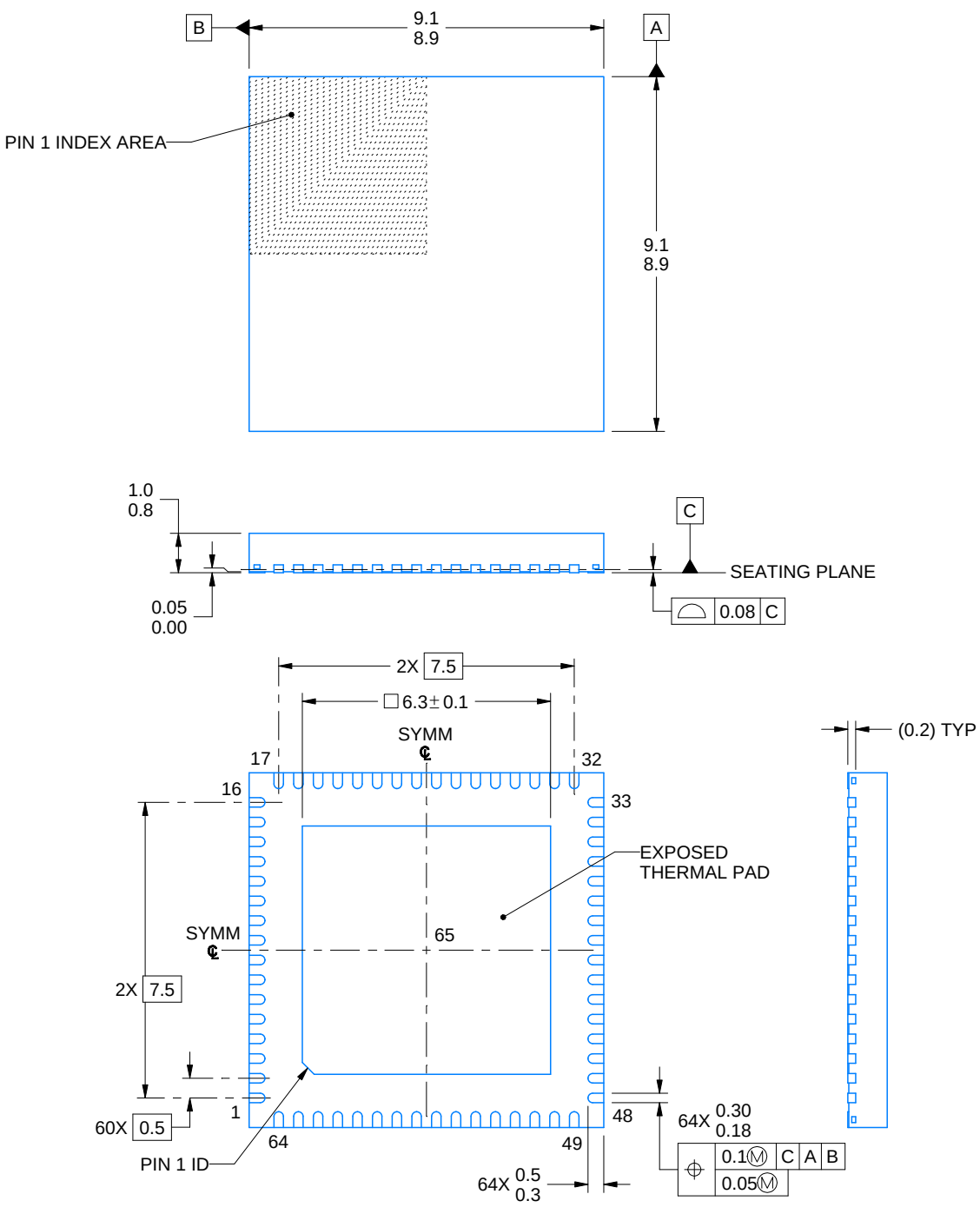
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGK0064B

PACKAGE OUTLINE

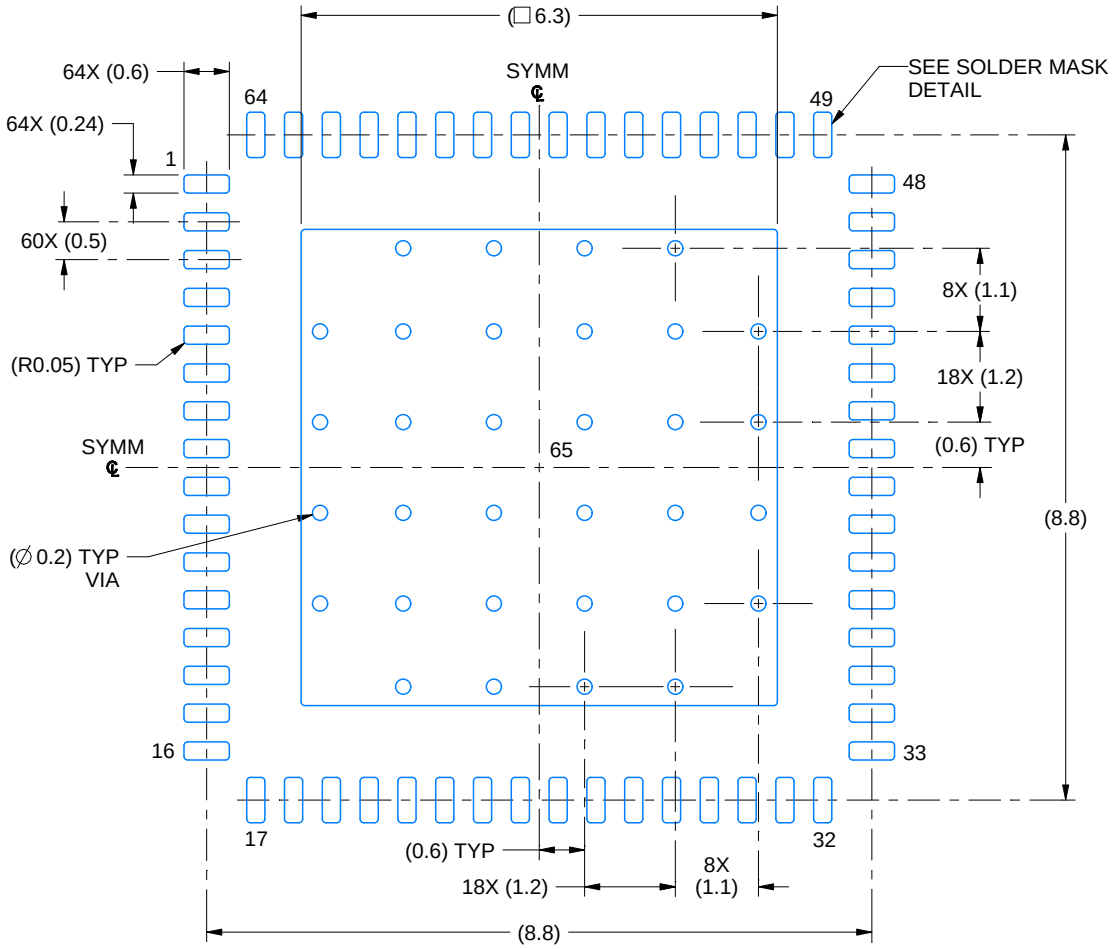
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

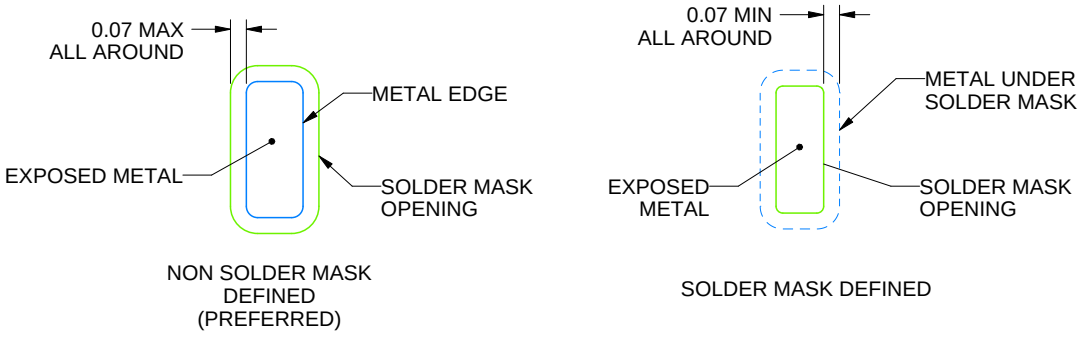


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

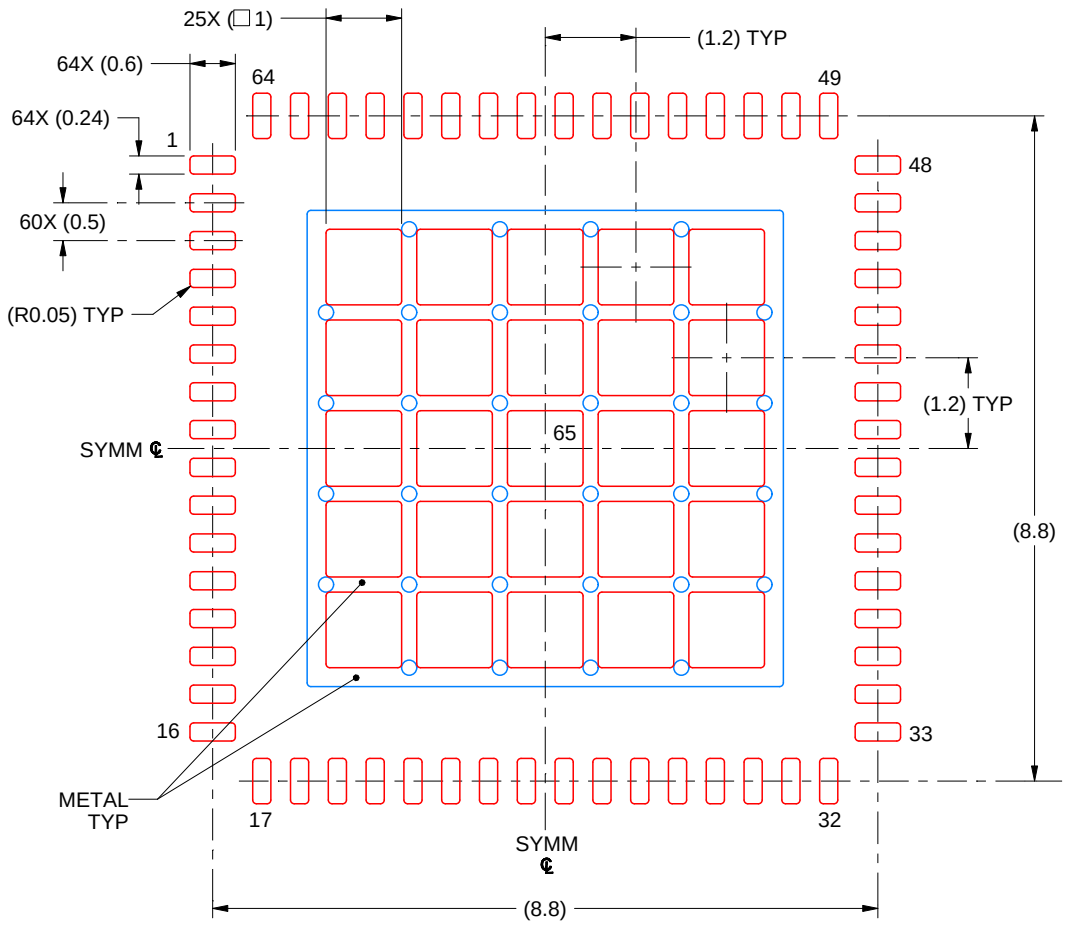


SOLDER MASK DETAILS

4222201/B 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4222201/B 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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