CDCVF2509 3.3V 锁相环时钟驱动器

1 特性

- 旨在满足并超过 PC133 SDRAM 寄存 DIMM 规范 1.1 版
- 与扩频时钟兼容
- 工作频率：50MHz 至 175MHz
- 66MHz 至 166MHz 的静态相位误差分布为 ±125ps
- 66MHz 至 166MHz 的抖动 (cyc - cyc) 典型值 = 70ps
- 先进的深亚微米工艺使功耗比当前一代 PC133 器件降低 40% 以上
- 采用塑料 24 引脚 TSSOP 封装
- 适用于同步 DRAM 应用的锁相环时钟分配
- 将一个时钟输入分配至一组五个输出和一组四个输出
- 每个输出组的单独输出使能
- 外部反馈 (FBIN) 端子用于将输出同步到时钟输入
- 25Ω 片上串联阻尼电阻器
- 无需外部 RC 网络
- 工作电压为 3.3V

2 应用

- DRAM 应用
- 基于 PLL 的时钟分配器
- 非 PLL 时钟缓冲器

3 说明

CDCVF2509 是一款高性能、低偏差、低抖动锁相环 (PLL) 时钟驱动器。该器件使用 PLL 根据时钟 (CLK) 输入信号对反馈 (FBOUT) 输出的频率和相位进行精准校准。该器件专门设计用于同步 DRAM。CDCVF2509 在 3.3V V_{CC} 电压下工作，并提供专为驱动点对点负载而设计的集成串联阻尼电阻器。

一组五个输出和一组四个输出提供九个低偏差、低抖动的 CLK 副本。输出信号占空比调整为 50%，与 CLK 处的占空比无关。每组输出可通过控制（1G 和 2G）输入单独启用或禁用。当 G 输入为高电平时，输出随 CLK 进行相位和频率切换。当 G 输入为低电平时，输出被禁用为逻辑低电平状态。

与许多包含 PLL 的产品不同，CDCVF2509 不需要外部 RC 网络。PLL 的环路滤波器包含片上，可更大限度地减少元件数量、缩小电路板空间并降低成本。

该器件基于 PLL 电路，因此 CDCVF2509 需要稳定时间来实现反馈信号到基准信号的相位锁定。在上电并在 CLK 处施加固定频率、固定相位的信号之后，以及在 PLL 基准或反馈信号发生任何变化之后，需要该稳定时间。PLL 可通过将 AV_{CC} 接地来旁路。

CDCVF2509A 的工作温度范围是 0°C 至 85°C。

有关应用信息，请参阅 *CDC509/516/2509/2510/2516 的高速分布设计技巧*和 *使用带展频时钟 (SSC) 的 CDC2509A/2510A PLL* 应用手册。

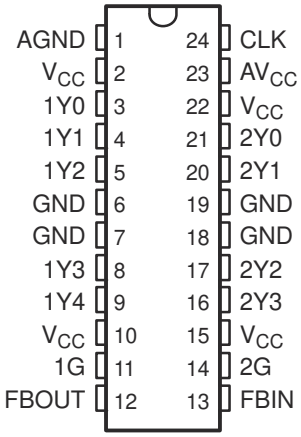
功能表

输入			输出		
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

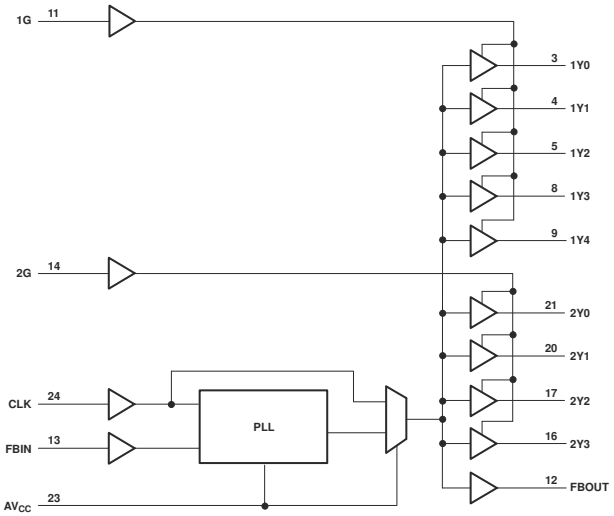
提供的选项

T_A	封装
	SMALL OUTLINE (PW)
0°C 至 85°C	CDCVF2509PWR
	CDCVF2509PW

PW PACKAGE
(TOP VIEW)



引脚分配



功能方框图

Table of Contents

Pin Configuration and Functions

PW PACKAGE
(TOP VIEW)

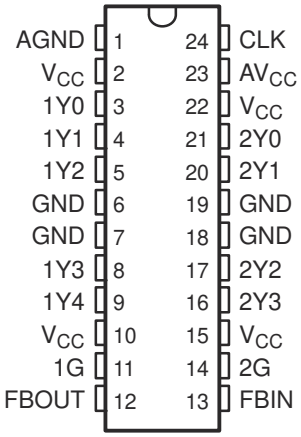


表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDCVF2509A clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25-Ω series-damping resistor.
1Y (0:4)	3, 4, 5, 8, 9	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated 25-Ω series-damping resistor.
2Y (0:3)	16, 17, 21, 20	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each output has an integrated 25-Ω series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
AV_{CC}	Supply voltage range (2)	$AV_{CC} < V_{CC}$ +0.7 V
V_{CC}	Supply voltage range	– 0.5 V to 4.3 V
V_I	Input voltage range (3)	– 0.5 V to 4.6 V
V_O	Voltage range applied to any output in the high or low state(3) (4)	– 0.5 V to V_{CC} + 0.5 V
I_{IK}	Input clamp current (V_I< 0)	– 50 mA
I_{OK}	Output clamp current (V_O< 0 or $V_O > V_{CC}$)	±50 mA
I_O	Continuous output current (V_O = 0 to V_{CC})	±50 mA
	Continuous current through each V_{CC} or GND	±100 mA
	Maximum power dissipation at T_A = 55°C (in still air)(5)	0.7 W
T_{stg}	Storage temperature range	– 65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AV_{CC} **must not** exceed V_{CC}+ 0.7 V
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 4.6 V maximum.
(5) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, see the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book* (SCBD002).

4.2 Dissipation Ratings

PACKAGE	BOARD TYPE	$R_{\theta JA}$	$T_A \leqslant 25°C$ POWER RATING	DERATING FACTORS ABOVE $T_A \leqslant 25°C$	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PW	JEDEC low-K	114.5°C/W	920 mW	8.7 mW/°C	520 mW	390 mW
	JEDEC high-K	62.1°C/W	1690 mW	16.1 mW/°C	960 mW	720 mW

4.3 Recommended Operating Conditions

See (1)

		MIN	MAX	UNIT
V_{CC}, AV_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		– 12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	85	°C

(1) Unused inputs must be held high or low to prevent them from floating.

4.4 Package Thermal Resistance

CDCVF2509APW 24-PIN TSSOP(1)			THERMAL AIRFLOW (CFM)				UNIT
			0	150	250	500	
$R_{\theta JA}$	High K		88	83	81	77	°C/W
$R_{\theta JC}$	High K	26.5					

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}, AV_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA	3 V			-1.2	V
V_{OH}	High-level output voltage	I_{OH} = -100 µA	MIN to MAX	V_{CC} - 0.2			V
		I_{OH} = -12 mA	3 V	2.1			
		I_{OH} = -6 mA	3 V	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA	MIN to MAX			0.2	V
		I_{OL} = 12 mA	3 V			0.8	
		I_{OL} = 6 mA	3 V			0.55	
I_{OH}	High-level output current	V_O= 1 V	3 V	-28			mA
		V_O = 1.65 V	3.3 V		-36		
		V_O = 3.135 V	3.6 V			-8	
I_{OL}	Low-level output current	V_O= 1.95 V	3 V	30			mA
		V_O = 1.65 V	3.3 V		40		
		V_O = 0.4 V	3.6 V			10	
I_I	Input current	V_I = V_{CC} or GND	3.6 V			±5	µA
I_{CC} (2)	Supply current (static, output not switching)	V_I = V_{CC} or GND, I_O = 0, Outputs: low or high	3.6 V, 0 V			40	µA
ΔI_{CC}	Change in supply current	One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3.3 V to 3.6 V			500	µA
C_i	Input capacitance	V_I = V_{CC} or GND	3.3 V		2.5		pF
C_o	Output capacitance	V_O = V_{CC} or GND	3.3 V		2.8		pF

(1) For conditions shown as MIN or MAX, use the appropriate value specified under the *recommended operating conditions* section.
(2) For dynamic I_{CC} vs Frequency, see 图 4-6 and 图 4-7.

4.6 Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f_{clk}	Clock frequency	50	175	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time(1)		1	ms

(1) The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew and jitter parameters given in the *switching characteristics* table are not applicable. This parameter does not apply for input modulation under SSC application.

4.7 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF (see 图 5-1 and 图 5-2)(3) (1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}, AV_{CC} = 3.3 V ± 0.3 V			UNIT
				MIN	TYP	MAX	
$t_{(\phi)}$	Phase error time- static (normalized) (see 图 4-1 through 图 4-4)	CLK ↑ = 66 MHz to 166 MHz	FBIN ↑	-125		125	ps
$t_{sk(o)}$	Output skew time(2)	Any Y	Any Y			100	ps
	Phase error time-jitter (4)	CLK = 66 MHz to 100 MHz	Any Y or FBOUT	-50		50	ps
	$Jitter_{(cycle-cycle)}$ (see 图 4-5)	CLK = 66 MHz to 100 MHz	Any Y or FBOUT		-70		ps
		CLK = 100 MHz to 166 MHz			-65		

over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF (see 图 5-1 and 图 5-2)(3) (1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}, AV_{CC} = 3.3 V ± 0.3 V			UNIT
				MIN	TYP	MAX	
	Duty cycle	$f_{(CLK)}$ > 60 MHz	Any Y or FBOUT	45%		55%	
t_r	Rise time	V_O = 0.4 V to 2 V	Any Y or FBOUT	0.3		1.1	ns/V
t_f	Fall time	V_O = 2 V to 0.4 V	Any Y or FBOUT	0.3		1.1	ns/V
t_{PLH}	Low-to-high propagation delay time, bypass mode	CLK	Any Y or FBOUT	1.8		3.9	ns
t_{PHL}	High-to-low propagation delay time, bypass mode	CLK	Any Y or FBOUT	1.8		3.9	ns

(1) These parameters are not production tested.
(2) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
(3) The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
(4) Calculated per PC DRAM SPEC ($t_{phase\ error}$, static-jitter$_{(cycle\text{-}to\text{-}cycle)}$).

4.8 Typical Characteristics

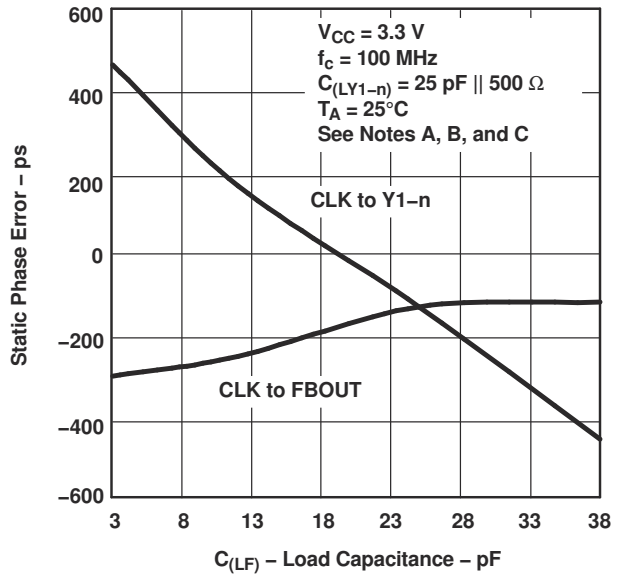


图 4-1. Static Phase Error vs Load Capacitance

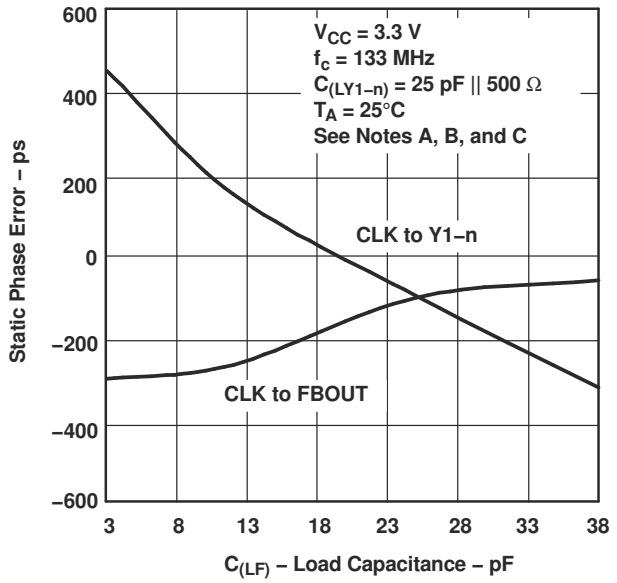


图 4-2. Static Phase Error vs Load Capacitance

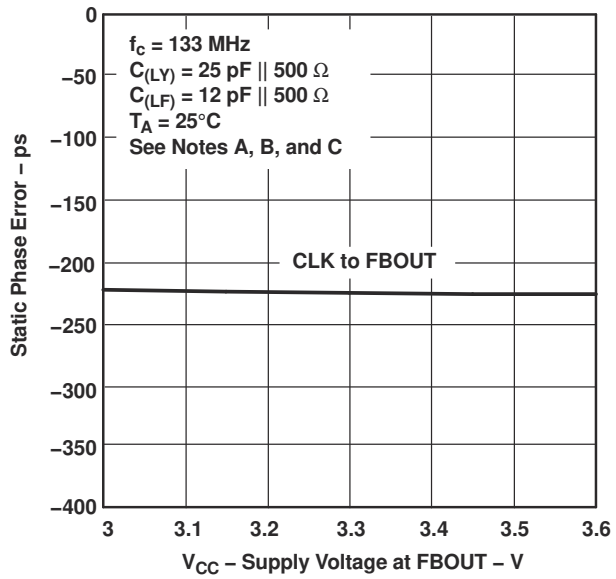


图 4-3. Static Phase Error vs Supply Voltage at FBOUT

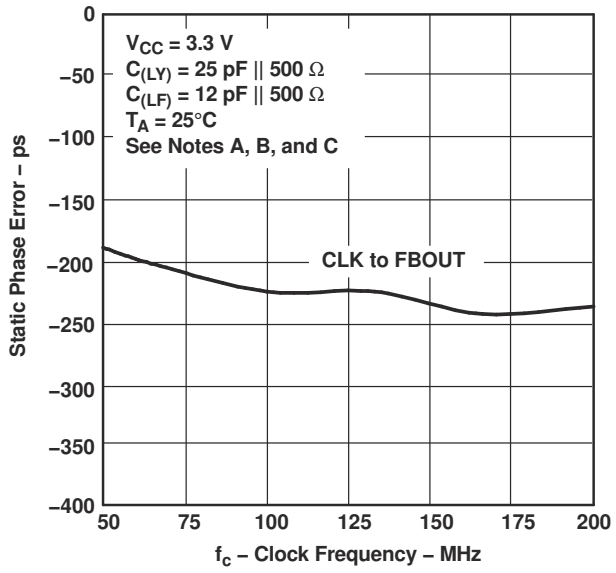


图 4-4. Static Phase Error vs Clock Frequency

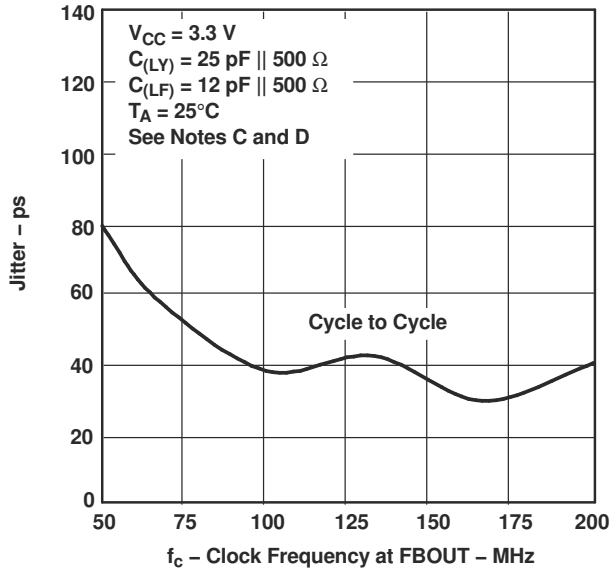


图 4-5. Jitter vs Clock Frequency at FBOUT

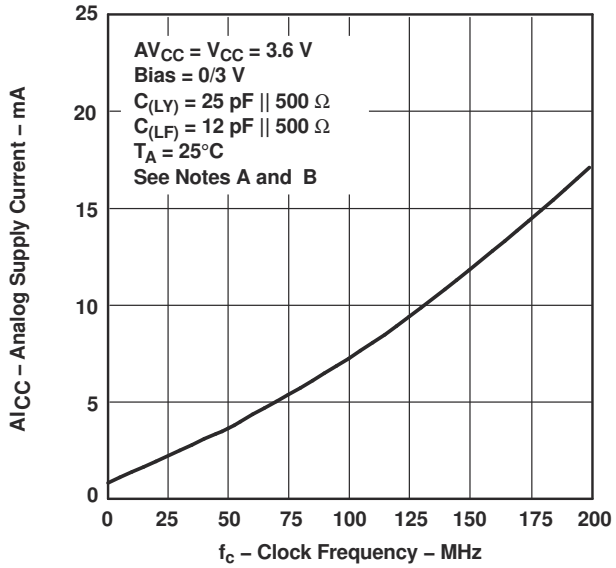


图 4-6. Analog Supply Current vs Clock Frequency

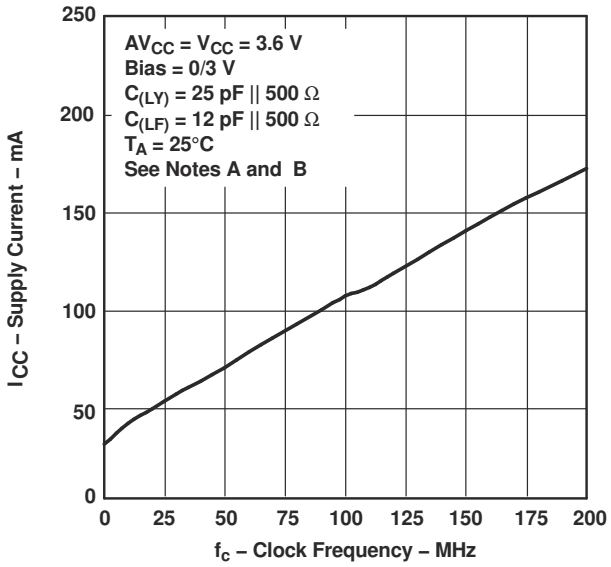
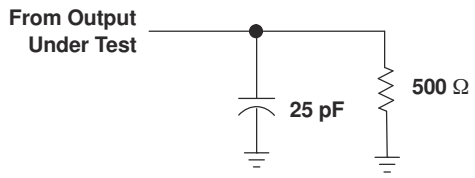


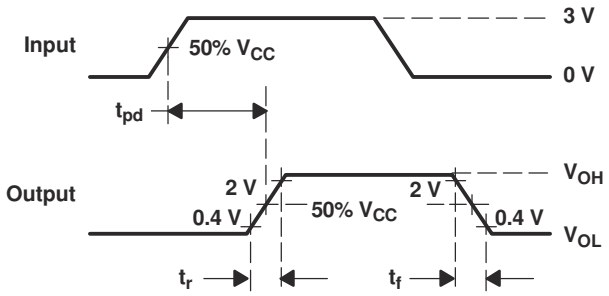
图 4-7. Supply Current vs Clock Frequency

1. Trace length FBOUT to FBIN = 5 mm, Z_O = 50 Ω
2. $C_{(LY)}$ = Lumped capacitive load Y_{1-n}
3. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN
4. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN.

5 Parameter Measurement Information



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 133 MHz, Z_O = 50 Ω, t_r ≤ 1.2 ns, t_f ≤ 1.2 ns.
C. The outputs are measured one at a time with one transition per measurement.

图 5-1. Load Circuit and Voltage Waveforms

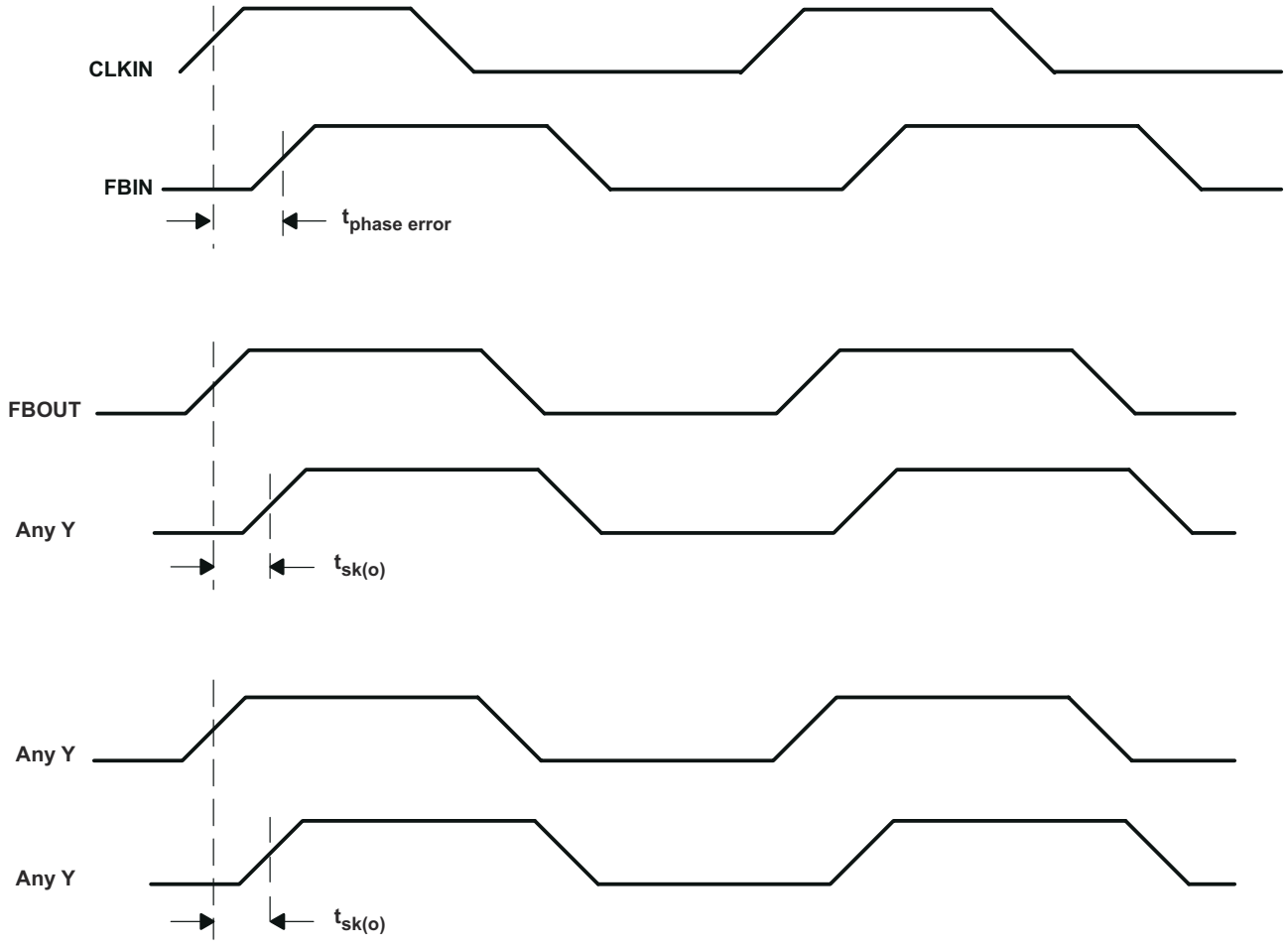


图 5-2. Skew Calculations

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High Speed Distribution Design Techniques for CDC509/516/2509/2510/2516* application note
- Texas Instruments, *Using CDC2509A/2510A PLL with Spread Spectrum Clocking (SSC)* application note

6.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

6.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

6.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

7 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (February 2010) to Revision E (February 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 从*特性* 中删除了以下要点：使用 CDCVF2509A (SCAS765) 作为该器件的替代品	1
• Added *Device and Documentation Support* section	12

Changes from Revision C (January 2009) to Revision D (February 2010)	Page
• Added the PACKAGE THERMAL RESISTANCE table	6

Changes from Revision B (June 2005) to Revision C (January 2009)	Page
• 添加了“不推荐用于新设计”	1

Changes from Revision A (July 2004) to Revision B (June 2005)	Page
• Changed Rise time values in the Switching Characteristics table From: Min =0.5 Max = 2.5 To: Min = 0.3 Max = 1.1	7
• Changed Fall time values in the Switching Characteristics table From: Min =0.5 Max = 2.5 To: Min = 0.3 Max = 1.1	7
• Changed Low-to-high propagation delay time values in the Switching Characteristics table From: Min =0.4 Max = 2.3 To: Min = 1.8 Max = 3.9	7
• Changed High-to-low propagation delay time values in the Switching Characteristics table From: Min =0.4 Max = 2.3 To: Min = 1.8 Max = 3.9	7

Changes from Revision * (April 2004) to Revision A (July 2004)	Page
• 向“提供的选项”表中添加了 CDCVF2509PW 封装编号	1

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF2509PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2509	Samples
CDCVF2509PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2509	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

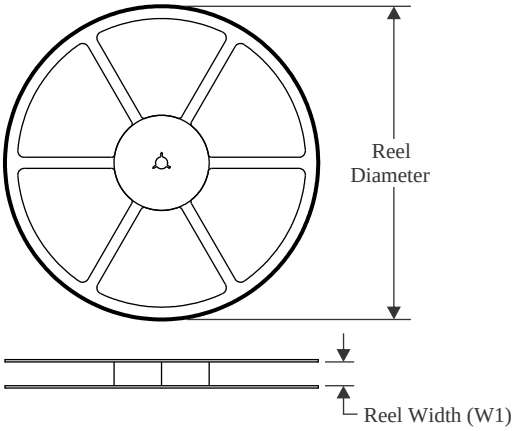
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

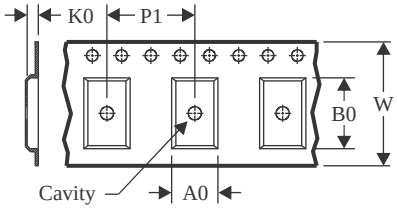
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

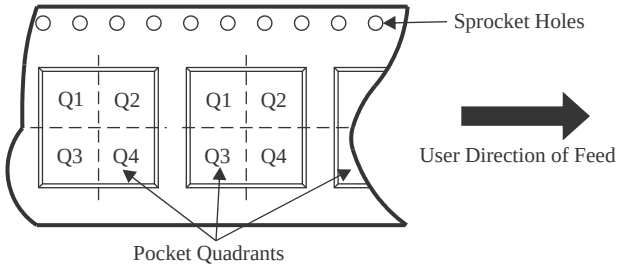


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

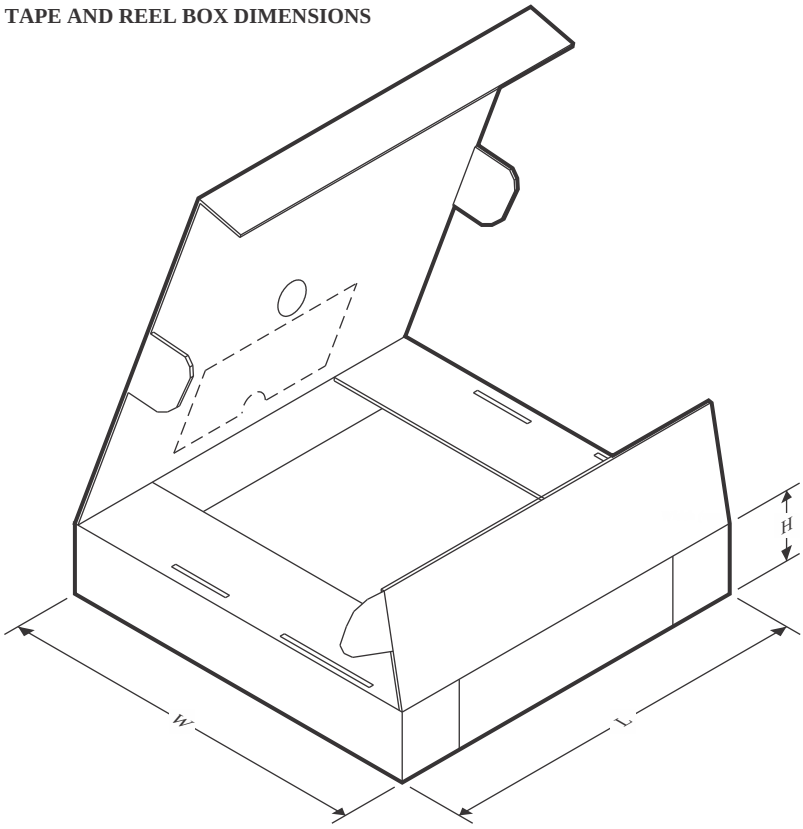
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2509PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

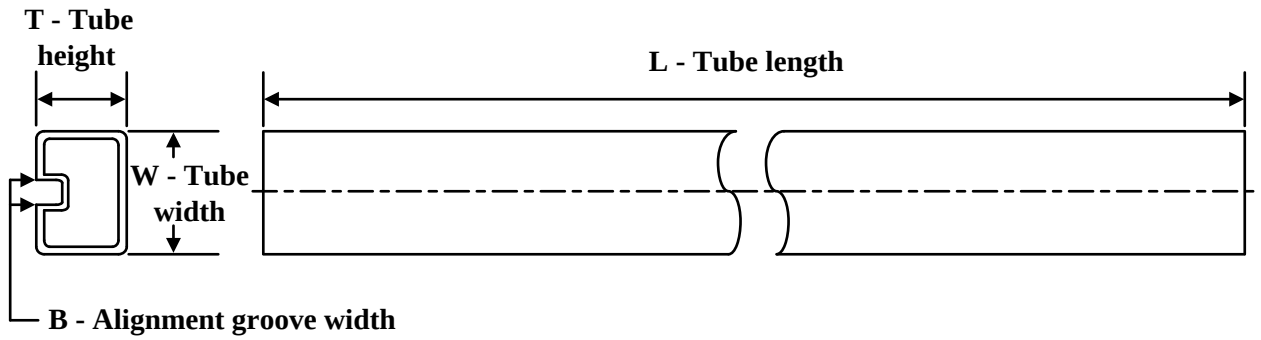
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2509PWR	TSSOP	PW	24	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

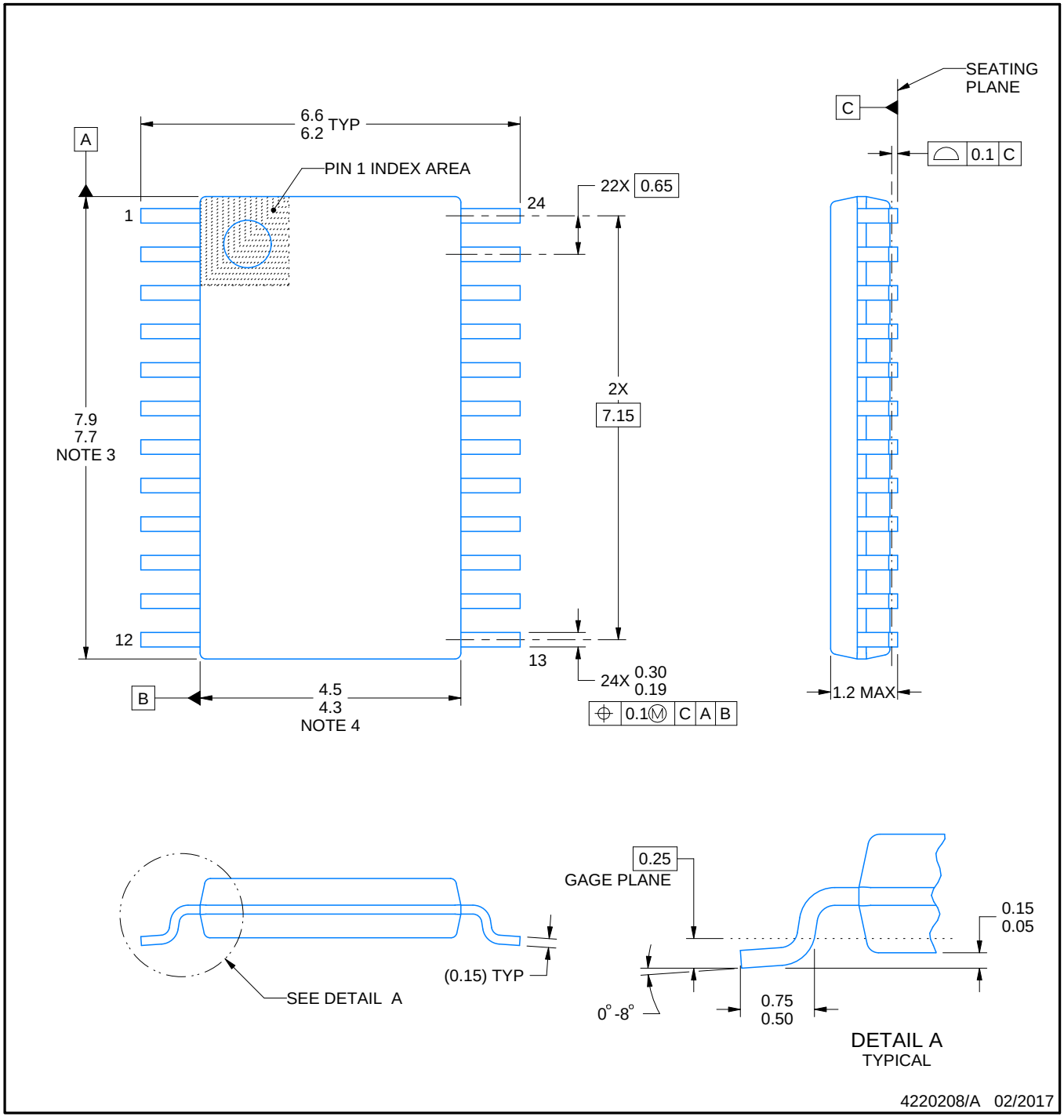
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDCVF2509PW	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

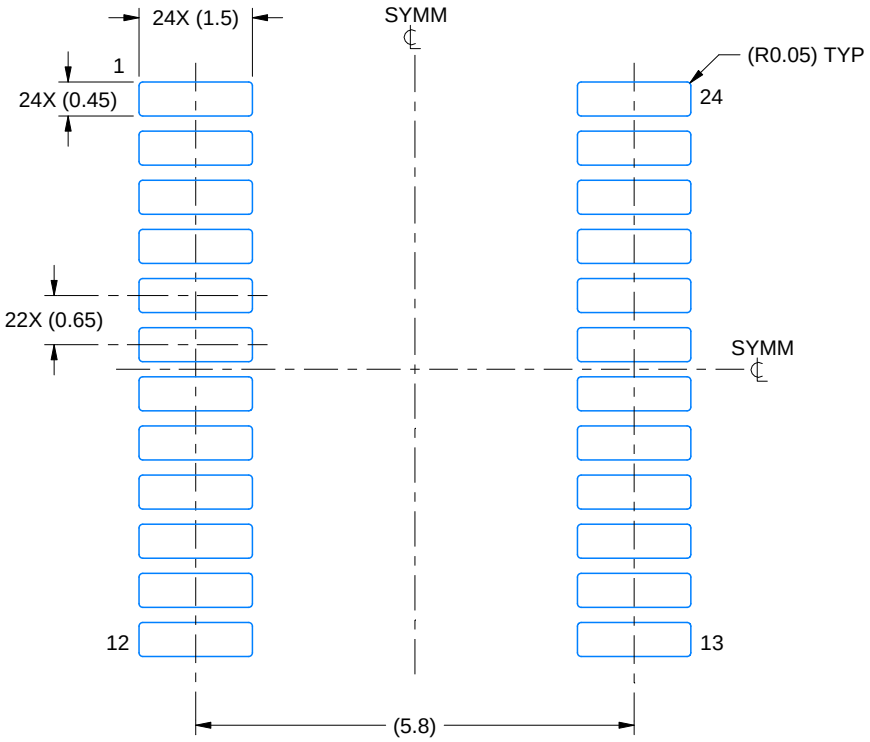
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

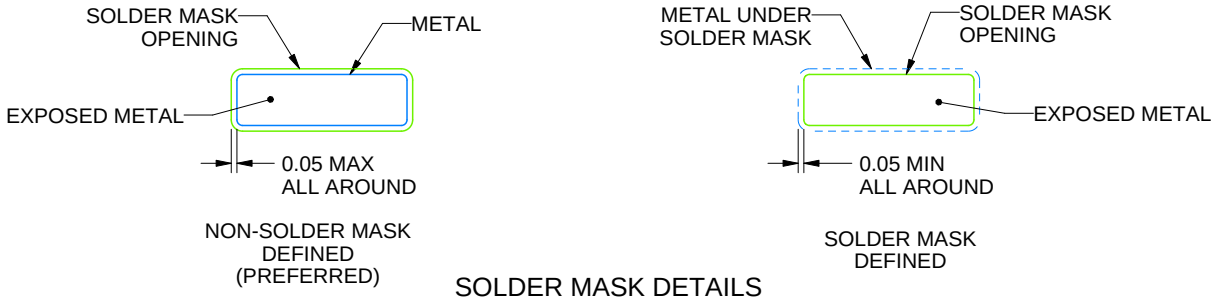


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

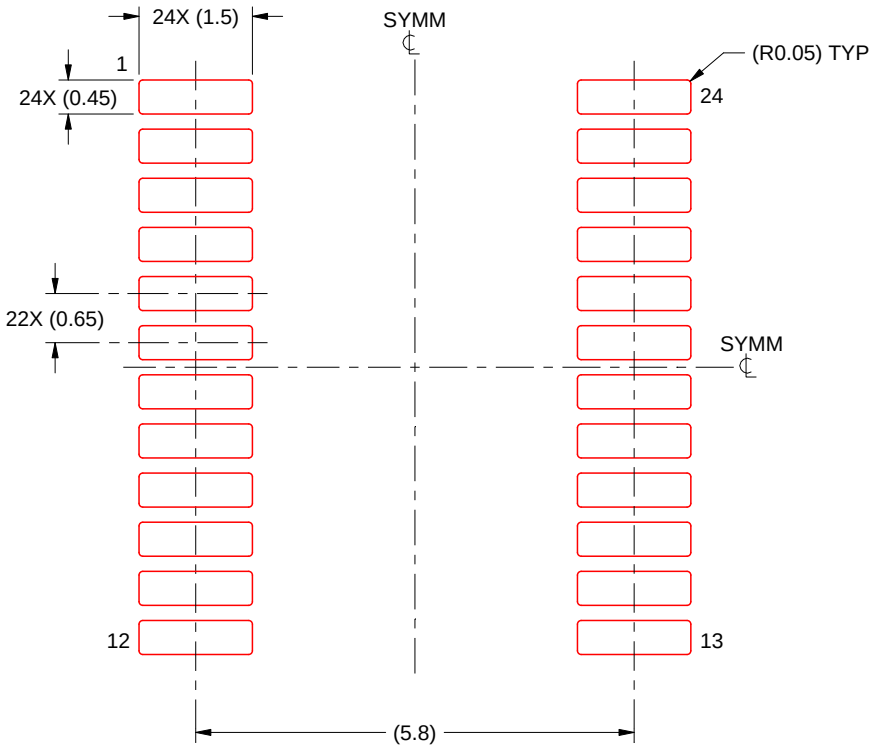


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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