N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

查询样品: CSD13201W10

特性

- 超低栅极电荷 **(Qg)** 和栅漏电荷 **(Qgd)**
- 小型封装尺寸 **1mm x 1mm**
- 低高度（高度为 **0.62mm**）
- 无铅
- 符合 **RoHS** 标准
- 无卤素
- 栅 **-** 源电压钳位

应用范围

- 电池管理
- 负载开关
- 电池保护

说明

此器件设计用于在 超低高度并具有出色散热特性的 尽可能小外形尺寸封装内产生最低的导通 电阻和栅极电荷。

产品概述

V_{DS}	漏源电压	12		V
Q_g	栅极电荷总量 (4.5V)	2.3		nC
Q_{gd}	栅漏栅极电荷	0.3		nC
R_{DS}（接通）	漏源导通电阻	V_{GS}=1.8V	38	mΩ
		V_{GS} = 2.5V	29	
		V_{GS}=4.5V	26	mΩ
$V_{GS(th)}$	阀值电压	0.8		V

订购信息

器件	封装	介质	数量	出货
CSD13201W10	1 × 1 晶圆级封装	7 英寸卷带	3000	卷带封装

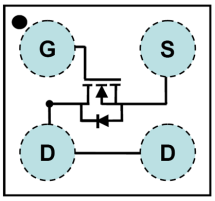
绝对最大额定值

T_A=25°C 时测得，除非另外注明		值	单位
V_{DS}	漏源电压	12	V
V_{GS}	栅源电压	±8	V
I_D	持续漏极电流，T_A=25°C 时测得(1)	1.6	A
I_{DM}	脉冲漏极电流，T_A=25°C 时测得(2)	20.2	A
P_D	功率耗散(1)	1.2	W
T_J，T_{STG}	运行结温和储存温度范围	-55 至 150	°C

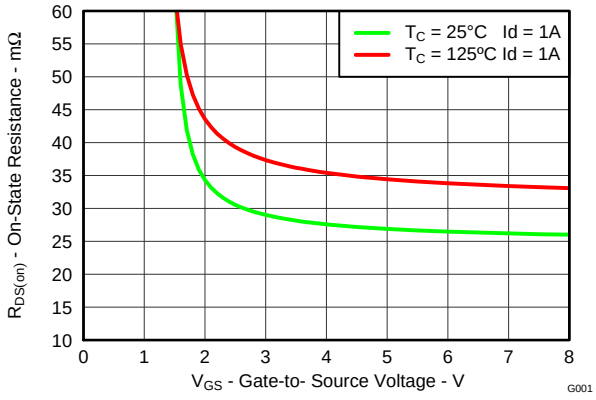
(1) 在 1 in^2 2 盎司纯铜 (Cu) (2 oz.) 且厚度为 0.060" 的环氧板 (FR4) 印刷电路板 (PCB) 上，$R_{\theta JA}$=105°C/W （典型值）。

(2) 脉宽 ≤ 300μs，占空比 ≤ 2%

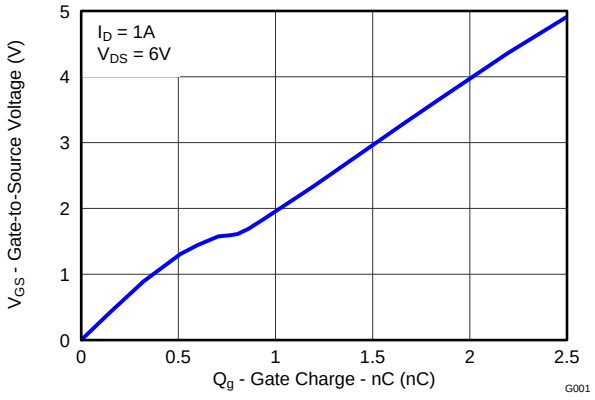
图 **1.** 顶视图



$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

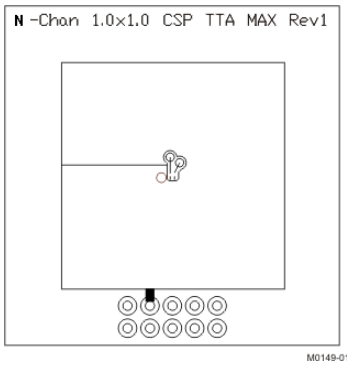
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	12			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 9.6V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.65	0.8	1.1	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 1.8V, I_D = 1A		38	53	mΩ
		V_{GS} = 2.5V, I_D = 1A		29	39	
		V_{GS} = 4.5V, I_D = 1A		26	34	mΩ
g_{fs}	Transconductance	V_{DS} = 6V, I_D = 1A		23		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 6V, f = 1MHz		385	462	pF
C_{OSS}	Output Capacitance			245	294	pF
C_{RSS}	Reverse Transfer Capacitance			18.1	22.6	pF
R_g	Series Gate Resistance			3		Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 6V, I_D = 1A		2.3	2.9	nC
Q_{gd}	Gate Charge Gate to Drain			0.3		nC
Q_{gs}	Gate Charge Gate to Source			0.5		nC
$Q_{g(th)}$	Gate Charge at Vth			0.3		nC
Q_{OSS}	Output Charge	V_{DS} = 6.0V, V_{GS} = 0V		1.8		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 6V, V_{GS} = 4.5V, I_D = 1A R_G = 20Ω		3.9		ns
t_r	Rise Time			5.9		ns
$t_{d(off)}$	Turn Off Delay Time			14.4		ns
t_f	Fall Time			9.7		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 1A, V_{GS} = 0V		0.7	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 6V, I_S = 1A, di/dt = 100A/µs		2.4		nC
t_{rr}	Reverse Recovery Time			11.5		ns

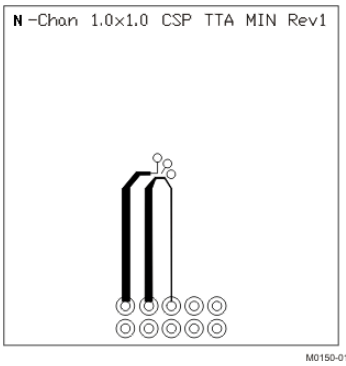
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			228.6	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1 in^2 Cu area)			131.1	°C/W



Max $R_{\theta JA}$ = 131.1°C/W when mounted on 1inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 228.6°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

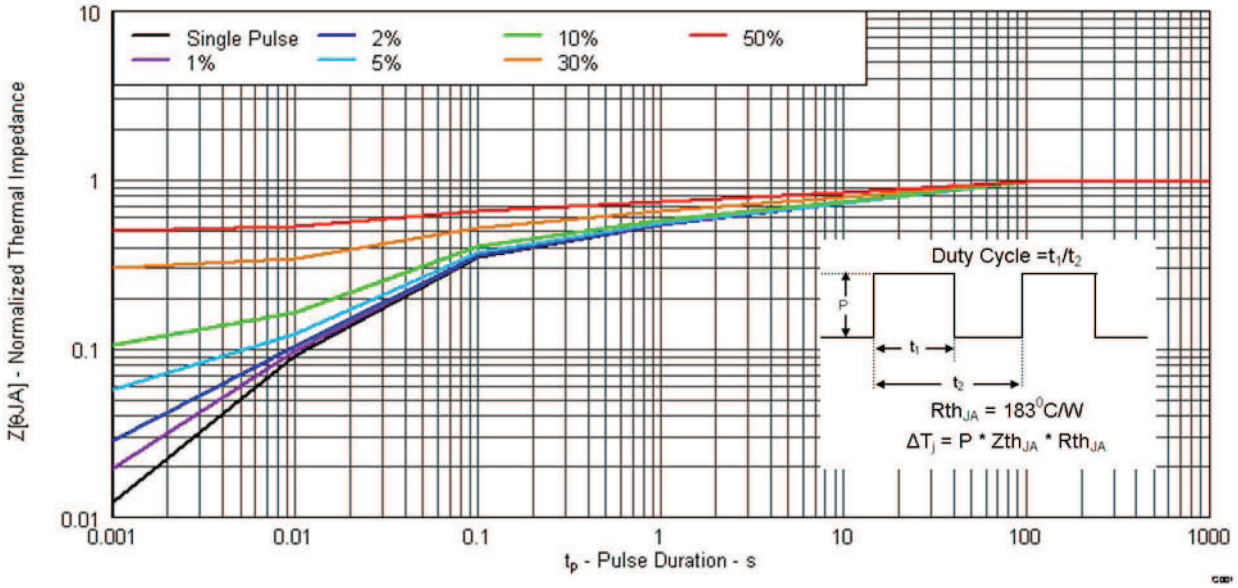


Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

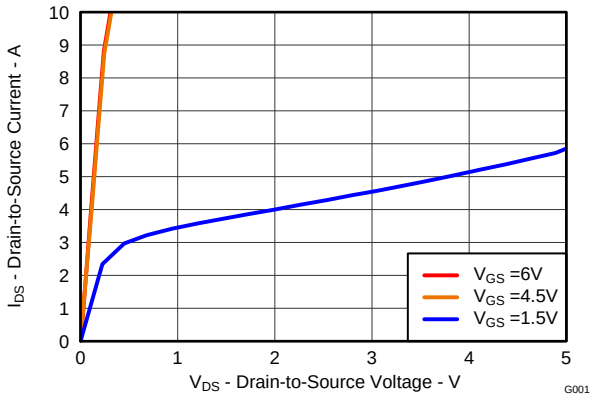


Figure 3. Saturation Characteristics

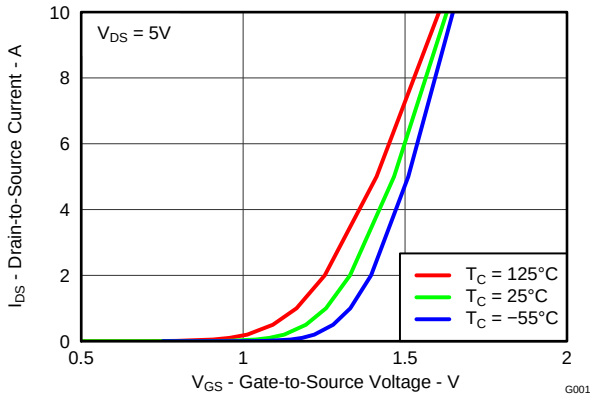


Figure 4. Transfer Characteristics

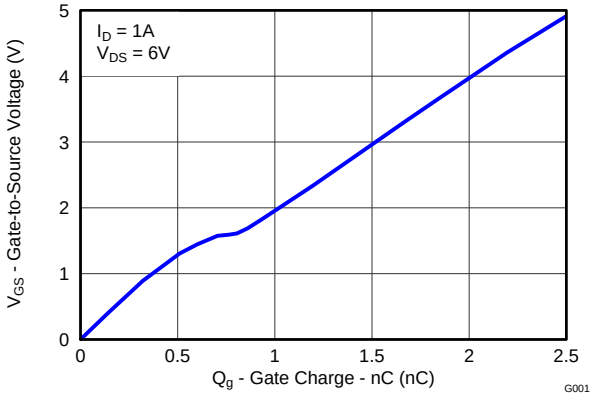


Figure 5. Gate Charge

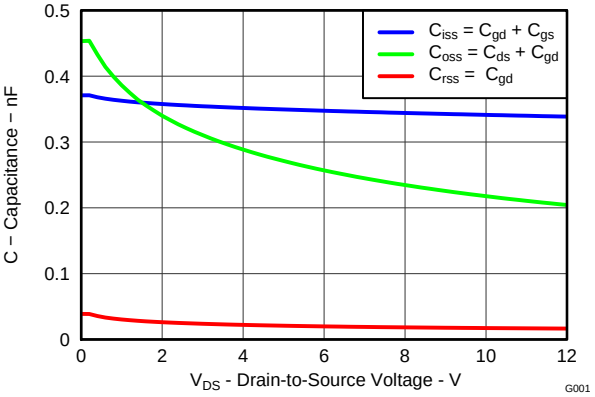


Figure 6. Capacitance

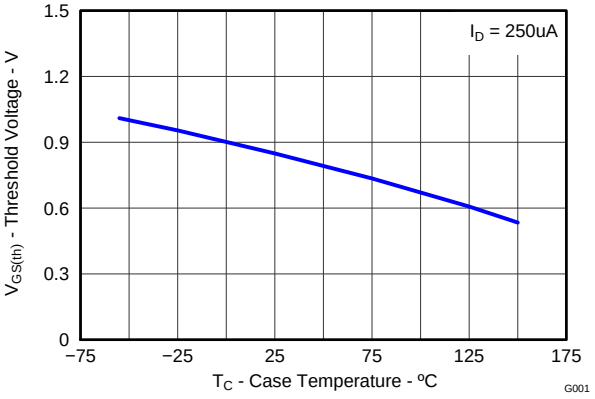


Figure 7. Threshold Voltage vs. Temperature

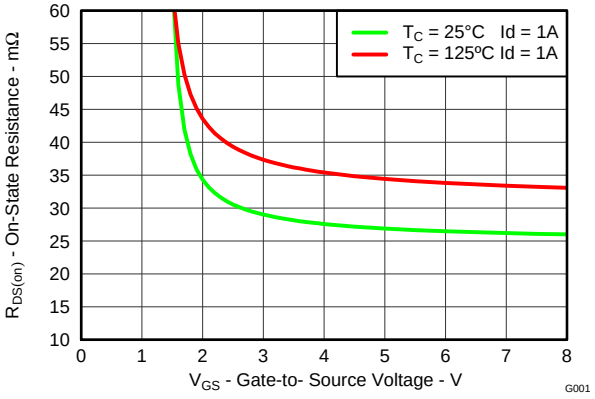


Figure 8. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

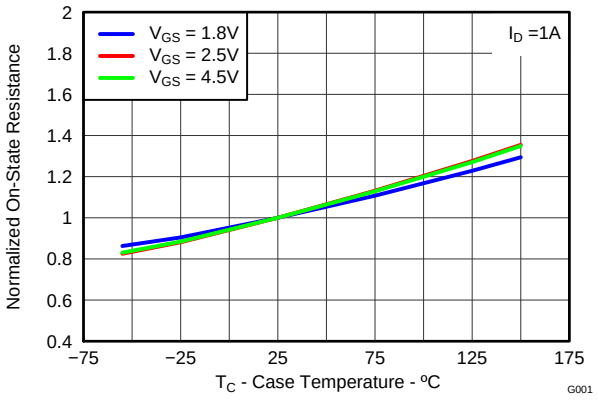


Figure 9. On Resistance vs. Temperature

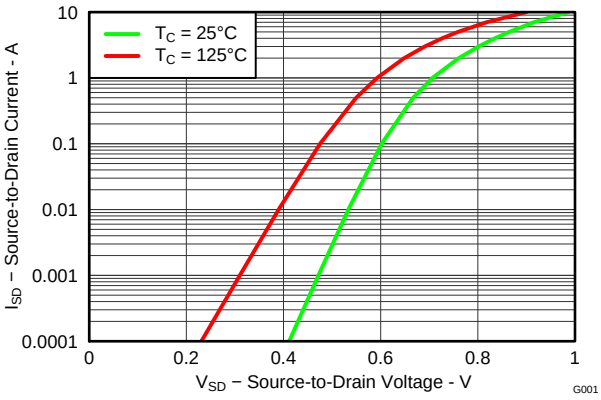


Figure 10. Typical Diode Forward Voltage

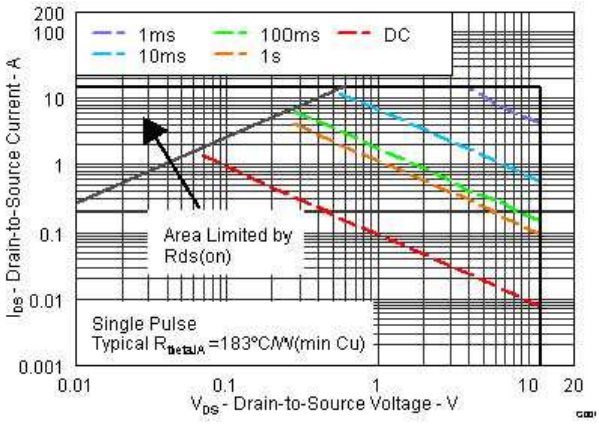


Figure 11. Maximum Safe Operating Area

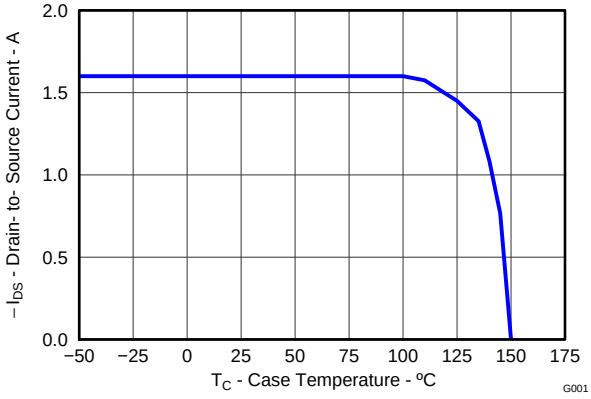
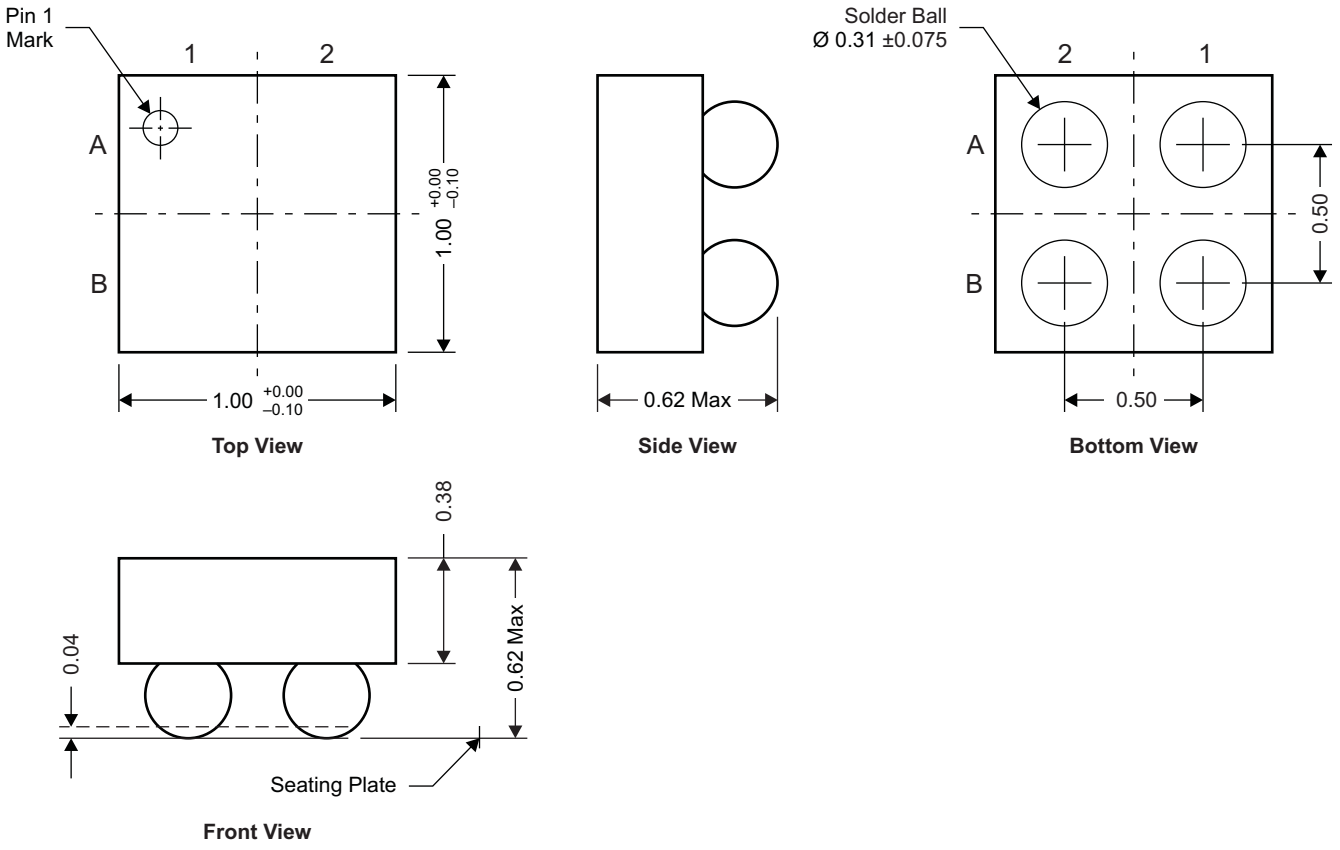


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD13201W10 Package Dimensions

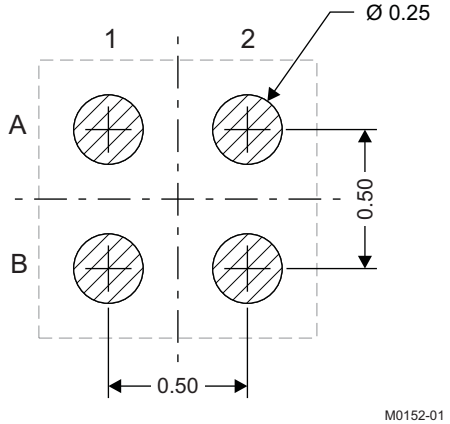


NOTE: All dimensions are in mm (unless otherwise specified)

Pin Configuration Table

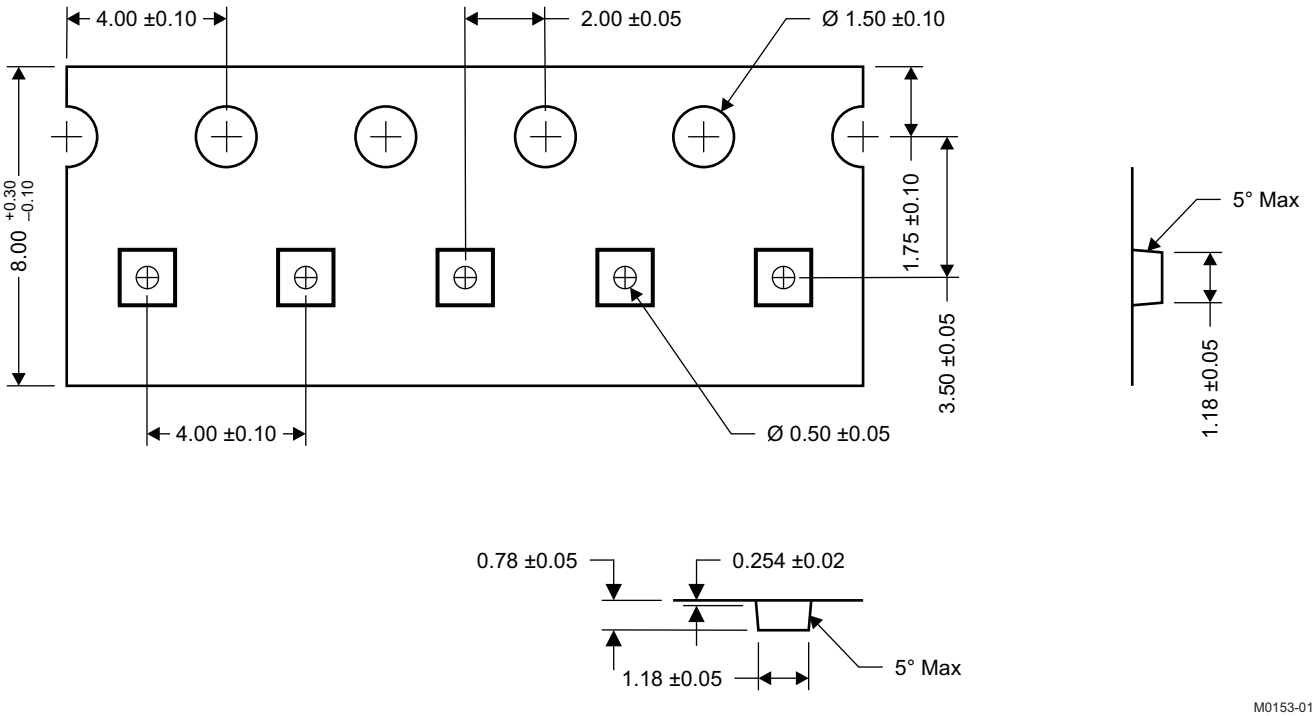
POSITION	DESIGNATION
A2	Source
A1	Gate
B1, B2	Drain

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13201W10	ACTIVE	DSBGA	YZB	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	201	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

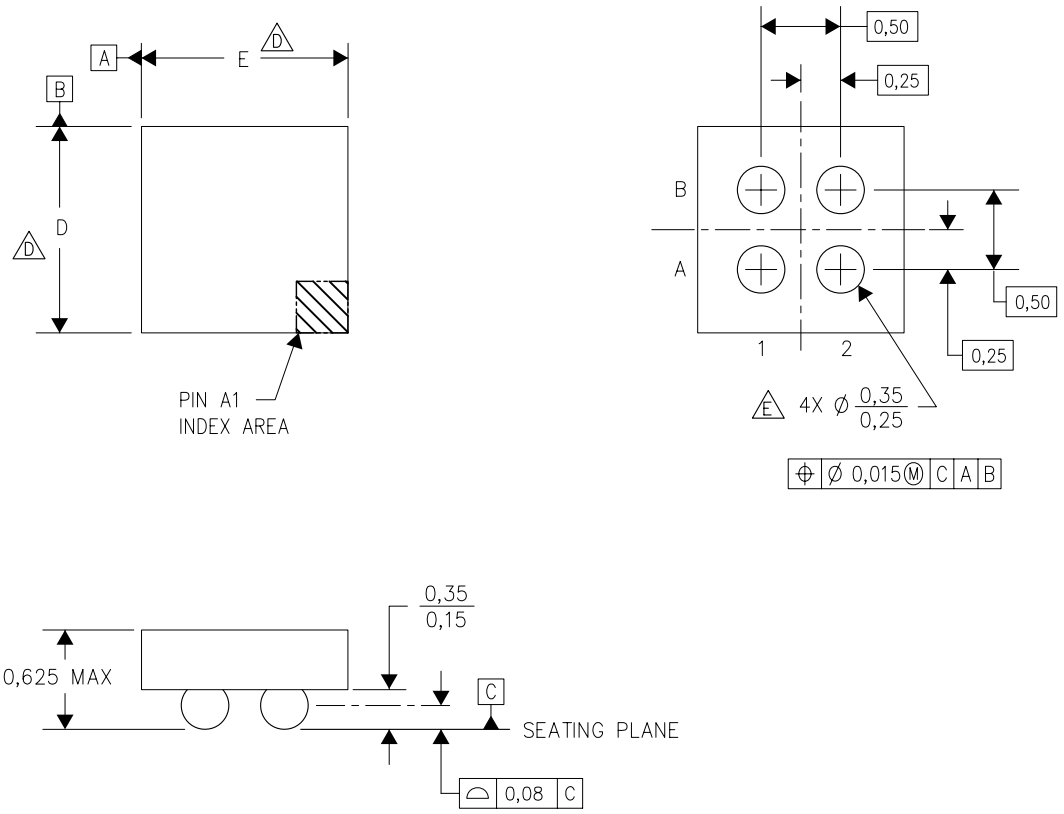
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

YZB (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



4205055/D 07/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
F. This package contains lead–free balls.
Refer to YEB (Drawing #4204178) for tin–lead (SnPb) balls.

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