

## CSD13381F4 12V N 沟道 FemtoFET™ MOSFET

### 1 特性

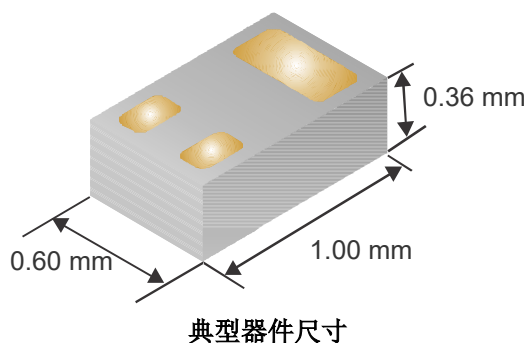
- 低导通电阻
- 低  $Q_g$  和  $Q_{gd}$
- 低阈值电压
- 超小封装尺寸 (0402 外壳尺寸)
  - 1.0mm × 0.6mm
- 超薄型封装
  - 最大高度 : 0.36mm
- 集成型 ESD 保护二极管
  - 额定值 > 4kV HBM
  - 额定值 > 2kV CDM
- 无铅且无卤素
- 符合 RoHS

### 2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 单节电池应用
- 手持式和移动类应用

### 3 说明

此 140mΩ、12V N 沟道 FemtoFET™ MOSFET 技术经过设计和优化，能够尽可能减小许多手持式和移动应用中的空间占用。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小至少 60%。



### 产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
$V_{DS}$	漏源电压	12		V
$Q_g$	栅极电荷总量 (4.5V)	1060		pC
$Q_{gd}$	栅极电荷 (栅漏极)	140		pC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 1.8\text{V}$	310	mΩ
		$V_{GS} = 2.5\text{V}$	170	mΩ
		$V_{GS} = 4.5\text{V}$	140	mΩ
$V_{GS(th)}$	阈值电压	0.85		V

### 订购信息

器件 <sup>(1)</sup>	数量	包装介质	封装	配送
CSD13381F4	3000	7 英寸卷带	Femto (0402) 1.0mm × 0.6mm 无引线 SMD	卷带包装
CSD13381F4T	250			

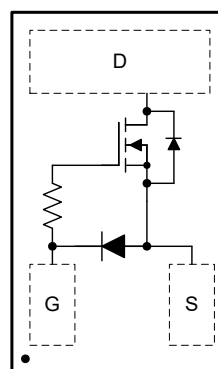
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

### 绝对最大额定值

$T_A = 25^\circ\text{C}$ 时测得，除非另外注明		值	单位
$V_{DS}$	漏源电压	12	V
$V_{GS}$	栅源电压	8	V
$I_D$	持续漏极电流， $T_A = 25^\circ\text{C}$ 时测得 <sup>(1)</sup>	2.1	A
$I_{DM}$	脉冲漏极电流， $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	7	A
$I_G$	持续栅极钳位电流	35	mA
	脉冲栅极钳位电流 <sup>(2)</sup>	350	
$P_D$	功率耗散 <sup>(1)</sup>	500	mW
ESD 等级	人体放电模型 (HBM)	4	kV
	充电器件模型 (CDM)	2	kV
$T_J$ 、 $T_{stg}$	运行结温和贮存温度范围	-55 至 150	°C
$E_{AS}$	雪崩能量，单脉冲 $I_D = 7.4\text{A}$ ， $L = 0.1\text{mH}$ ， $R_G = 25\Omega$	2.7	mJ

(1) 典型  $R_{\theta JA} = 90^\circ\text{C/W}$  (在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm<sup>2</sup>)、2oz、0.071mm 厚的铜焊盘时)。

(2) 脉冲持续时间  $\leq 300\ \mu\text{s}$ ，占空比  $\leq 2\%$



顶视图



## Table of Contents

<b>1 特性</b> .....	<b>1</b>	6.1 Trademarks.....	<b>7</b>
<b>2 应用</b> .....	<b>1</b>	6.2 Electrostatic Discharge Caution.....	<b>7</b>
<b>3 说明</b> .....	<b>1</b>	6.3 术语表.....	<b>7</b>
<b>4 Revision History</b> .....	<b>2</b>	<b>7 Mechanical, Packaging, and Orderable Information</b> ....	<b>8</b>
<b>5 Specifications</b> .....	<b>3</b>	7.1 Mechanical Dimensions.....	<b>8</b>
5.1 Electrical Characteristics.....	<b>3</b>	7.2 Recommended Minimum PCB Layout.....	<b>9</b>
5.2 Thermal Information.....	<b>3</b>	7.3 Recommended Stencil Pattern.....	<b>9</b>
5.3 Typical MOSFET Characteristics.....	<b>4</b>	7.4 CSD13381F4 Embossed Carrier Tape Dimensions..	<b>10</b>
<b>6 Device and Documentation Support</b> .....	<b>7</b>		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision E (October 2021) to Revision F (January 2022)</b>	<b>Page</b>
• 将特性中的最大高度从“0.35mm”更改为“0.36mm” .....	<b>1</b>
• 将典型器件尺寸中的封装高度从“0.35mm”更改为“0.36mm” .....	<b>1</b>
• Changed package height from "0.35 mm" to "0.36 mm" in <i>Mechanical Dimensions</i> .....	<b>8</b>
<b>Changes from Revision D (May 2015) to Revision E (October 2021)</b>	<b>Page</b>
• Added footnote with link to support document.....	<b>9</b>
<b>Changes from Revision C (September 2014) to Revision D (May 2015)</b>	<b>Page</b>
• Corrected typo for I <sub>GSS</sub> Test Condition .....	<b>3</b>

## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	12			V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 9.6\text{ V}$			100	nA
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 8\text{ V}$			50	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.65	0.85	1.10	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 1.8\text{ V}, I_{DS} = 0.5\text{ A}$		310	400	m $\Omega$
		$V_{GS} = 2.5\text{ V}, I_{DS} = 0.5\text{ A}$		170	225	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_{DS} = 0.5\text{ A}$		140	180	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 6\text{ V}, I_{DS} = 0.5\text{ A}$		3.2		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 6\text{ V}, f = 1\text{ MHz}$		155	200	pF
$C_{oss}$	Output Capacitance			47	62	pF
$C_{riss}$	Reverse Transfer Capacitance			2.5	3.3	pF
$R_G$	Series Gate Resistance			23		$\Omega$
$Q_g$	Gate Charge Total (4.5 V)	$V_{DS} = 6\text{ V}, I_{DS} = 0.5\text{ A}$		1060	1400	pC
$Q_{gd}$	Gate Charge Gate-to-Drain			140		pC
$Q_{gs}$	Gate Charge Gate-to-Source			230		pC
$Q_{g(th)}$	Gate Charge at $V_{th}$			155		pC
$Q_{oss}$	Output Charge	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$		1120		pC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_{DS} = 0.5\text{ A}, R_G = 2\ \Omega$		3.7		ns
$t_r$	Rise Time			1.5		ns
$t_{d(off)}$	Turn Off Delay Time			11.0		ns
$t_f$	Fall Time			3.8		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 0.5\text{ A}, V_{GS} = 0\text{ V}$		0.73	0.9	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 6\text{ V}, I_F = 0.5\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		1550		pC
$t_{rr}$	Reverse Recovery Time			6		ns

### 5.2 Thermal Information

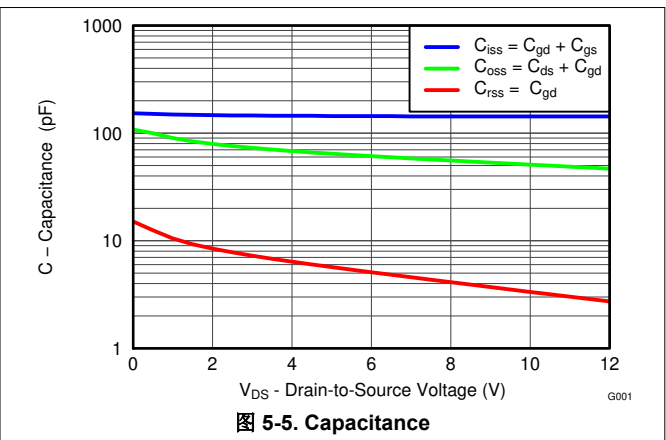
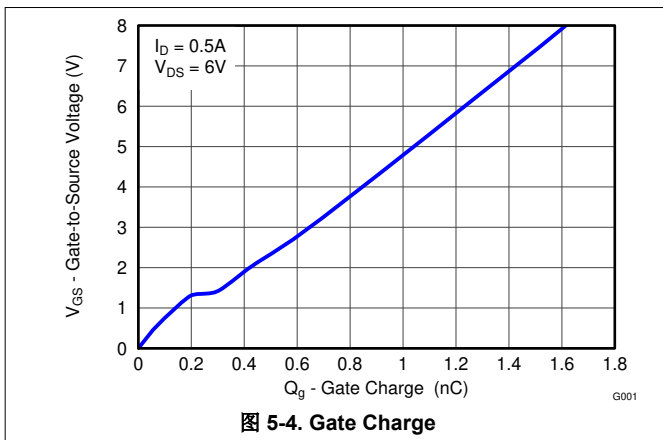
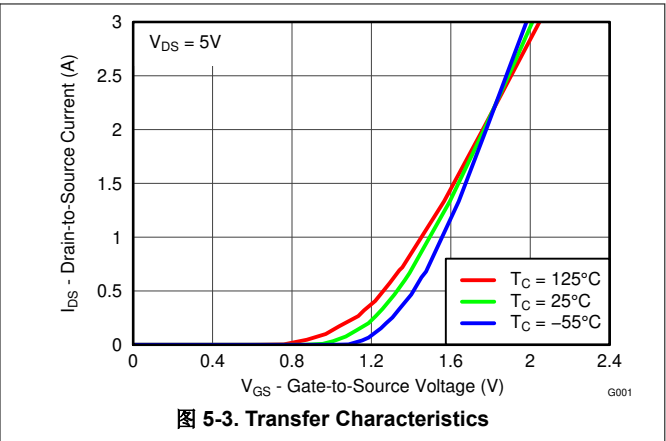
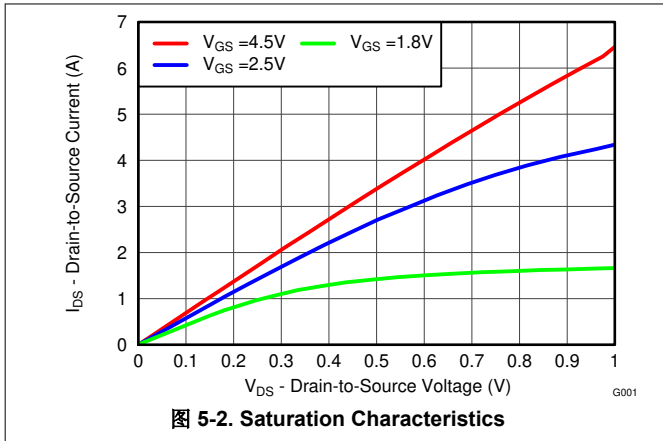
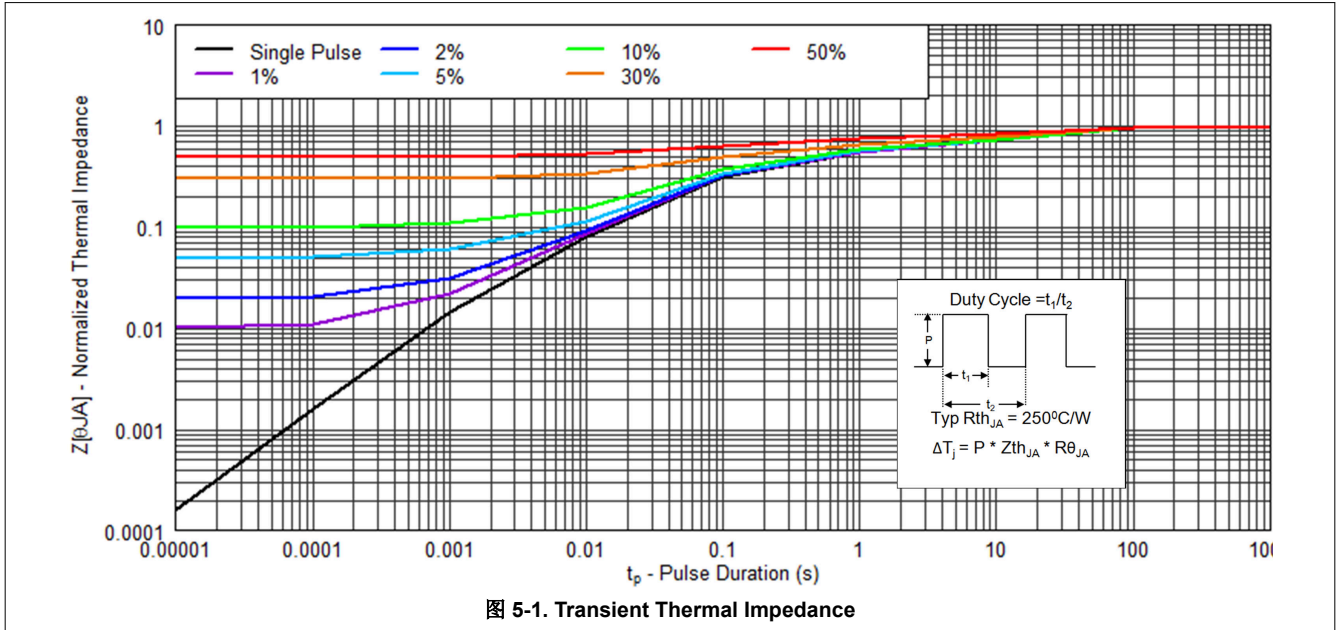
( $T_A = 25^\circ\text{C}$  unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>(1)</sup>	90	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance <sup>(2)</sup>	250	

- (1) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.  
(2) Device mounted on FR4 material with minimum Cu mounting area.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



### 5.3 Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

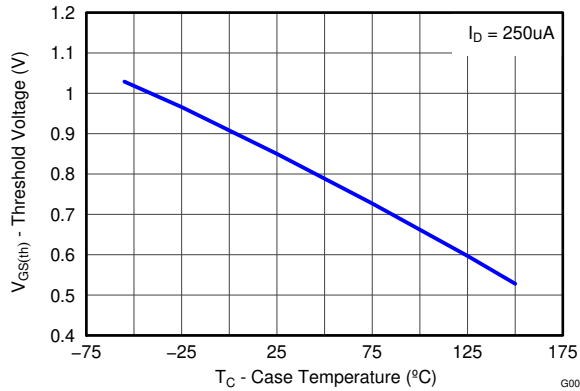


图 5-6. Threshold Voltage vs Temperature

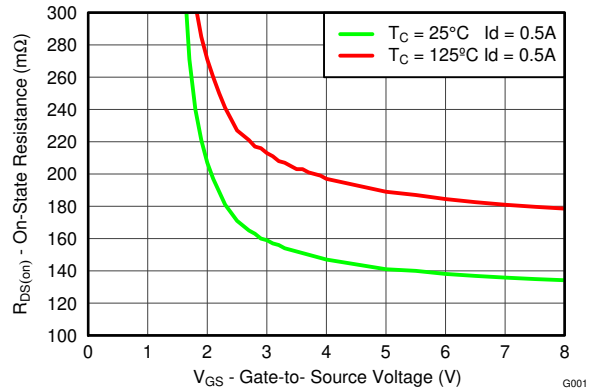


图 5-7. On-State Resistance vs Gate-to-Source Voltage

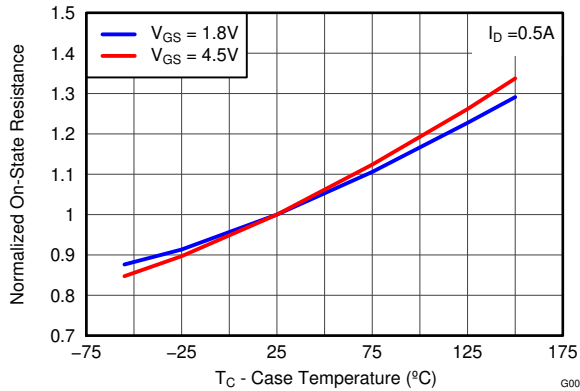


图 5-8. Normalized On-State Resistance vs Temperature

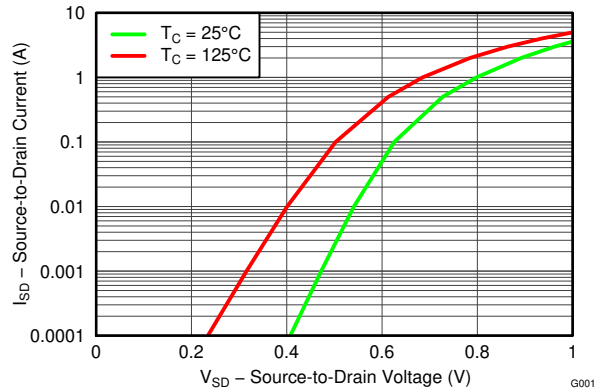


图 5-9. Typical Diode Forward Voltage

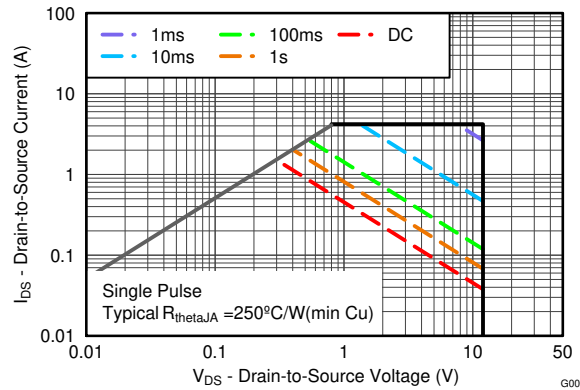


图 5-10. Maximum Safe Operating Area (SOA)

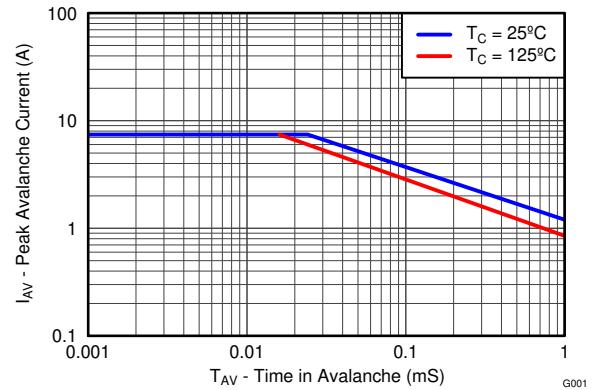


图 5-11. Single Pulse Unclamped Inductive Switching

### 5.3 Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

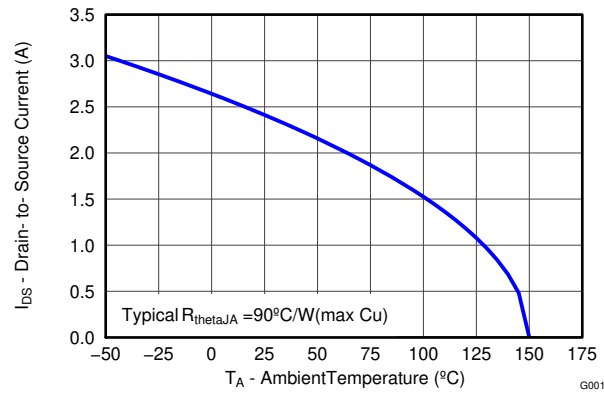


图 5-12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Trademarks

FemtoFET™ is a trademark of Texas Instruments.  
所有商标均为其各自所有者的财产。

### 6.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 6.3 术语表

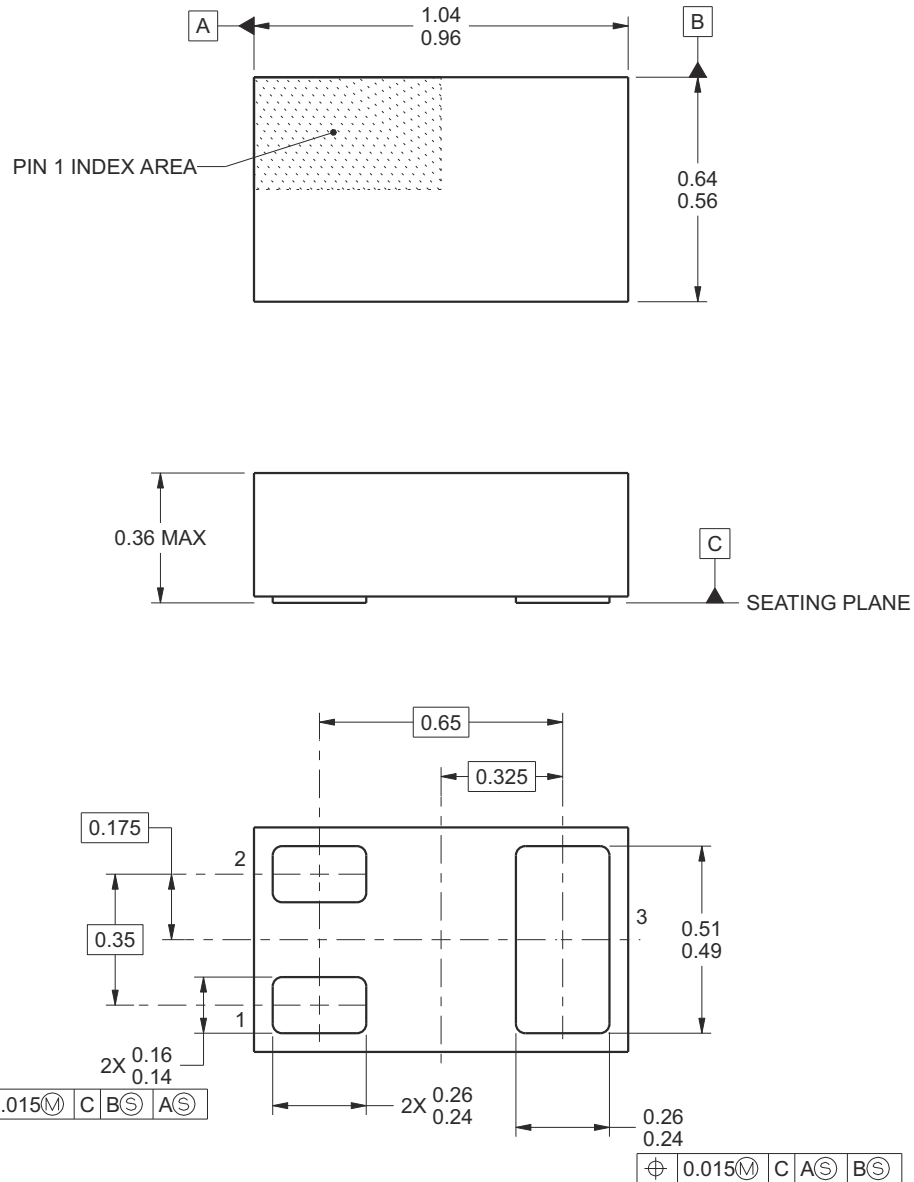
#### [TI 术语表](#)

本术语表列出并解释了术语、首字母缩略词和定义。

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

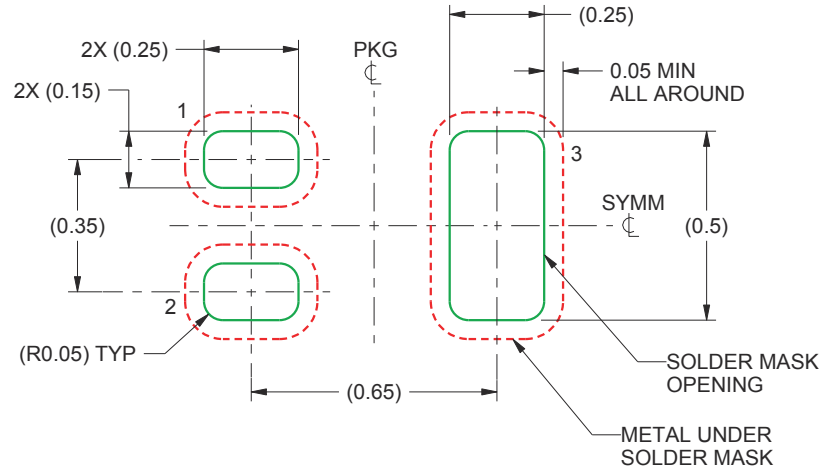
### 7.1 Mechanical Dimensions



- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a PB-free solder land design.

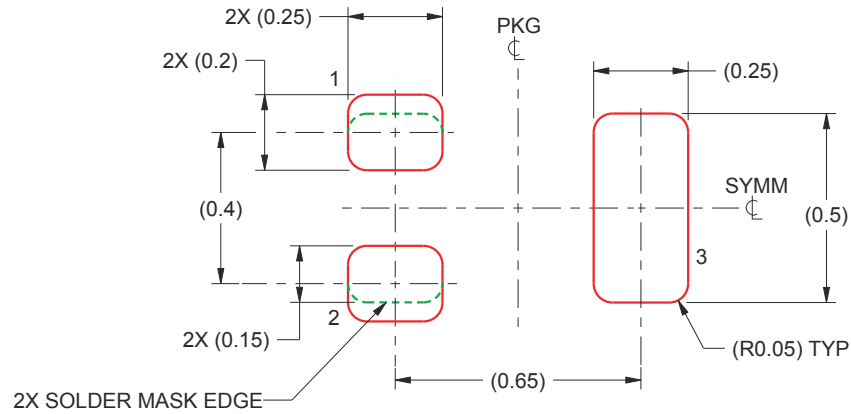


## 7.2 Recommended Minimum PCB Layout



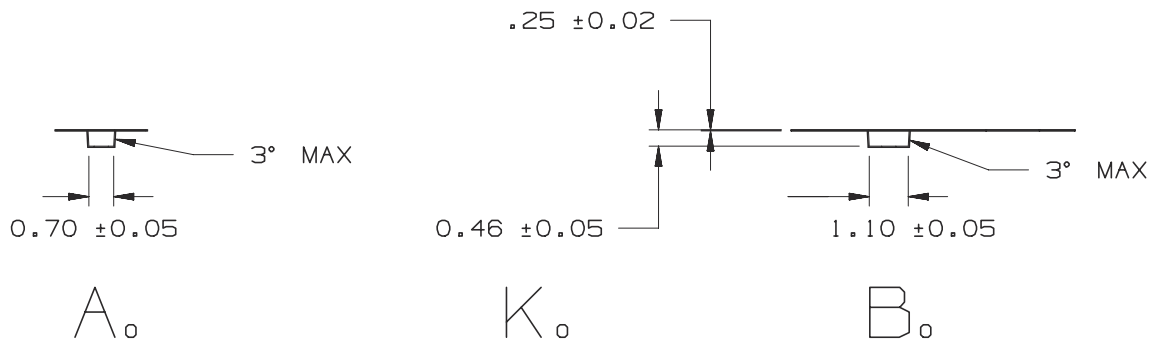
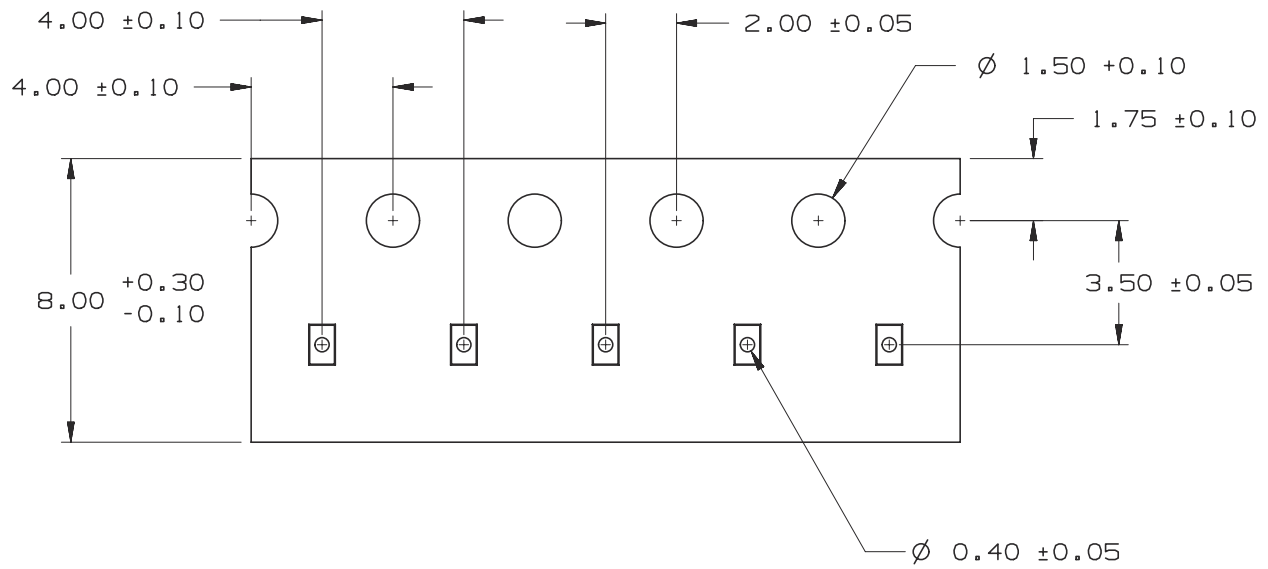
- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide \(SLRA003D\)](#).

## 7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

### 7.4 CSD13381F4 Embossed Carrier Tape Dimensions



- A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13381F4	ACTIVE	PICOSTAR	YJC	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	DQ	<a href="#">Samples</a>
CSD13381F4T	ACTIVE	PICOSTAR	YJC	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	DQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13381F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13381F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13381F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD13381F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司