CSD17318Q2 30V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 针对 5V 栅极驱动进行了优化
- 低电容和电荷
- 低 $R_{DS(ON)}$
- 低热阻
- 无铅
- 符合 RoHS
- 无卤素
- SON 2mm × 2mm 塑料封装

2 应用

- 存储、平板电脑和手持设备
- 针对负载开关应用进行了优化
- 直流/直流转换器
- 电池和负载管理应用

3 说明

该 30V 12.6mΩ 2mm x 2mm SON NexFET™ 功率 MOSFET 可以极大地降低功率转换应用中的损耗，并针对 5V 栅极驱动应用进行了优化。2mm × 2mm SON 封装可提供相对于封装尺寸而言出色的热性能。

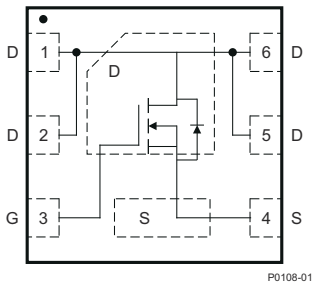
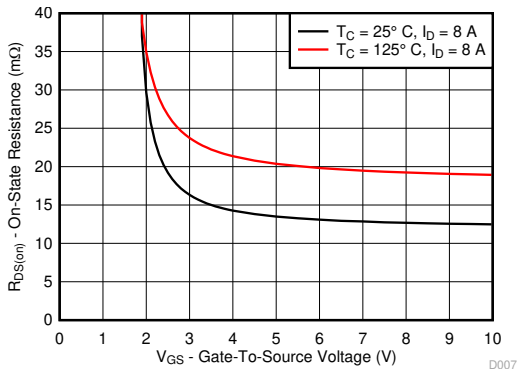


图 3-1. 顶视图



导通电阻与栅极至源极电压

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	6.0		nC
Q_{gd}	栅极电荷（栅极到漏极）	1.3		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 2.5V	20	mΩ
		V_{GS} = 4.5V	13.9	
		V_{GS} = 8V	12.6	
$V_{GS(th)}$	阈值电压	0.9		V

器件信息 (1)

器件型号	数量	介质	封装	运输
CSD17318Q2	3000	7 英寸卷带	SON 2.00mm × 2.00mm 塑料封装	卷带包装
CSD17318Q2T	250			

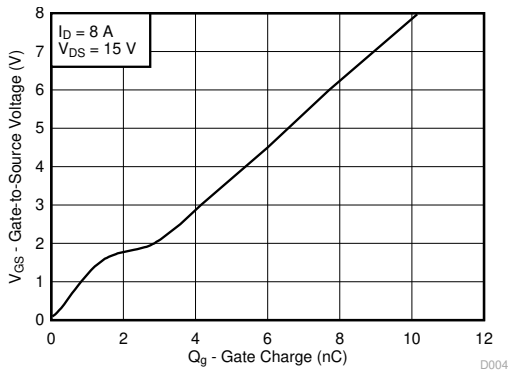
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±10	V
I_D	持续漏极电流（受封装限制）	21.5	A
	持续漏极电流（受器件限制），T_C = 25°C 时测得	25	
	持续漏极电流(1)	10	
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	68	A
P_D	功率耗散(1)	2.5	W
	功率耗散，T_C = 25°C	16	
T_J，T_{STG}	工作结温，贮存温度	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 12.4A，L = 0.1mH，R_G = 25Ω	7.7	mJ

(1) 0.06 英寸厚 FR4 PCB 上 1 平方英寸、2oz 铜焊盘上的 $R_{\theta JA}$ = 55°C/W（典型值）。

(2) 最大 $R_{\theta JC}$ = 7°C/W，脉冲持续时间 ≤ 100 µs，占空比 ≤ 1%。



栅极电荷

Table of Contents

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

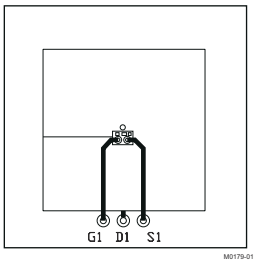
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-source leakage	V_{GS} = 0V, V_{DS} = 24V			1	μA
I_{GSS}	Gate-to-source leakage	V_{DS} = 0V, V_{GS} = 10V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.6	0.9	1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5V, I_D = 8A		20	30	mΩ
		V_{GS} = 4.5V, I_D = 8A		13.9	16.9	
		V_{GS} = 8V, I_D = 8A		12.6	15.1	
g_{fs}	Transconductance	V_{DS} = 3V, I_D = 8A		42		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		676	879	pF
C_{oss}	Output capacitance			71	92	pF
C_{rss}	Reverse transfer capacitance			39	51	pF
R_G	Series gate resistance			1.0	2.0	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15V, I_D = 8A		6.0		nC
Q_{gd}	Gate charge gate-to-drain			1.3		nC
Q_{gs}	Gate charge gate-to-source			1.5		nC
$Q_{g(th)}$	Gate charge at Vth			0.7		nC
Q_{oss}	Output charge	V_{DS} = 15V, V_{GS} = 0V		2.7		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15V, V_{GS} = 4.5V, I_D = 8A, R_G = 2Ω		5		ns
t_r	Rise time			16		ns
$t_{d(off)}$	Turnoff delay time			13		ns
t_f	Fall time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 8A, V_{GS} = 0V		0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{DD}= 15V, I_F = 8A, di/dt = 300A/μs		2.9		nC
t_{rr}	Reverse recovery time			12		ns

4.2 Thermal Characteristics

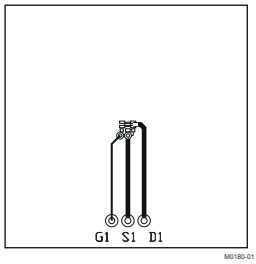
T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance junction-to-case(1)			7.9	°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient(1) (2)			65	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1in² (6.45cm²), 2oz (0.071mm) thick Cu pad on a 1.5in × 1.5in (3.81cm × 3.81cm), 0.06in (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1in² (6.45cm²), 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 65°C/W when mounted on 1in^2 (6.45cm^2) of 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 250°C/W when mounted on a minimum pad area of 2oz (0.071mm) thick Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

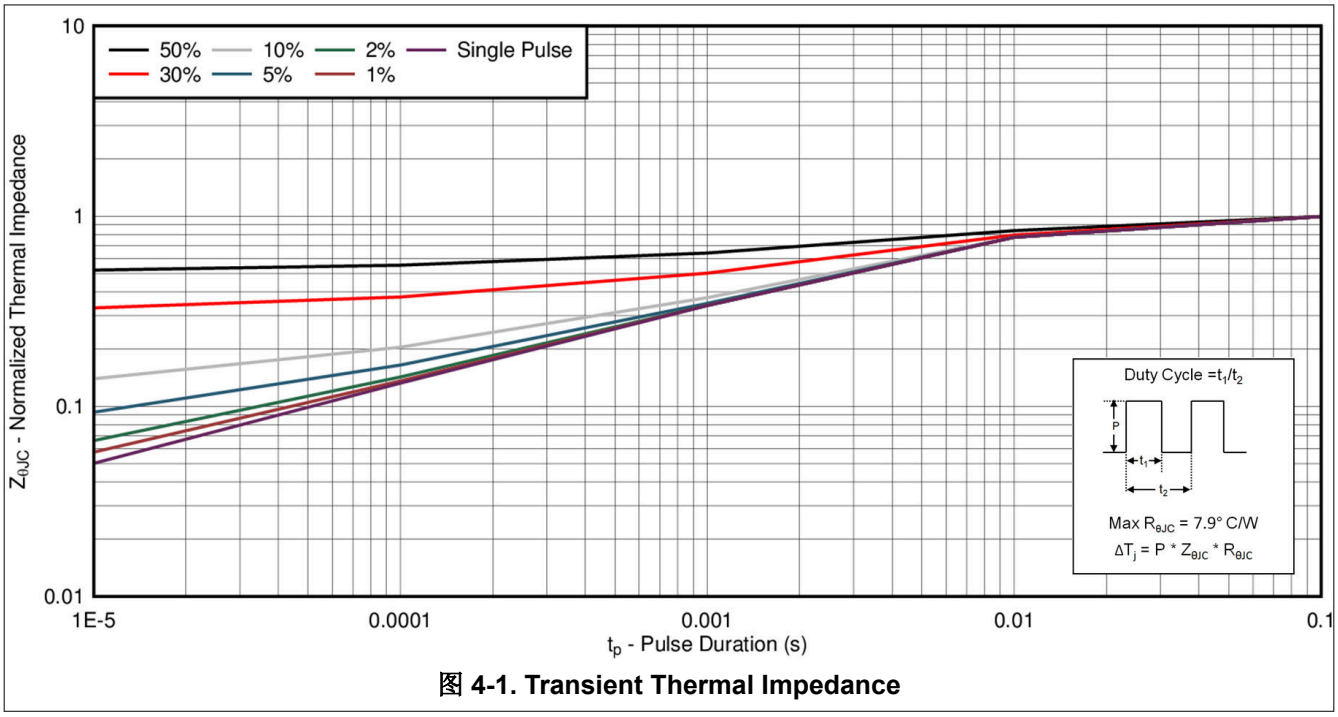


图 4-1. Transient Thermal Impedance

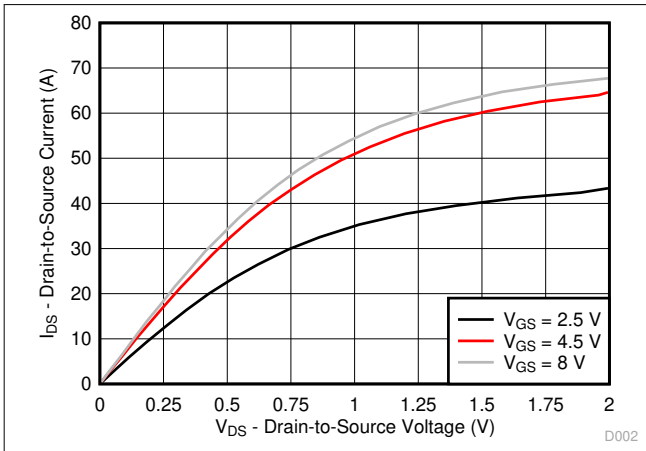
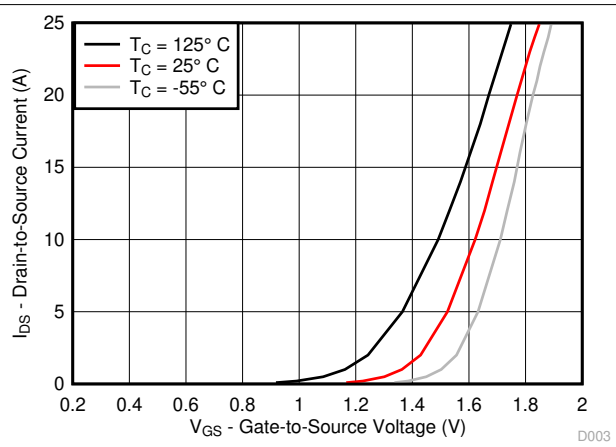
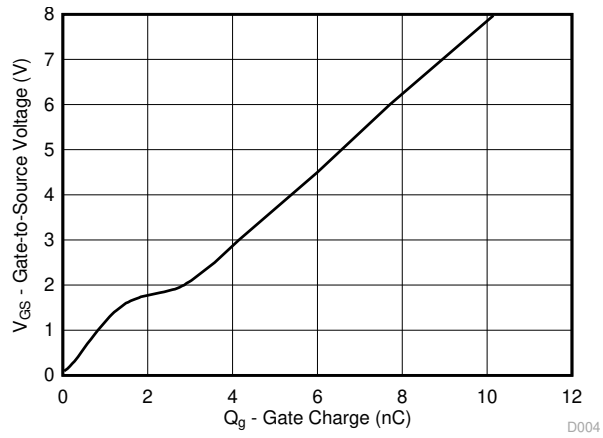


图 4-2. Saturation Characteristics



V_{DS} = 5V

图 4-3. Transfer Characteristics



I_D = 8A V_{DS} = 15V

图 4-4. Gate Charge

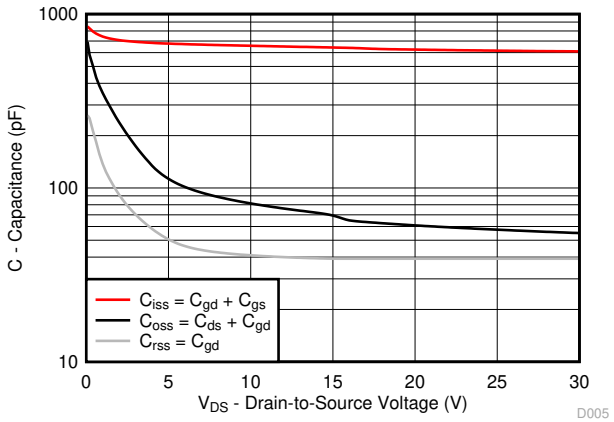
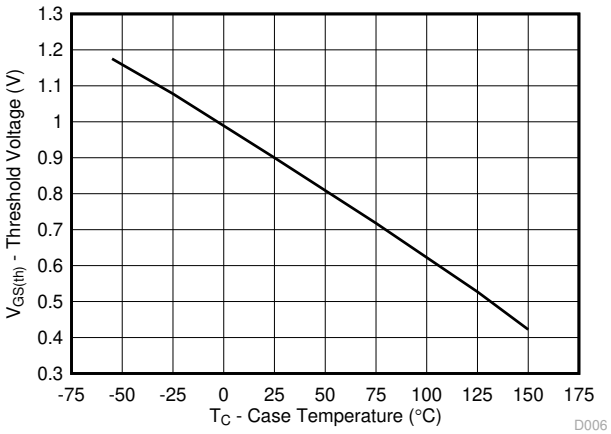
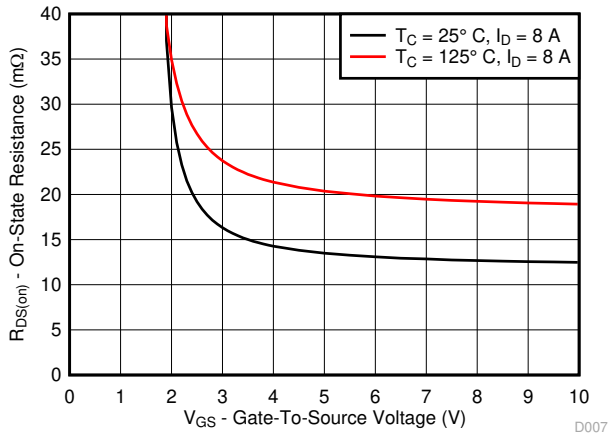


图 4-5. Capacitance



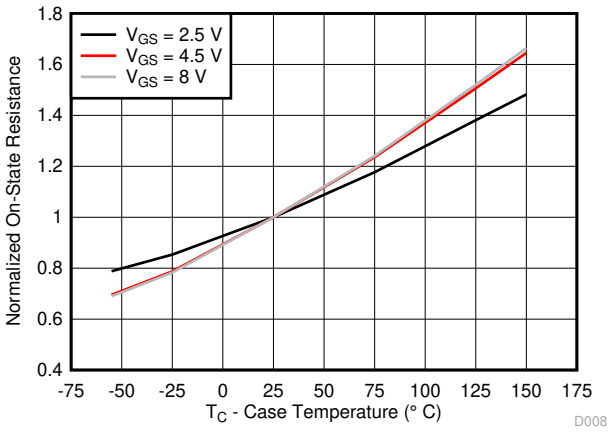
I_D = 250µA

图 4-6. Threshold Voltage vs Temperature



I_D = 8A

图 4-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 8A

图 4-8. Normalized On-State Resistance vs Temperature

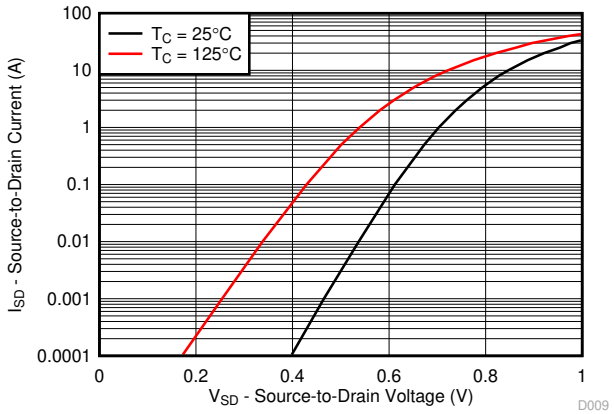
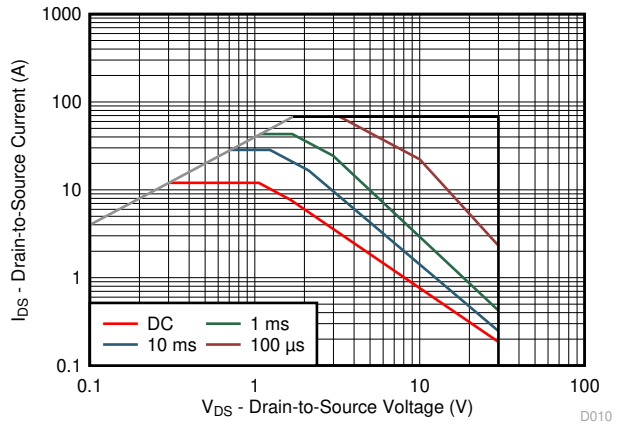


图 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 7.9°C/W

图 4-10. Maximum Safe Operating Area

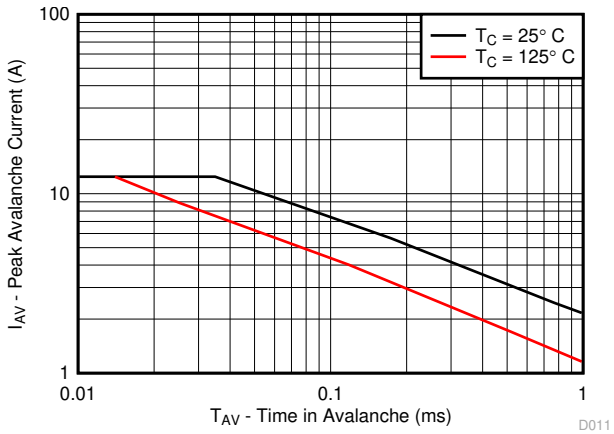


图 4-11. Single Pulse Unclamped Inductive Switching

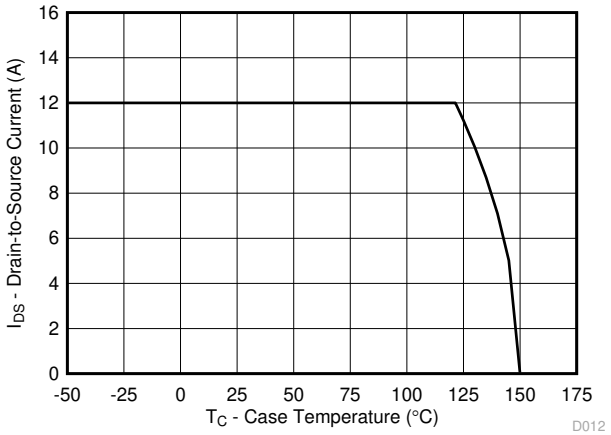


图 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.3 Trademarks

NexFET™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

6 Revision History

Changes from Revision A (February 2017) to Revision B (June 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17318Q2	ACTIVE	WSON	DQK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1718	Samples
CSD17318Q2T	ACTIVE	WSON	DQK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1718	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

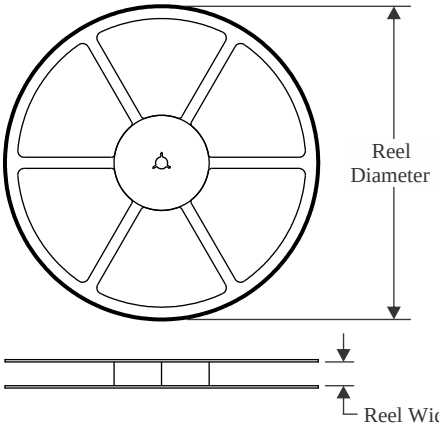
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

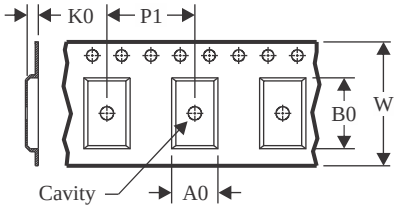
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

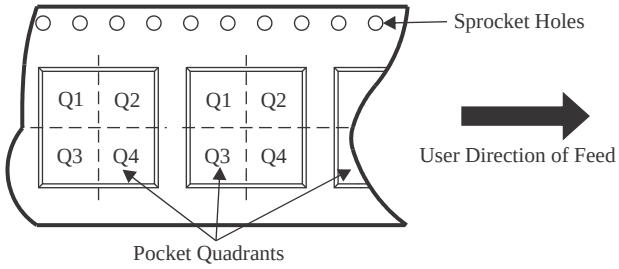


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

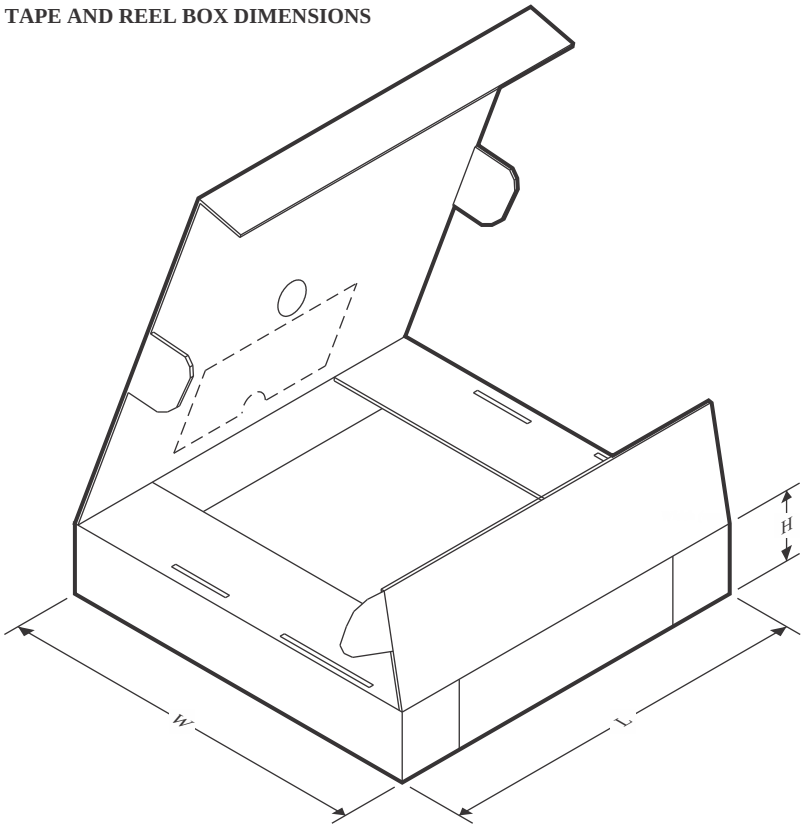
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17318Q2	WSON	DQK	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1
CSD17318Q2T	WSON	DQK	6	250	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17318Q2	WSON	DQK	6	3000	189.0	185.0	36.0
CSD17318Q2T	WSON	DQK	6	250	189.0	185.0	36.0

GENERIC PACKAGE VIEW

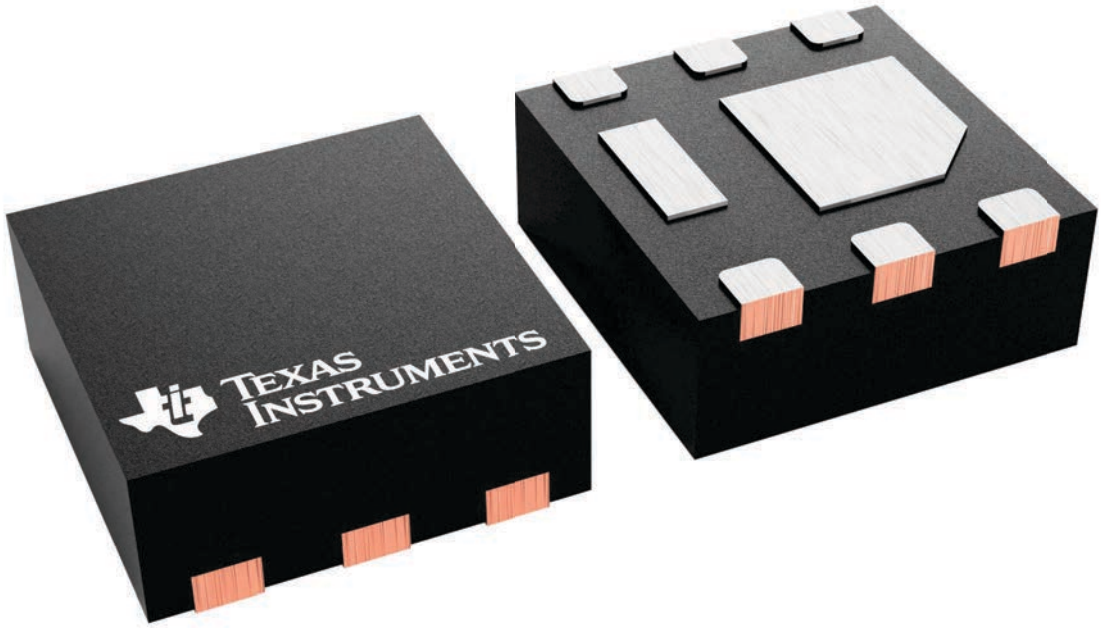
DQK 6

WSON - 0.8 mm max height

2 x 2, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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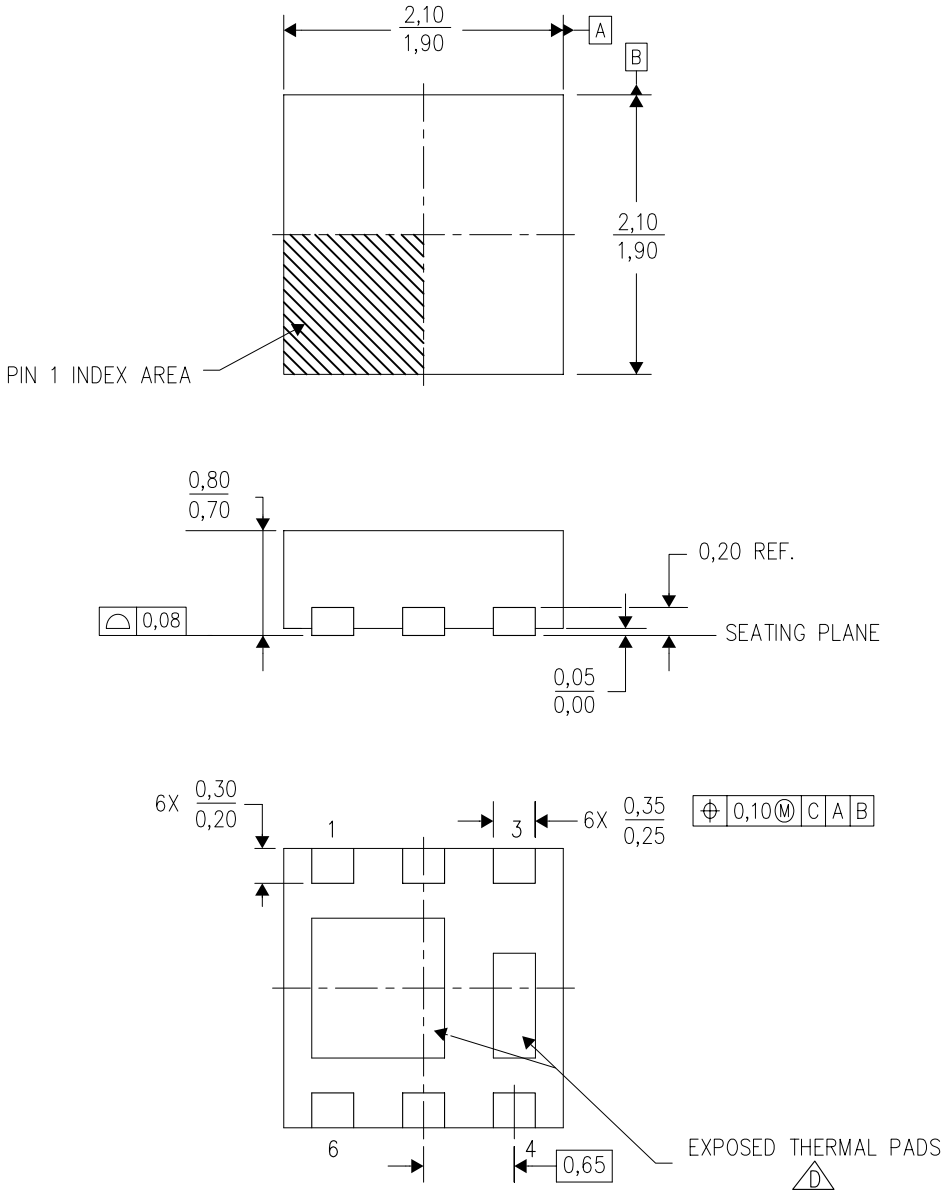
DQK (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4210192/B 01/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

THERMAL PAD MECHANICAL DATA

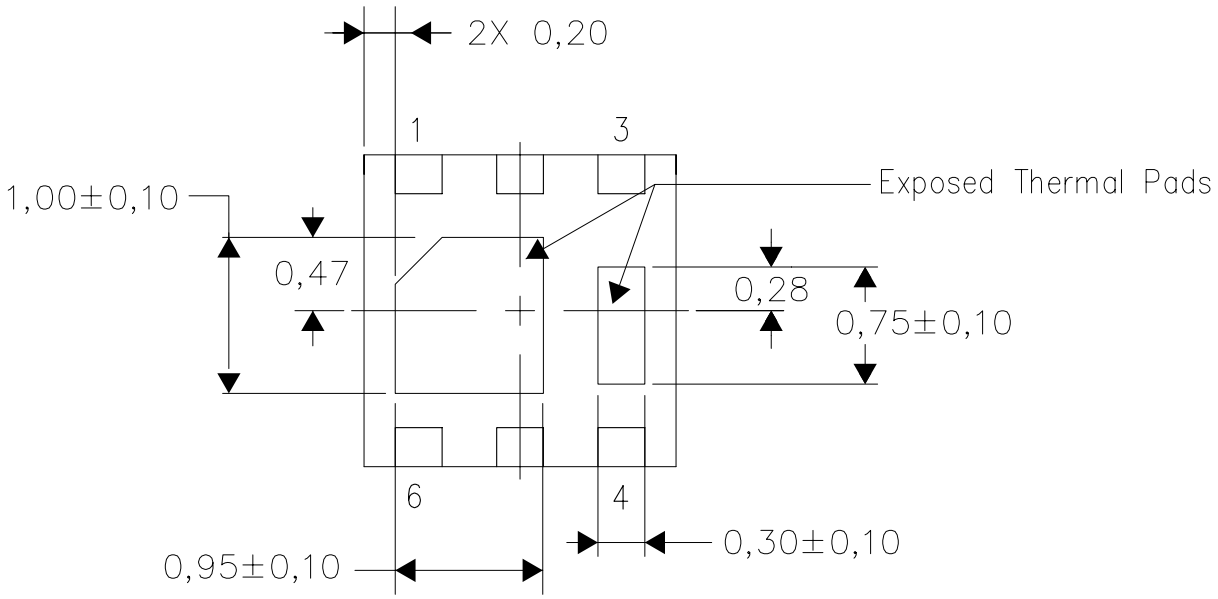
DQK (S–PWSON–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

重要声明和免责声明

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