



30V、N 沟道 NexFET™ 功率 MOSFET

 查询样品: [CSD17322Q5A](#)

特性

- 针对 **5V** 栅极驱动而优化
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定
- 无铅终端镀层
- 符合 **RoHS** 标准
- 无卤素
- **SON 5 毫米 × 6 毫米** 塑料封装

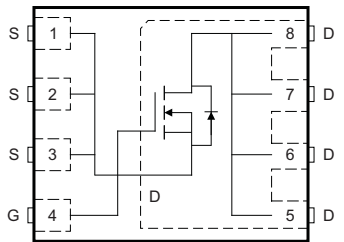
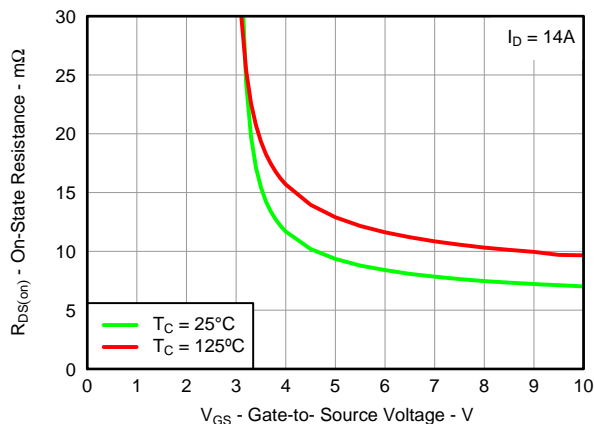
应用

- 笔记本电脑负载点
- 网络、电信和计算系统中的负载点同步降压

说明

此 NexFET™ 功率 MOSFET 专为最大限度地减少功率转换应用中的损耗而设计，并针对 **5V** 栅极驱动应用进行了优化。

图 1. 顶视图


 $R_{DS(on)}$ vs V_{GS}


产品汇总

V_{DS}	漏极至源极电压	30	V
Q_g	总栅极电荷 (4.5V)	3.6	nC
Q_{gd}	栅极电荷 (栅极至漏极)	1.1	nC
$R_{DS(on)}$	漏极至源极导通电阻	$V_{GS} = 4.5V$	10 mΩ
		$V_{GS} = 8V$	7.3 mΩ
$V_{GS(th)}$	门限电压	1.6	V

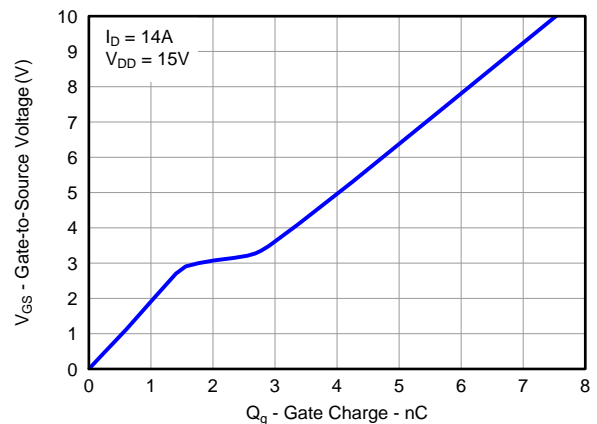
订购信息

器件	封装	介质	数量	出货
CSD17322Q5A	SON 5 毫米 × 6 毫米塑料封装	13 英寸卷带	2500	卷带封装

最大绝对额定值

$T_A = 25^\circ C$, 除非另有说明。		数值	单位
V_{DS}	漏极至源极电压	30	V
V_{GS}	漏极至源极电压	+10 / -10	V
I_D	连续漏极电流, $T_C = 25^\circ C$	87	A
	连续漏极电流 ⁽¹⁾	16	A
$I_{数据手册}$	脉冲漏极电流, $T_A = 25^\circ C$ ⁽²⁾	104	A
P_D	功耗 ⁽¹⁾	3	W
T_J, T_{STG}	工作结温及存储温度范围	-55 至 150	$^\circ C$
E_{AS}	雪崩能量, 单脉冲 $I_D = 33A, L = 0.1mH, R_G = 25\Omega$	54	mJ

- (1) 典型 $R_{\theta JA} = 41^\circ C/W$, 在一个 1 英寸² (6.45-cm²)、2 盎司 (0.071-mm 厚) 铜焊盘上, 该焊盘位于一块厚度为 0.06 英寸 (1.52-mm) 的 FR4 PCB 之上。
- (2) 脉冲持续时间 $\leq 300\mu s$, 占空比 $\leq 2\%$

GATE CHARGE


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NexFET is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

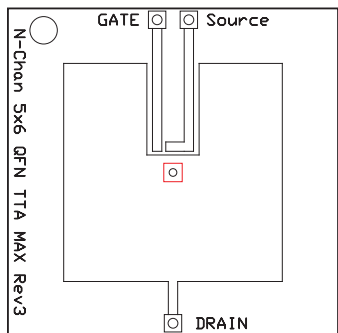
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10 / -10V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.1	1.6	2.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 14A$		10	12.4	$m\Omega$
		$V_{GS} = 8V, I_D = 14A$		7.3	8.8	$m\Omega$
g_{fs}	Transconductance	$V_{DS} = 15V, I_D = 14A$		37		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		580	695	pF
C_{oss}	Output Capacitance			390	470	pF
C_{riss}	Reverse Transfer Capacitance			35	44	pF
R_G	Series Gate Resistance			4.7		Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_D = 14A$		3.6	4.3	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			1.6		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.9		nC
Q_{oss}	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		8.6		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V,$ $I_{DS} = 14A, R_G = 2\Omega$		6.7		ns
t_r	Rise Time			12		ns
$t_{d(off)}$	Turn Off Delay Time			10.5		ns
t_f	Fall Time			3.7		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD} = 14A, V_{GS} = 0V$		0.85	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 13V, I_F = 14A,$ $di/dt = 300A/\mu s$		19.6		nC
t_{rr}	Reverse Recovery Time			17.8		ns

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

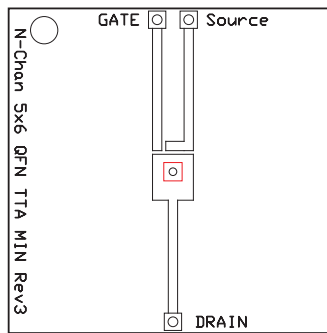
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			51	$^\circ\text{C/W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 51^\circ\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

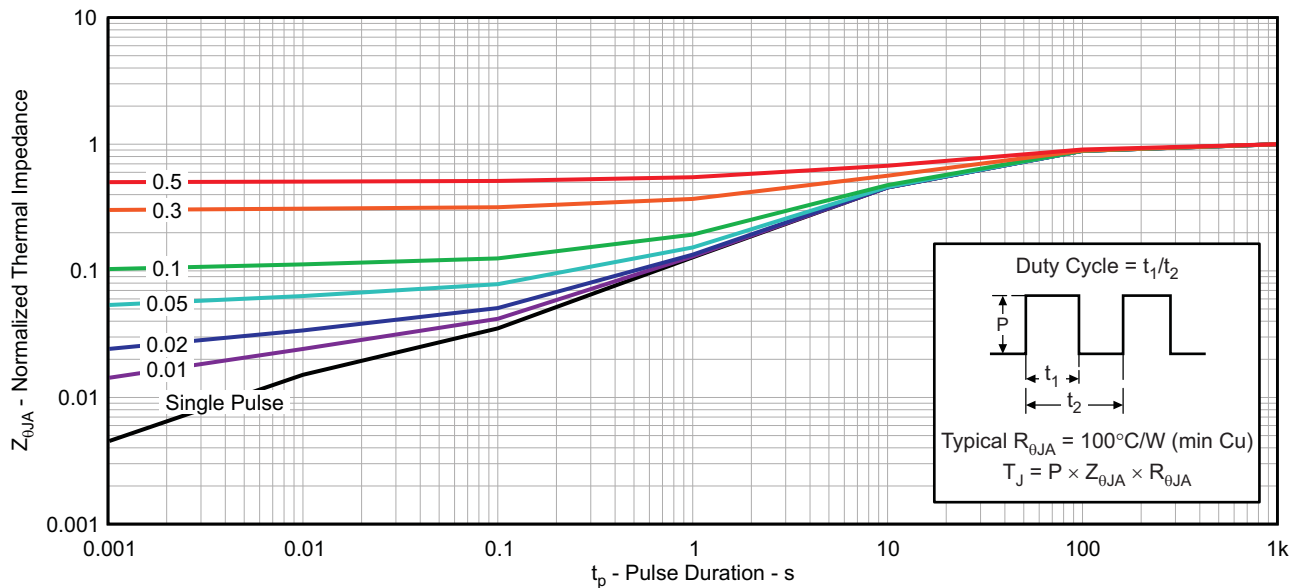


M0137-02

Max $R_{\theta JA} = 125^\circ\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)



G012

Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

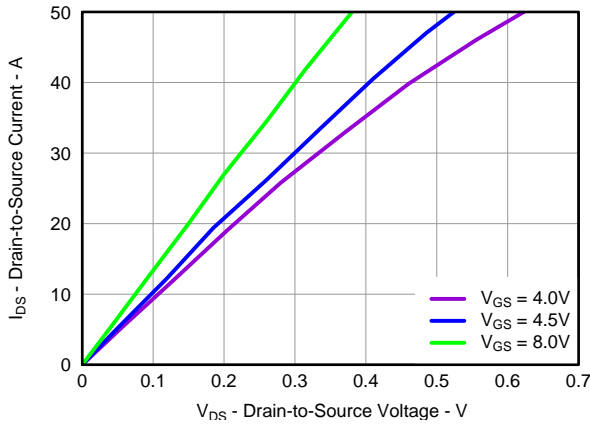


Figure 3. Saturation Characteristics

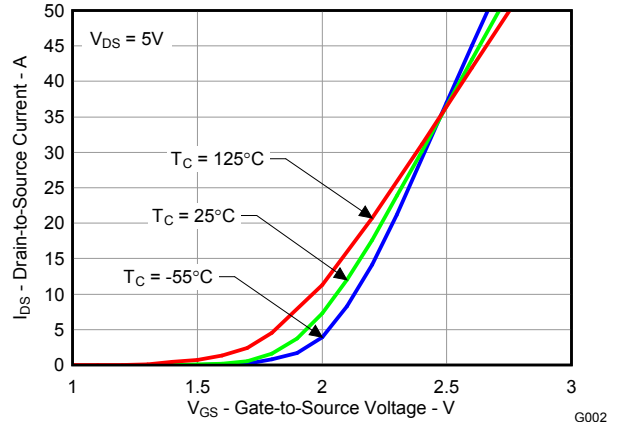


Figure 4. Transfer Characteristics

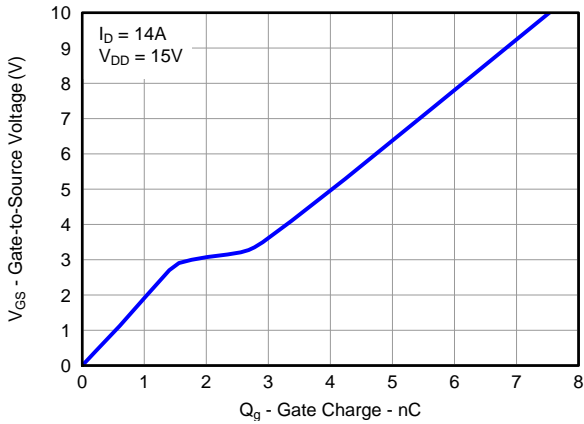


Figure 5. Gate Charge

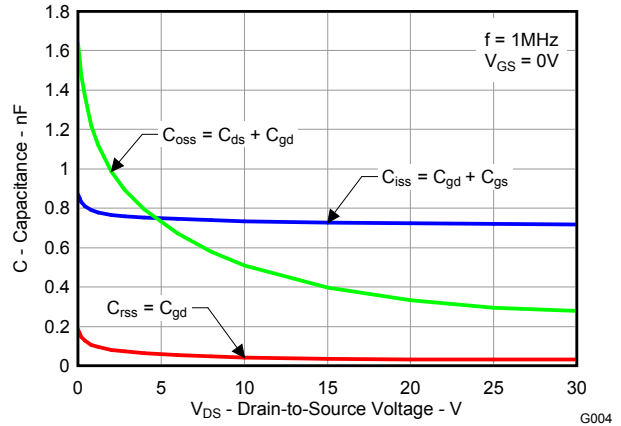


Figure 6. Capacitance

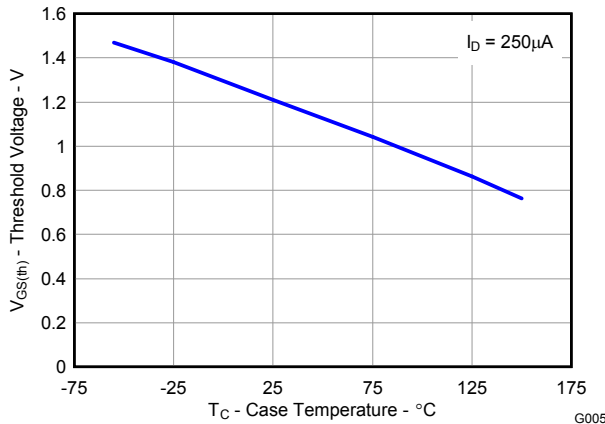


Figure 7. Threshold Voltage vs. Temperature

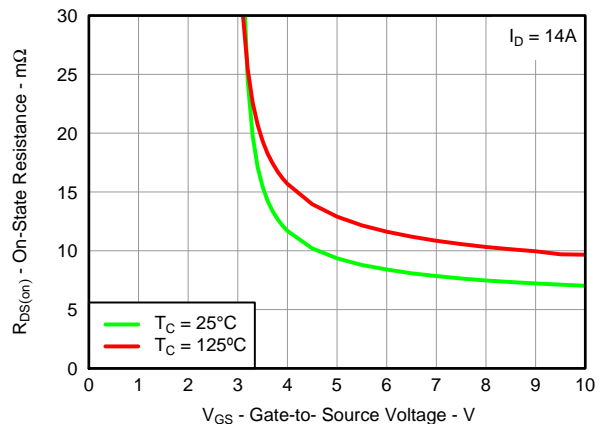


Figure 8. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

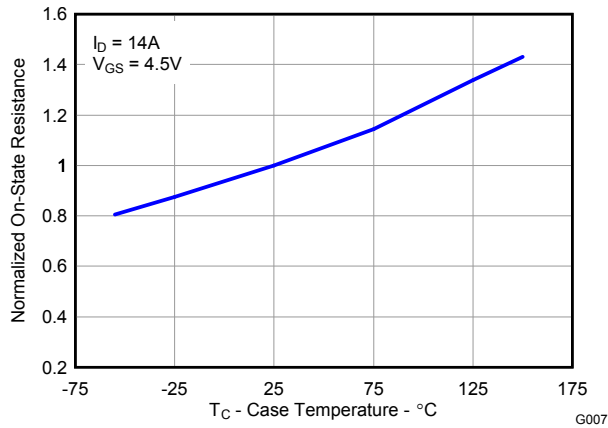


Figure 9. Normalized On-State Resistance vs. Temperature

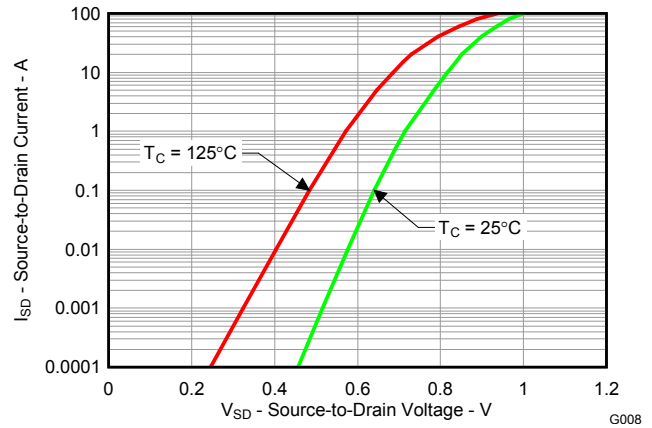


Figure 10. Typical Diode Forward Voltage

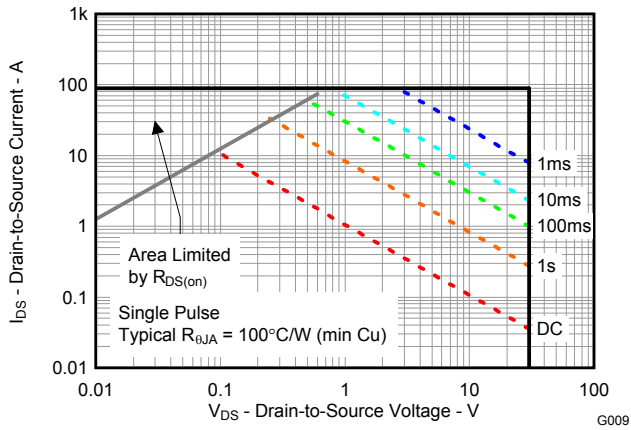


Figure 11. Maximum Safe Operating Area

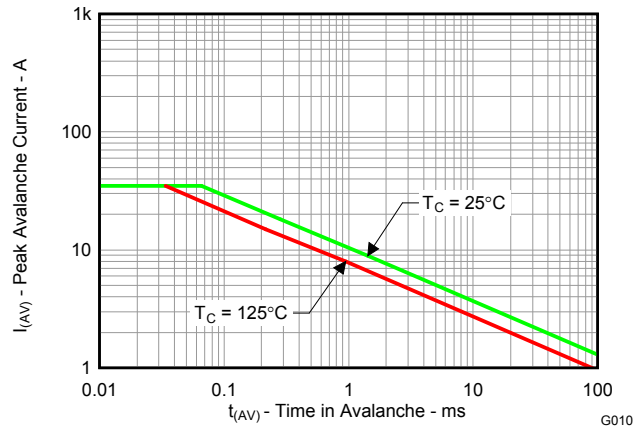


Figure 12. Single Pulse Unclamped Inductive Switching

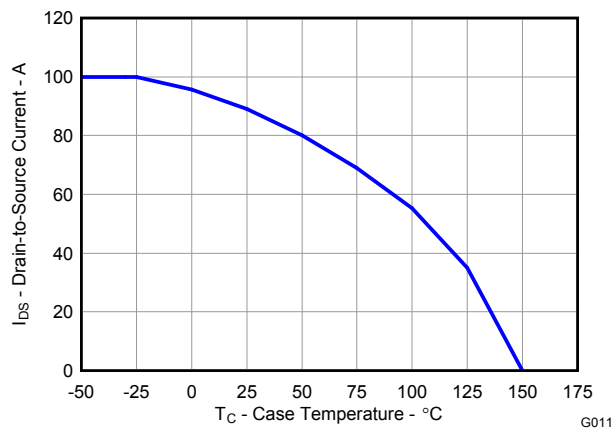
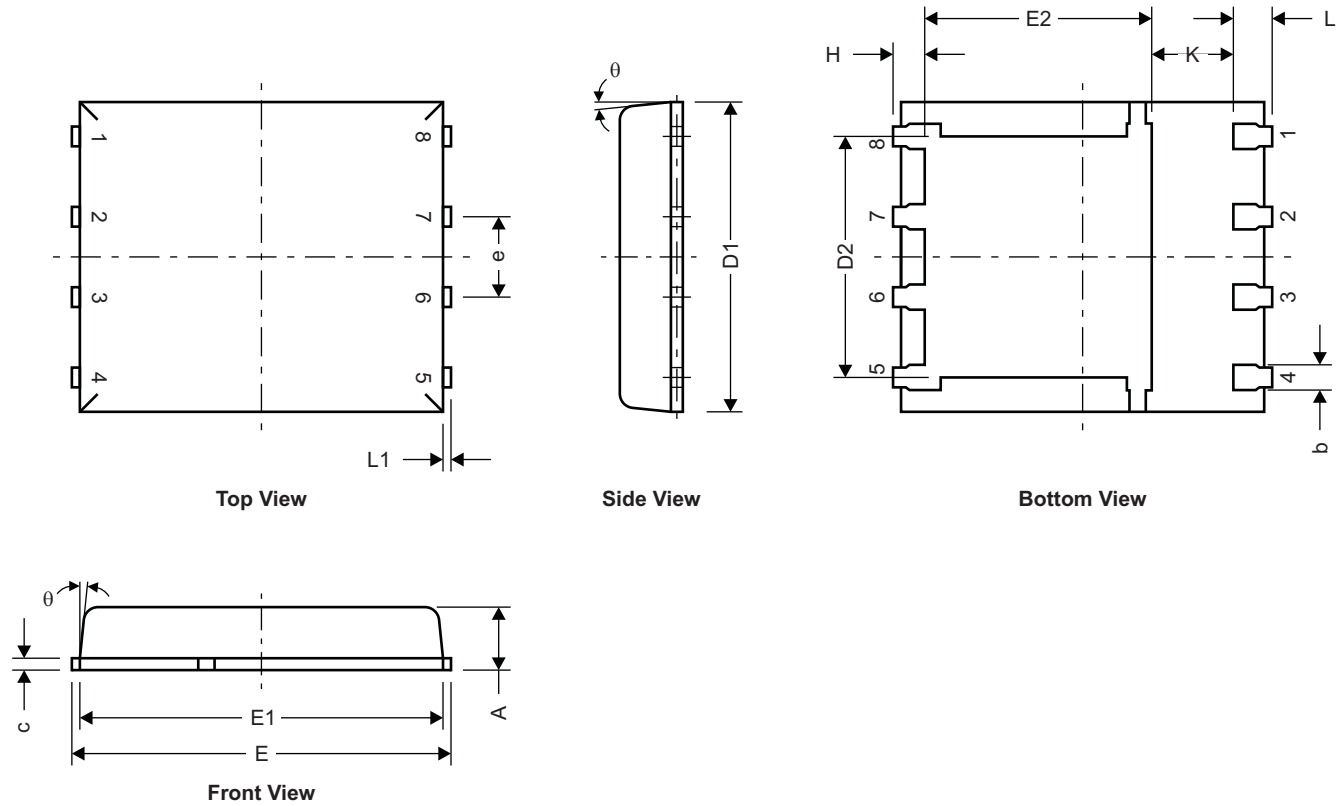


Figure 13. Maximum Drain Current vs. Temperature

MECHANICAL DATA

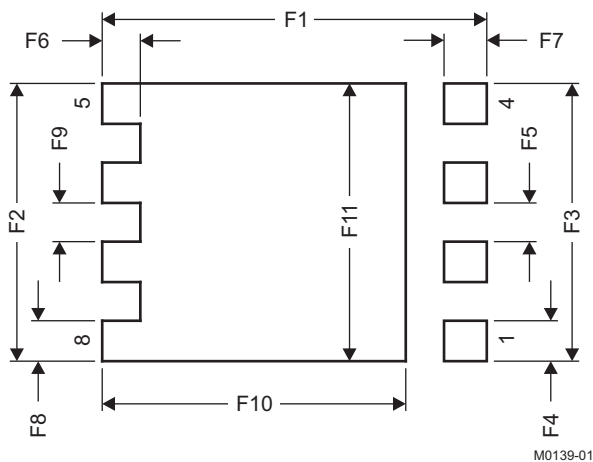
Q5A Package Dimensions



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

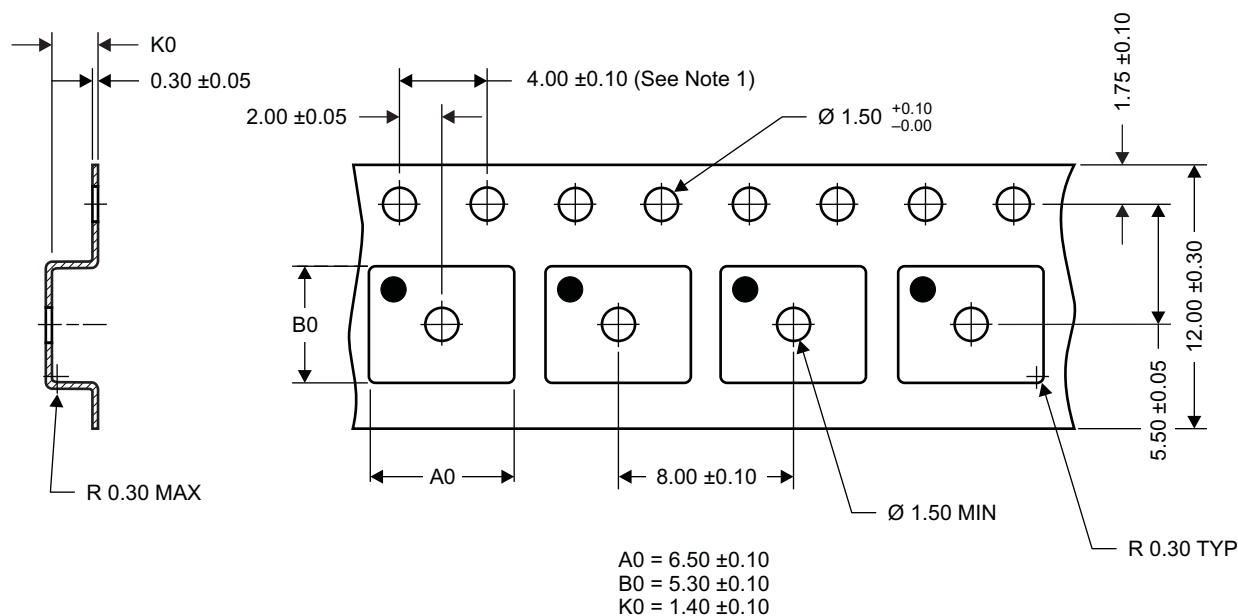
Figure 14. Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Q5A Tape and Reel Information




M0138-01

Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17322Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD17322	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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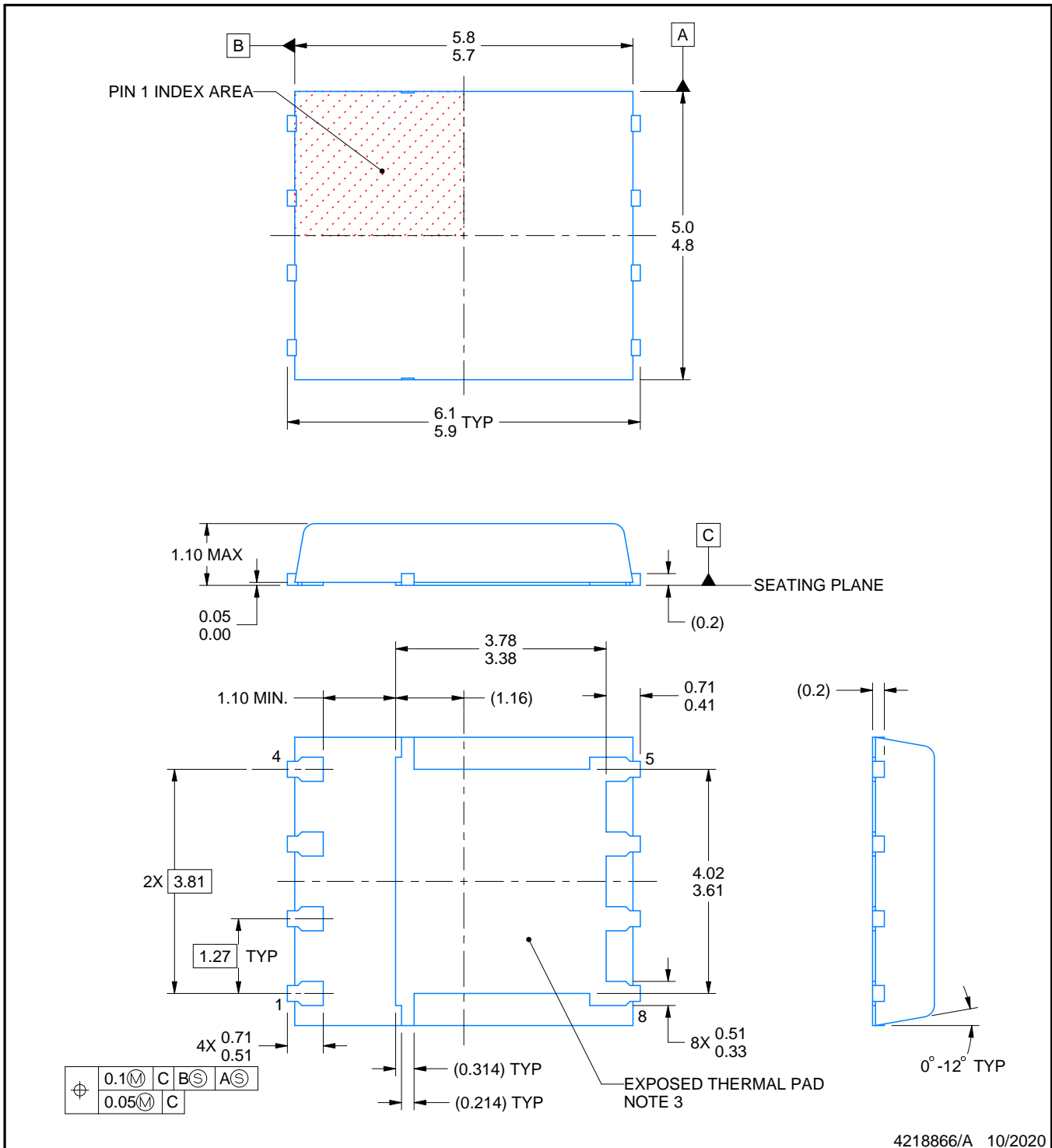
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PACKAGE OUTLINE

DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

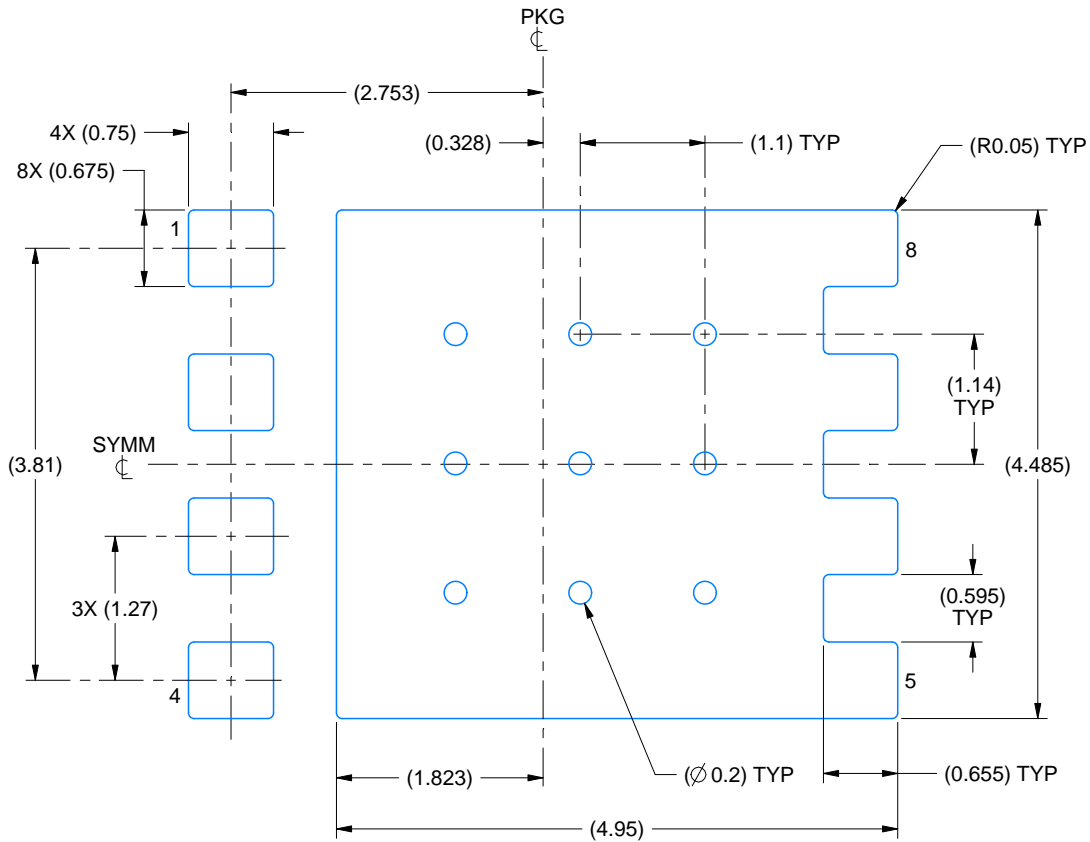
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.

EXAMPLE BOARD LAYOUT

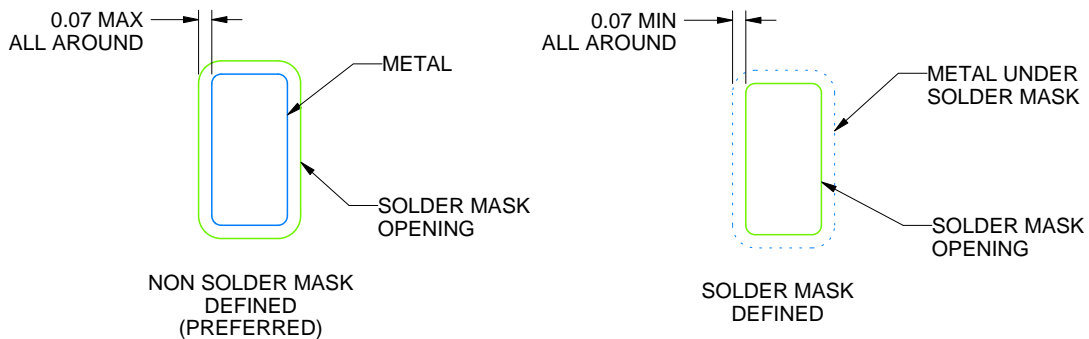
DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X



SOLDER MASK DETAILS

4218866/A 10/2020

NOTES: (continued)

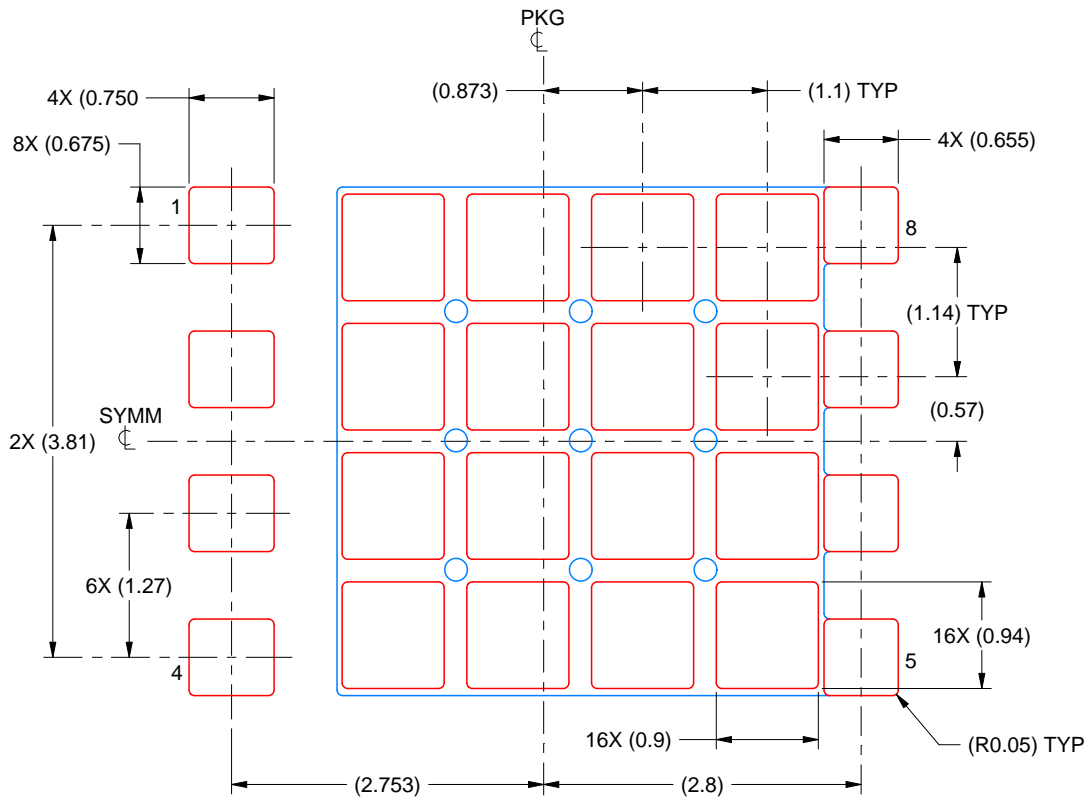
6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

4218866/A 10/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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