



# 30V、N 沟道 NexFET™ 功率 MOSFET

 查询样品: [CSD17327Q5A](#)

## 特性

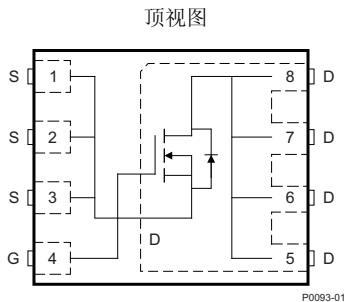
- 超低  $Q_g$  和  $Q_{gd}$
- 低热阻
- 雪崩额定
- 无铅终端镀层
- 符合 **RoHS** 标准
- 无卤素
- **SON 5 毫米 × 6 毫米塑料封装**

## 应用

- 网络、电信和计算系统中的负载点同步降压
- 针对控制 **FET** 应用进行了优化

## 说明

此 NexFET™ 功率 MOSFET 专为最大限度地减少功率转换应用中的损耗而设计。



## 产品汇总

$V_{DS}$	漏极至源极电压	30	V
$Q_g$	总栅极电荷 (4.5V)	2.8	nC
$Q_{gd}$	栅极电荷 (栅极至漏极)	0.8	nC
$R_{DS(on)}$	漏极至源极导通电阻	$V_{GS} = 4.5V$	12.5 mΩ
		$V_{GS} = 8V$	9.9 mΩ
$V_{GS(th)}$	门限电压	1.6	V

## 订购信息

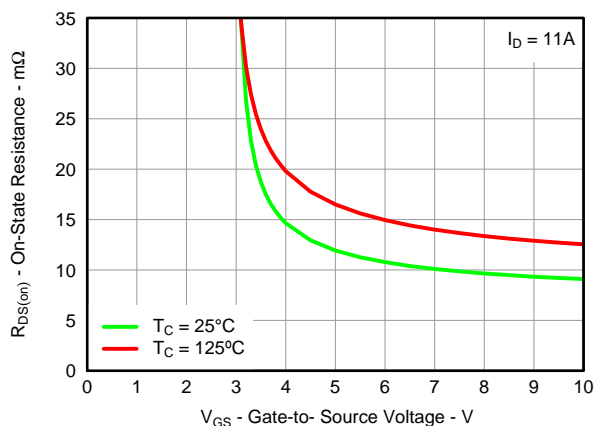
器件	封装	介质	数量	出货
CSD17327Q5A	SON 5-mm × 6-mm 塑料封装	13 英寸卷带	2500	卷带封装

## 最大绝对额定值

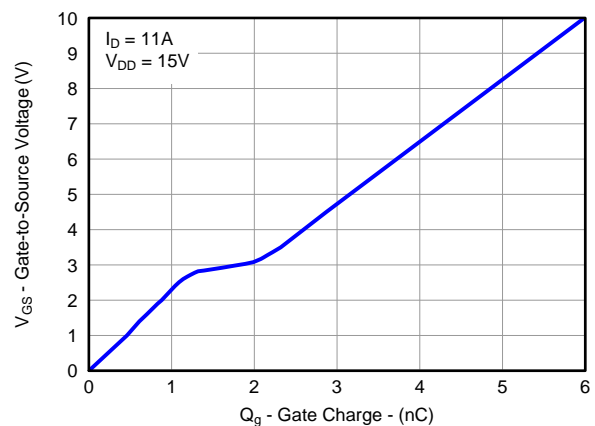
$T_A = 25^\circ C$ , 除非另有说明。		数值	单位
$V_{DS}$	漏极至源极电压	30	V
$V_{GS}$	漏极至源极电压	+10 / -10	V
$I_D$	连续漏极电流, $T_C = 25^\circ C$	65	A
	连续漏极电流 <sup>(1)</sup>	13	A
$I_{DM}$	脉冲漏极电流, $T_A = 25^\circ C$ <sup>(2)</sup>	85	A
$P_D$	功耗 <sup>(1)</sup>	3	W
$T_J, T_{STG}$	工作结温及存储温度范围	-55 至 150	°C
$E_{AS}$	雪崩能量, 单脉冲 $I_D = 30A, L = 0.1mH, R_G = 25\Omega$	45	mJ

- (1) 典型  $R_{\theta JA} = 44^\circ C/W$ , 在一块 1 英寸<sup>2</sup> (6.45-cm<sup>2</sup>)、2 盎司 (0.071-mm 厚) 铜焊盘上, 该铜焊盘位于一块厚度为 0.06 英寸 (1.52-mm) 的 FR4 PCB 之上。
- (2) 脉冲持续时间  $\leq 300\mu s$ , 占空比  $\leq 2\%$

$R_{DS(on)}$  与  $V_{GS}$  的关系曲线



栅极电荷



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = 250\mu A$	30			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-10V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\mu A$	1.1	1.6	2.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_{DS} = 11A$		12.5	15.5	m $\Omega$
		$V_{GS} = 8V, I_{DS} = 11A$		9.9	12.2	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_{DS} = 11A$		44		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V,$ $f = 1MHz$		422	506	pF
$C_{oss}$	Output Capacitance			286	343	pF
$C_{riss}$	Reverse Transfer Capacitance			26	33	pF
$R_G$	Series Gate Resistance			4.7		$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_{DS} = 11A$		2.8	3.4	nC
$Q_{gd}$	Gate Charge Gate to Drain			0.8		nC
$Q_{gs}$	Gate Charge Gate to Source			1.2		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			0.6		nC
$Q_{oss}$	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		6.8		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V,$ $I_{DS} = 11A, R_G = 2\Omega$		5.6		ns
$t_r$	Rise Time			8.2		ns
$t_{d(off)}$	Turn Off Delay Time			9.8		ns
$t_f$	Fall Time			3.2		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 11A, V_{GS} = 0V$		0.85	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 13V, I_F = 11A, di/dt = 300A/\mu s$		10.5		nC
$t_{rr}$	Reverse Recovery Time			14.6		ns

## THERMAL CHARACTERISTICS

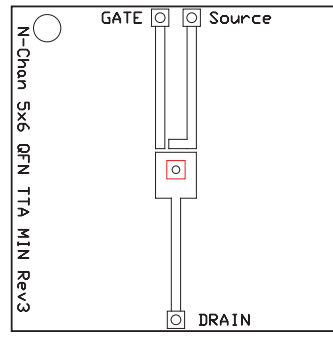
( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			51	$^\circ\text{C/W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



Max  $R_{\theta JA} = 51^\circ\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2-oz. (0.071-mm thick)  
Cu.



Max  $R_{\theta JA} = 131^\circ\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

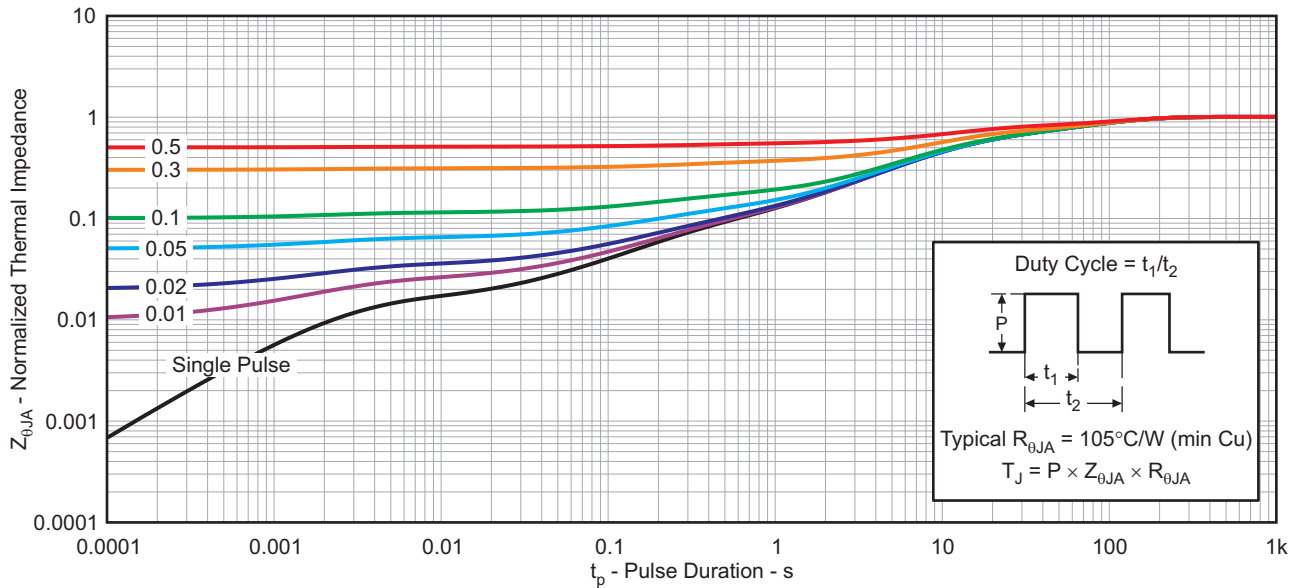
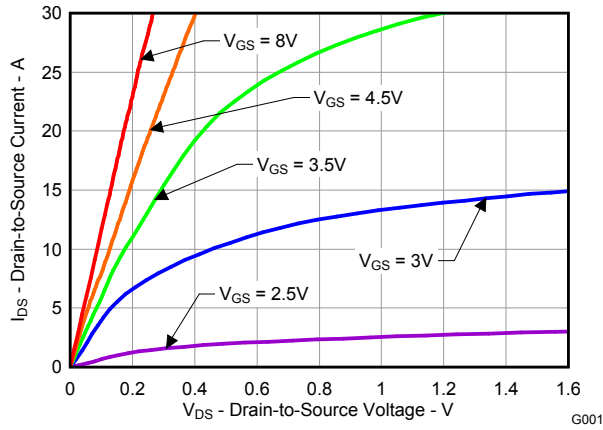


Figure 1. Transient Thermal Impedance

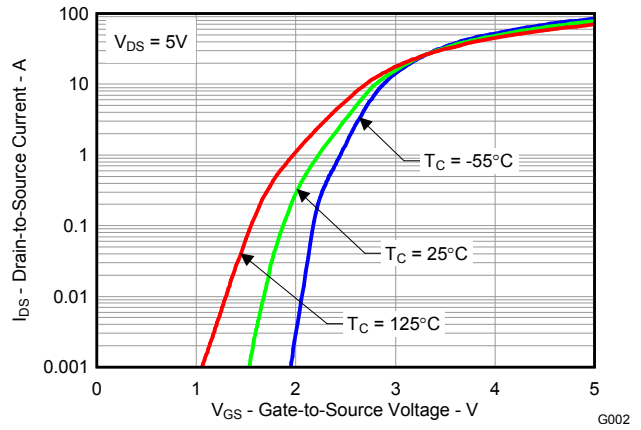
G012

**TYPICAL MOSFET CHARACTERISTICS (continued)**

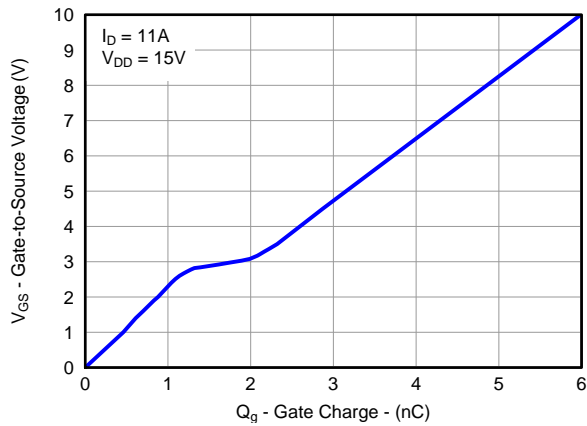
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



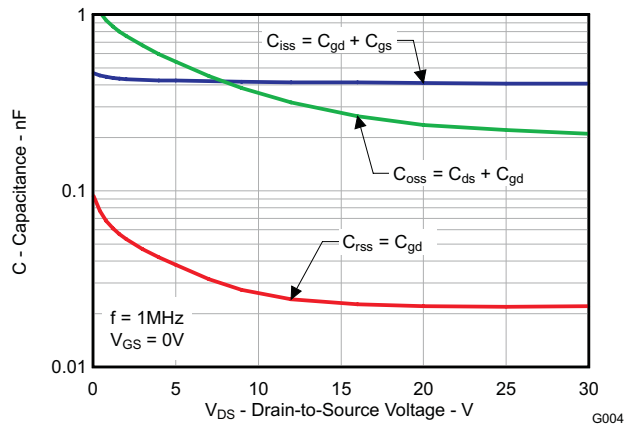
**Figure 2. Saturation Characteristics**



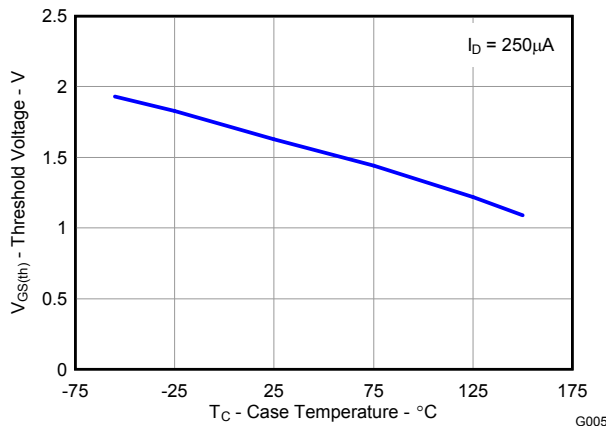
**Figure 3. Transfer Characteristics**



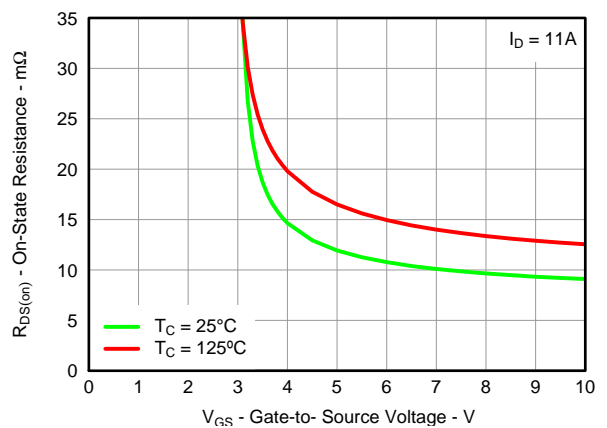
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

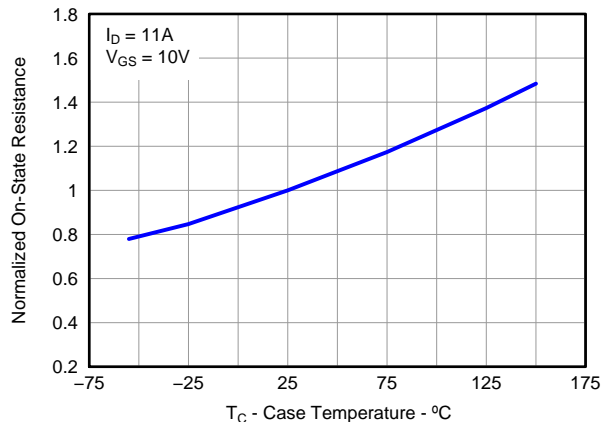


Figure 8. Normalized On-State Resistance vs. Temperature

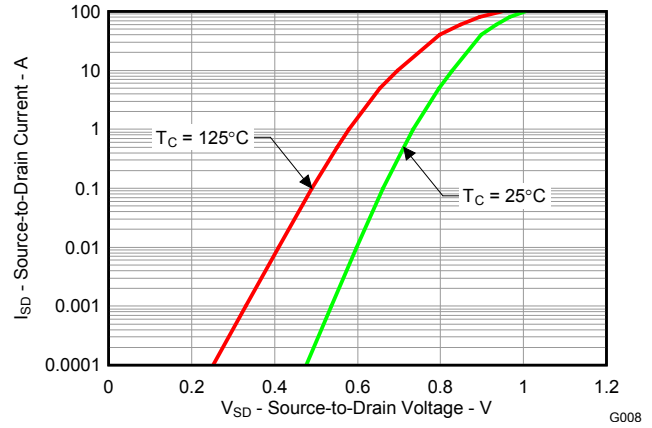


Figure 9. Typical Diode Forward Voltage

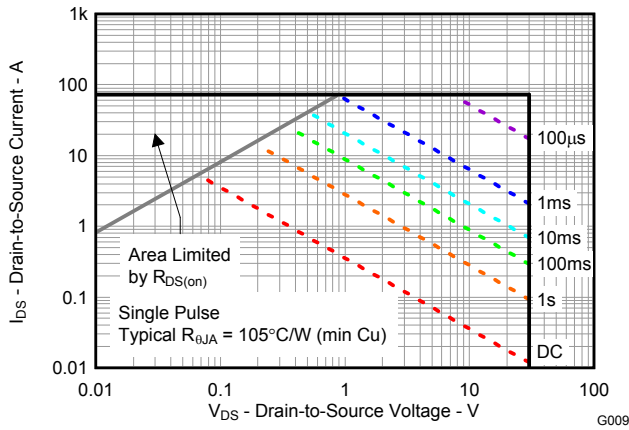


Figure 10. Maximum Safe Operating Area

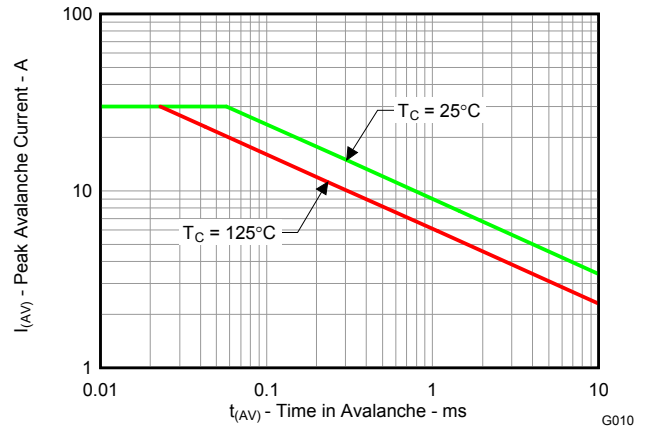


Figure 11. Single Pulse Unclamped Inductive Switching

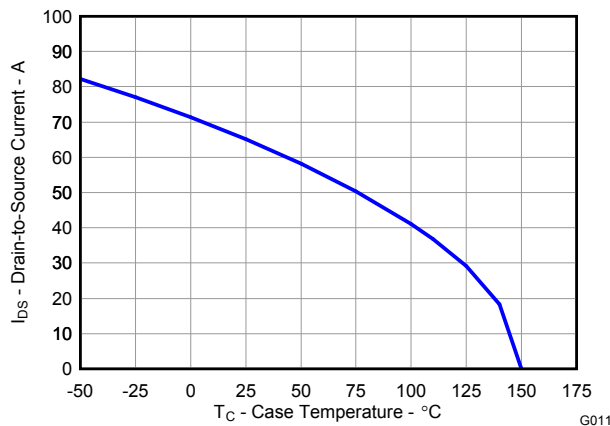
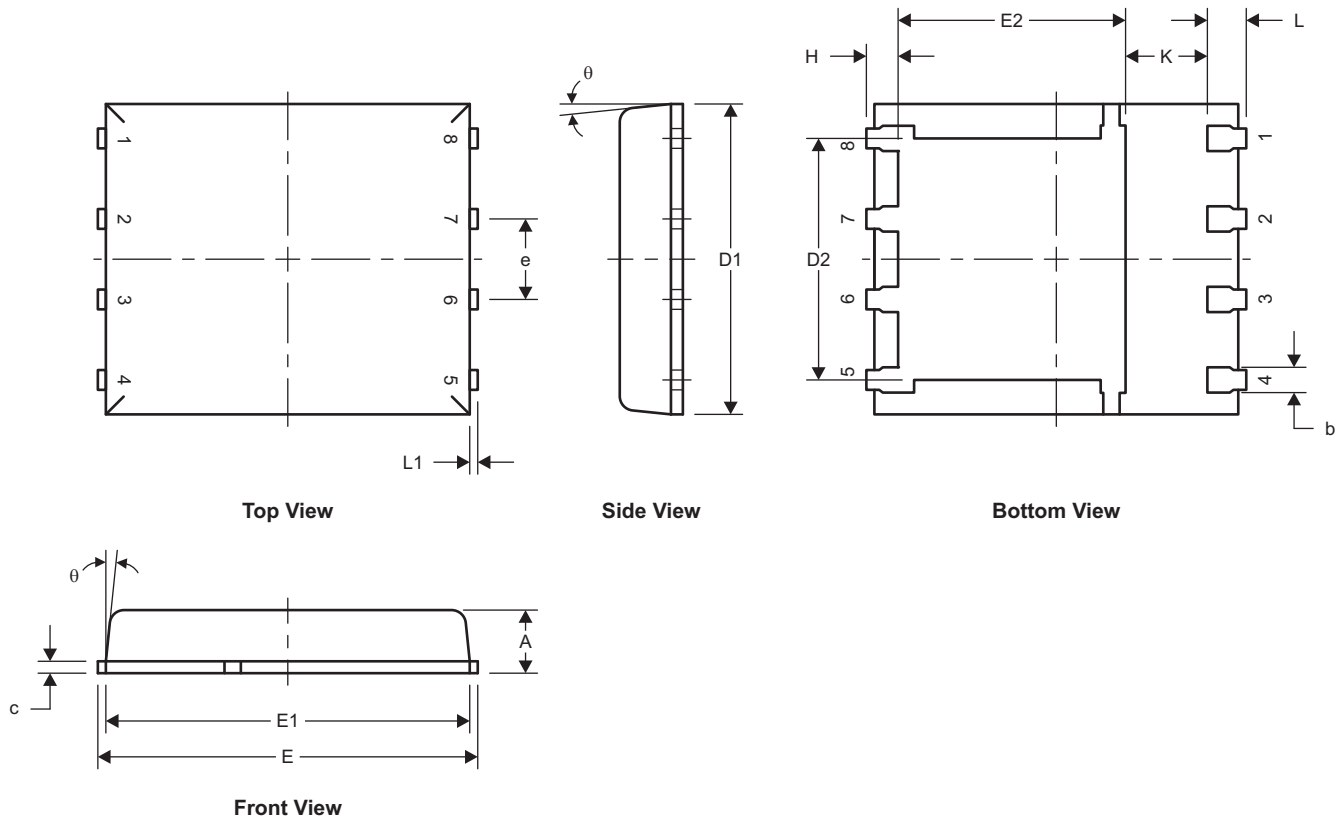


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

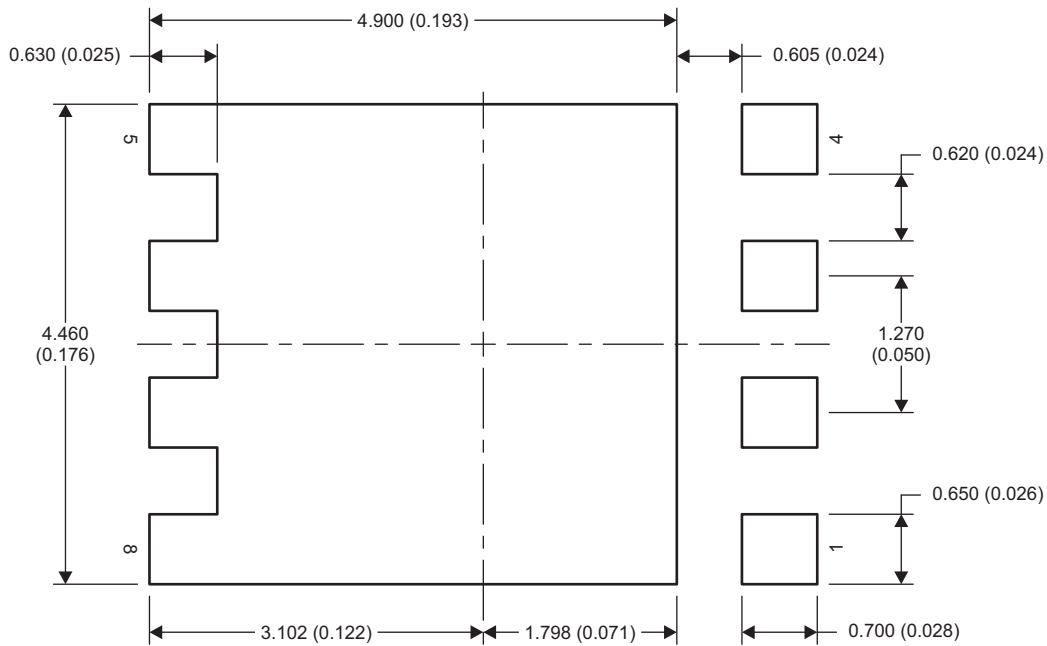
**Q5A Package Dimensions**



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\theta$	0°		12°

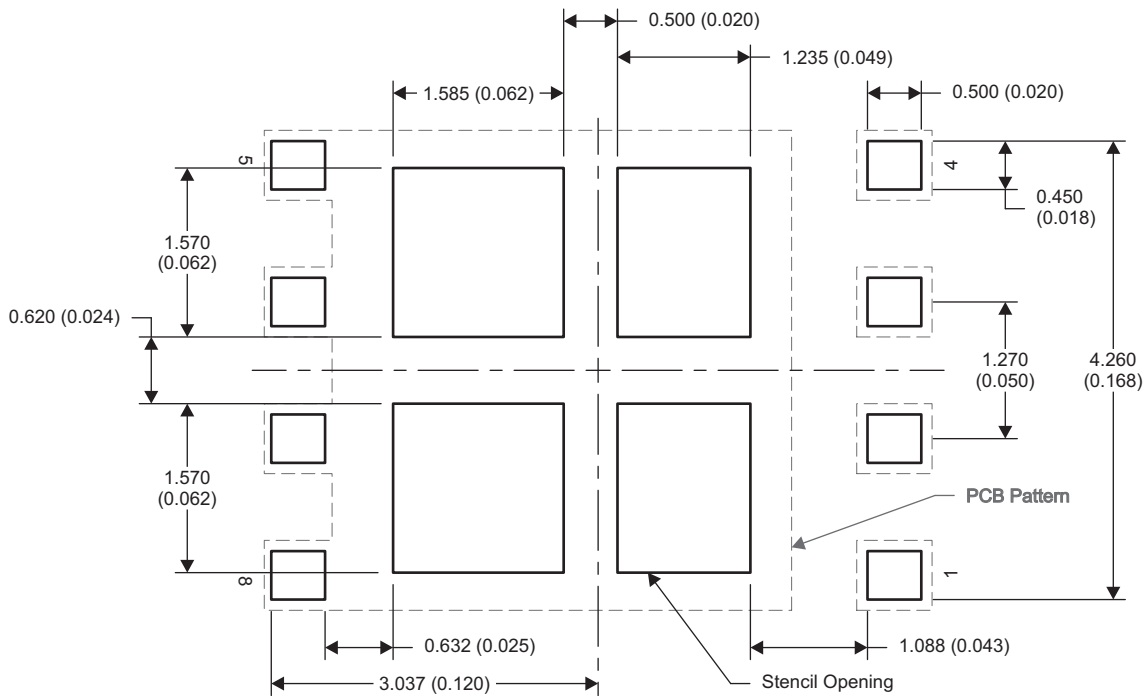
### Recommended PCB Pattern



M0139-01

NOTE: Dimensions are in mm (inches).

### Stencil Recommendation

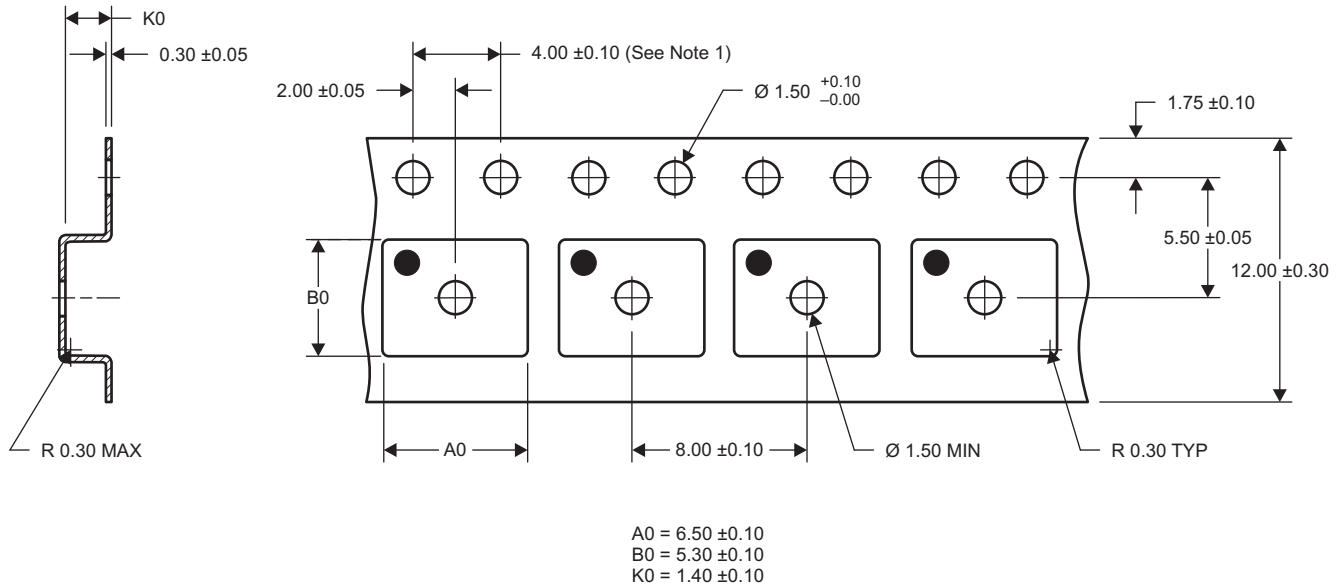


M0209-01

NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

**Q5A Tape and Reel Information**



M0138-01

- NOTES: 1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17327Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD17327	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

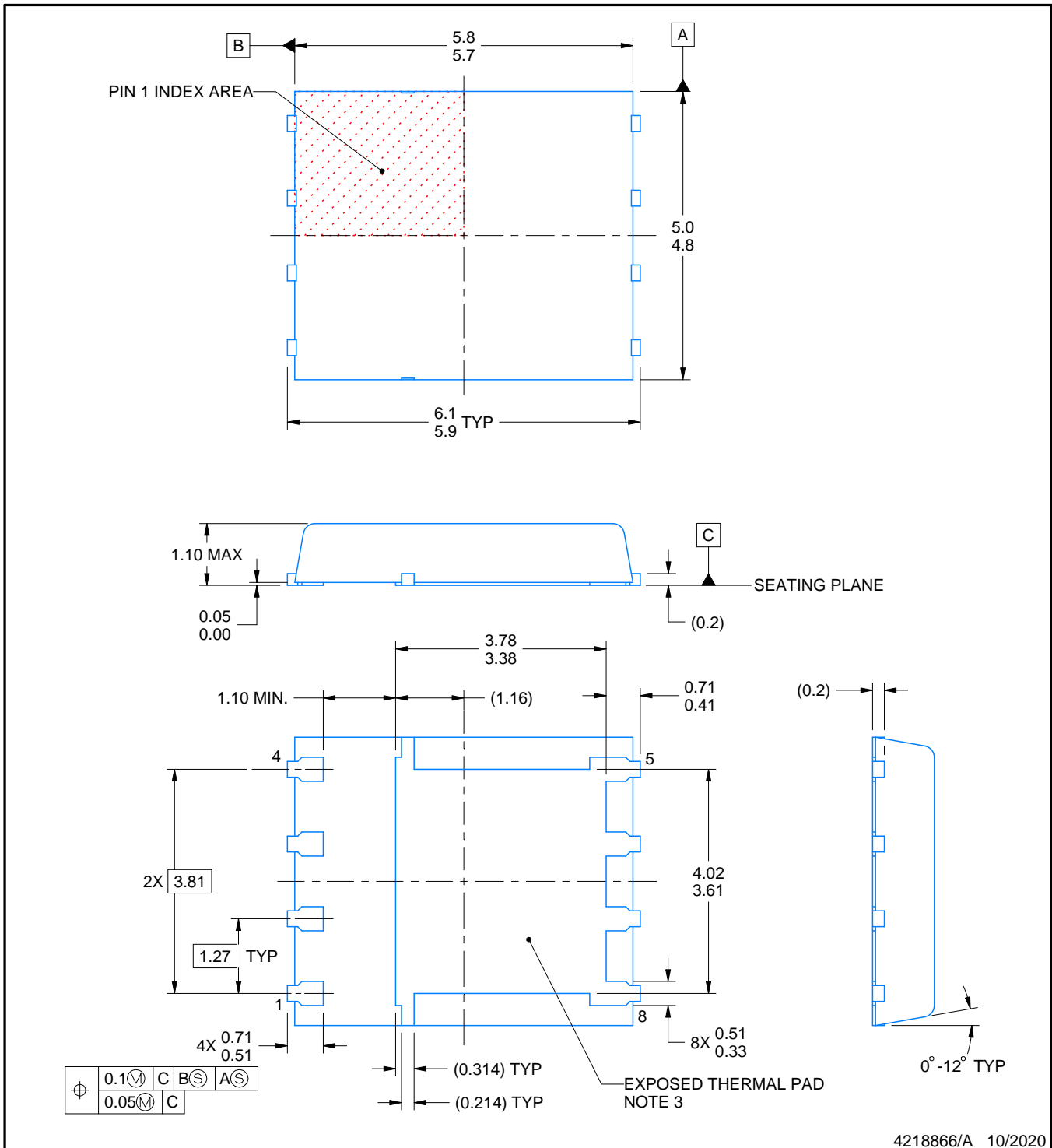
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE OUTLINE

DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**NOTES:**

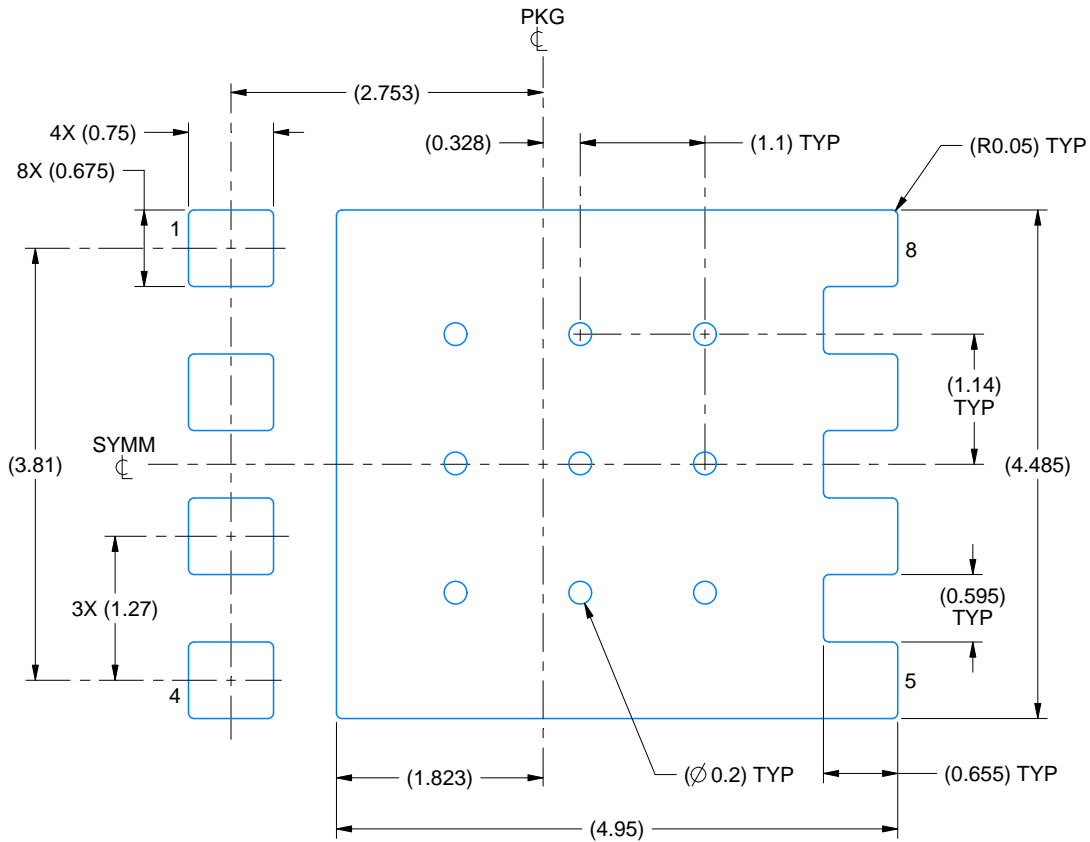
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.

# EXAMPLE BOARD LAYOUT

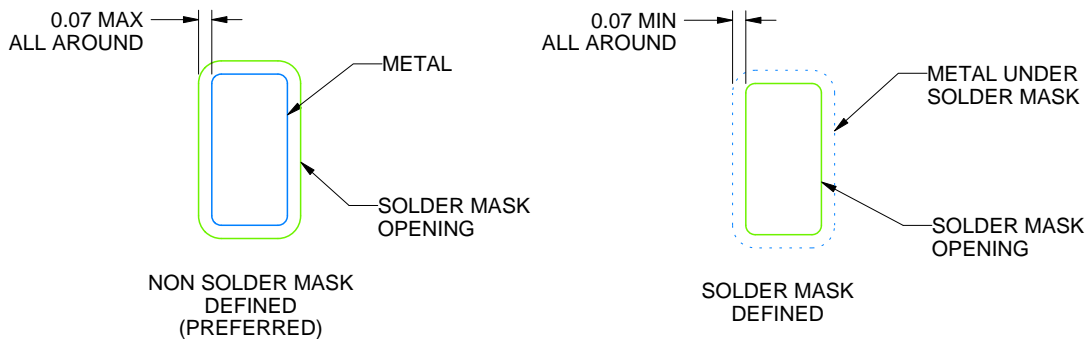
DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE: 15X



SOLDER MASK DETAILS

4218866/A 10/2020

NOTES: (continued)

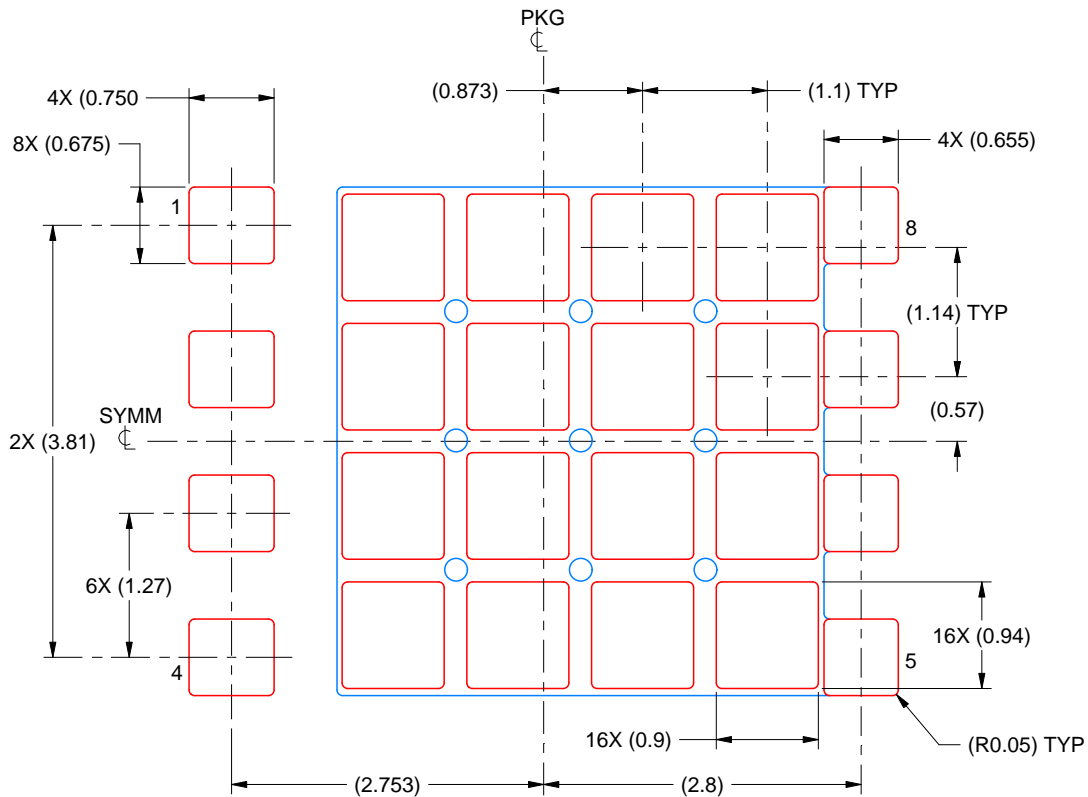
6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:  
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE: 15X

4218866/A 10/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司