30V，N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

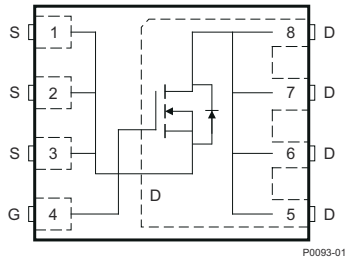
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 具有雪崩能力
- 无铅引脚镀层
- 符合 RoHS
- 无卤素
- SON 5mm × 6mm 塑料封装

2 应用

- 网络、电信和计算系统的负载点同步降压
- 针对控制和同步 FET 应用进行了优化

3 说明

NexFET™ 功率 MOSFET 旨在更大限度地降低功率转换应用中的损耗。



顶视图

产品概要

V_{DS}	漏源极电压	30		V
Q_g	栅极电荷总量 (4.5V)	6.4		nC
Q_{gd}	栅漏栅极电荷	1.9		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	5.4	mΩ
		V_{GS} = 10V	4.1	mΩ
$V_{GS(th)}$	阈值电压	1.5		V

订购信息

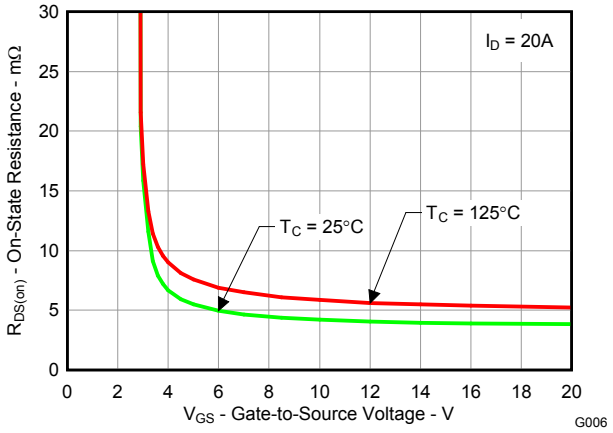
器件	封装	介质	数量	运输
CSD17510Q5A	SON 5mm × 6mm 塑料封装	13 英寸卷带	2500	卷带包装

绝对最大额定值

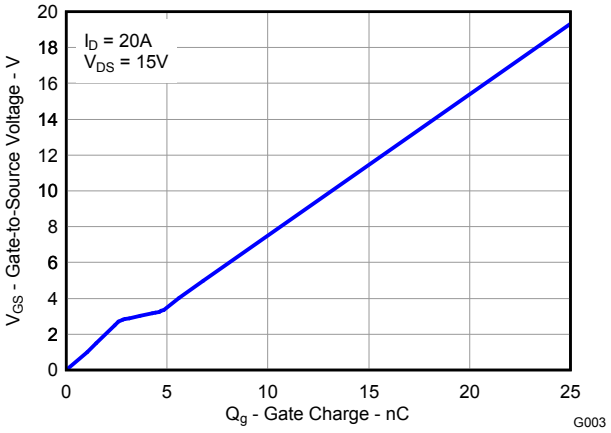
T_A = 25°C 时测得，除非另有说明		值	单位
V_{DS}	漏源极电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流，T_C = 25°C	55	A
	持续漏极电流(1)	20	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	129	A
P_D	功率耗散(1)	3	W
T_J，T_{STG}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 54A，L = 0.1mH，R_G = 25Ω	146	mJ

(1) $R_{\theta JA}$ = 41°C/W，这是在一块厚度为 0.06 英寸 (1.52mm) 的环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸 ^{2} (6.45cm^2)，2 盎司（厚度为 0.071mm）的覆铜焊盘上测得的典型值。

(2) 脉冲持续时间 ≤ 300 μs，占空比 ≤2%



$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷

内容

4 电气特性

（T_A = 25°C 时测得，除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
静态特性						
BV_{DSS}	漏源极电压	V_{GS} = 0V，I_{DS} = 250 μA	30			V
I_{DSS}	漏源漏电流	V_{GS} = 0V，V_{DS} = 24V			1	μA
I_{GSS}	栅源漏电流	V_{DS} = 0V，V_{GS} = 20V			100	nA
$V_{GS(th)}$	栅源阈值电压	V_{DS} = $V_{GS}$$I_{DS}$ = 250 μA	1	1.5	2.1	V
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V，I_{DS} = 20A		5.4	7.3	mΩ
		V_{GS} = 10V，I_{DS} = 20A		4.1	5.2	mΩ
g_{fs}	跨导	V_{DS} = 15V，I_{DS} = 20A		59		S
动态特性						
C_{iss}	输入电容	V_{GS} = 0V，V_{DS} = 15V，f = 1MHz		960	1250	pF
C_{oss}	输出电容			630	820	pF
C_{rss}	反向传输电容			51	66	pF
R_G	串联栅极电阻			0.85	1.7	Ω
Q_g	栅极电荷总量 (4.5V)	V_{DS} = 15V，I_{DS} = 20A		6.4	8.3	nC
Q_{gd}	栅漏栅极电荷			1.9		nC
Q_{gs}	栅源栅极电荷			2.7		nC
$Q_{g(th)}$	Vth 下的栅极电荷			1.5		nC
Q_{oss}	输出电荷	V_{DS} = 13.5V，V_{GS} = 0V		16		nC
$t_{d(on)}$	导通延时时间	V_{DS} = 15V，V_{GS} = 4.5V，I_{DS} = 20A，R_G = 2Ω		7		ns
t_r	上升时间			11		ns
$t_{d(off)}$	关断延迟时间			9		ns
t_f	下降时间			4.1		ns
二极管特性						
V_{SD}	二极管正向电压	I_{SD} = 20A，V_{GS} = 0V		0.85	1	V
Q_{rr}	反向恢复电荷	V_{DD}= 13.5V，I_F = 20A，di/dt = 300A/μs		25		nC
t_{rr}	反向恢复时间			24		ns

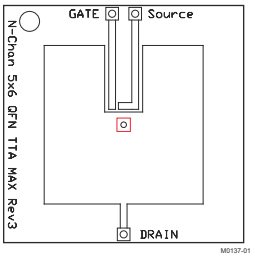
5 热特性

（T_A = 25°C 时测得，除非另有说明）

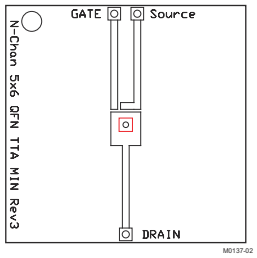
参数		最小值	典型值	最大值	单位
$R_{\theta JC}$	结至外壳热阻(1)			1.6	°C/W
$R_{\theta JA}$	结至环境热阻(1) (2)			51	°C/W

(1) $R_{\theta JC}$ 是在器件安装在 1.5 英寸 × 1.5 英寸 (3.81cm × 3.81cm)、厚度为 0.06 英寸 (1.52mm) 的 FR4 PCB 上的 1 英寸 ^{2} (6.45cm^2)、2 盎司（厚度为 0.071mm）的覆铜焊盘上测得的典型值。$R_{\theta JC}$ 由设计指定，而 $R_{\theta JA}$ 由用户的电路板设计确定。

(2) 器件安装在具有 1 英寸 ^{2} (6.45cm^2)、2 盎司（厚度为 0.071mm）的覆铜焊盘的 FR4 材料上。



$R_{\theta JA}$ 最大值 = 51°C/W，安装在 1 英寸 ^{2} (6.45cm^2)、2 盎司（厚度为 0.071mm）的覆铜焊盘上时。



$R_{\theta JA}$ 最大值 = 125°C/W，安装在最小面积的 2 盎司（厚度为 0.071mm）覆铜焊盘上时。

6 典型 MOSFET 特性

（T_A = 25°C 时测得，除非另有说明）

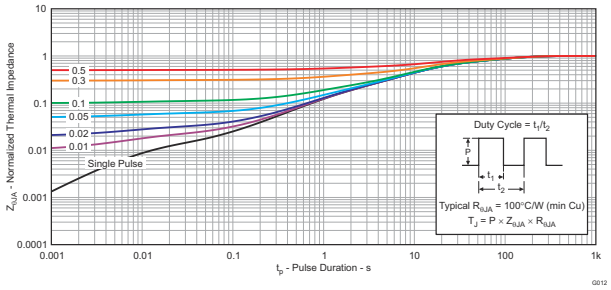


图 6-1. 瞬态热阻抗

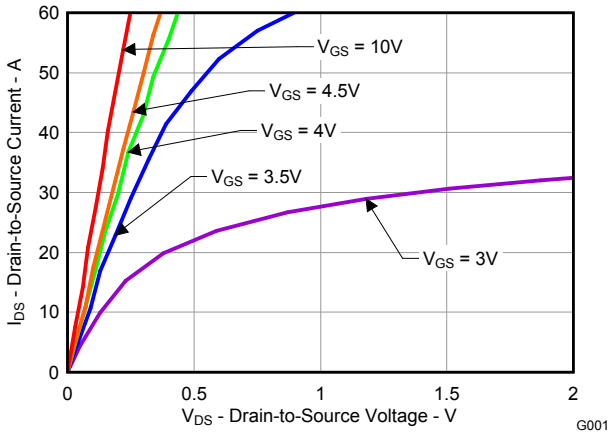


图 6-2. 饱和特性

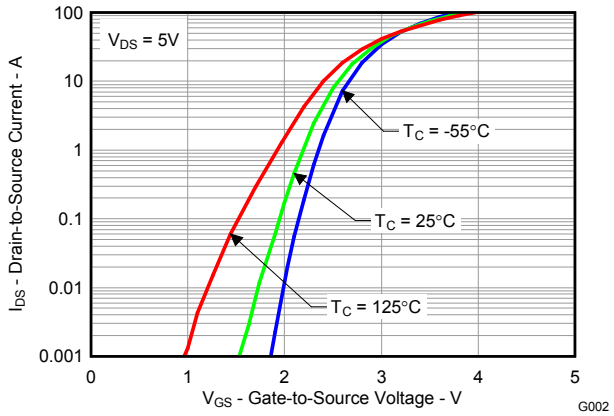


图 6-3. 传输特性

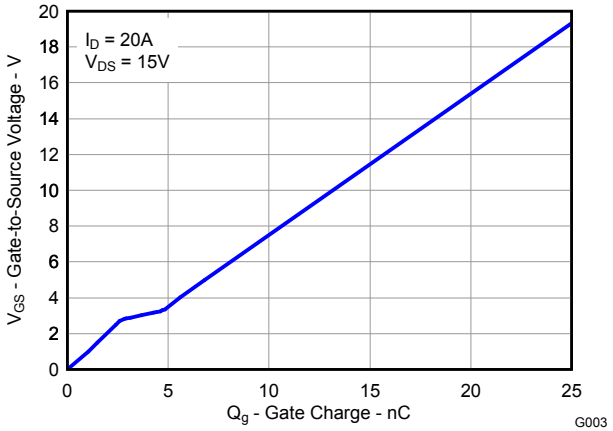


图 6-4. 栅极电荷

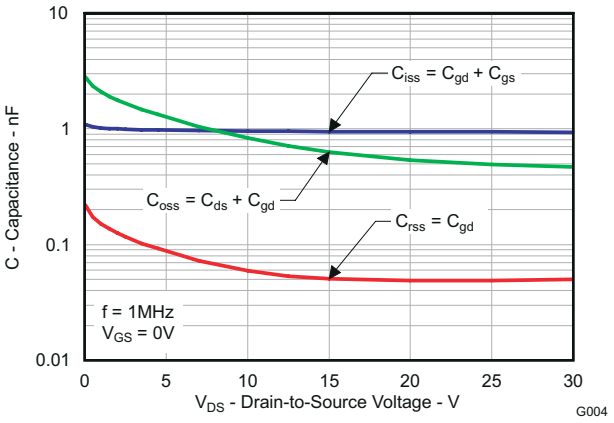


图 6-5. 电容

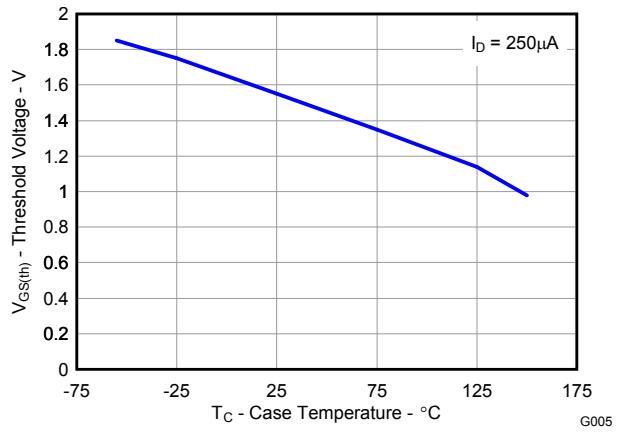


图 6-6. 阈值电压与温度间的关系

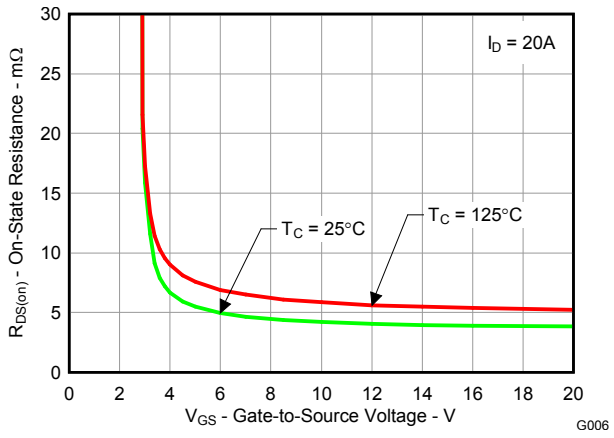


图 6-7. 通态电阻与栅源电压间的关系

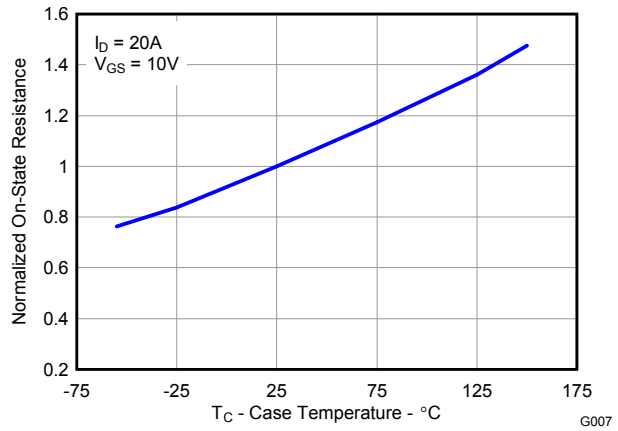


图 6-8. 标准化通态电阻与温度间的关系

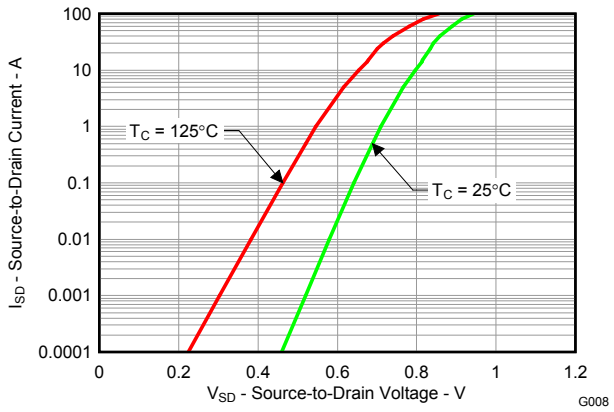


图 6-9. 典型二极管正向电压

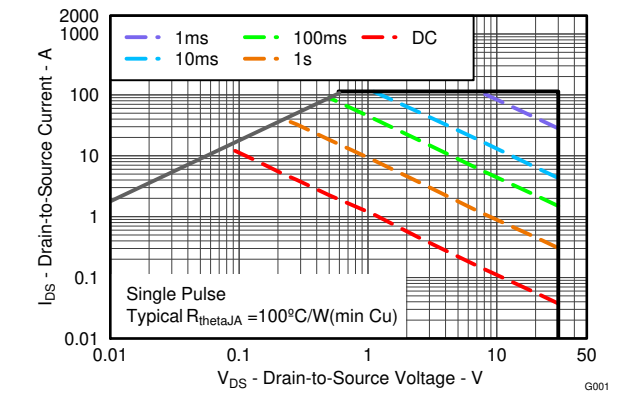


图 6-10. 最大安全工作区

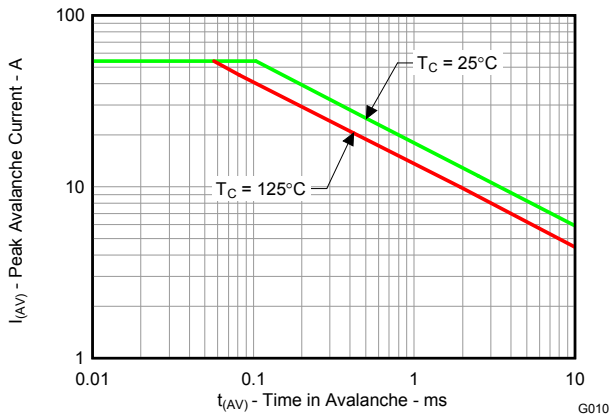


图 6-11. 单脉冲非钳位电感式开关

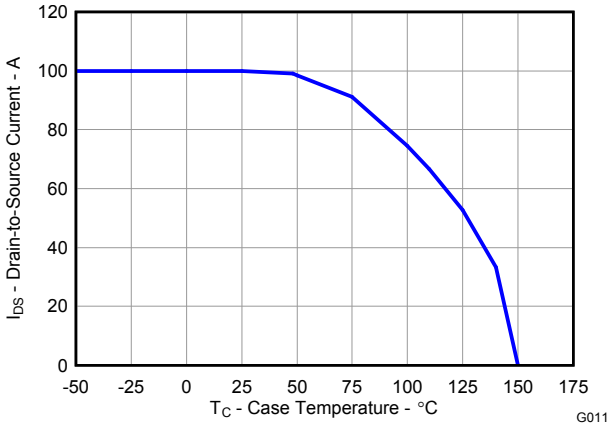


图 6-12. 最大漏极电流与温度间的关系

7 器件和文档支持

TI 提供大量的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

7.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

7.2 文档支持

7.2.1 相关文档

7.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.5 商标

NexFET™ and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

7.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

8

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (September 2012) to Revision H (December 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

Changes from Revision * (July 2010) to Revision A ()	Page
• 更改了 图 6-5 的 Y 轴标度	5

Changes from Revision F (October 2011) to Revision G (September 2012)	Page
• 更改了图 6-10	5

Changes from Revision E (July 2011) to Revision F (October 2011) **Page**

- 将 T_C = 25°C 时的持续漏极电流 I_D 值从 100A 更改为 55A。.....1
- 更改了图 6-10 5

Changes from Revision A (August 2010) to Revision B () **Page**

- 将 $R_{DS(on)}$ 测试条件从 V_{GS} = 8V 更改为：V_{GS} = 10V.....3

Changes from Revision B (September 2010) to Revision C () **Page**

- 绝对最大额定值，将 E_{AS} 值从 45mJ 更改为 146mJ..... 1

Changes from Revision C (September 2010) to Revision D () **Page**

Changes from Revision D (November 2010) to Revision E () **Page**

- 将绝对最大额定值表中的 V_{GS} 从+20/-12V 更改为±20V..... 1
- 从 +20/-12V 更改为 20V.....3

9 机械数据

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17510Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD17510	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

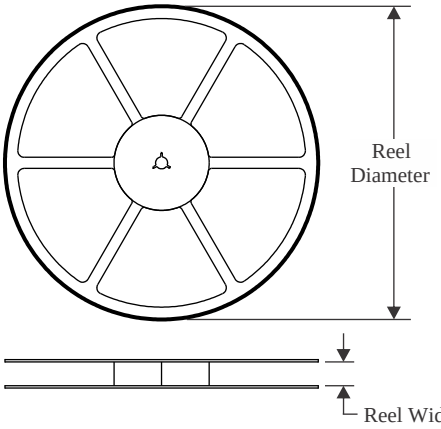
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

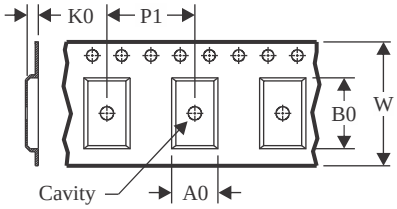
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

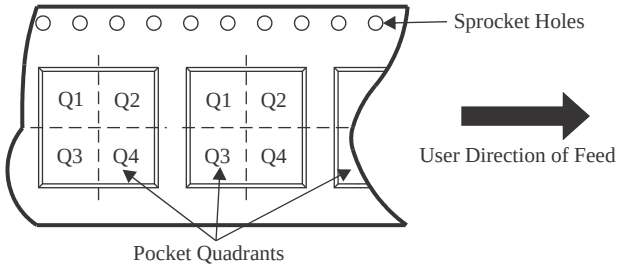


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

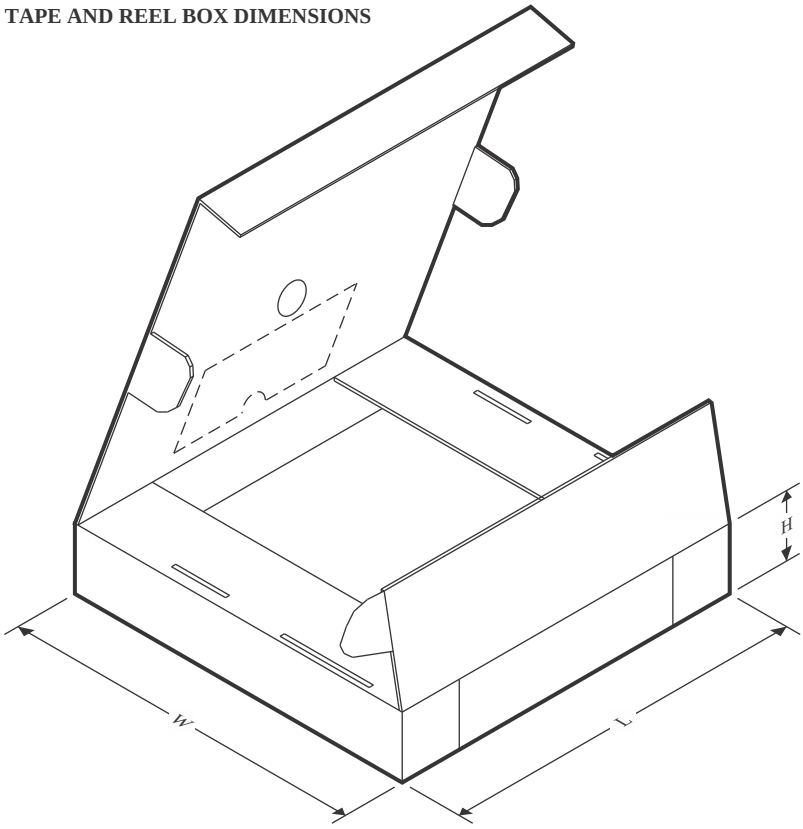
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

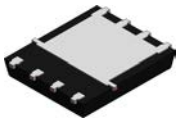
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17510Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17510Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0

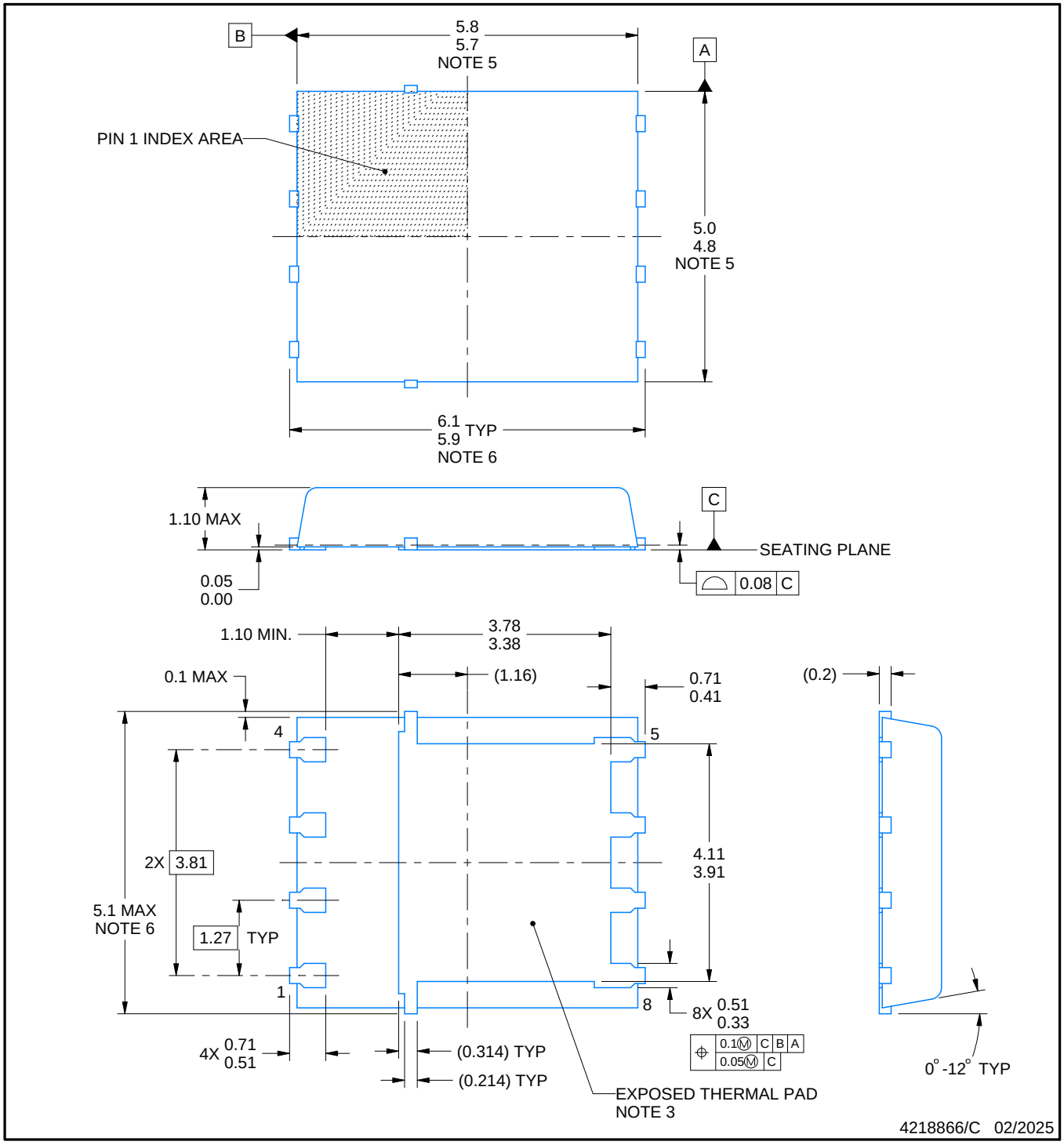


PACKAGE OUTLINE

DQJ0008A

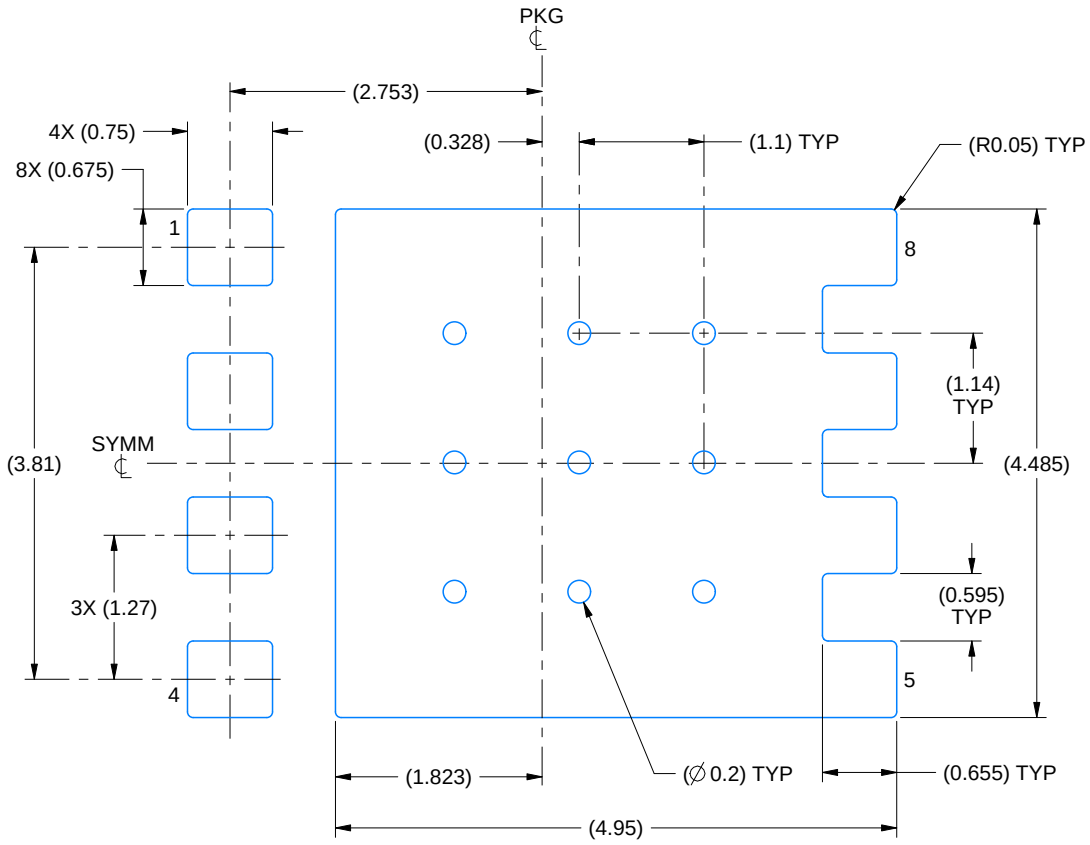
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

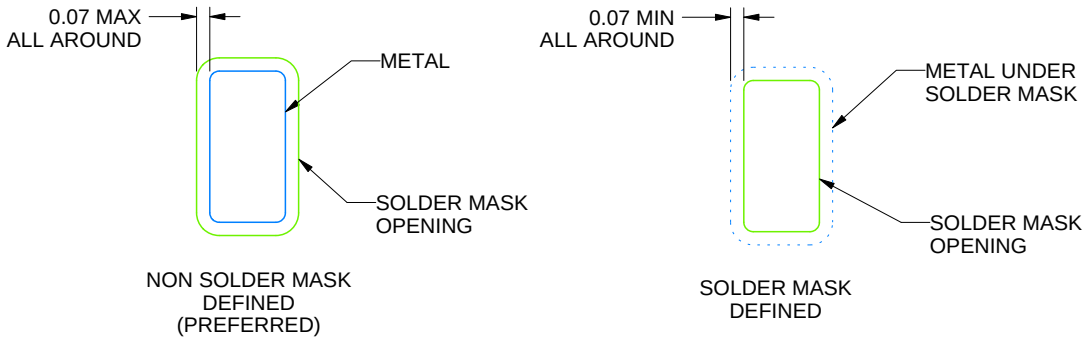


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X

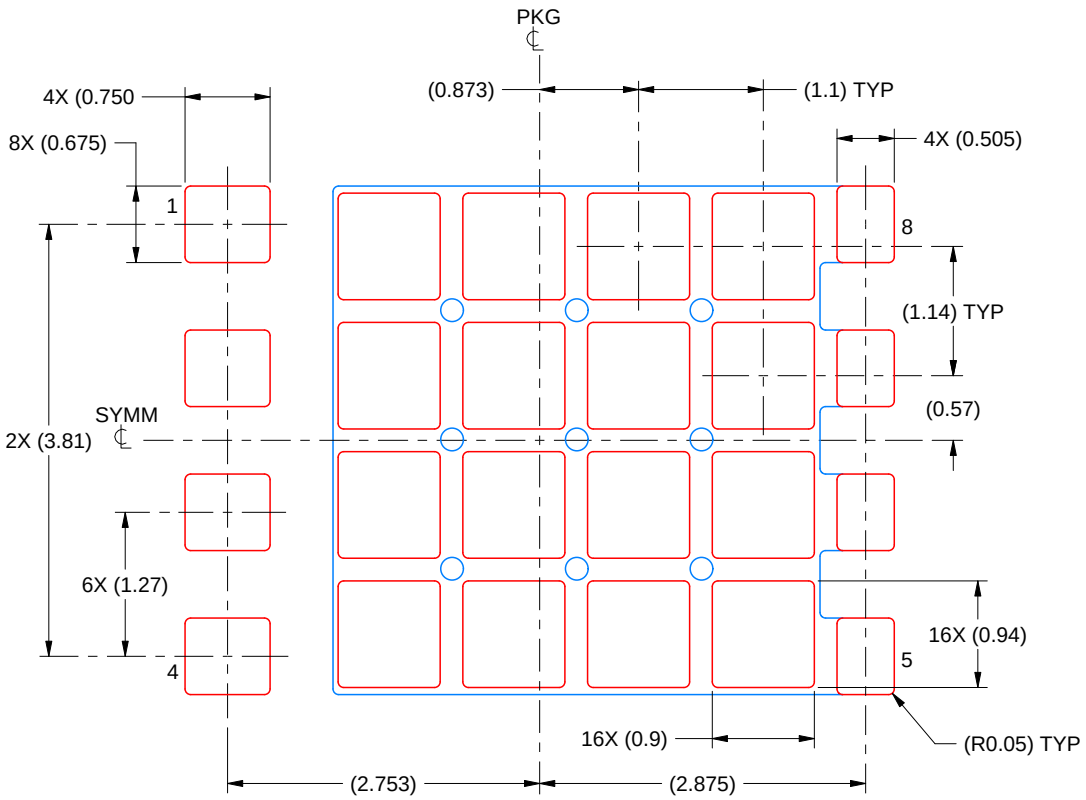


SOLDER MASK DETAILS

4218866/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

4218866/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265