CSD17577Q5A 30V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 5mm x 6mm 塑料封装

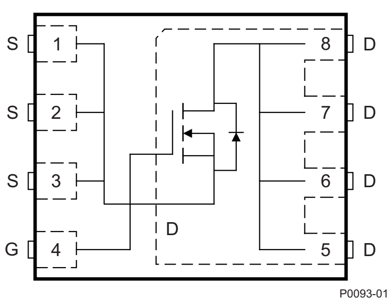
2 应用范围

- 网络互联、电信和计算系统中的负载点同步降压
- 针对控制和同步 FET 应用进行了优化

3 说明

这款 30V，3.5mΩ，SON 5mm × 6mm NexFET™ 功率 MOSFET 被设计成在功率转换应用中以最大程度降低电阻。

顶部图标



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	13		nC
Q_{gd}	栅漏栅极电荷	2.8		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	4.8	mΩ
		V_{GS} = 10V	3.5	mΩ
$V_{GS(th)}$	阀值电压	1.4		V

订购信息[(1)]

器件	数量	介质	封装	出货
CSD17577Q5A	2500	13 英寸卷带	SON 5mm x 6mm 塑料封装	卷带封装
CSD17577Q5AT	250	7 英寸卷带		

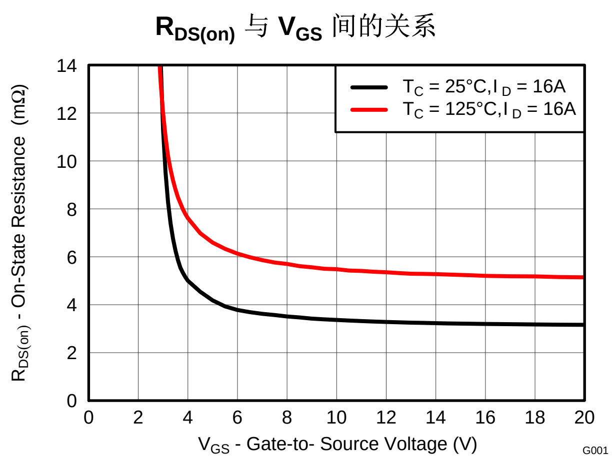
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

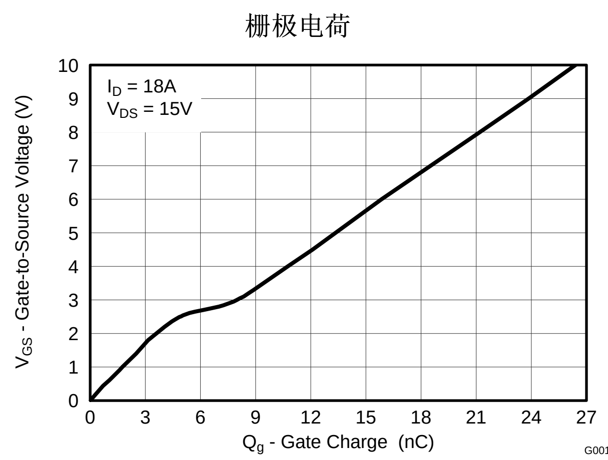
最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	60	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	83	
	持续漏极电流 (1)	22	
I_{DM}	脉冲漏极电流 (2)	280	A
P_D	功率耗散(1)	3	W
	功率耗散，T_C = 25°C	53	
T_J，T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 28，L = 0.1mH，R_G = 25Ω	39	mJ

(1) $R_{\theta JA}$= 40°C/W，这是在一个厚度 0.06 英寸的环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司 的铜焊盘上测得的典型值
。

(2) 最大 $R_{\theta JC}$ = 2.8°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%


RDS(on) 与 VGS 间的关系
TC = 25°C, I D = 16A
TC = 125°C, I D = 16A
RDS(on) - On-State Resistance (mΩ)
VGS - Gate-to- Source Voltage (V)
0 2 4 6 8 10 12 14 16 18 20
0 2 4 6 8 10 12 14
G001


栅极电荷
ID = 18A
VDS = 15V
VGS - Gate-to-Source Voltage (V)
Qg - Gate Charge (nC)
0 3 6 9 12 15 18 21 24 27
0 1 2 3 4 5 6 7 8 9 10
G001

目录

4 修订历史记录

日期	修订版本	注释
2014 年 8 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

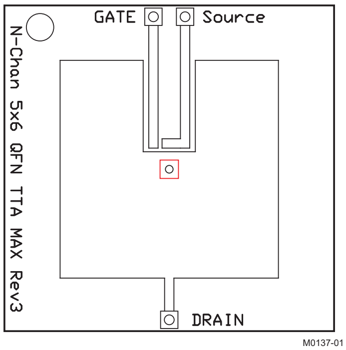
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.1	1.4	1.8	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 10 A		4.8	5.8	mΩ
		V_{GS} = 10 V, I_D = 18 A		3.5	4.2	mΩ
$g_{ƒs}$	Transconductance	V_{DS} = 3 V, I_D = 18 A		79		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, ƒ = 1 MHz		1780	2310	pF
C_{oss}	Output Capacitance			208	270	pF
C_{rss}	Reverse Transfer Capacitance			79	102	pF
R_G	Series Gate Resistance			1.4	2.8	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_D = 18 A		13	17	nC
Q_g	Gate Charge Total (10 V)			27	35	nC
Q_{gd}	Gate Charge Gate-to-Drain			2.8		nC
Q_{gs}	Gate Charge Gate-to-Source			5.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			2.5		nC
Q_{oss}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 10 V, I_{DS} = 18 A, R_G = 0 Ω		3		ns
t_r	Rise Time			12		ns
$t_{d(off)}$	Turn Off Delay Time			18		ns
$t_ƒ$	Fall Time			2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 18 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 15 V, I_F = 18 A, di/dt = 300 A/μs		8.2		nC
t_{rr}	Reverse Recovery Time			9.3		ns

5.2 Thermal Information

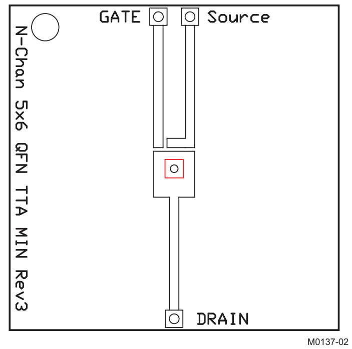
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJC}$	Junction-to-Case Thermal Resistance (1)			2.8	°C/W
$R_{θJA}$	Junction-to-Ambient Thermal Resistance (1)(2)			50	

(1) $R_{θJC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 140°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

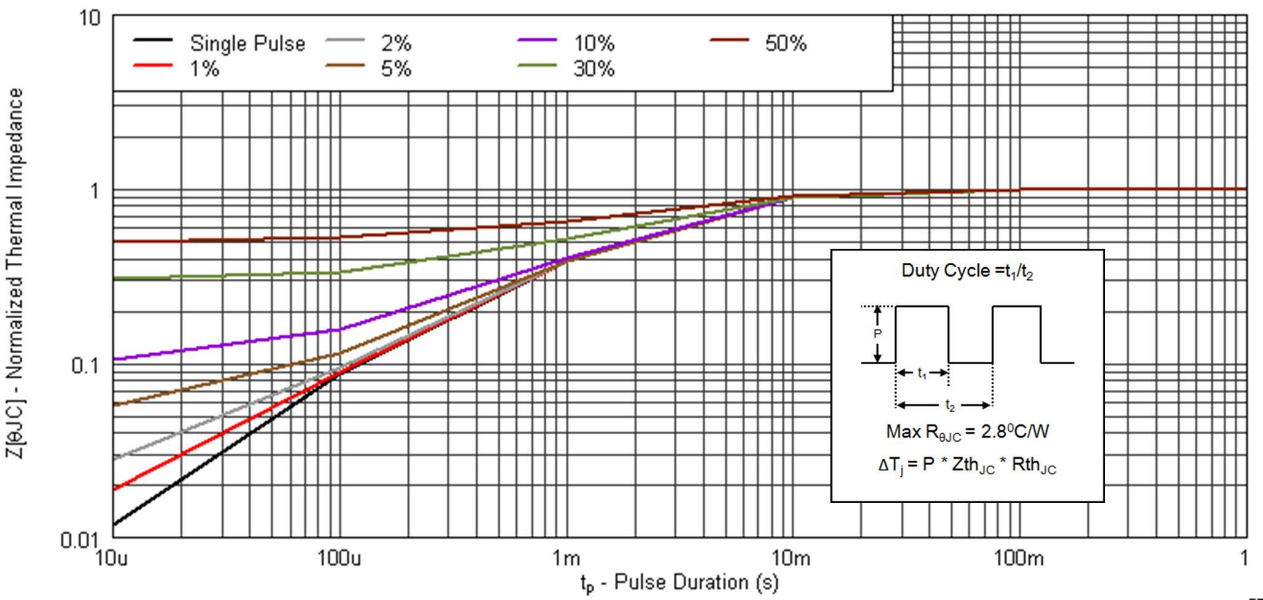


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

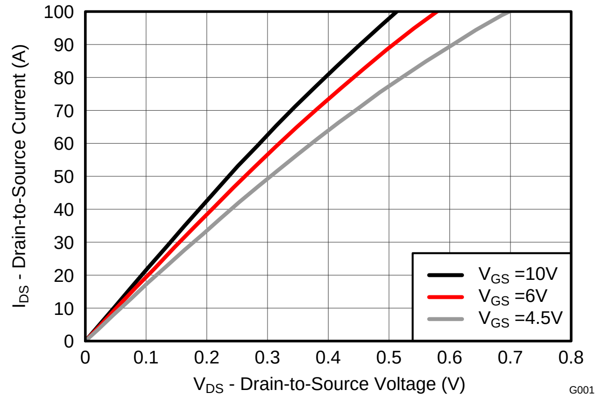
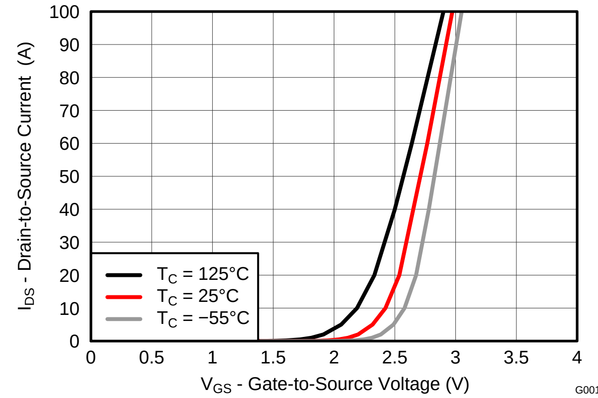
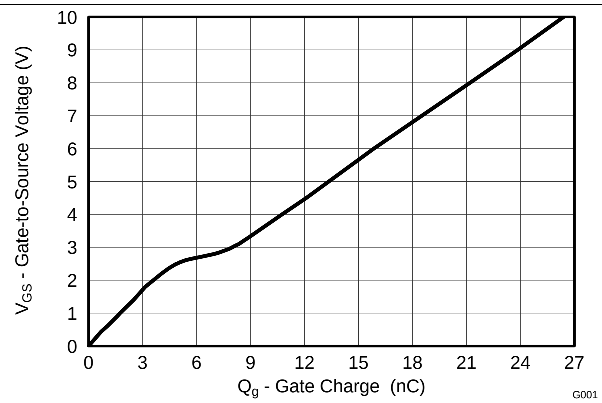


Figure 2. Saturation Characteristics



V_{DS} = 5 V

Figure 3. Transfer Characteristics



I_D = 18 A V_{DS} = 15 V

Figure 4. Gate Charge

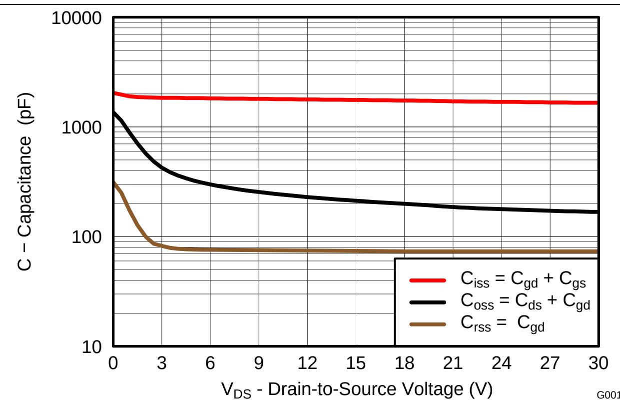
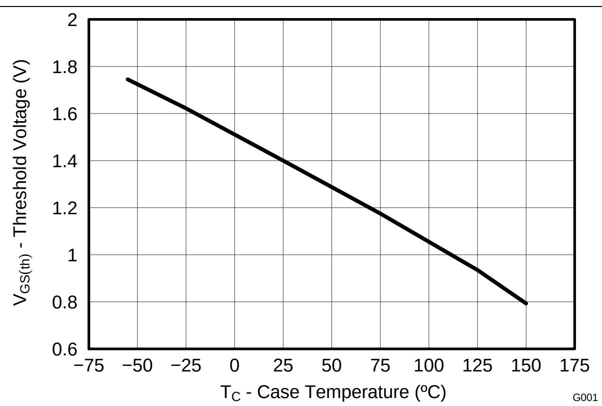


Figure 5. Capacitance



I_D = 250 µA

Figure 6. Threshold Voltage vs Temperature

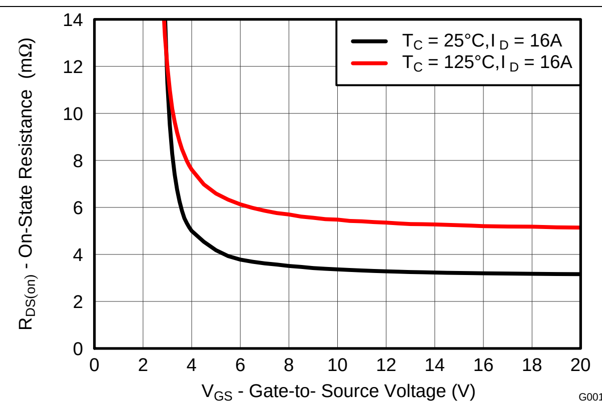
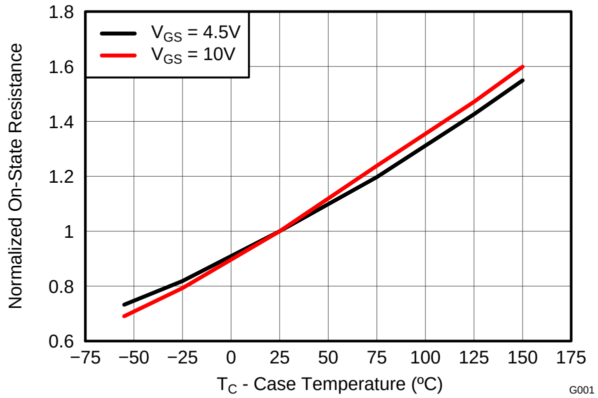


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



I_D = 18 A

Figure 8. Normalized On-State Resistance vs Temperature

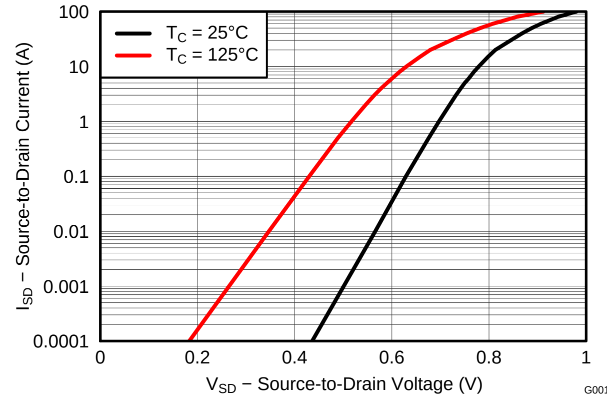
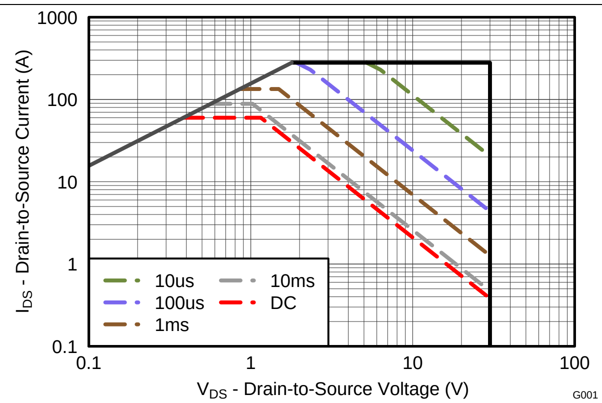


Figure 9. Typical Diode Forward Voltage



Single Pulse, Max $R_{\theta JC}$ = 2.8°C/W

Figure 10. Maximum Safe Operating Area

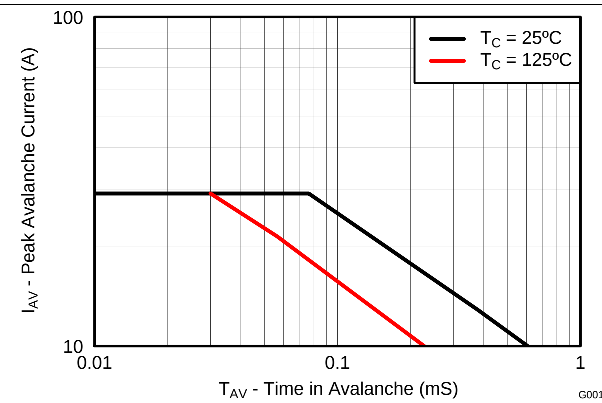


Figure 11. Single Pulse Unclamped Inductive Switching

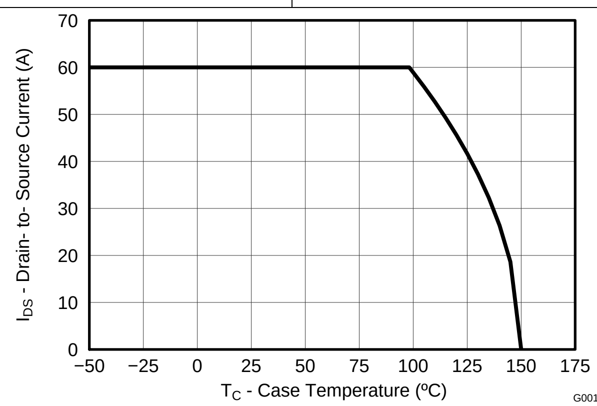


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 术语表

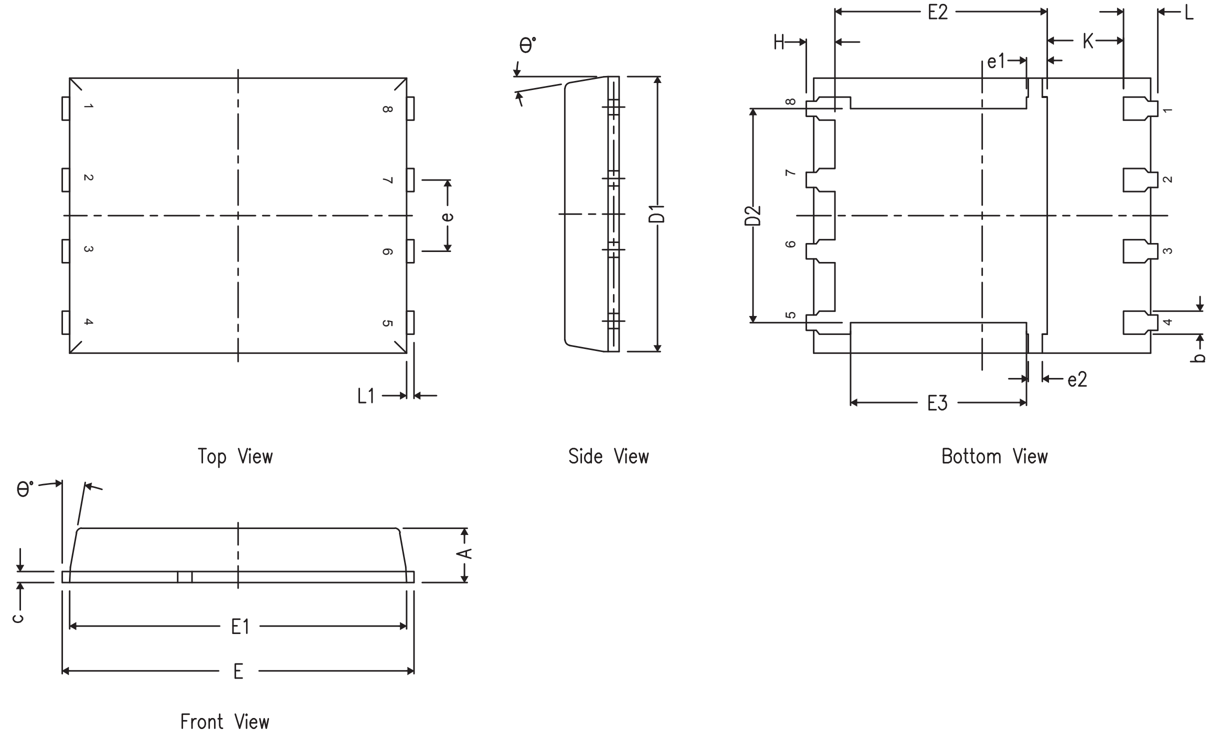
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

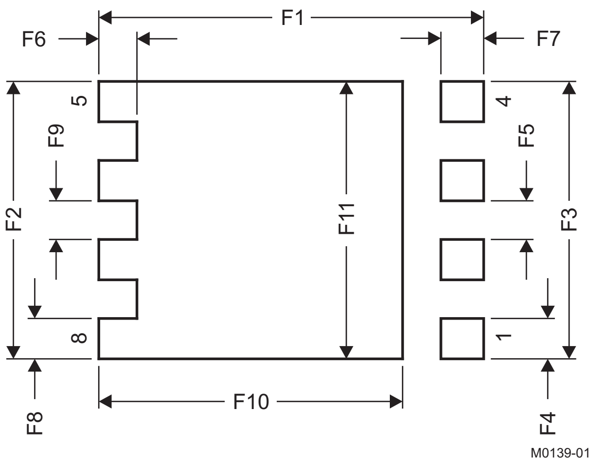
以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q5A 封装尺寸



DIM	毫米		
	最小值	标称值	最大值
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10	—	—
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°	—	12°

7.2 建议印刷电路板 (PCB) 布局

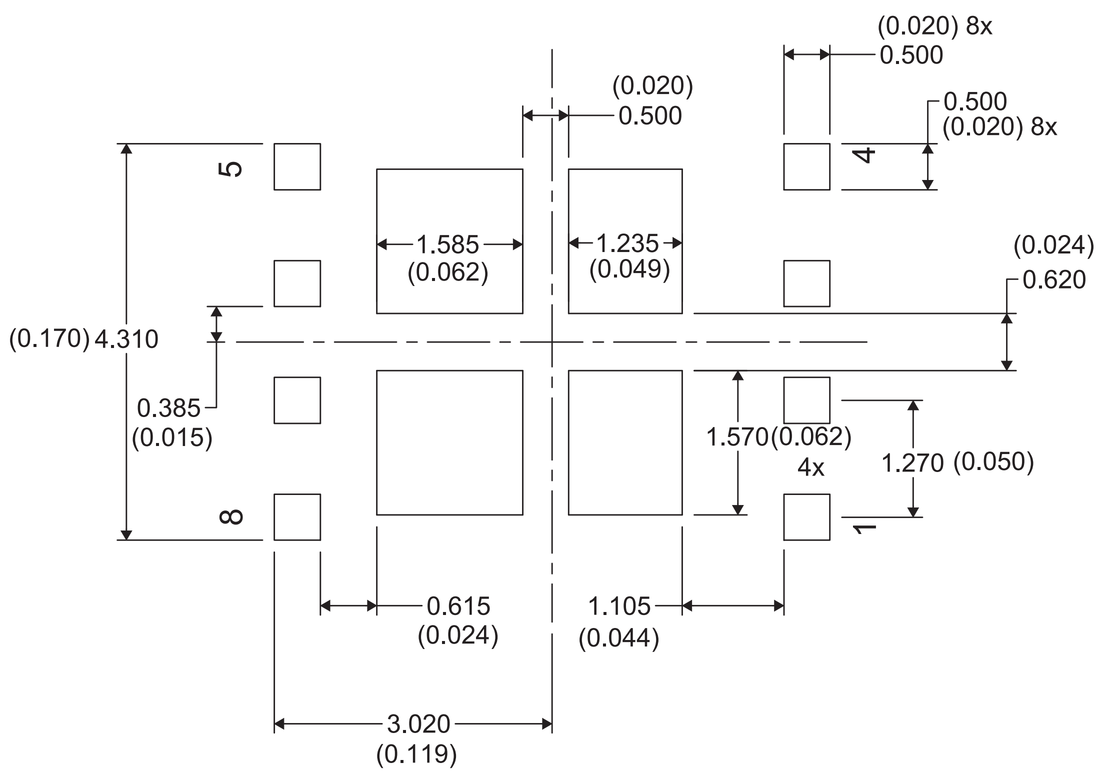


建议印刷电路板 (PCB) 布局 (continued)

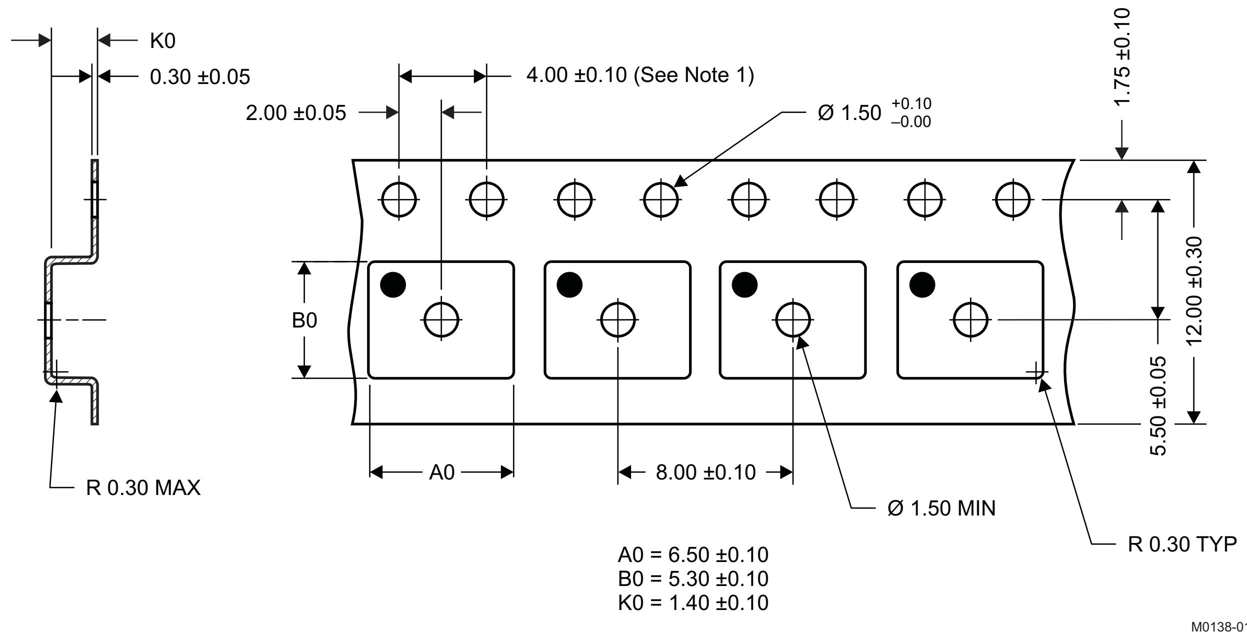
DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模板开口



7.4 Q5A 卷带信息



谨记：

1. 10 个链齿孔的累积容差为 ±0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 高于孔眼底部 0.3mm 的平面上测得的 A0 和 B0。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17577Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD17577	Samples
CSD17577Q5AT	ACTIVE	VSONP	DQJ	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD17577	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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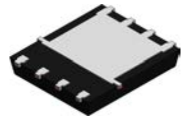
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

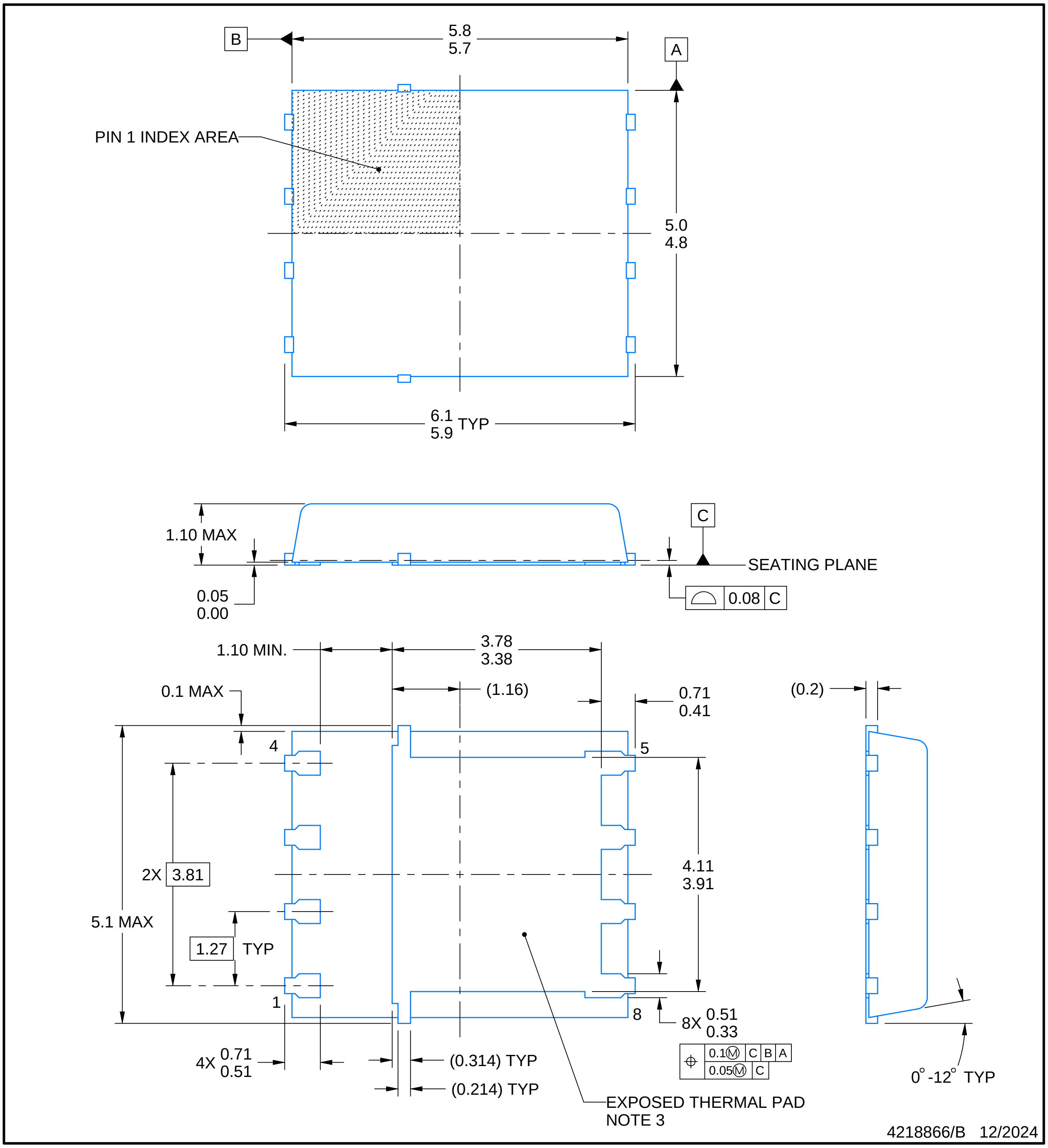


PACKAGE OUTLINE

DQJ0008A

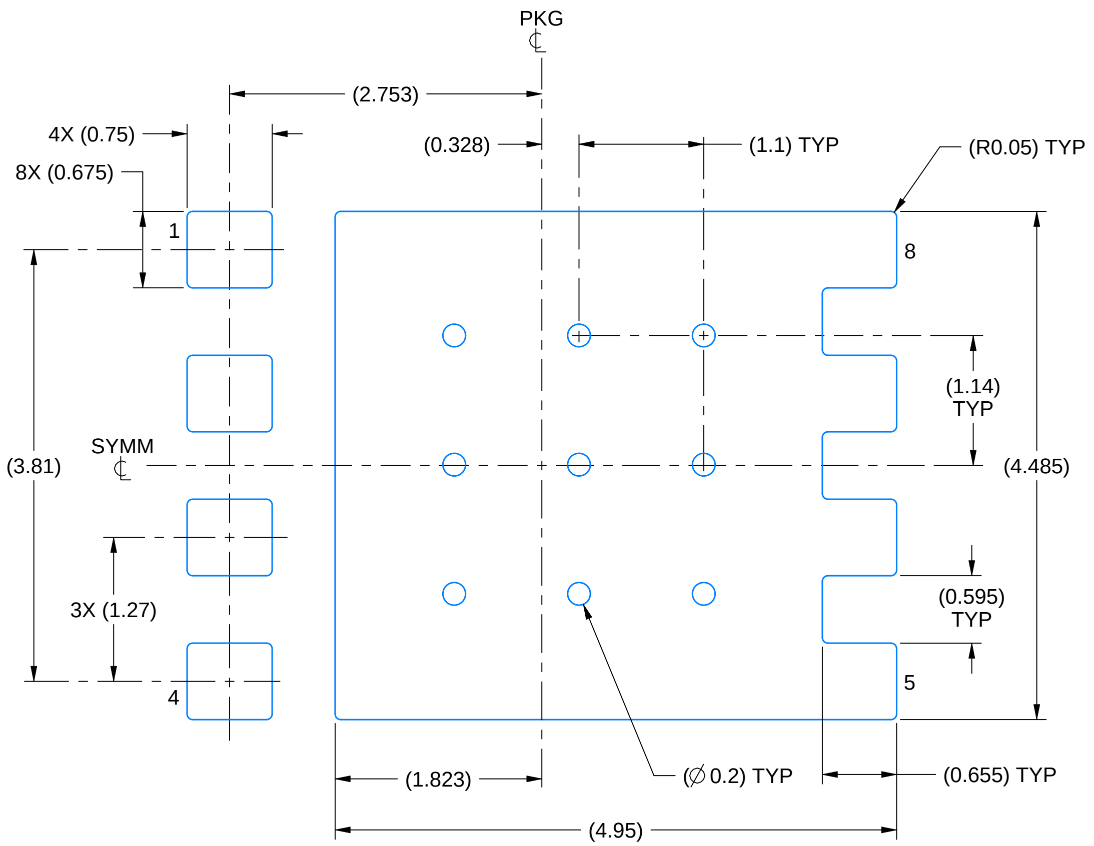
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

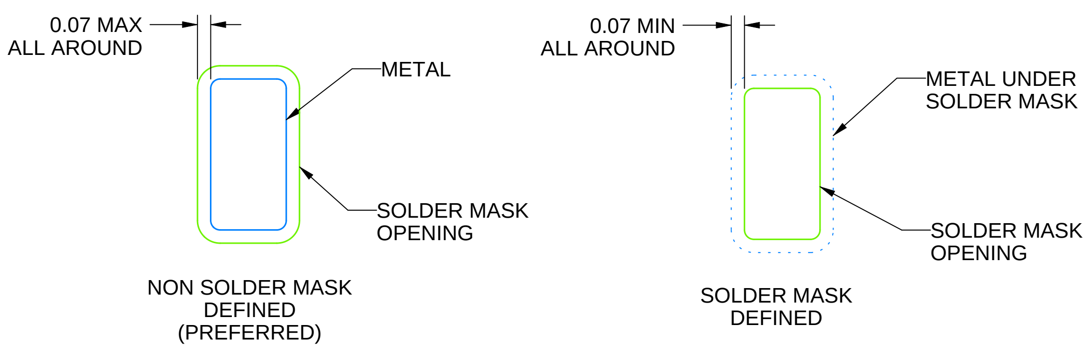


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X

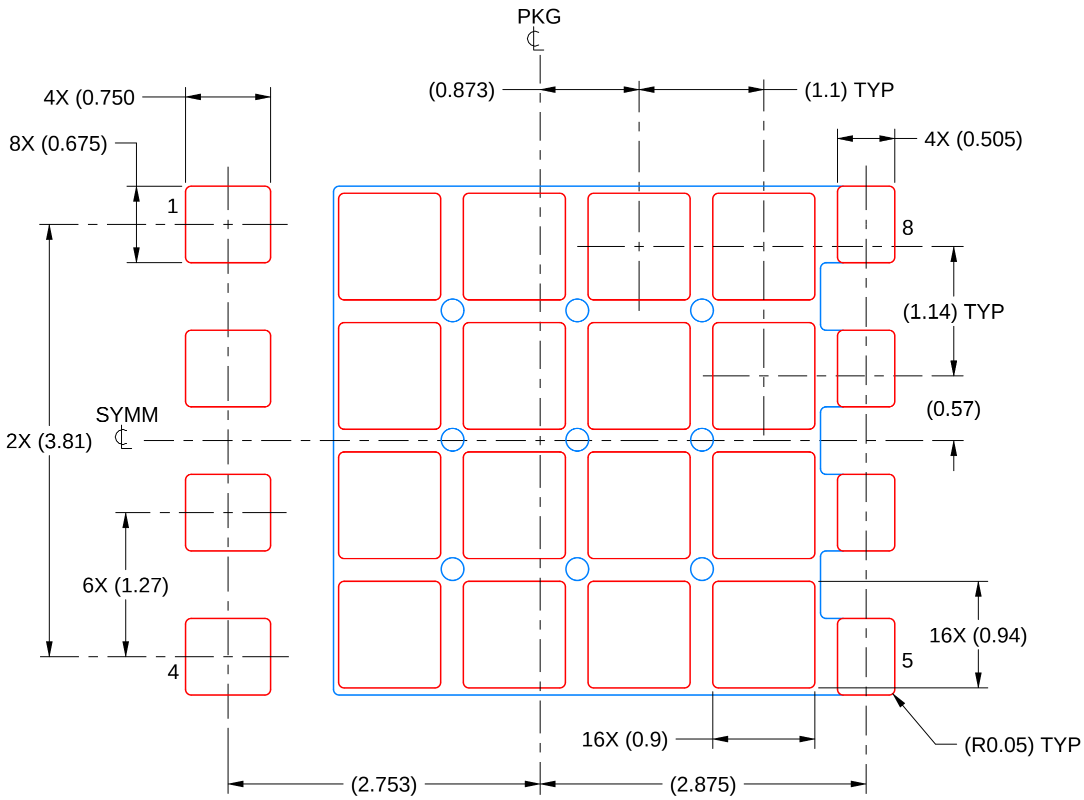


SOLDER MASK DETAILS

4218866/B 12/2024

NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

4218866/B 12/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明