CSD19536KTT 100V N 通道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- D^2PAK 塑料封装

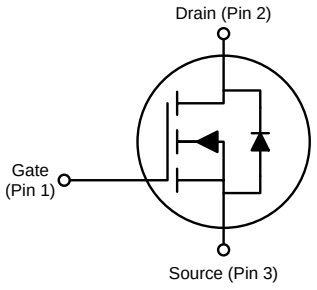
2 应用

- 次级侧同步整流器
- 热插拔
- 电机控制

3 说明

这款 100V、2mΩ、D^2PAK (TO-263) NexFET™功率 MOSFET 旨在最大限度地降低功率转换应用中的 损耗。

引脚分配



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	100		V
Q_g	栅极电荷总量 (10V)	118		nC
Q_{gd}	栅极电荷（栅极到漏极）	17		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	2.2	mΩ
		V_{GS} = 10V	2	
$V_{GS(th)}$	阈值电压	2.5		V

器件信息(1)

器件	数量	包装介质	封装	运输
CSD19536KTT	500	13 英寸卷带	D^2PAK 塑料封装	卷带封装
CSD19536KTTT	50			

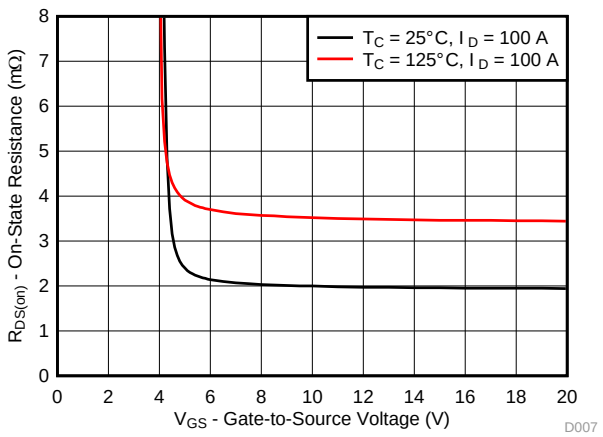
(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

绝对最大额定值

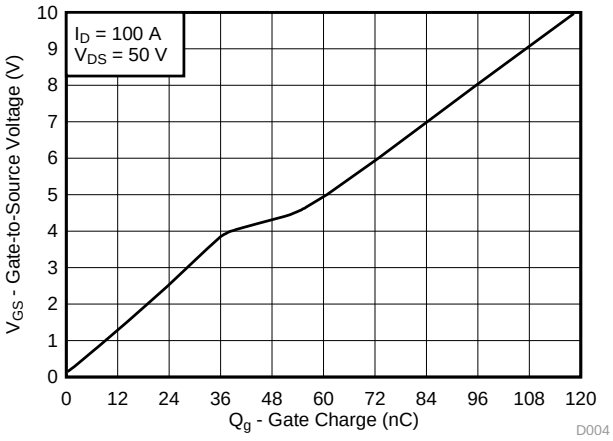
T_A = 25°C		值	单位
V_{DS}	漏源电压	100	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	200	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	272	
	持续漏极电流（受芯片限制），T_C = 100°C 时测得	192	
I_{DM}	脉冲漏极电流(1)	400	A
P_D	功率耗散	375	W
T_J, T_{stg}	工作结温，储存温度	-55 至 175	°C
E_{AS}	雪崩能量，单脉冲 I_D = 127A，L = 0.1mH，R_G = 25Ω	806	mJ

(1) 最大 $R_{\theta JC}$ = 0.4°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



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4 修订历史记录

Changes from Revision A (May 2015) to Revision B **Page**

- 已添加 *接收文档更新通知* 部分 ... 7
- 更新了封装图 ... 8
- 更新了 PCB 图 ... 9
- 更新了模版图 ... 10

Changes from Original (March 2015) to Revision A **Page**

- 添加了*社区资源*部分 ... 7
- 已添加 PCB 和模板布局图至 *机械、封装和可订购信息* ... 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	100			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 80 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.1	2.5	3.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 6 V, I_D = 100 A		2.2	2.8	mΩ
		V_{GS} = 10 V, I_D = 100 A		2	2.4	
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 100 A		329		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz		9250	12000	pF
C_{oss}	Output capacitance			1820	2370	pF
C_{rss}	Reverse transfer capacitance			47	61	pF
R_G	Series gate resistance			1.4	2.8	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 50 V, I_D = 100 A		118	153	nC
Q_{gd}	Gate charge gate-to-drain			17		nC
Q_{gs}	Gate charge gate-to-source			37		nC
$Q_{g(th)}$	Gate charge at V_{th}			24		nC
Q_{oss}	Output charge	V_{DS} = 50 V, V_{GS} = 0 V		335		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 50 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω		13		ns
t_r	Rise time			8		ns
$t_{d(off)}$	Turnoff delay time			32		ns
t_f	Fall time			6		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 100 A, V_{GS} = 0 V		0.9	1.1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50 V, I_F = 100 A, di/dt = 300 A/μs		548		nC
t_{rr}	Reverse recovery time			103		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.4	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	°C/W

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

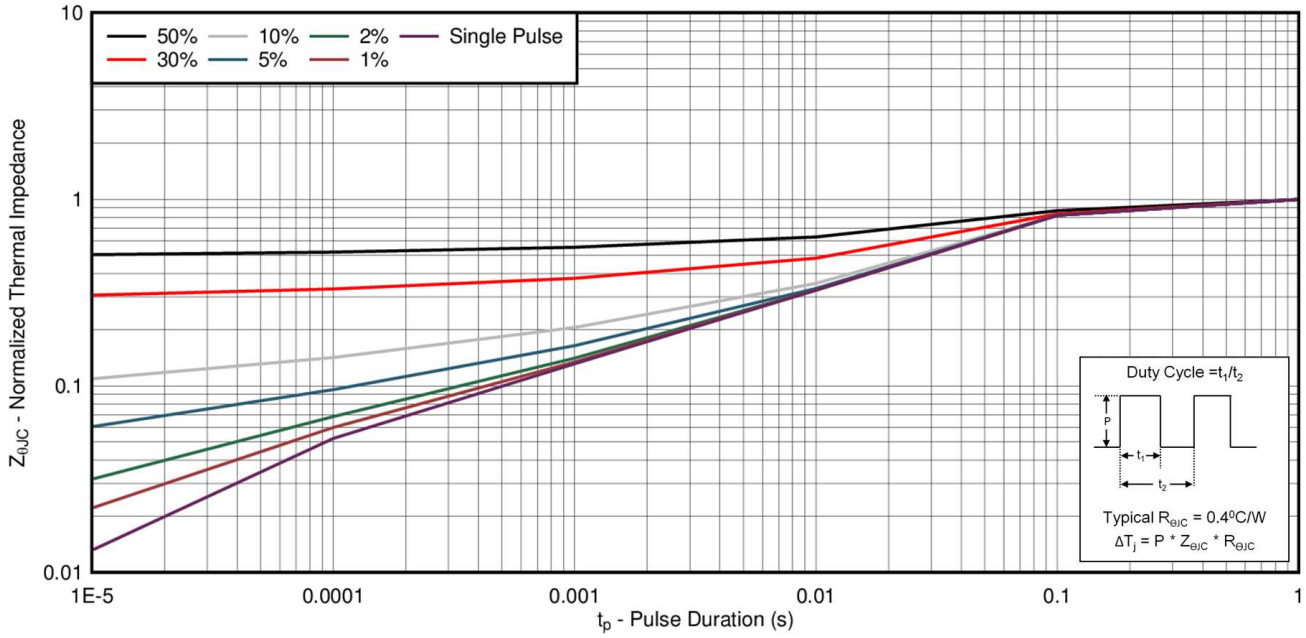


Figure 1. Transient Thermal Impedance

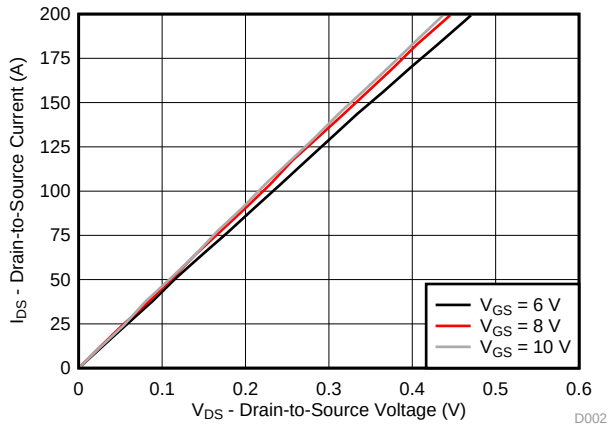


Figure 2. Saturation Characteristics

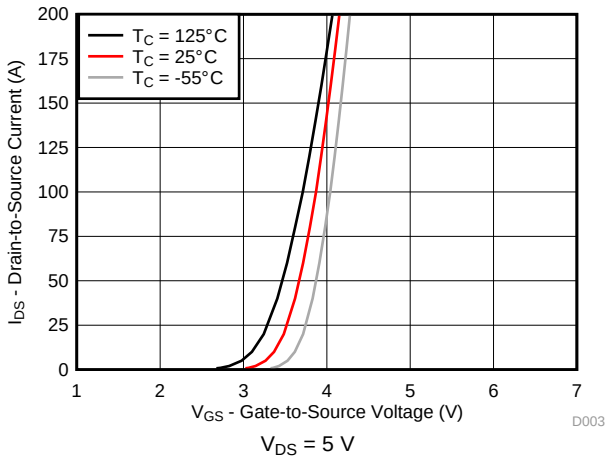


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

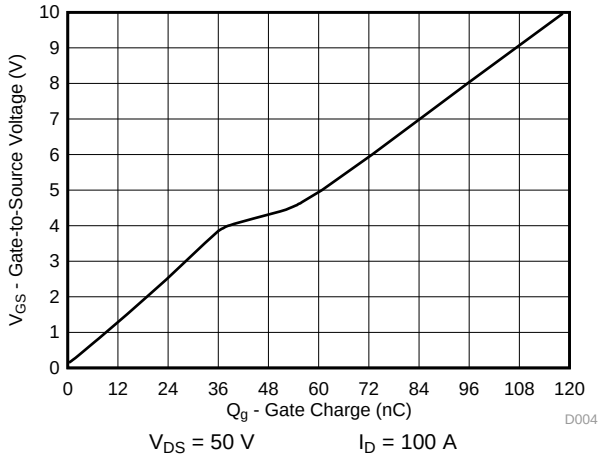


Figure 4. Gate Charge

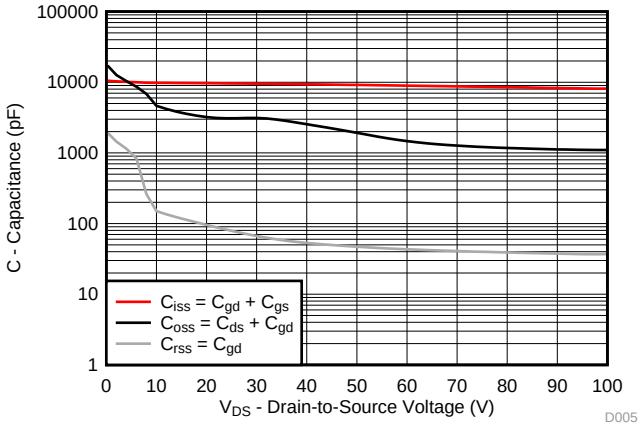


Figure 5. Capacitance

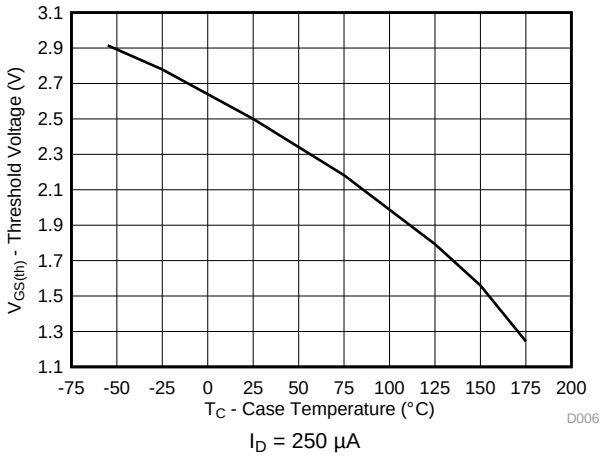


Figure 6. Threshold Voltage vs Temperature

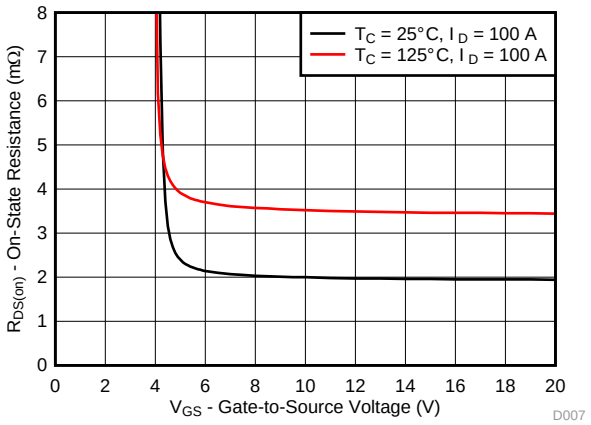


Figure 7. On-State Resistance vs Gate-to-Source Voltage

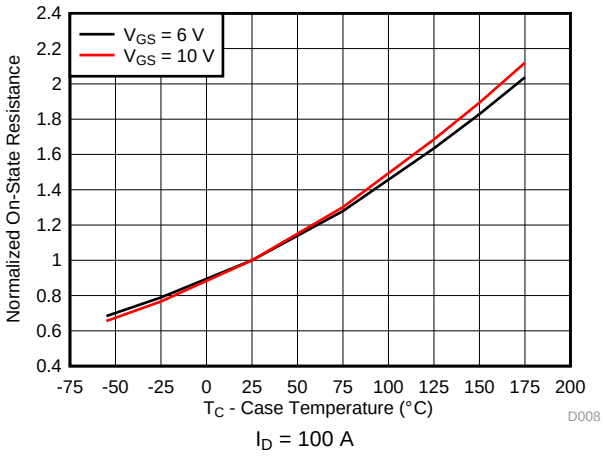


Figure 8. Normalized On-State Resistance vs Temperature

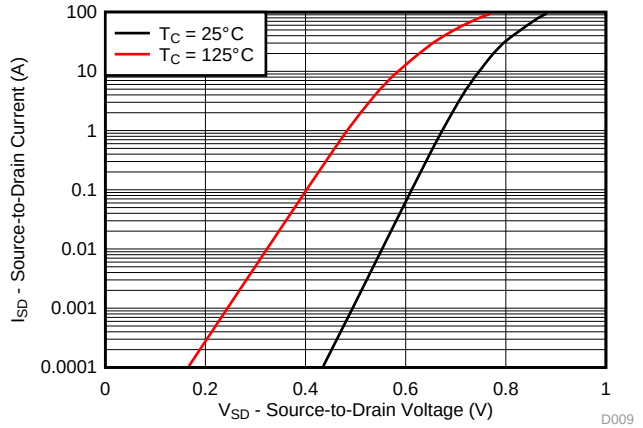


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

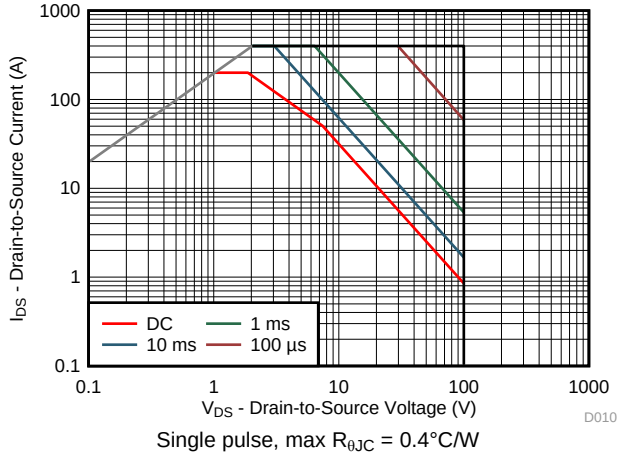


Figure 10. Maximum Safe Operating Area

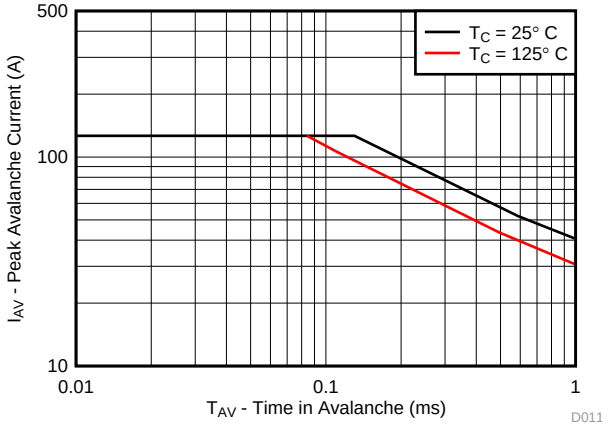


Figure 11. Single Pulse Unclamped Inductive Switching

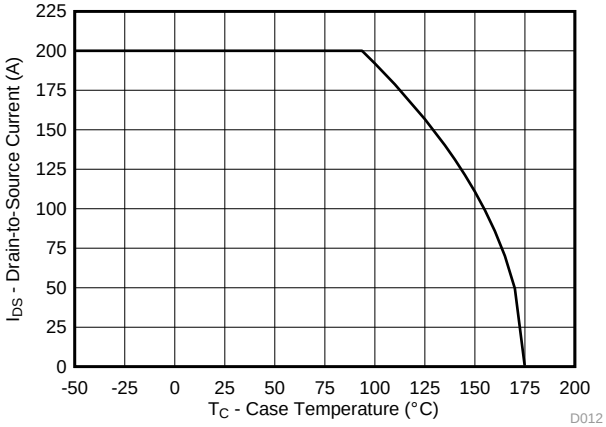


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

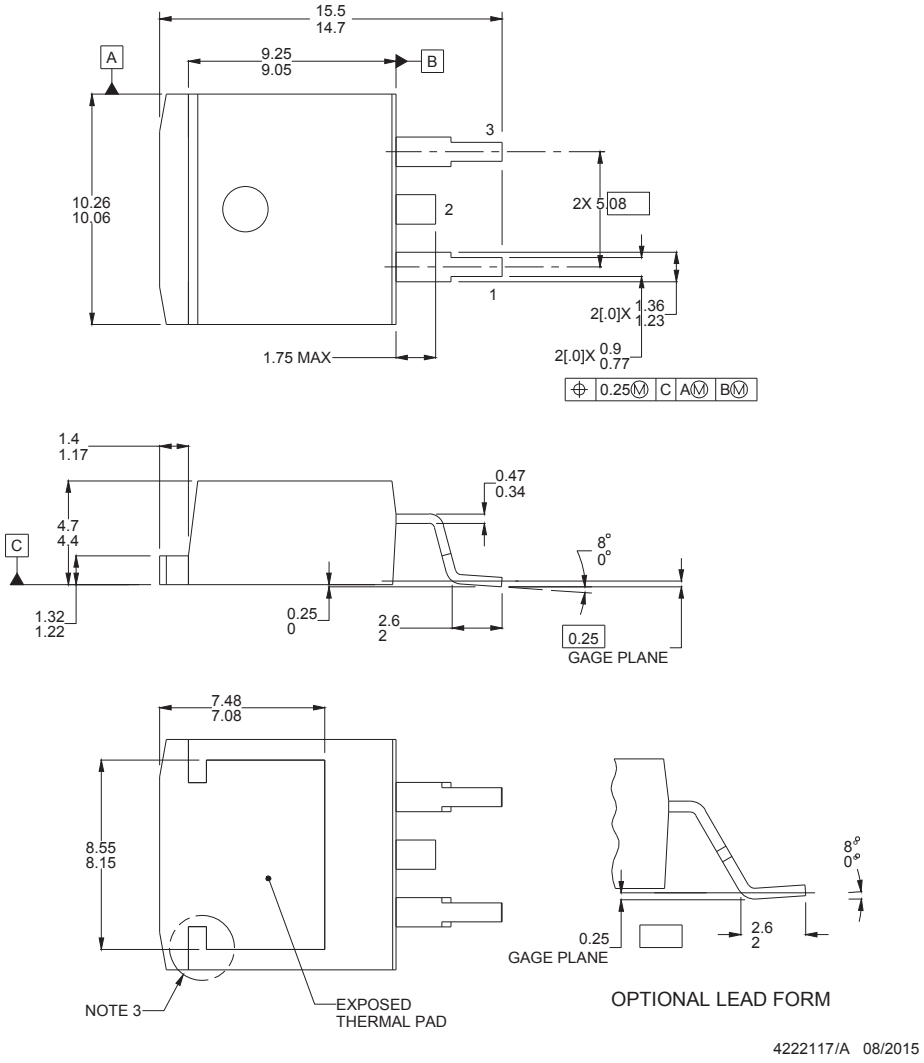
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

7.1 KTT 封装尺寸



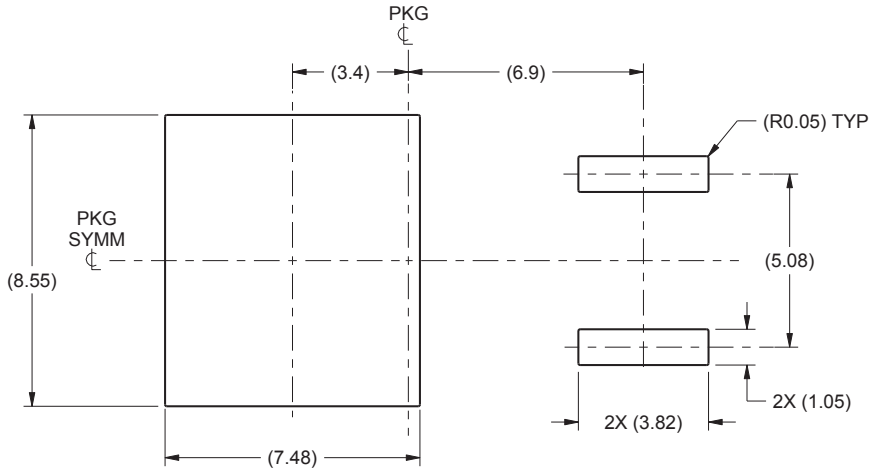
注：

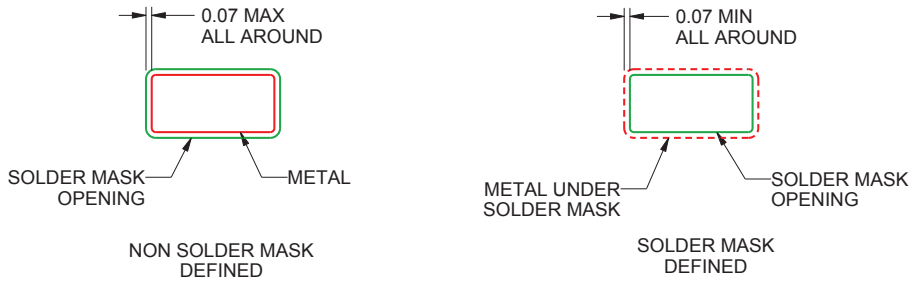
1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和容限值遵循 ASME Y14.5M。
2. 本图纸如有变更，恕不通知。
3. 来自 不同装配现场的产品可能不具备某些特性，形状也可能有所不同。

表 1. 引脚配置

位置	名称
引脚 1	栅极
引脚 2 / 标签	漏极
引脚 3	源极

7.2 推荐的 PCB 布局





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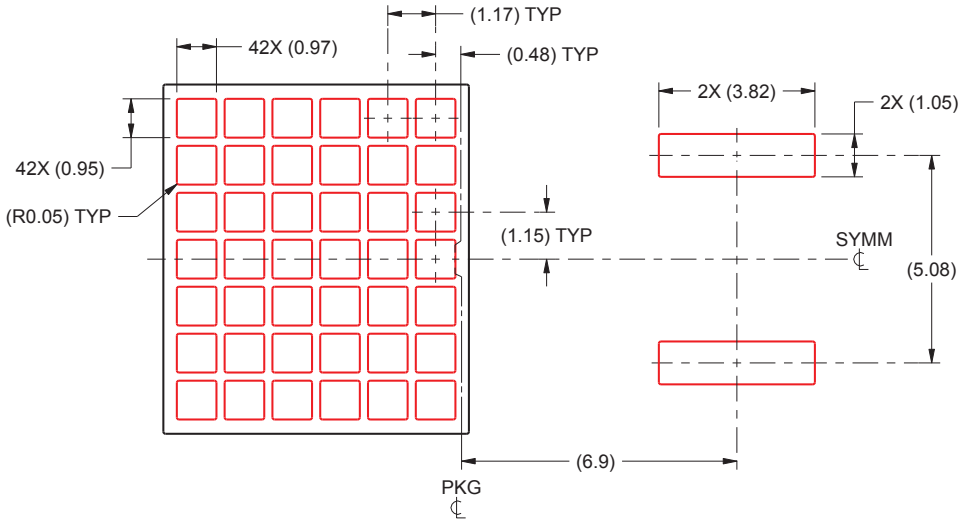
注：

1. 此封装设计用于焊接到电路板的散热焊盘上。有关详细信息，请参阅德州仪器 (TI) 文献编号 SLMA002 (www.ti.com/cn/lit/slma002) 和 SLMA004 (www.ti.com/cn/lit/slma004)。

7.3 建议模版开孔



注：

1. 具有漏斗形壁和圆角的激光切割窗孔将提供更佳的焊锡膏脱离。IPC-7525 可能提供其他替代性设计建议。
2. 在电路板装配现场，对于模板设计可能有不同的建议。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19536KTT	ACTIVE	DDPAK/ TO-263	KTT	2	500	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19536KTT	Samples
CSD19536KTTT	ACTIVE	DDPAK/ TO-263	KTT	2	50	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19536KTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

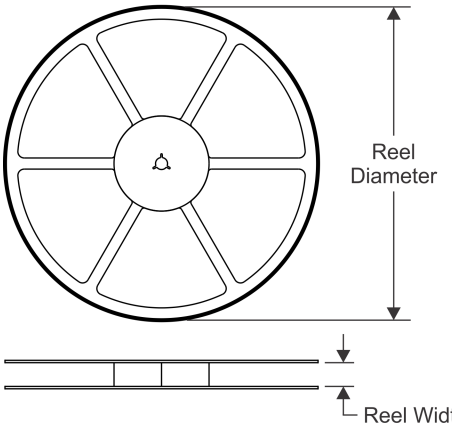
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

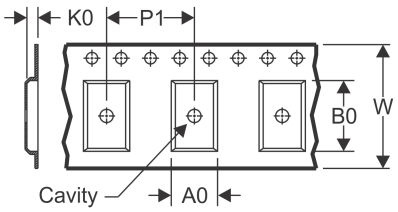
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

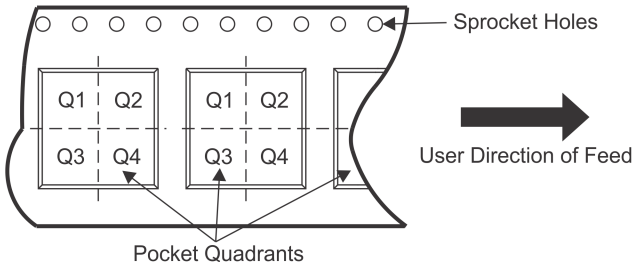


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

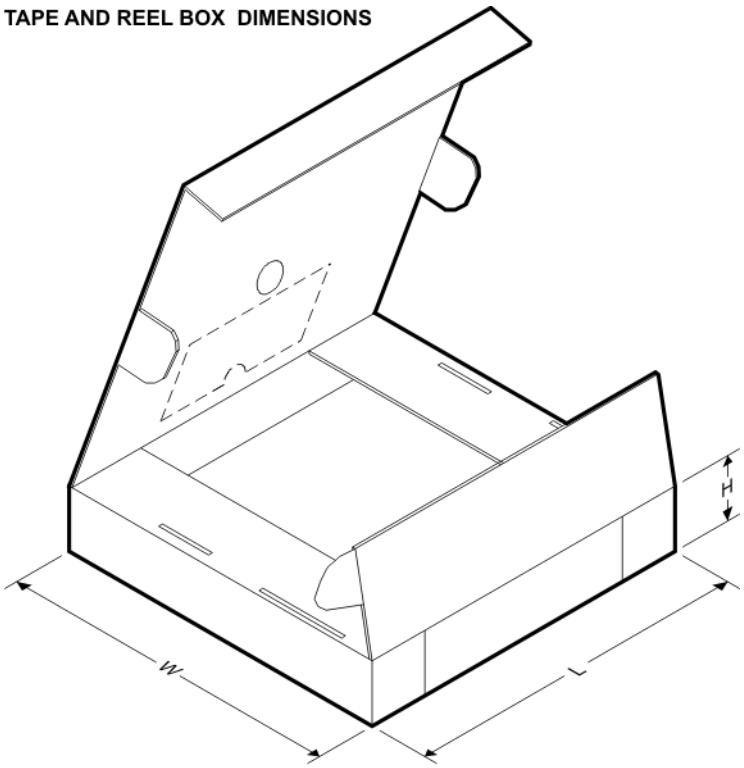
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD19536KTT	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD19536KTTT	DDPAK/ TO-263	KTT	3	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD19536KTT	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
CSD19536KTTT	DDPAK/TO-263	KTT	3	50	340.0	340.0	38.0

重要声明和免责声明

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