CSD23382F4 12V P 沟道 FemtoFET™ MOSFET

1 特性

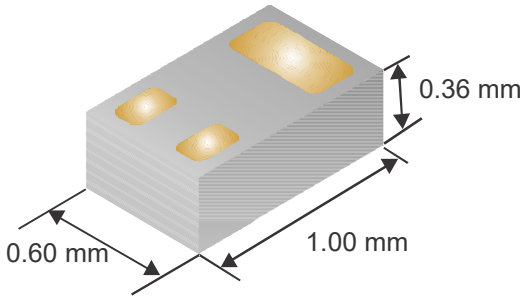
- 低导通电阻
- 超低 Q_g 和 Q_{gd}
- 超小封装尺寸（0402 外壳尺寸）
  - 1.0mm × 0.6mm
- 薄型封装
  - 最大高度为 0.36mm
- 集成型 ESD 保护二极管
  - 额定值 > 2kV HBM
  - 额定值 > 2kV CDM
- 铅端子镀层
- 无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 电池应用
- 手持式和移动类应用

3 说明

此 66mΩ、12V P 沟道 FemtoFET™ MOSFET 经过设计和优化，能够尽可能减小许多手持式和移动应用中的空间占用。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小至少 60%。



典型器件尺寸

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-12		V
Q_g	栅极电荷总量 (-4.5V)	1.04		nC
Q_{gd}	栅极电荷（栅漏极）	0.15		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -1.8V	149	mΩ
		V_{GS} = -2.5V	90	
		V_{GS} = -4.5V	66	
$V_{GS(th)}$	阈值电压	-0.8		V

订购信息(1)

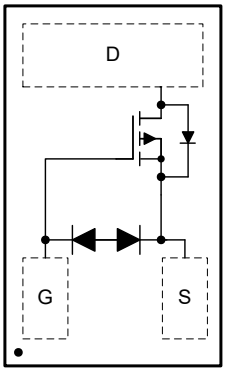
器件	数量	介质	封装	配送
CSD23382F4	3000	7 英寸卷带	Femto (0402) 1.0mm × 0.6mm 基板栅格阵列 (LGA)	卷带包装
CSD23382F4T	250	7 英寸卷带		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-12	V
V_{GS}	栅源电压	±8	V
I_D	持续漏极电流(1)	-3.5	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	-22	A
I_G	持续栅极钳位电流	-35	mA
	脉冲栅极钳位电流(2)	-350	
P_D	功率耗散(1)	500	mW
$V_{(ESD)}$	人体放电模型 (HBM)	2	kV
	充电器件模型 (CDM)	2	kV
T_J、T_{stg}	运行结温和贮存温度范围	-55 至 150	°C

(1) $R_{\theta JA}$ = 85°C/W（0.06 英寸 (1.52mm) 厚 FR4 PCB 上 1 平方英寸 (6.45cm²) 2oz (0.071mm) 厚的铜焊盘上的典型值）。
(2) 脉冲持续时间 ≤ 100 µs，占空比 ≤ 1%



顶视图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (October 2021) to Revision E (January 2022) — **Page**

- 将*特性* 部分中的最大高度从“0.35mm”更改为“0.36mm” 1
- 将*典型器件尺寸* 中的最大高度从“0.35mm”更改为“0.36mm” 1
- Changed maximum height from "0.35-mm" to "0.36-mm" in *Mechanical Dimensions* section 8

Changes from Revision C (October 2014) to Revision D (October 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Added footnote with link to support document 9

Changes from Revision B (July 2014) to Revision C (October 2014) — **Page**

- Corrected timing V_{DS} to read – 6 V 3

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–12			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –9.6 V			–1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –8 V			–10	μA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	–0.5	–0.8	–1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		149	199	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.5 A		90	105	mΩ
		V_{GS} = –4.5 V, I_{DS} = –0.5 A		66	76	mΩ
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.5 A		3.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –6 V, f = 1 MHz		180	235	pF
C_{oss}	Output Capacitance			118	154	pF
C_{rss}	Reverse Transfer Capacitance			12.8	16.6	pF
R_G	Series Gate Resistance			350		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –6 V, I_{DS} = –0.5 A		1.04	1.35	nC
Q_{gd}	Gate Charge Gate-to-Drain			0.15		nC
Q_{gs}	Gate Charge Gate-to-Source			0.50		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.18		nC
Q_{oss}	Output Charge	V_{DS} = –6 V, V_{GS} = 0 V		1.08		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –6 V, V_{GS} = –4.5 V, I_{DS} = –0.5 A, R_G = 2 Ω		28		ns
t_r	Rise Time			25		ns
$t_{d(off)}$	Turn Off Delay Time			66		ns
t_f	Fall Time			41		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = –0.5 A, V_{GS} = 0 V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= –6 V, I_F = –0.5 A, di/dt = 200 A/μs		1.8		nC
t_{rr}	Reverse Recovery Time			8.4		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYP	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)	85	°C/W
	Junction-to-Ambient Thermal Resistance(2)	245	

(1) Device mounted on FR4 material with 1-inch^2 (6.45 cm^2), 2-oz. (0.071-mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

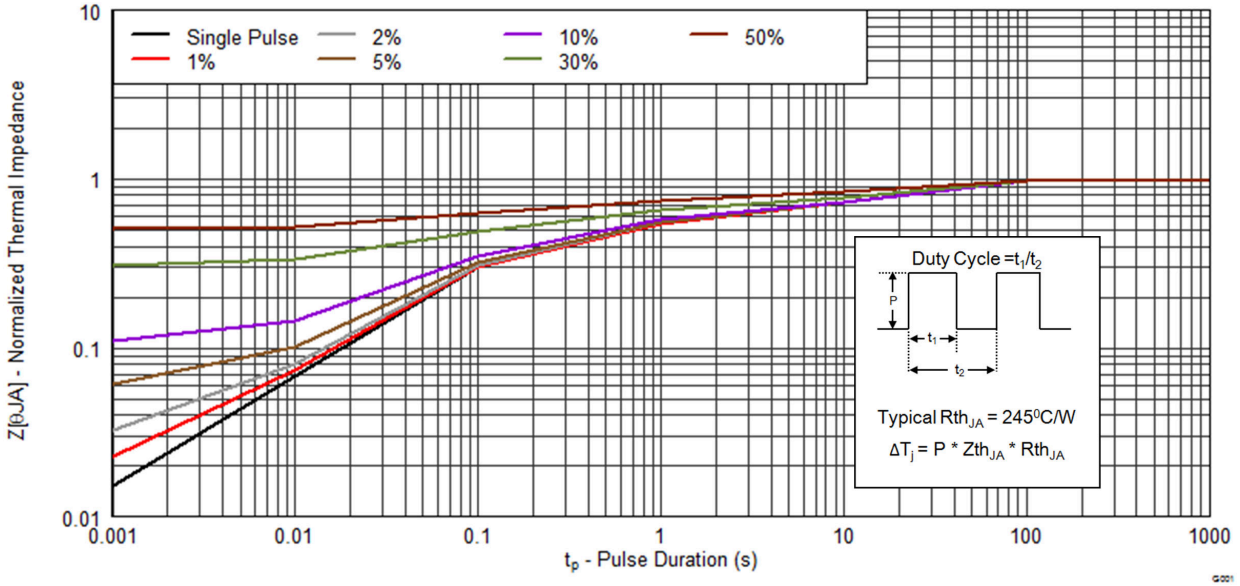


图 5-1. Transient Thermal Impedance

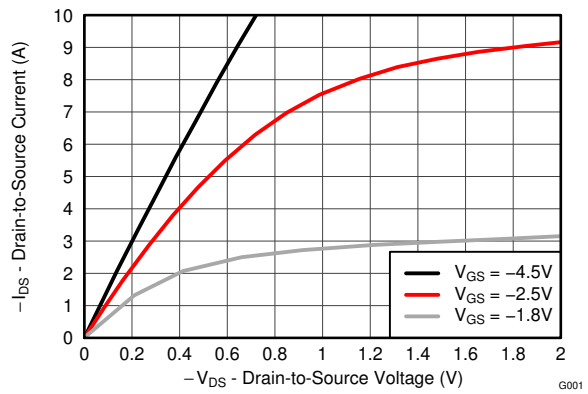
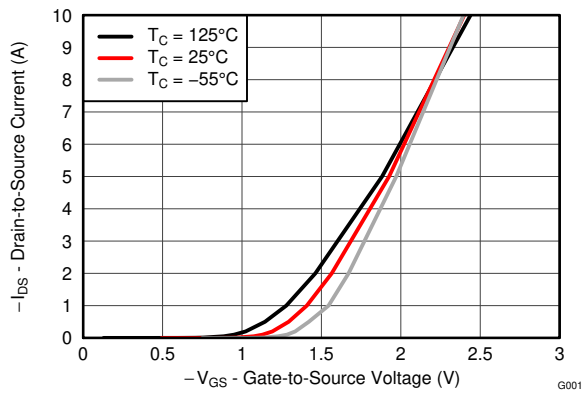


图 5-2. Saturation Characteristics

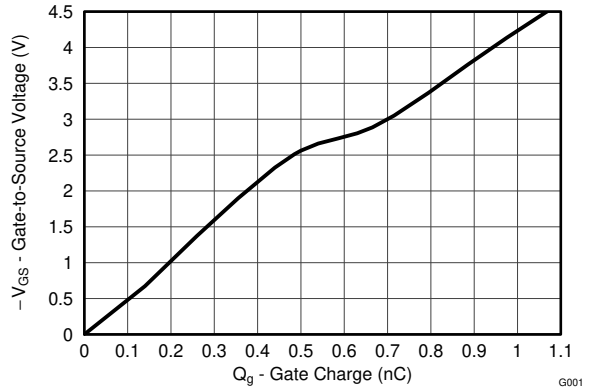


VDS = – 5 V

图 5-3. Transfer Characteristics

5.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



I_D = –0.5 A V_{DS} = 6 V

图 5-4. Gate Charge

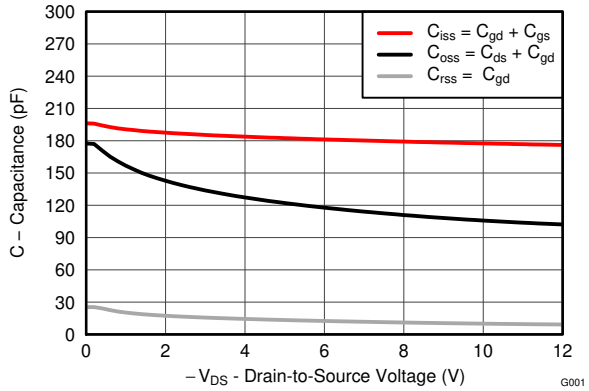
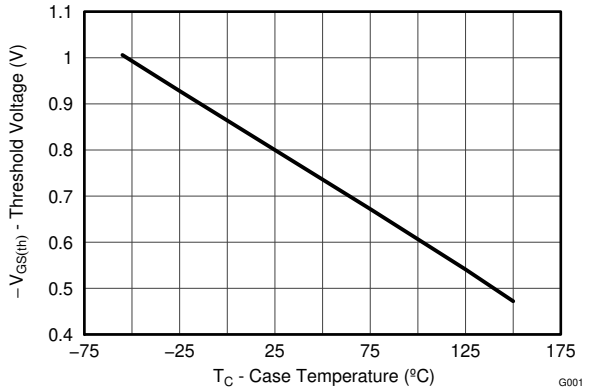


图 5-5. Capacitance



I_D = –250 µA

图 5-6. Threshold Voltage vs Temperature

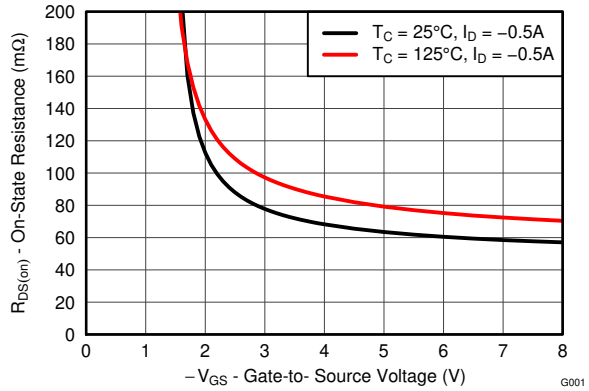
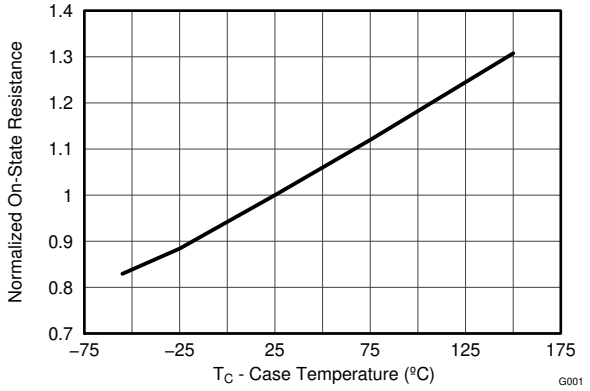


图 5-7. On-State Resistance vs Gate-to-Source Voltage



V_{GS} = –4.5 V I_D = –0.5 A

图 5-8. Normalized On-State Resistance vs Temperature

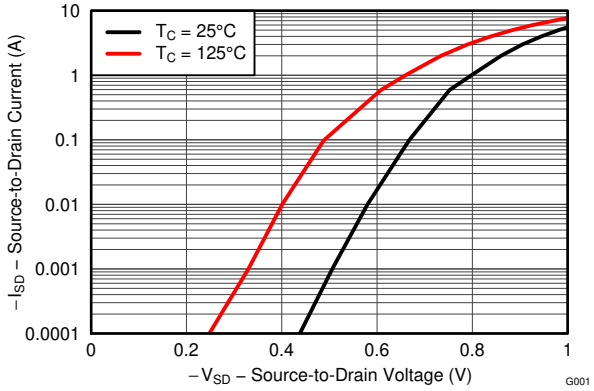
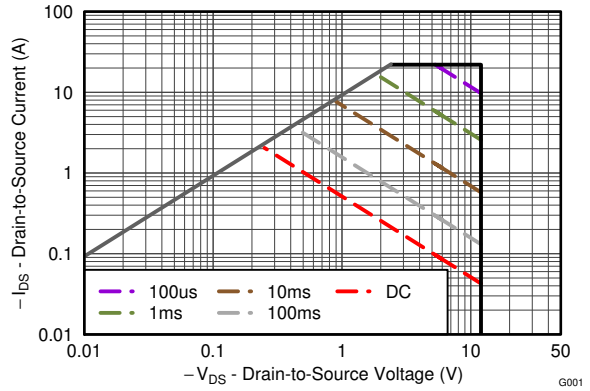


图 5-9. Typical Diode Forward Voltage

5.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



Single Pulse Typ $R_{\theta JA}$ = 245°C/W

图 5-10. Maximum Safe Operating Area

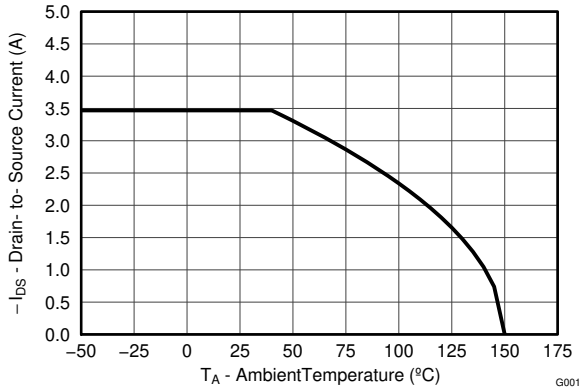


图 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

6.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

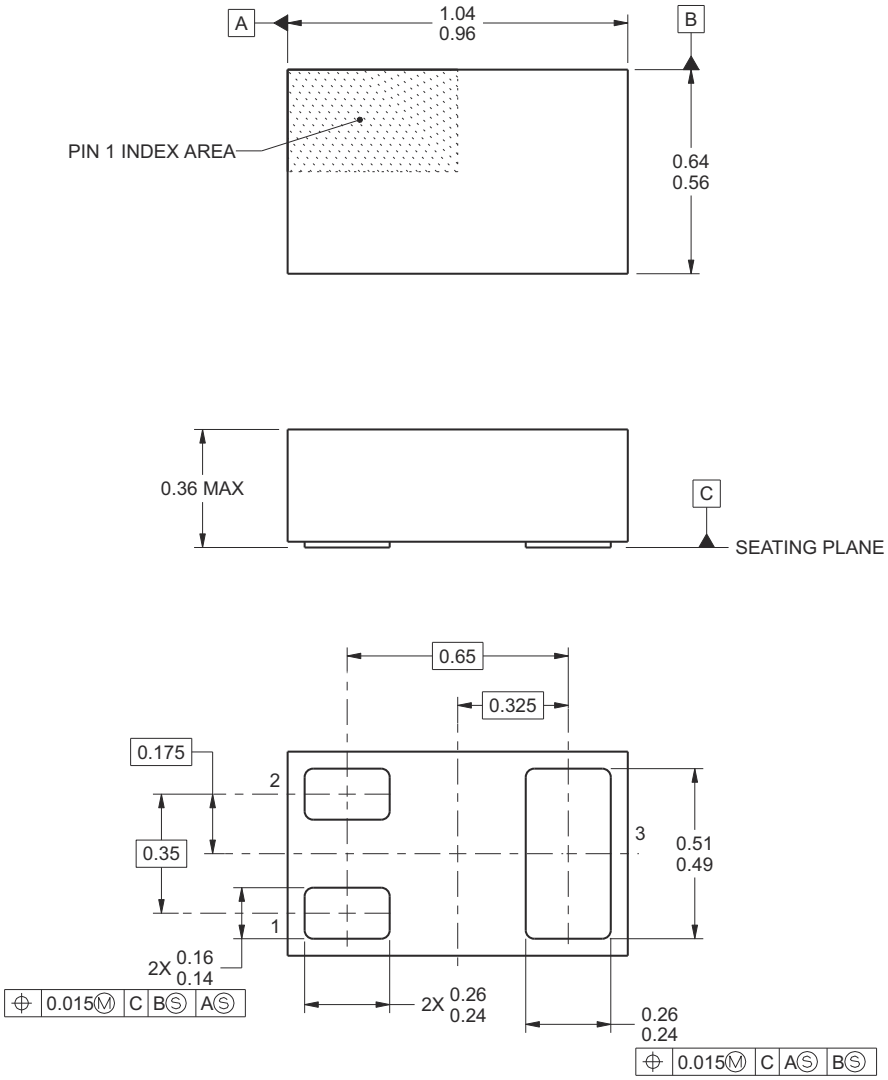
6.3 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

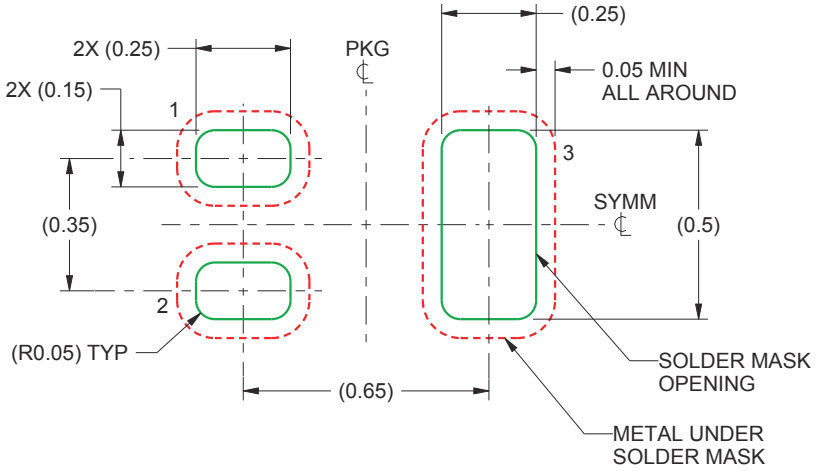


A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

Pin Configuration

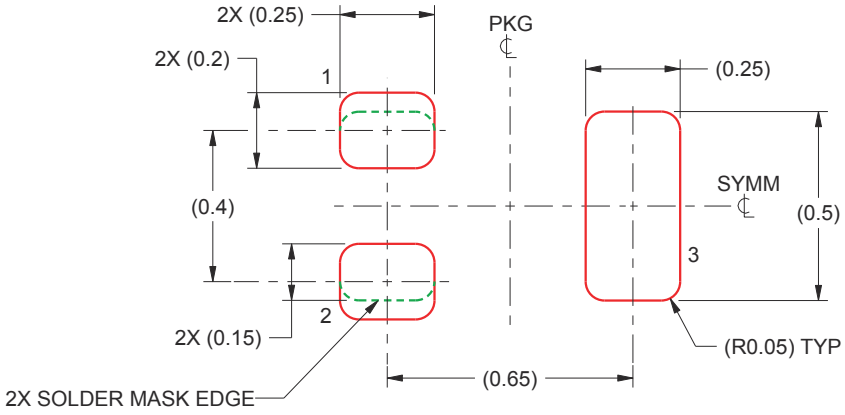
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



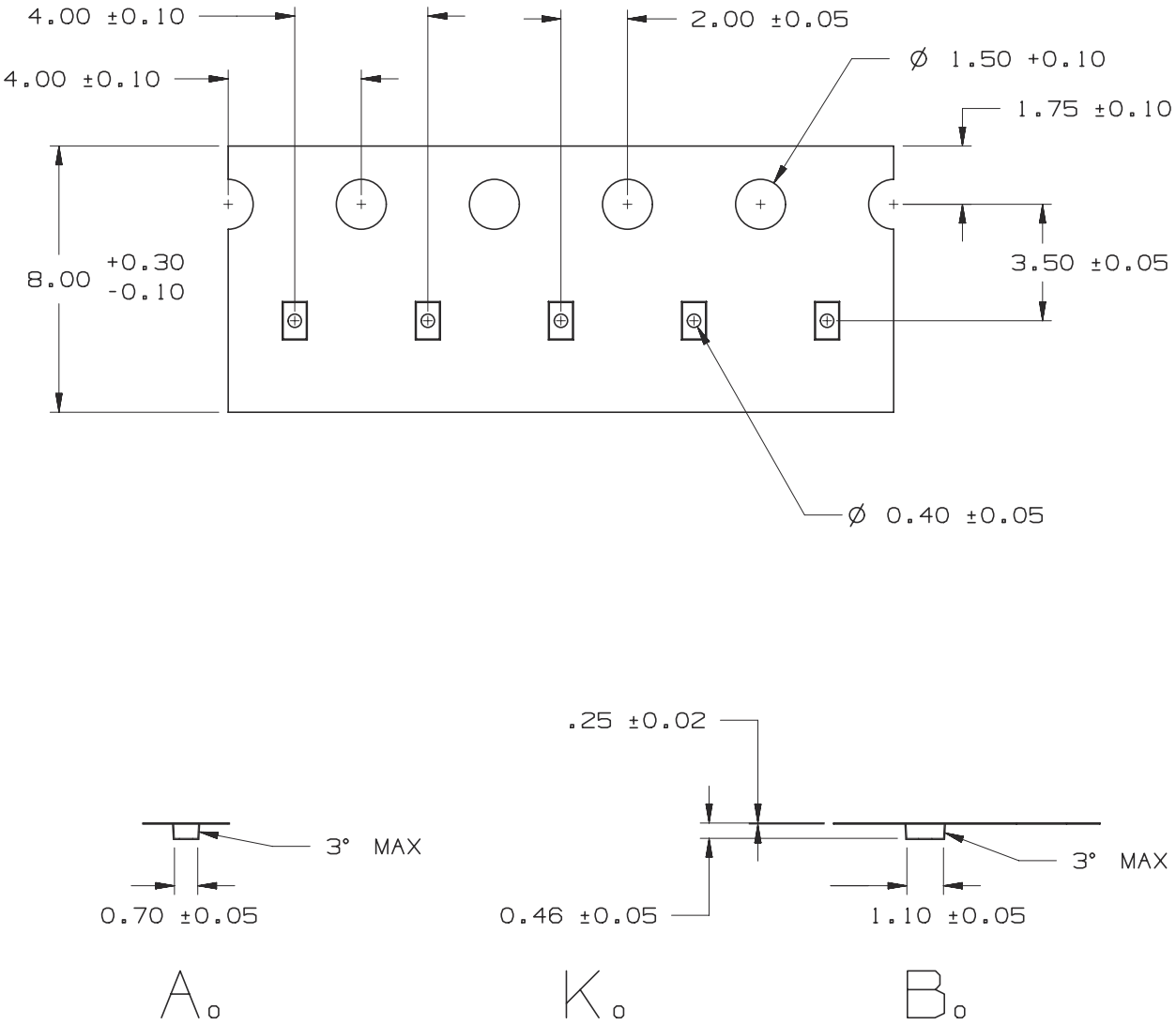
A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

7.4 CSD23382F4 Embossed Carrier Tape Dimensions



A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23382F4	ACTIVE	PICOSTAR	YJC	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	0 to 0	EM	Samples
CSD23382F4T	ACTIVE	PICOSTAR	YJC	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	EM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

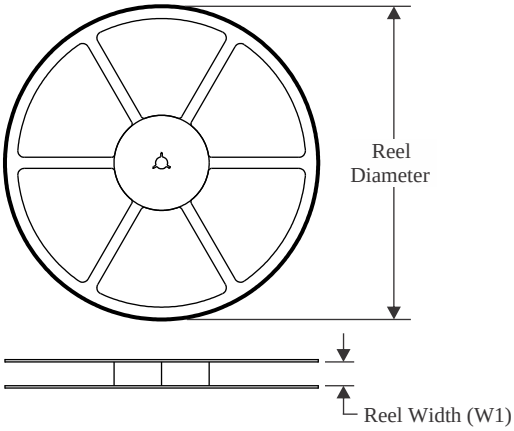
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

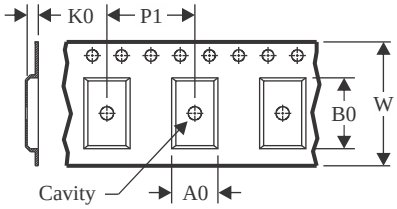
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

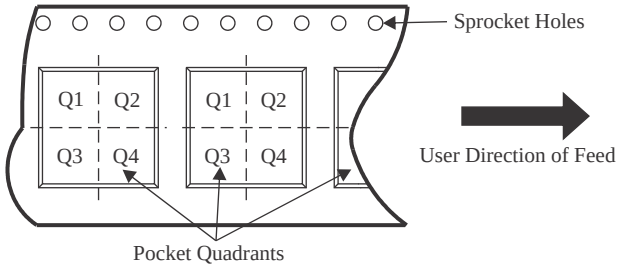


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

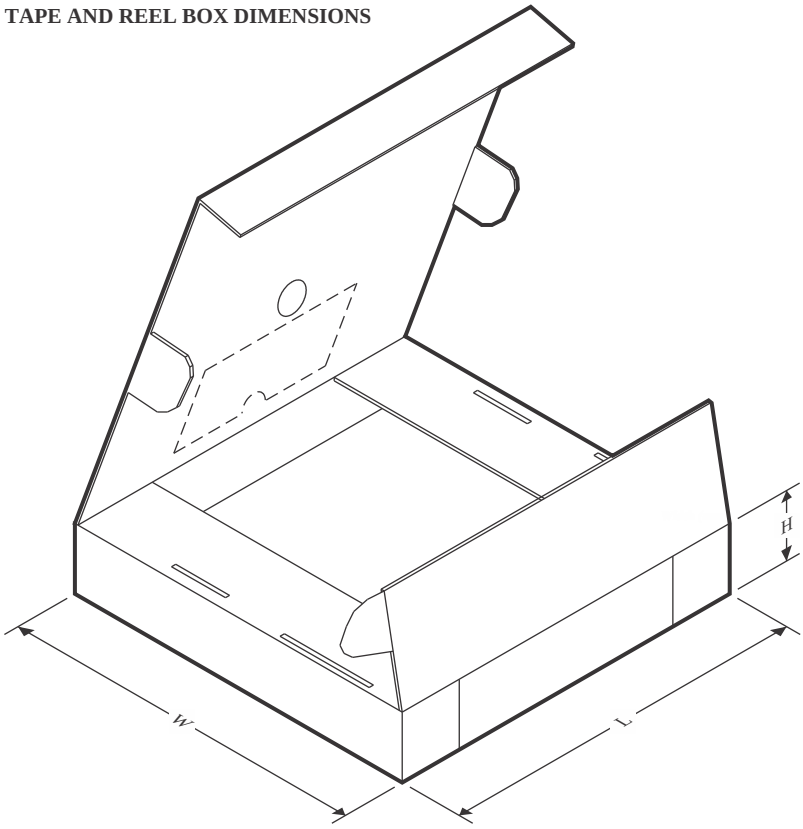
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD23382F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD23382F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD23382F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD23382F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

重要声明和免责声明

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