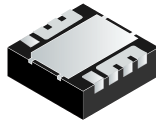


双路 20V N 通道 NextFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

特性

- 共源连接
- 超低漏极到漏极导通电阻
- 节省空间的小外形尺寸无引线 **(SON) 3.3mm x 3.3mm** 塑料封装
- 针对 **5V** 栅极驱动进行了优化
- 低热阻
- 雪崩额定值
- 无铅端子电镀
- 符合 **RoHS** 环保标准
- 无卤素

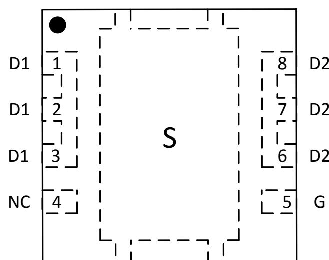
应用范围

- 针对笔记本个人电脑 **(PC)** 和平板电脑的适配器或 **USB** 输入保护

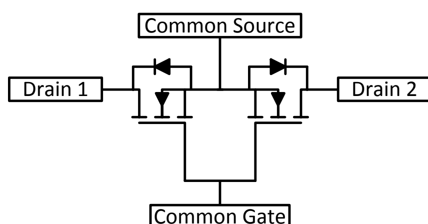
描述

CSD85312Q3E 是一款设计用于适配器或 USB 输入保护的 20V 共源、双路 N 通道器件。 此类 SON 3.3mm x 3.3mm 器件有低漏极到漏极导通电阻，这大大减少了损耗并且为空间受限的多节电池充电类应用提供低组件数量。

顶视图



电路图



产品概述

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	20		V
Q_g	栅极电荷总量 (4.5V)	11.7		nC
Q_{gd}	栅漏栅极电荷	1.6		nC
$R_{DD(on)}$	漏极到漏极导通电阻 (Q1 + Q2)	V_{GS} = 4.5V	11.7	mΩ
		V_{GS} = 8V	10.3	mΩ
$V_{GS(th)}$	阀值电压	1.1		V

订购信息

器件	封装	介质	数量	出货
CSD85312Q3E	SON 3.3mm x 3.3mm 塑料封装	13 英寸卷带	2500	卷带封装

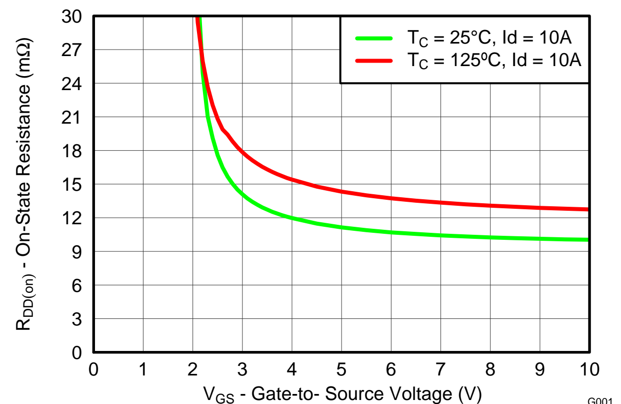
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	20	V
V_{GS}	栅源电压	+10 / -8	V
I_D	持续漏极电流（受封装限制）	39	A
	持续漏极电流 (1)	12	A
I_{DM}	脉冲漏极电流 (2)	76	A
P_D	功率耗散	2.5	W
T_J，T_{STG}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 38A，L = 0.1mH，R_G = 25Ω	72	mJ

(1) $R_{\theta JA}$ = 63°C/W，这是在一块厚度为 0.06 英寸 (1.52mm) 的 FR4 印刷电路板 (PCB) 上的一英寸^2（2 盎司）铜过渡垫片上测得的典型值

(2) 脉冲持续时间 ≤ 300μs，占空比 ≤ 2%

V_{GS} 与 $R_{DD(on)}$ 间的关系



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English Data Sheet: SLPS457

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0 V, I_D = 250 μA	20			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0 V, V_{DS} = 16 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0 V, V_{GS} = +10/–8 V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.85	1.10	1.40	V
$R_{DD(on)}$	Drain to Drain On Resistance (Q1 + Q2)	V_{GS} = 4.5 V, I_D = 10 A		11.7	14.0	mΩ
		V_{GS} = 8 V, I_D = 10 A		10.3	12.4	mΩ
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 10 A		99		S
Dynamic Characteristics(1)						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 10 V, f = 1 MHz		1840	2390	pF
C_{oss}	Output Capacitance			492	640	pF
C_{rss}	Reverse Transfer Capacitance			31	40	pF
R_G	Series Gate Resistance			5.5	11	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 10 V, I_D = 10 A		11.7	15.2	nC
Q_{gd}	Gate Charge Gate to Drain			1.6		nC
Q_{gs}	Gate Charge Gate to Source			3.5		nC
$Q_{g(th)}$	Gate Charge at Vth			1.8		nC
Q_{oss}	Output Charge	V_{DS} = 10 V, V_{GS} = 0 V		8.9		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 10 V, V_{GS} = 4.5 V, I_{DS} = 10 A, R_G = 2 Ω		11		ns
t_r	Rise Time			27		ns
$t_{d(off)}$	Turn Off Delay Time			24		ns
t_f	Fall Time			6		ns
Diode Characteristics(1)						
V_{SD}	Diode Forward Voltage	I_{SD} = 10 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 10 V, I_F = 10 A, di/dt = 300 A/μs		15		nC
t_{rr}	Reverse Recovery Time			23		ns

(1) All Dynamic and Diode Characteristics were measured with respect to one of the two drains, with the other left floating.

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{θJC}$	Thermal Resistance Junction to Case(1)			3.0	°C/W
$R_{θJA}$	Thermal Resistance Junction to Ambient(1)(2)			63	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2-oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.

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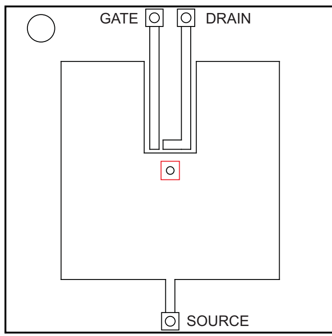
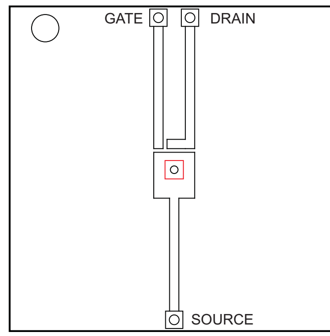


Max $R_{θJA}$ = 63°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{θJA}$ = 150°C/W when mounted on a minimum pad area of 2 oz. (0.071 mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

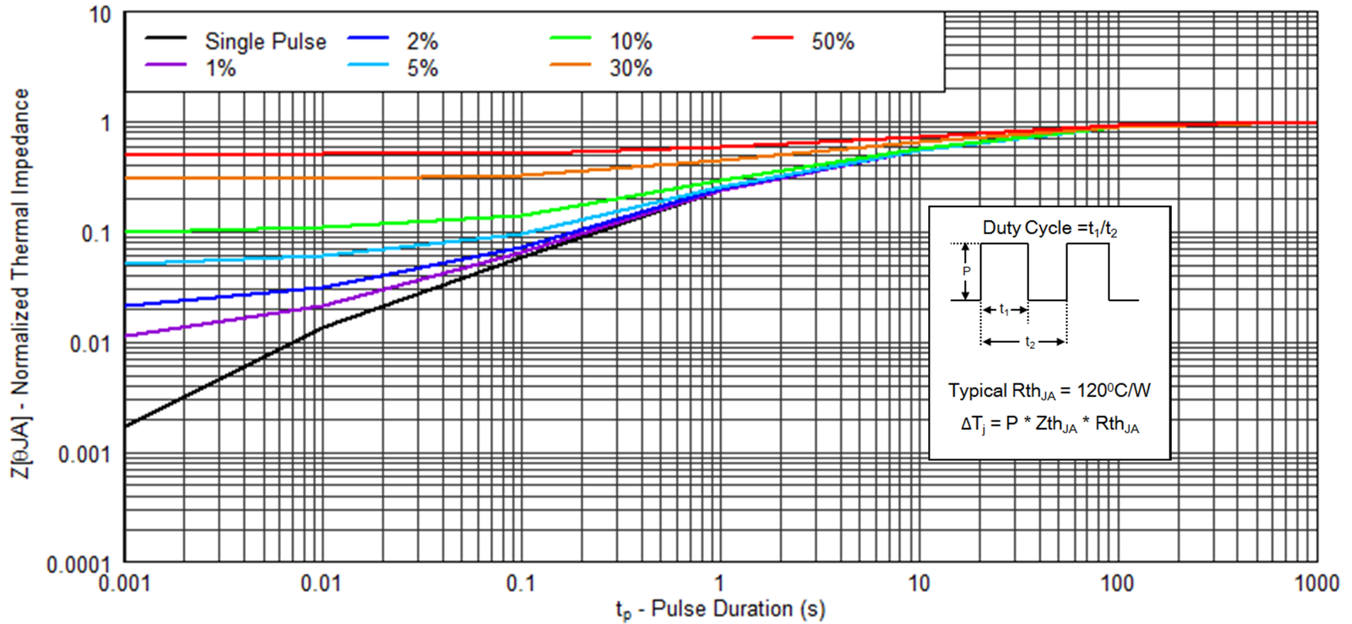


Figure 1. Transient Thermal Impedance

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

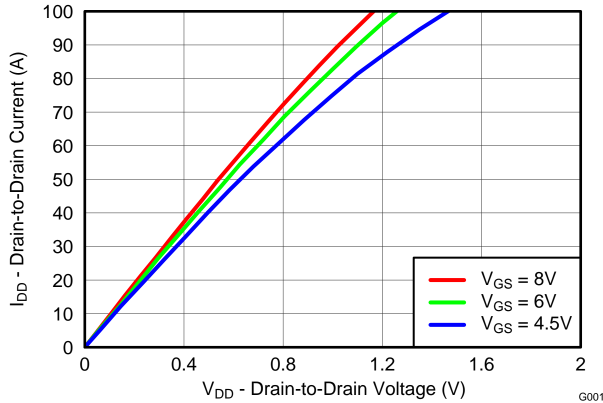

Figure 2. Saturation Characteristics

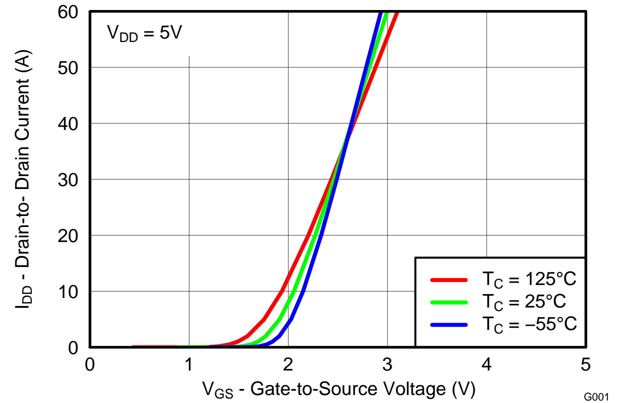

Figure 3. Transfer Characteristics

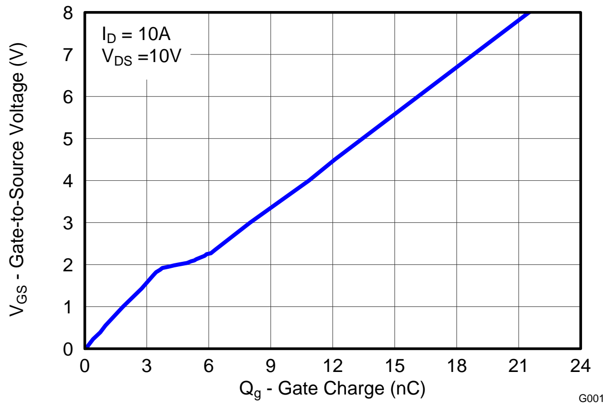

Figure 4. Gate Charge

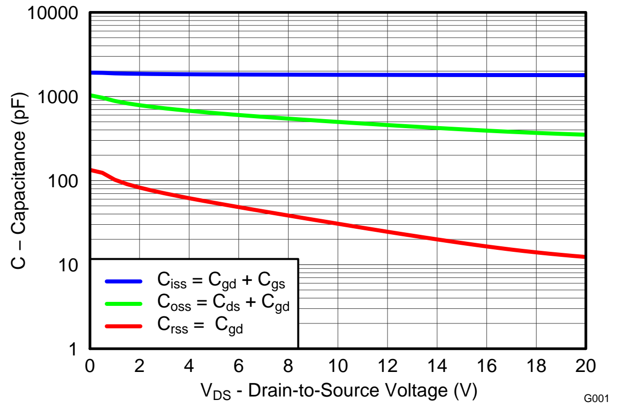

Figure 5. Capacitance

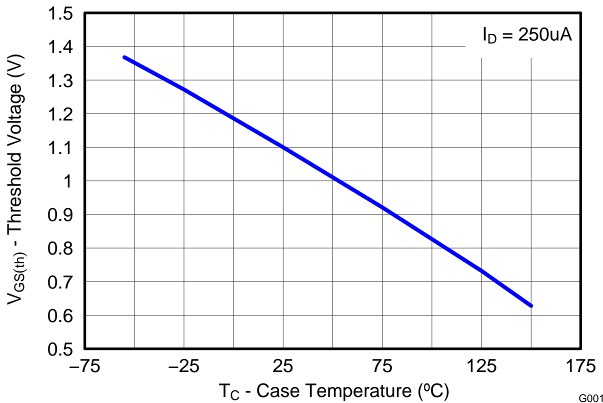

Figure 6. Threshold Voltage vs. Temperature

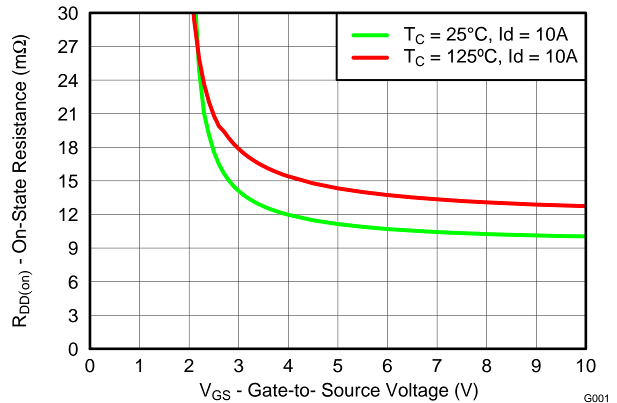

Figure 7. On-State Resistance vs. Gate-to-Source Voltage

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

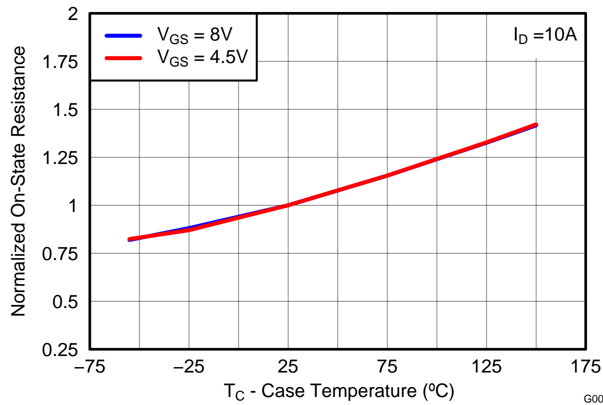

Figure 8. Normalized On-State Resistance vs. Temperature

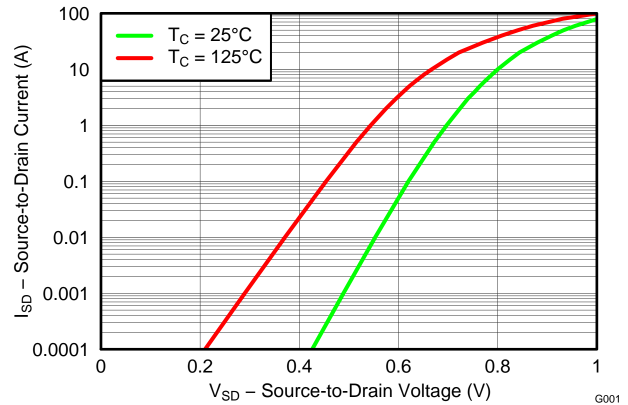

Figure 9. Typical Diode Forward Voltage

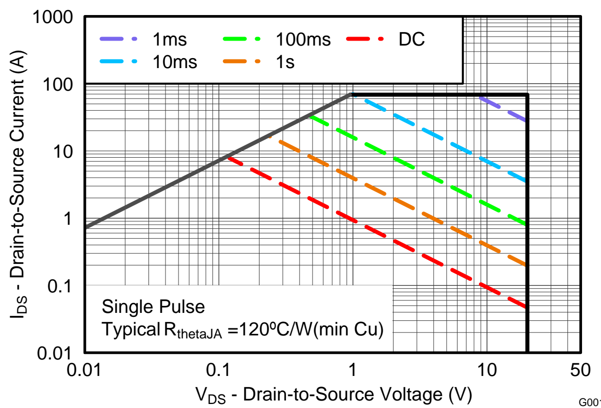

Figure 10. Maximum Safe Operating Area

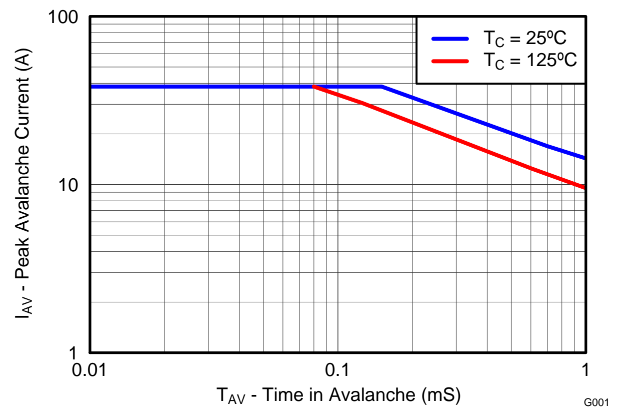

Figure 11. Single Pulse Unclamped Inductive Switching

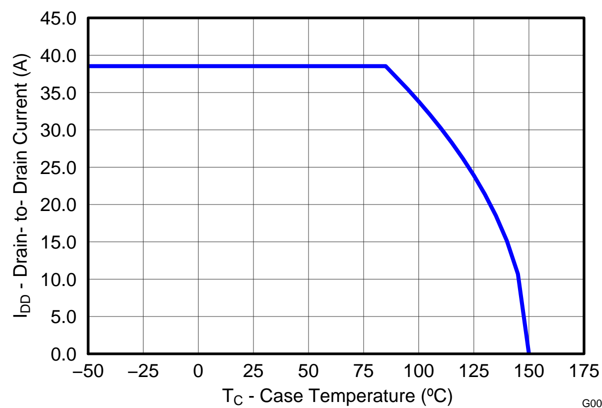

Figure 12. Maximum Drain Current vs. Temperature

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MECHANICAL DATA

CSD85312Q3E Package Dimensions

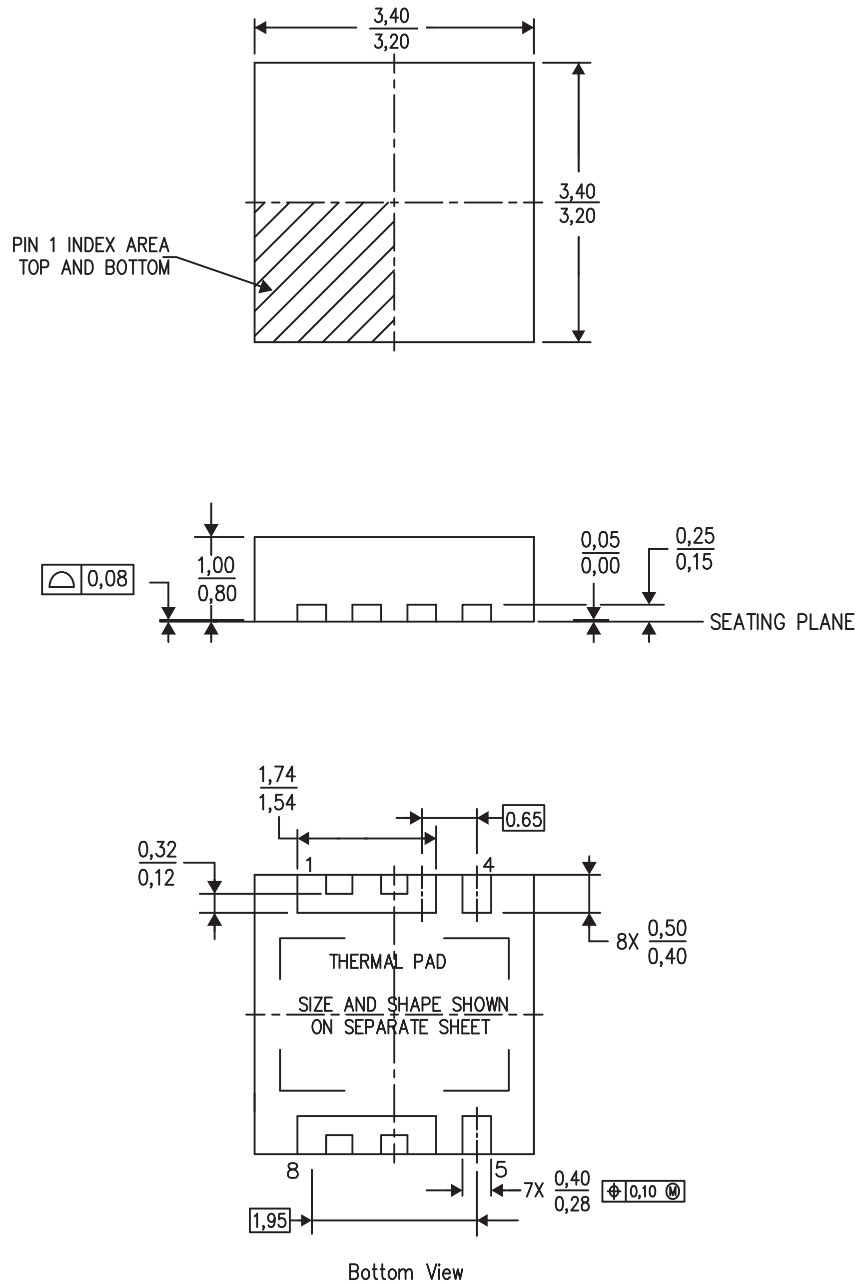

Table 1. Pin Configuration

Position	Designation
Pin 1 – 3	Drain 1
Pin 4	No Connect
Pin 5	Gate
Pin 6 – 8	Drain 2
Pin 9 (Thermal Pad)	Source

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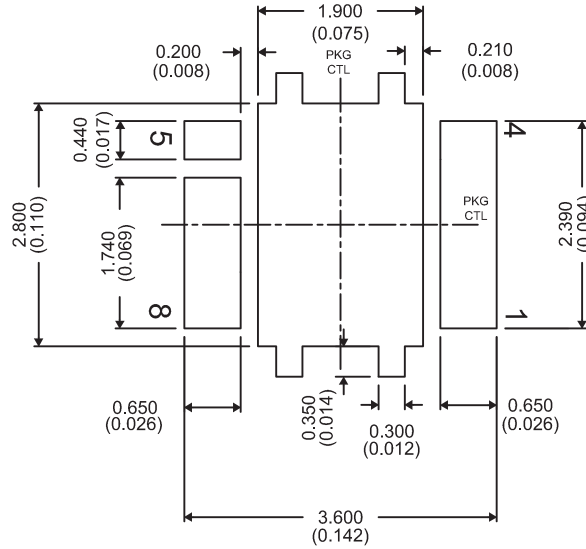
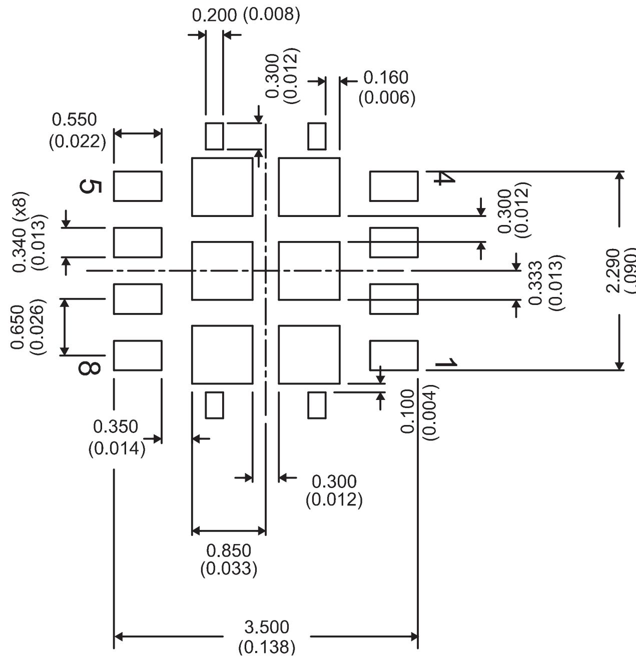
Recommended PCB Pattern



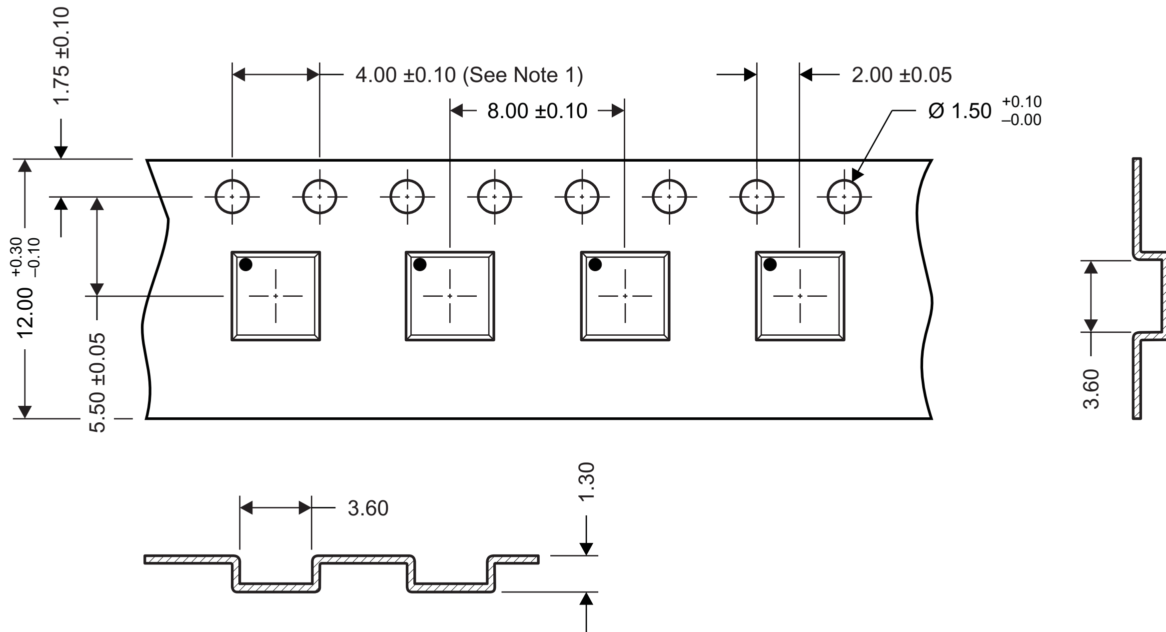
Recommended Stencil Opening



1. All Dimensions are in millimeters (inches)
2. Stencil Opening Thickness 4 mils

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q3E Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
3. Material:black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD85312Q3E	ACTIVE	VSON	DPA	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	85312E	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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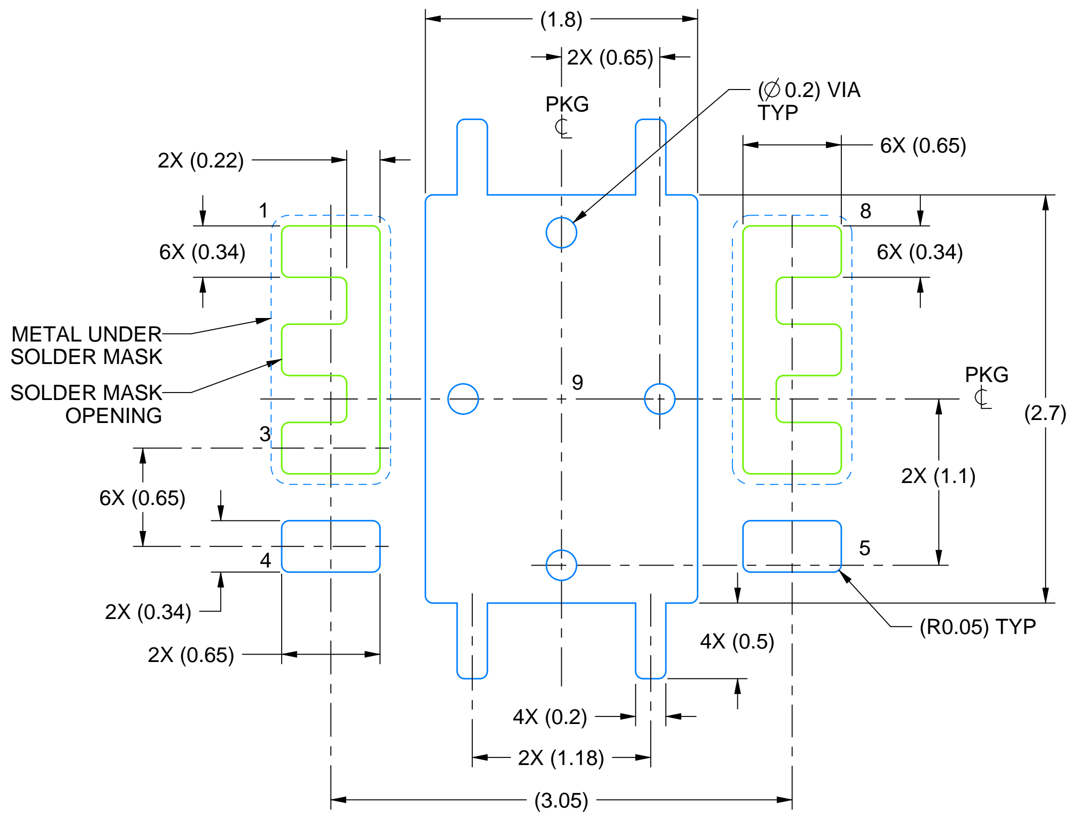
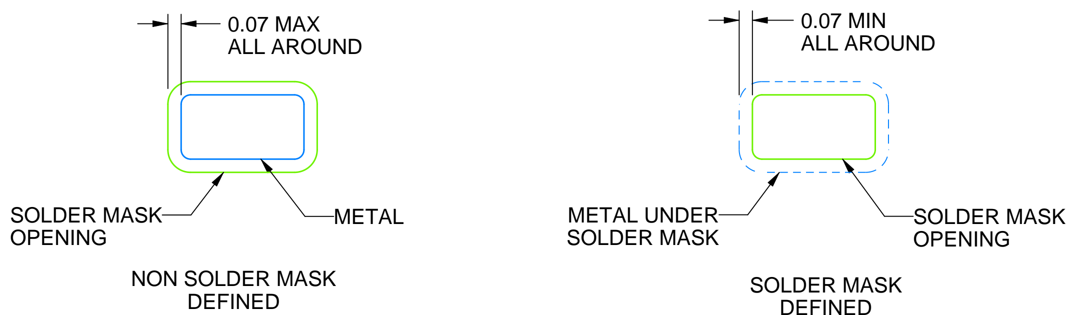
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK DEFINED

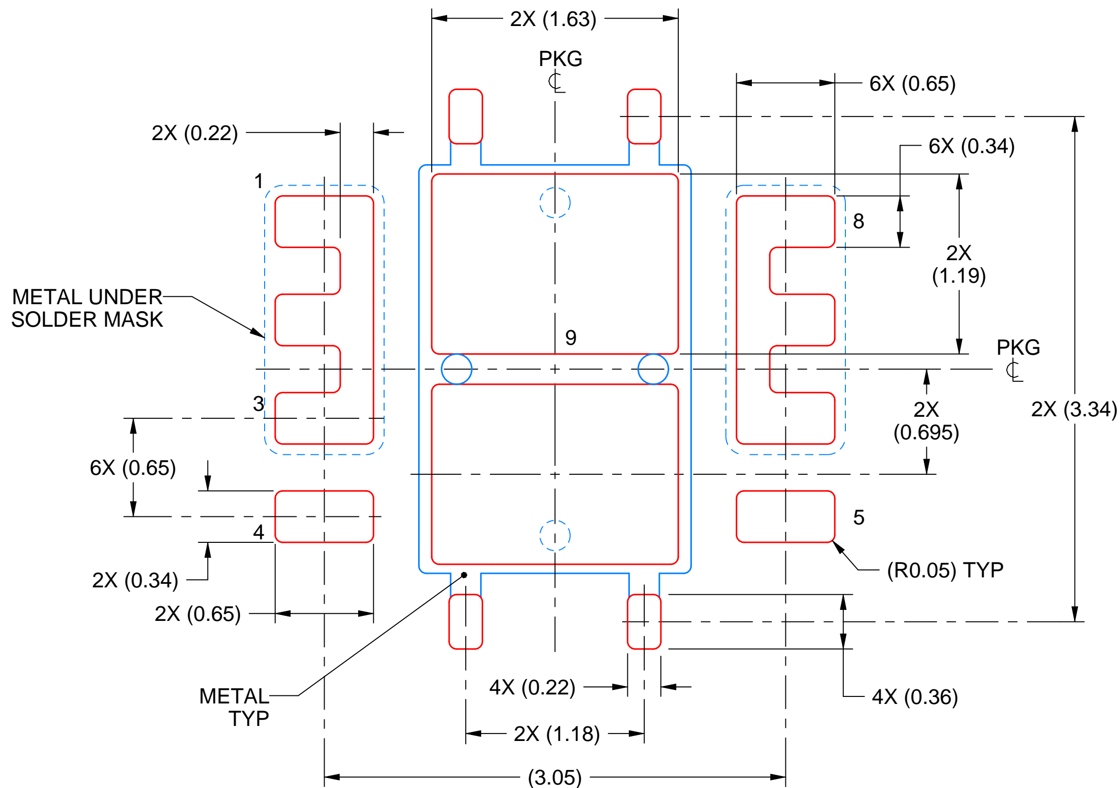
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220449/A 07/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4220449/A 07/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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