CSD87502Q2 30V 双路 N 沟道 NexFET™ 功率 MOSFET

1 特性

- 低导通电阻
- 两个独立的金属氧化物半导体场效应晶体管 (MOSFET)
- 节省空间的小外形尺寸无引线 (SON) 2mm × 2mm 塑料封装
- 针对 5V 栅极驱动器而优化
- 雪崩级
- 无铅且无卤素
- 符合 RoHS 环保标准

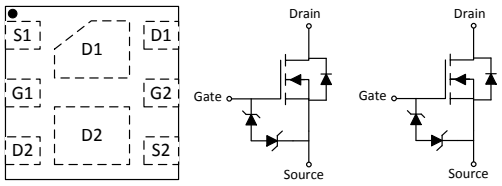
2 应用范围

- 用于网络互联、电信和计算系统的 负载点 同步降压转换器
- 针对笔记本个人电脑 (PC) 和平板电脑的适配器或 USB 输入保护
- 电池保护

3 说明

CSD87502Q2 是一款 30V、27mΩ N 沟道器件。它具有两个独立的 MOSFET，采用 2mm x 2mm SON 塑料封装。这两个场效应管 (FET) 采用半桥配置，适用于同步降压等电源 应用。此外，这些 NexFET™功率 MOSFET 还可用于适配器、USB 输入保护和电池充电应用。两个 FET 的漏源导通电阻均较低，可最大限度地降低损耗并减少元件数，非常适合空间受限型 应用。

顶视图和电路图



产品概要

T_A=25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	2.2		nC
Q_{gd}	栅极电荷 栅极到漏极	0.5		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 3.8V	42.0	mΩ
		V_{GS} = 4.5V	35.5	mΩ
		V_{GS} = 10V	27.0	mΩ
$V_{GS(th)}$	阈值电压	1.6		V

订购信息(1)

器件	包装介质	数量	封装	运输
CSD87502Q2	7 英寸卷带	3000	SON 2mm x 2mm 塑料封装	卷带封装
CSD87502Q2T	7 英寸卷带	250		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

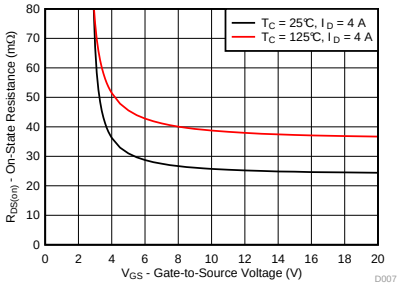
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	5.0	A
I_{DM}	脉冲漏极电流(1)	23	A
P_D	功率耗散(2)	2.3	W
T_J, T_{stg}	工作结温，储存温度	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 7.9A，L = 0.1mH，R_G = 25Ω	3.1	mJ

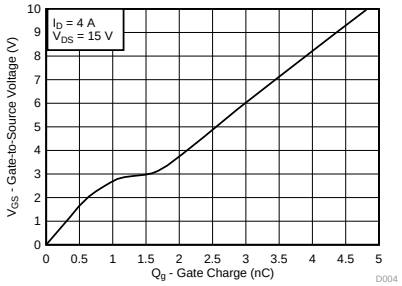
(1) 最大 $R_{\theta JA}$ = 185°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。

(2) $R_{\theta JA}$ = 55°C/W，这是在厚度为 0.06 英寸的环氧板 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2 2 盎司的铜过渡垫片上测得的典型值。

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



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4 修订历史记录

日期	修订版本	注释
2015 年 12 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

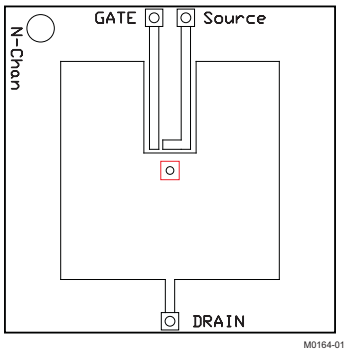
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			4	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.2	1.6	2.0	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 3.8 V, I_D = 4 A		42.0	60.0	mΩ
		V_{GS} = 4.5 V, I_D = 4 A		35.5	42.0	mΩ
		V_{GS} = 10 V, I_D = 4 A		27.0	32.4	mΩ
g_{fs}	Transconductance	V_{DS} = 3 V, I_D = 4 A		75		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		272	353	pF
C_{oss}	Output capacitance			42	55	pF
C_{rss}	Reverse transfer capacitance			22	29	pF
R_G	Series gate resistance			6.9		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_D = 4 A		2.2	2.9	nC
Q_g	Gate charge total (10 V)			4.6	6.0	nC
Q_{gd}	Gate charge gate to drain			0.5		nC
Q_{gs}	Gate charge gate to source			1.0		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.5		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		1.4		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 15 V, V_{GS} = 5 V, I_{DS} = 4 A, R_G = 0 Ω		3		ns
t_r	Rise time			11		ns
$t_{d(off)}$	Turn off delay time			12		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 4 A, V_{GS} = 0 V		0.85	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 15 V, I_F = 4 A, di/dt = 300 A/µs		4.0		nC
t_{rr}	Reverse recovery time			6.4		ns

5.2 Thermal Information

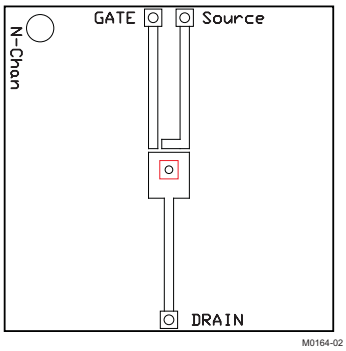
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)			70	°C/W
	Junction-to-ambient thermal resistance(2)			185	

(1) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.



Max $R_{\theta JA}$ = 70 when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 185 when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

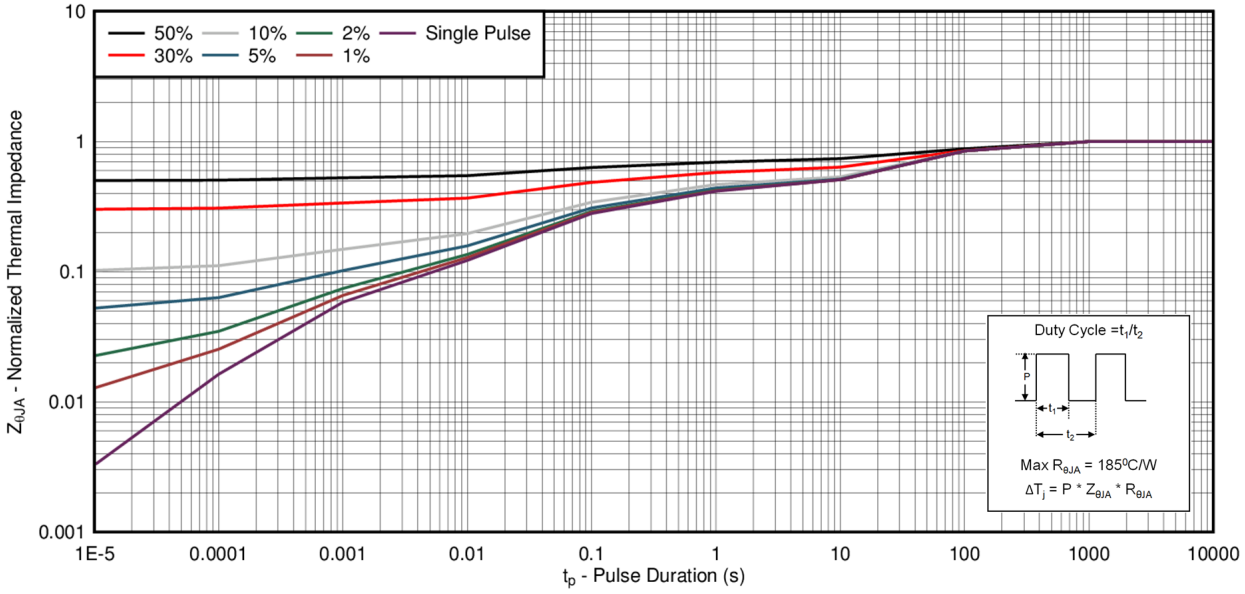


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

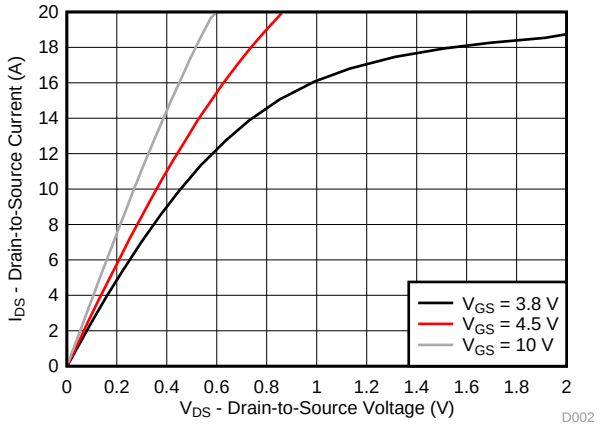


Figure 2. Saturation Characteristics

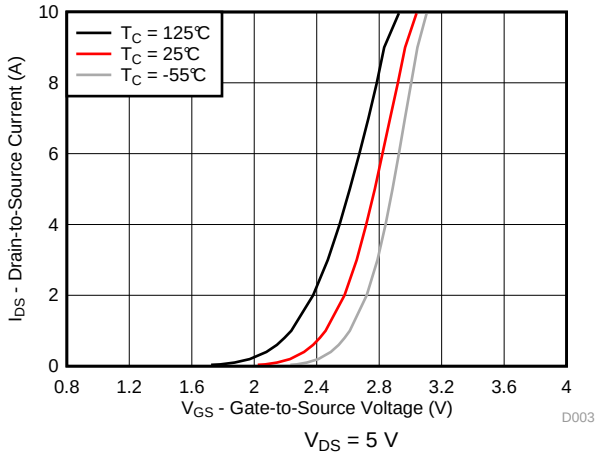


Figure 3. Transfer Characteristics

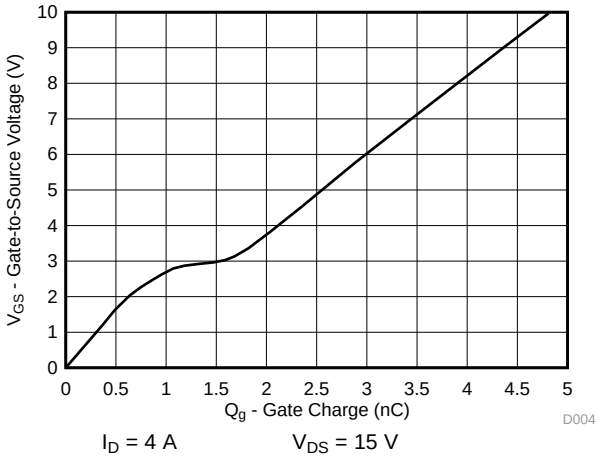


Figure 4. Gate Charge

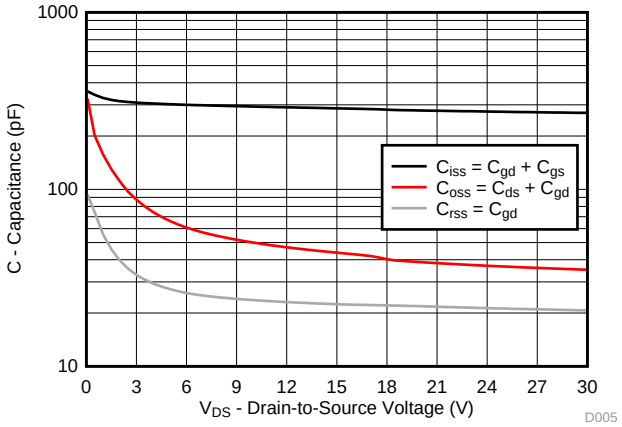


Figure 5. Capacitance

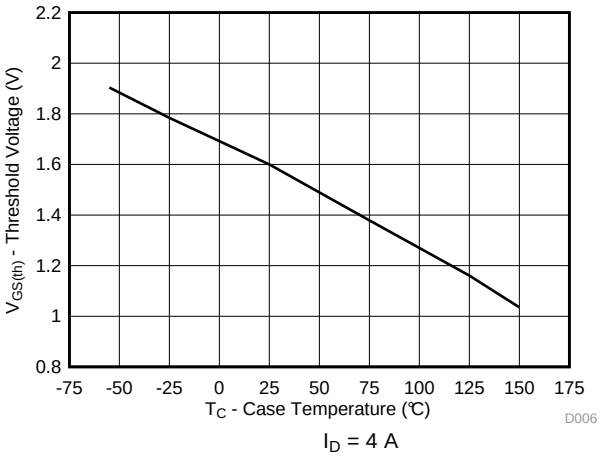


Figure 6. Threshold Voltage vs Temperature

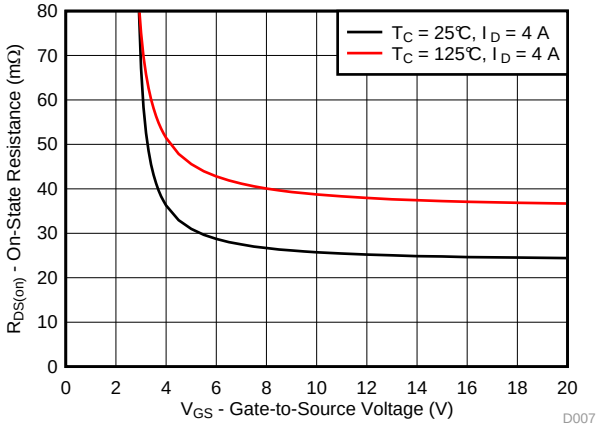


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

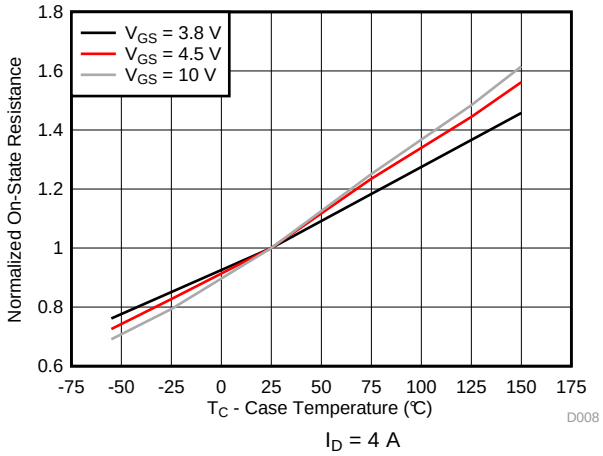


Figure 8. Normalized On-State Resistance vs Temperature

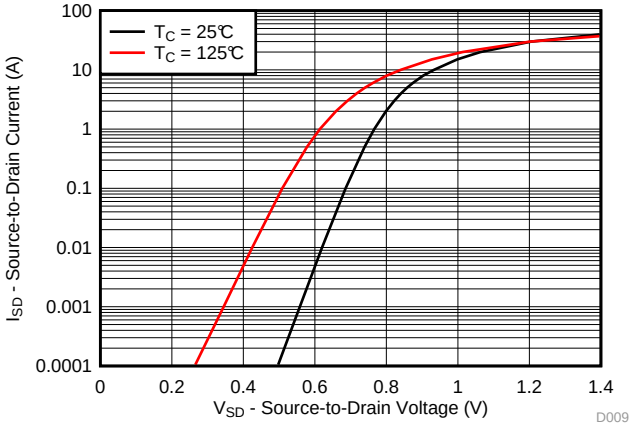


Figure 9. Typical Diode Forward Voltage

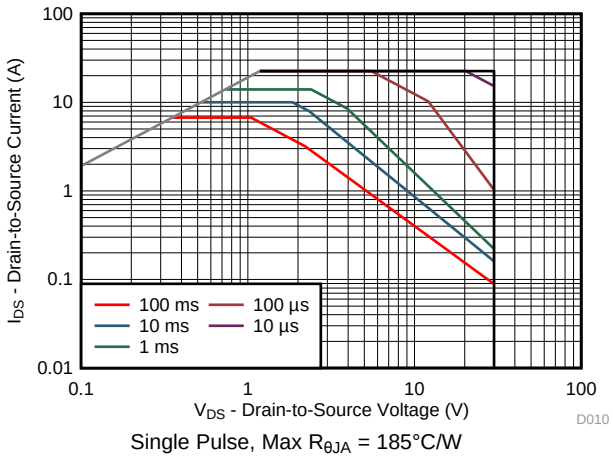


Figure 10. Maximum Safe Operating Area

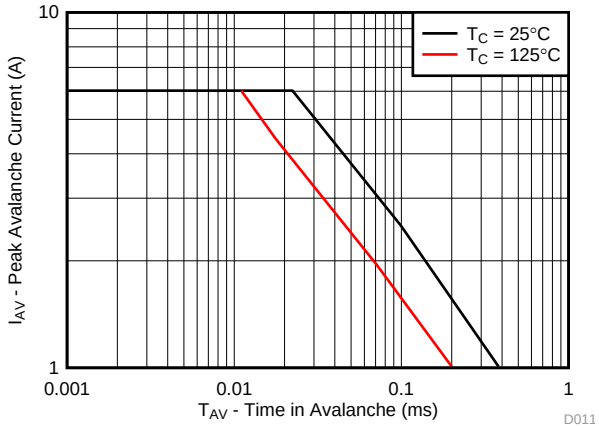


Figure 11. Single Pulse Unclamped Inductive Switching

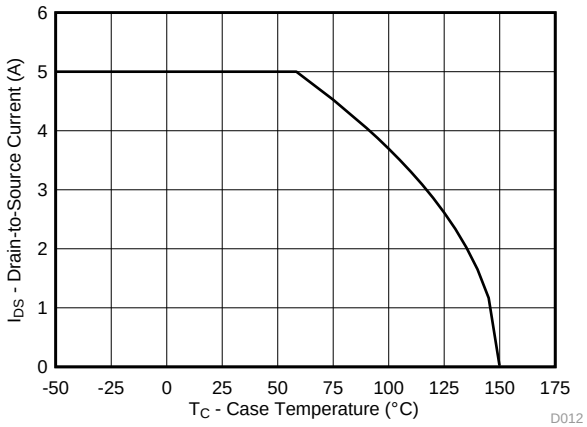


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 商标

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6.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.4 Glossary

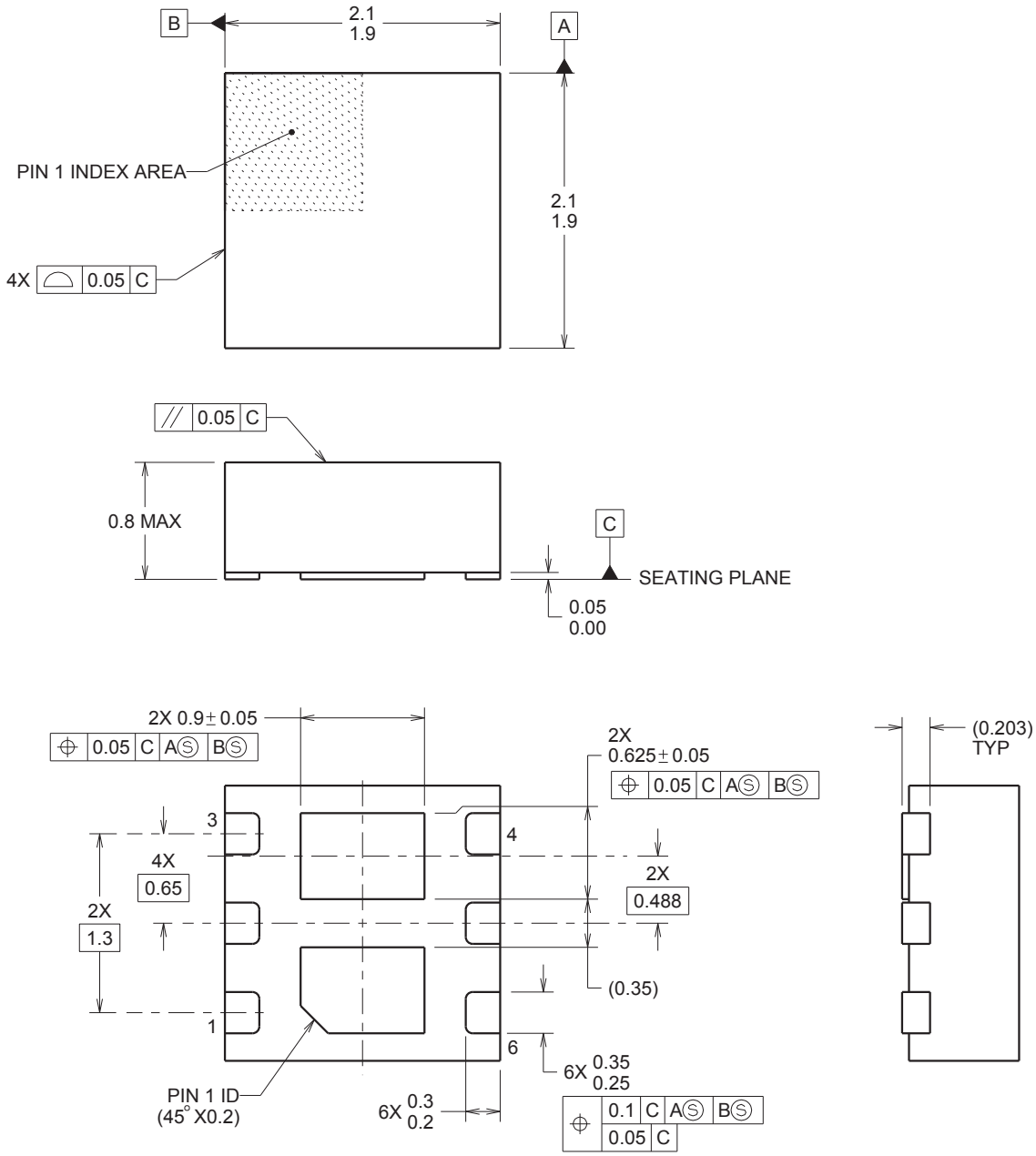
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

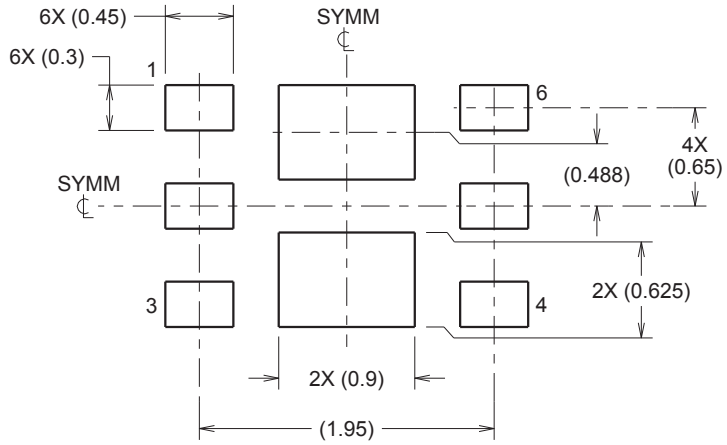
以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 封装尺寸



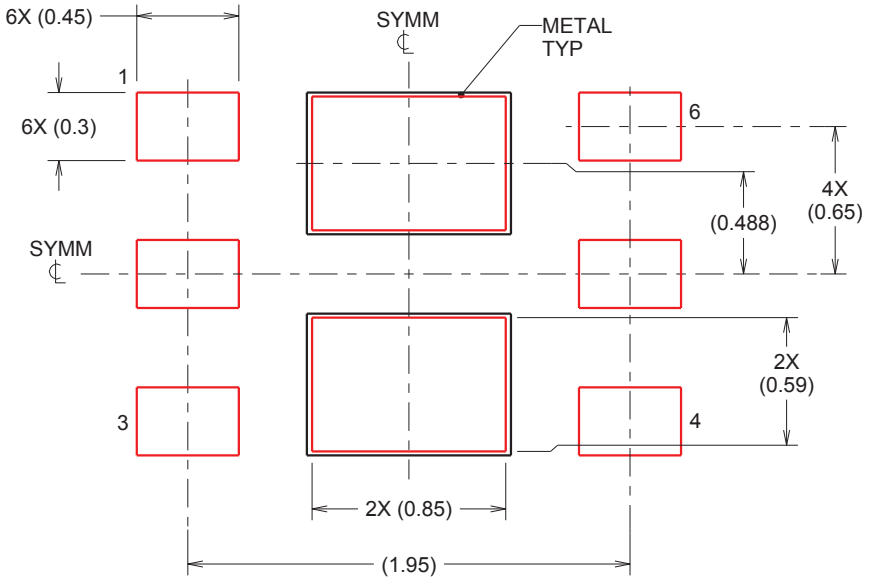
除非另外注明，否则全部尺寸单位均为 mm。

7.2 印刷电路板 (PCB) 焊盘图案



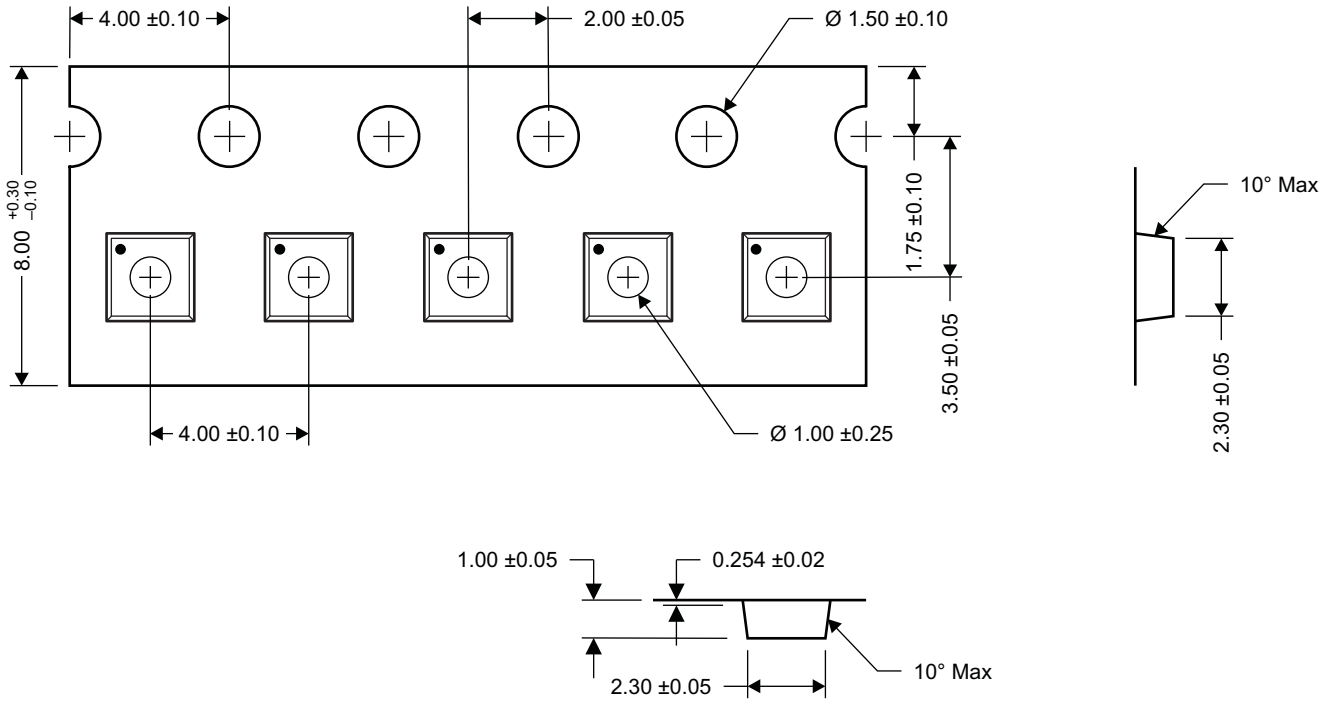
要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》文献编号：SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模板开口



除非另外注明，否则全部尺寸单位均为 mm。

7.4 Q2 卷带信息



Notes: 1. 测自链齿孔中心线到孔眼中心线
2. 10 个链齿孔的累积容差为 ±0.20
3. 其他材料可用
4. 卷带的 SR 典型值最大为 10^9 OHM/SQ
5. 全部尺寸单位为 mm，除非另外注明。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87502Q2	ACTIVE	WSON	DLV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8752	Samples
CSD87502Q2T	ACTIVE	WSON	DLV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8752	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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