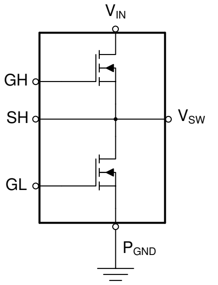
CSD88584Q5DC 40V 半桥 NexFET™ 电源块

1 特性

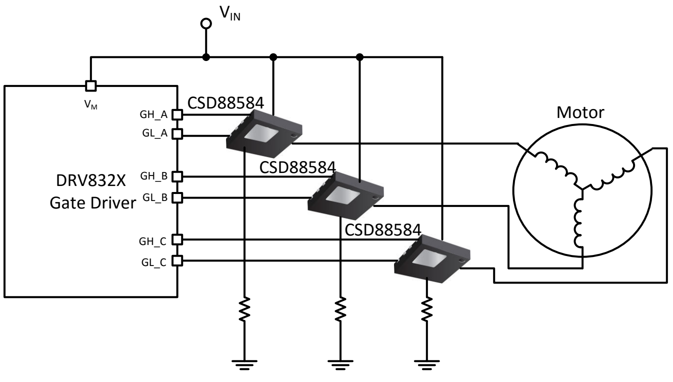
- 半桥电源块
- 高密度 5mm × 6mm SON 封装
- 低 $R_{DS(ON)}$，可更大限度地降低传导损耗
  - 电流为 35A 时，P_{Loss} 为 2.4W
- DualCool™ 散热增强型封装
- 超低电感封装
- 符合 RoHS
- 无卤素
- 无铅端子镀层

2 应用

- 用于无刷直流电机控制的三相桥
- 多达 8s 电池的电动工具
- 其他半桥和全桥拓扑



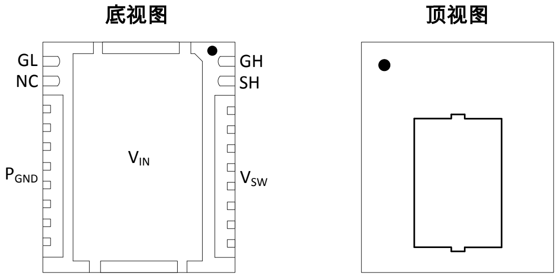
电源块原理图



典型电路

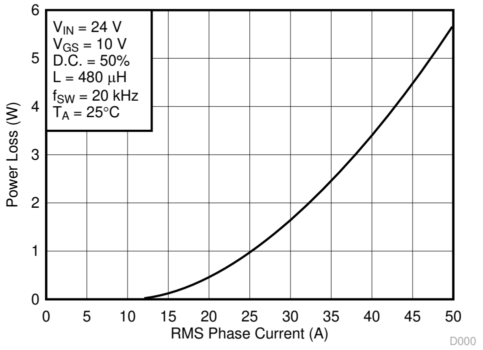
3 说明

CSD88584Q5DC 40V 电源块是一款针对手持设备、无绳园艺工具和电动工具等高电流电机控制应用的优化设计。该器件利用 TI 获得专利的堆叠裸片技术来更大限度地减小寄生电感，同时采用节省空间的散热增强型 DualCool™ 5mm × 6mm 封装，可提供完整半桥。利用外露的金属顶部，该电源块器件允许简单散热应用通过封装顶部散发 PCB 热量，从而在许多电机控制应用所要求的较高电流下，实现出色的热性能。



器件信息

器件	数量	介质	封装	配送
CSD88584Q5DC	2500	13 英寸卷带	SON 5.00mm × 6.00mm 塑料封装	卷带包装
CSD88584Q5DCT	250	7 英寸卷带		



功率损耗与输出电流

English Data Sheet: SLPS598

Table of Contents

4 Revision History

Changes from Revision C (January 2018) to Revision D (December 2018)	**Page**
• Updated current sense resistor description in applications section	17

Changes from Revision * (May 2017) to Revision A (May 2017)	**Page**
• 更新了 *典型电路* 图中的栅极驱动器器件型号	1

Changes from Revision A (May 2017) to Revision B (September 2017)	**Page**
• Updated 图 5-3 to extend to 50 A	6

Changes from Revision B (September 2017) to Revision C (January 2018)	**Page**
• 在 *功率损耗与输出电流* 图 3-1 图中将 V_{DD} = 10V 改为 V_{GS} = 10V	1
• Changed V_{DD} to V_{GS} in sections *Recommended Operating Conditions*, *Block Performance*, & *Typical Power Block Device Characteristics*	3
• Changed I_{DSS} test condition from 20 V to 32 V in the *Electrical Characteristics* table	4

5 Specifications

5.1 Absolute Maximum Ratings(1)

T_J = 25°C (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voltage	V_{IN} to P_{GND}	–0.8	40	V
	V_{SW} to P_{GND}	–0.3	40	
	GH to SH	–20	20	
	GL to P_{GND}	–20	20	
Pulsed current rating, I_{DM} (2)			400	A
Power dissipation, P_D			12	W
Avalanche energy, E_{AS}	High-side FET, I_D = 103 A, L = 0.1 mH		525	mJ
	Low-side FET, I_D = 103 A, L = 0.1 mH		525	
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Single FET conduction, max $R_{\theta JC}$ = 1.1°C/W, pulse duration ≤ 100 µs, single pulse.

5.2 Recommended Operating Conditions

T_J = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{GS}	Gate drive voltage		4.5	16	V
V_{IN}	Input supply voltage(1)			36	V
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)	5	50	kHz
I_{OUT}	RMS motor winding current			50	A
T_J	Operating temperature			125	°C

(1) Up to 32-V input use one capacitor per phase, MLCC 10 nF, 100 V, X7S, 0402, PN: C1005X7S2A103K050BB from V_{IN} to GND return. Between 32-V to 36-V input operation, add RC switch-node snubber as described in the *节 7.1.1* section of this data sheet.

5.3 Power Block Performance

T_J = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power loss(1)	V_{IN} = 24 V, V_{GS} = 10 V, I_{OUT} = 35 A, f_{SW} = 20 kHz, T_J = 25°C, duty cycle = 50%, L = 480 µH		2.4		W
P_{LOSS}	Power loss	V_{IN} = 24 V, V_{GS} = 10 V, I_{OUT} = 35 A, f_{SW} = 20 kHz, T_J = 125°C, duty cycle = 50%, L = 480 µH		3.5		W

(1) Measurement made with eight 10-µF, 50-V, ±10% X5R (TDK C3225X5R1H106K250AB or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using UCC27210DDAR 100-V, 4-A driver IC.

5.4 Thermal Information

T_J = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu)(2)			125	°C/W
	Junction-to-ambient thermal resistance (max Cu)(2) (1)			50	

T_J = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)(2)			2.1	°C/W
	Junction-to-case thermal resistance (V_{IN} pin)(2)			1.1	

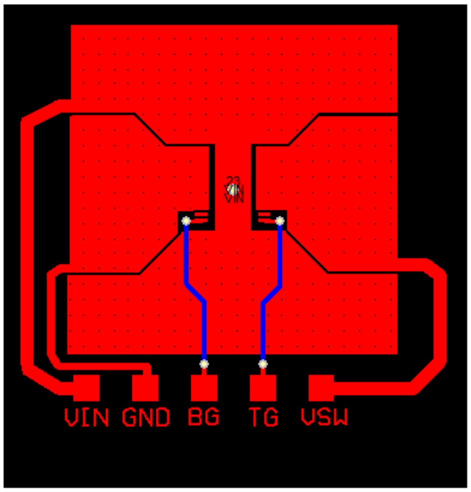
(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2) Cu.

(2) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

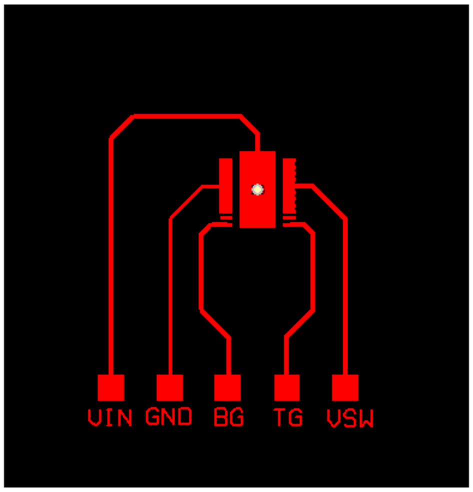
5.5 Electrical Characteristics

T_J = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	40			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 32 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1.2	1.7	2.3	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 4.5 V, I_{DS} = 30 A		1.0	1.5	mΩ
		V_{GS} = 10 V, I_{DS} = 30 A		0.68	0.95	
g_{fs}	Transconductance	V_{DS} = 4 V, I_{DS} = 30 A		149		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 20 V, *ƒ* = 1 MHz		9540	12400	pF
C_{OSS}	Output capacitance			957	1240	pF
C_{RSS}	Reverse transfer capacitance			474	616	pF
R_G	Series gate resistance			1.0	2.0	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 20 V, I_{DS} = 30 A		68	88	nC
Q_g	Gate charge total (10 V)			137	178	nC
Q_{gd}	Gate charge gate-to-drain			26		nC
Q_{gs}	Gate charge gate-to-source			24		nC
$Q_{g(th)}$	Gate charge at V_{th}			16		nC
Q_{OSS}	Output charge	V_{DS} = 20 V, V_{GS} = 0 V		42		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 20 V, V_{GS} = 10 V, I_{DS} = 30 A, R_G = 0 Ω		11		ns
t_r	Rise time			24		ns
$t_{d(off)}$	Turnoff delay time			53		ns
t_f	Fall time			17		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{DS} = 30 A, V_{GS} = 0 V		0.75	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS} = 20 V, I_F = 30 A, di/dt = 300 A/μs		34		nC
t_{rr}	Reverse recovery time			24		ns



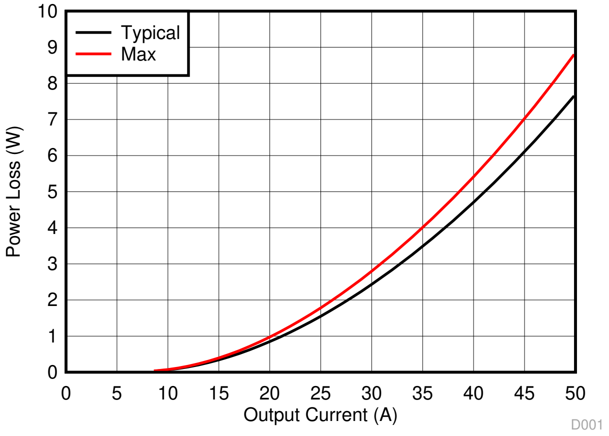
Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.6 Typical Power Block Device Characteristics

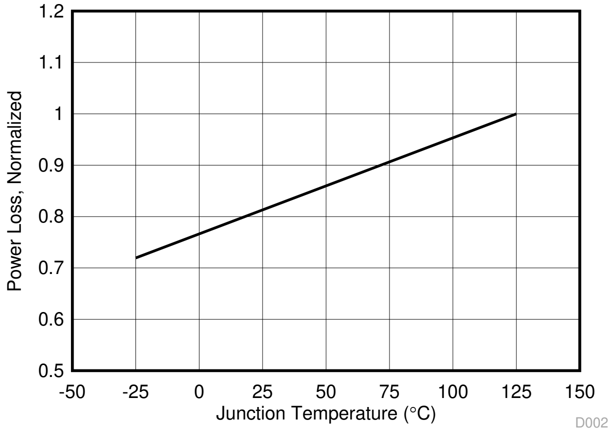
The typical power block system characteristic curves (图 5-1 through 图 5-6) are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 2-oz copper thickness. See 节 6 section for detailed explanation. T_J = 125°C, unless stated otherwise.



V_{IN} = 24 V V_{GS} = 10 V D.C. = 50%

f_{SW} = 20 kHz L = 480 μH

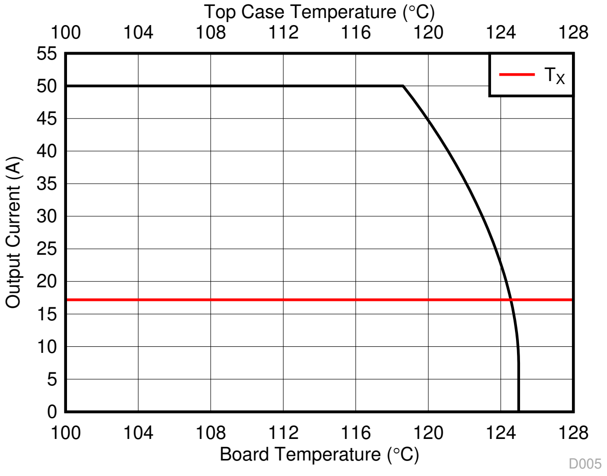
图 5-1. Power Loss vs Output Current



V_{IN} = 24 V V_{GS} = 10 V D.C. = 50%

f_{SW} = 20 kHz I_{OUT} = 50 A L = 480 μH

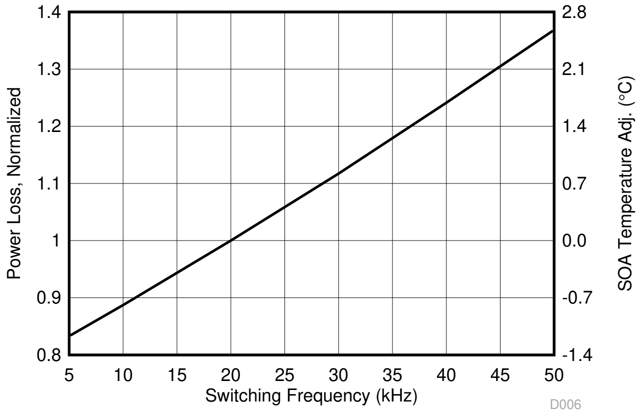
图 5-2. Power Loss vs Temperature



V_{IN} = 24 V V_{GS} = 10 V D.C. = 50%

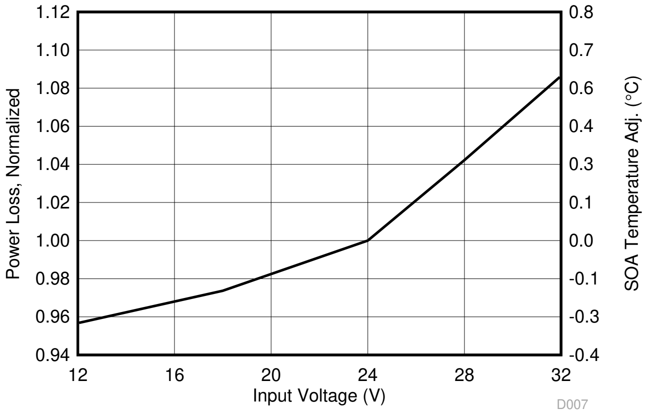
f_{SW} = 20 kHz L = 480 μH

图 5-3. Typical Safe Operating Area



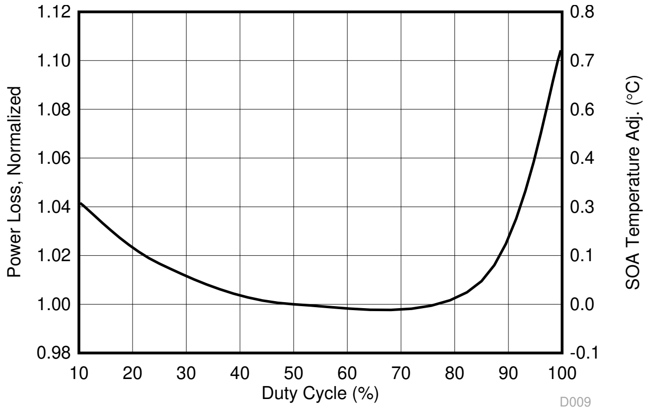
V_{IN} = 24 V V_{GS} = 10 V L = 480 µH
I_{OUT} = 50 A D. C. = 50%

图 5-4. Normalized Power Loss vs Switching Frequency



I_{OUT} = 50 A V_{GS} = 10 V L = 480 µH
f_{SW} = 20 kHz D. C. = 50%

图 5-5. Normalized Power Loss vs Input Voltage

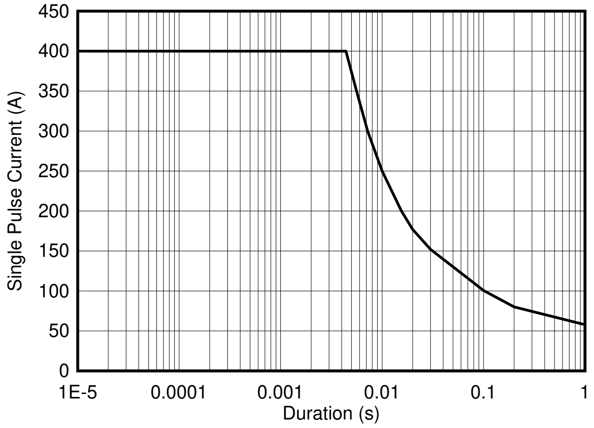


V_{IN} = 24 V V_{GS} = 10 V I_{OUT} = 50 A
f_{SW} = 20 kHz L = 480 µH

图 5-6. Normalized Power Loss vs Duty Cycle

5.7 Typical Power Block MOSFET Characteristics

T_J = 25°C, unless stated otherwise.



Max $R_{\theta JA}$ = 125°C/W

图 5-7. Single Pulse Current vs Pulse Duration

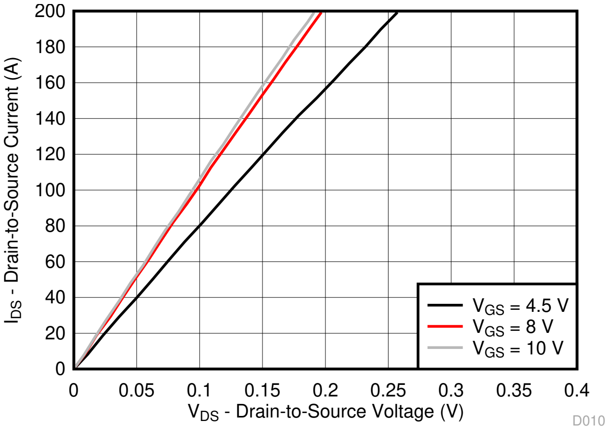
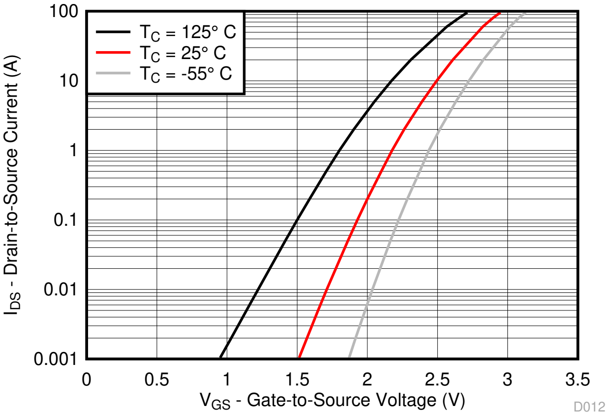
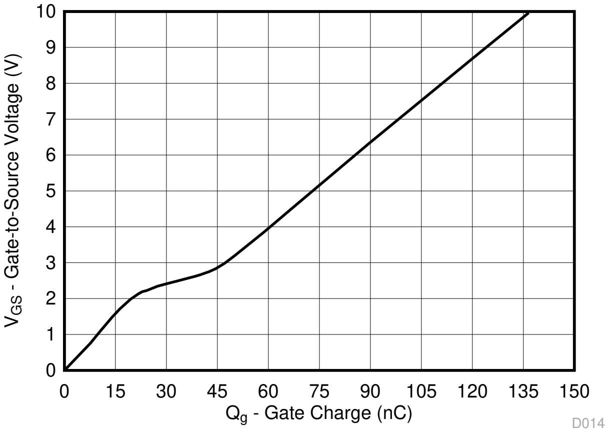


图 5-8. MOSFET Saturation Characteristics



V_{DS} = 5 V

图 5-9. MOSFET Transfer Characteristics



I_D = 30 A V_{DS} = 20 V

图 5-10. MOSFET Gate Charge

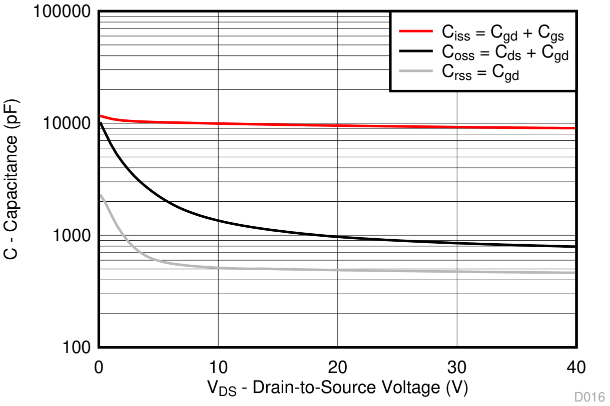
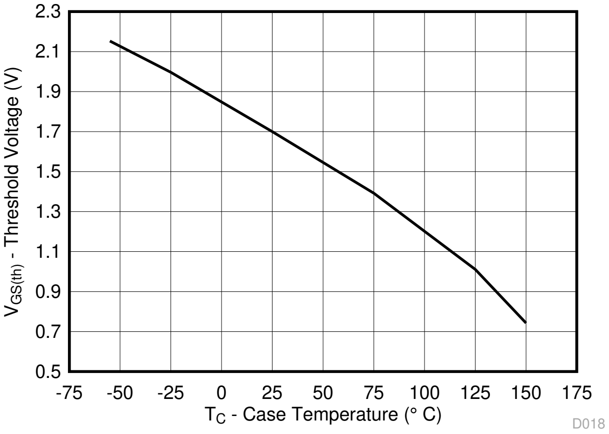


图 5-11. MOSFET Capacitance



I_D = 250 µA

图 5-12. Threshold Voltage vs Temperature

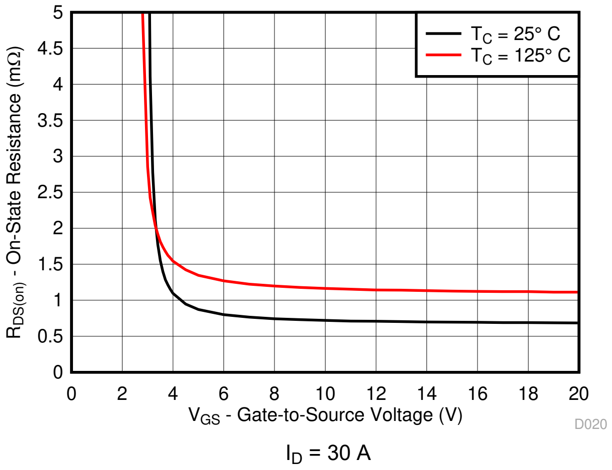


图 5-13. MOSFET $R_{DS(on)}$ vs V_{GS}

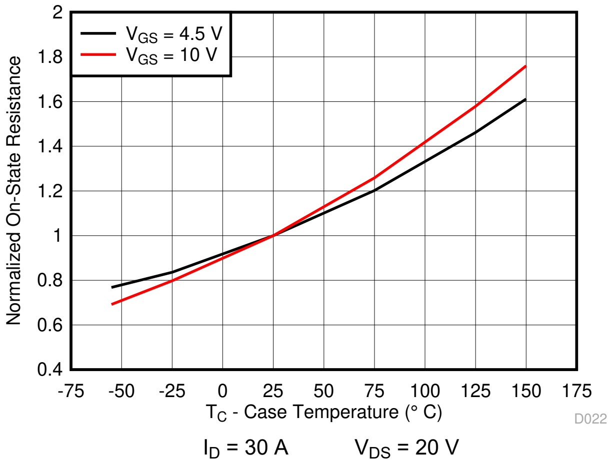


图 5-14. MOSFET Normalized $R_{DS(on)}$ vs Temperature

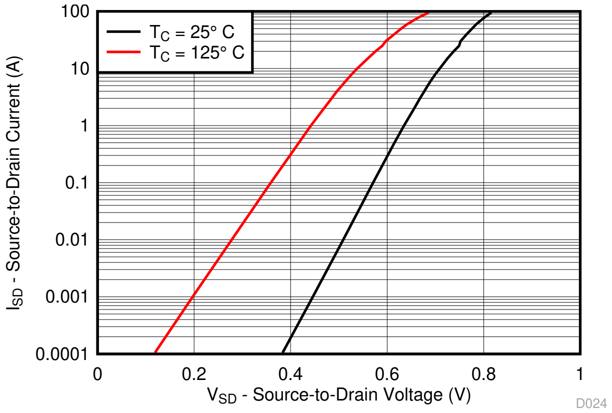


图 5-15. MOSFET Body Diode Forward Voltage

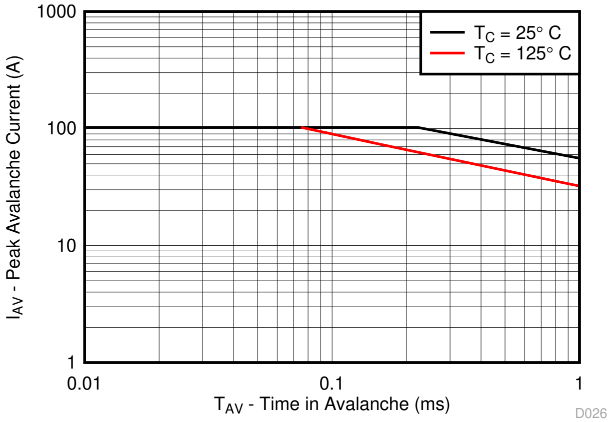


图 5-16. MOSFET Single Pulse Unclamped Inductive Switching

6 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

6.1 Application Information

Historically, battery powered tools have favored brushed DC configurations to spin their primary motors, but more recently, the advantages offered by brushless DC operation (BLDC) operation have brought about the advent of popular designs that favor the latter. Those advantages include, but are not limited to higher efficiency and therefore longer battery life, superior reliability, greater peak torque capability, and smooth operation over a wider range of speeds. However, BLDC designs put increased demand for higher power density and current handling capabilities on the power stage responsible for driving the motor.

The CSD88584Q5DC is part of TI’s power block product family and is a highly optimized product designed explicitly for the purpose driving higher current DC motors in power and gardening tools. It incorporates TI’s latest generation silicon which has been optimized for low resistance to minimize conduction losses and offer excellent thermal performance. The power block utilizes TI’s stacked die technology to offer one complete half bridge vertically integrated into a single 5-mm × 6-mm package with a DualCool exposed metal case. This feature allows the designer to apply a heatsink to the top of the package and pull heat away from the PCB, thus maximizing the power density while reducing the power stage footprint by up to 50%.

6.2 Brushless DC Motor With Trapezoidal Control

The trapezoidal commutation control is simple and has fewer switching losses compared to sinusoidal control.

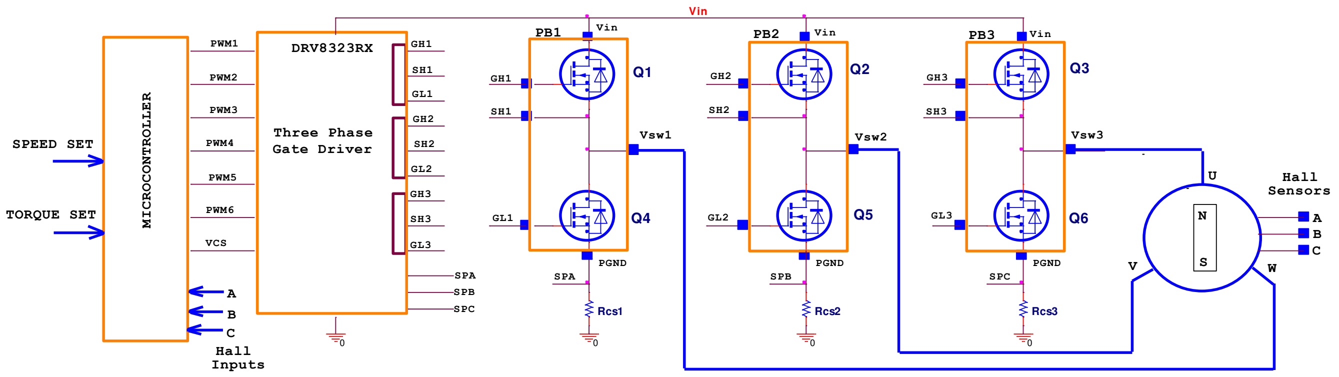


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图 6-1. Functional Block Diagram

The block diagram shown in 图 6-1 offers a simple instruction of what is required to drive a BLDC motor: one microcontroller, one three-phase driver IC, 3 power blocks (historically 6 power MOSFETs) and 3 Hall effect sensors. The microcontroller responsible for block commutation must always know the rotor orientation or its position relative to the stator coils. This is easy achieved with a brushed DC motor due to the fixed geometry and position of the rotor windings, shaft and commutator.

A three-phase BLDC motor requires three Hall effect sensors or a rotary encoder to detect the rotor position in relation to stator armature windings. Combining these three Hall effect sensors output signals, the microcontroller can determine the proper commutation sequence. The three Hall sensors named A, B, and C are mounted on the stator core at 120° intervals and the stator phase windings are implemented in a star configuration. For every 60° of motor rotation, one Hall sensor changes its state. Based on the Hall sensor outputs code, at the end of each block commutation interval the ampere conductors are commutated to the next position. There are 6 steps needed to complete a full electrical cycle. The number of block commutation cycles to complete a full mechanical rotation is determined by the number of rotor pole pairs.

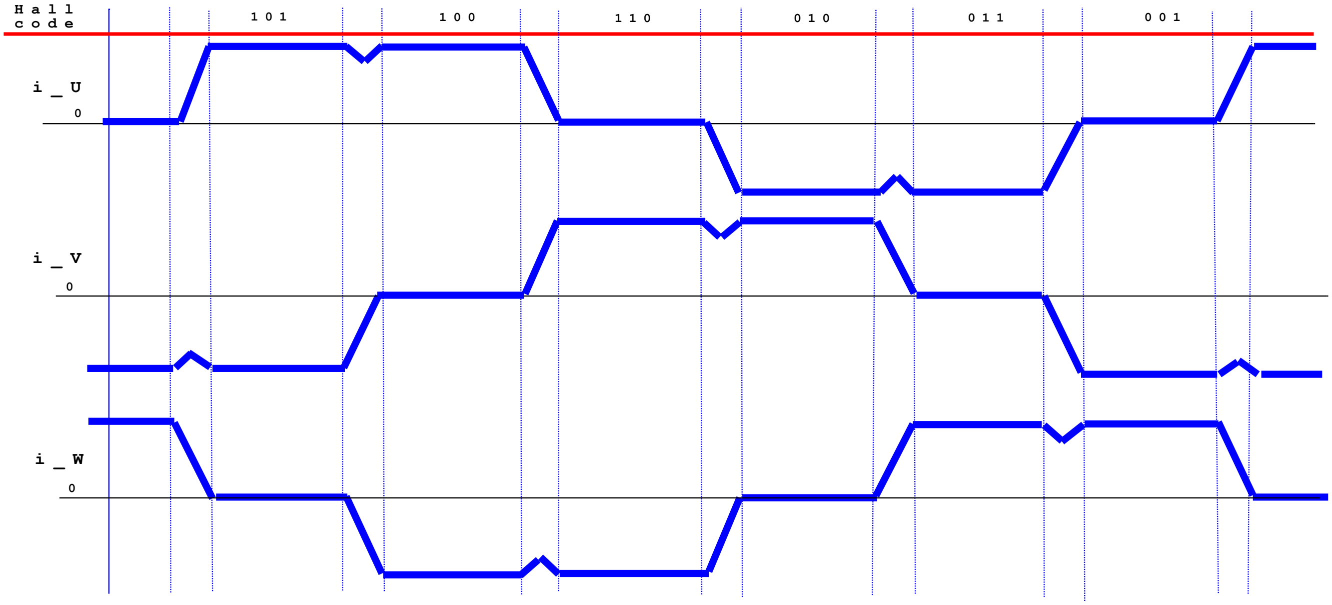

图 6-2. Winding Current Waveforms on a BLDC Motor

图 6-2 above shows the three phase motor winding currents i_U, i_V, and i_W when running at 100% duty cycle.

Trapezoidal commutation control offers the following advantages:

- Only two windings in series carry the phase winding current at any time while the third winding is open.
- Only one current sensor is necessary for all 3 windings U, V, and W.
- The position of the current sensor allows the use of low-cost shunt resistors.

However, trapezoidal commutation control has the disadvantage of commutation torque ripple. The current sense on a three-phase inverter can be configured to use a single-shunt or three different sense resistors. For cost sensitive applications targeting sensorless control, the three Hall effect sensors can be replaced with BEMF voltage feedback dividers.

To obtain faster motor rotations and higher revolutions per minute (RPM), shorter periods and higher V_{IN} voltage are necessary. Contrarily, to reduce the rotational speed of the motor, it is necessary to lower the RMS voltage applied across stator windings. This can easily be easily achieved by modulating the duty cycle, while maintain a constant switching frequency. Frequency for the three-phase inverter chosen is usually low between 10 kHz to 50 kHz to reduce winding losses and to avoid audible noise.

6.3 Power Loss Curves

CSD88584Q5DC was designed to operate up to 7-cell Li-Ion battery voltage applications ranging from 18 V to 32 V, typical 24 V. For 8s, input voltages between 32 V to 36 V, RC snubbers are required for each switch-node U, V, and W. To reduce ringing, refer to the *节 7.1.1* section. In an effort to simplify the design process, Texas Instruments has provided measured power loss performance curves over a variety of typical conditions.

图 5-1 plots the CSD88584Q5DC power loss as a function of load current. The measured power loss includes both input conversion loss and gate drive loss.

方程式 1 is used to generate the power loss curve:

$$\text{Power loss (W)} = (V_{IN} \times I_{IN\_SHUNT}) + (V_{DD} \times I_{DD\_SHUNT}) - (V_{SW\_AVG} \times I_{OUT}) \tag{1}$$

The power loss measurements were made on the circuit shown in 图 6-3, power block devices for legs U and V, PB1 and PB2 were disabled by shorting the CSD88584Q5DC high-side and low-side FETs gate-to-source terminals. Current shunt Iin_shunt provides Input current and Idd_SHUNT provides driver supply current measurements. The winding current is measured from the DC load. An averaging circuit provides switch node W equivalent RMS voltage.

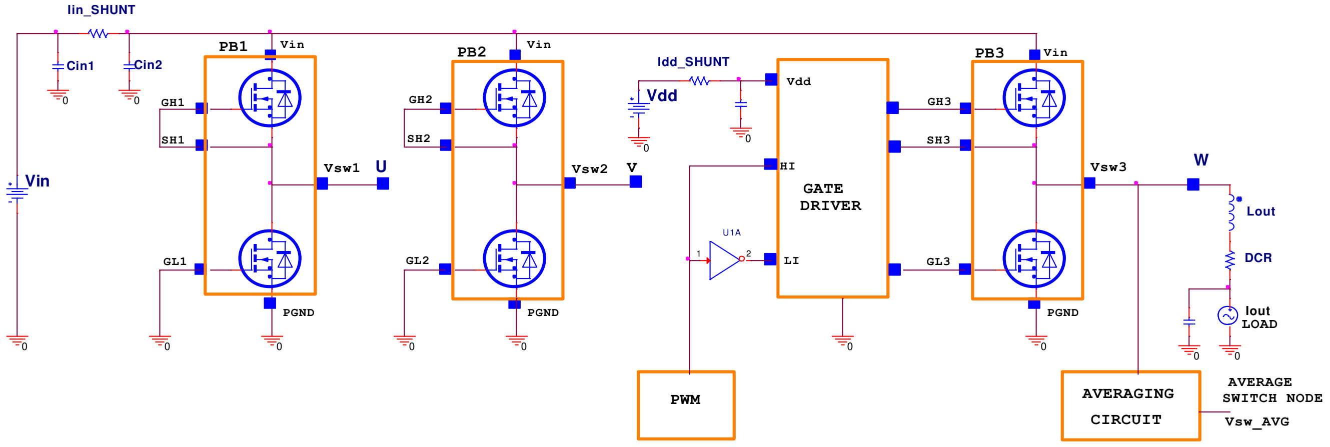

图 6-3. Power Loss Test Circuit

The RMS current on the CSD88584Q5DC device depends on the motor winding current. For trapezoidal control, the MOSFET RMS current is calculated using 方程式 2.

$$I_{RMS} = I_{OUT} \times \sqrt{2} \tag{2}$$

Taking into consideration system tolerances with the current measurement scheme, the inverter design needs to withstand a 20% overload current.

表 6-1. RMS and Overload Current Calculations

Winding RMS Current (A)	CSD88584Q5DC I_{RMS} (A)	Overload 120% × I_{RMS} (A)
30	42	51
40	56	68
50	70	85

6.4 Safe Operating Area (SOA) Curve

The SOA curve in 图 5-3 provide guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. This curve outlines the board and case temperatures required for a given load current. The area under the curve dictates the safe operating area. This curve is based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 2-oz copper thickness.

6.5 Normalized Power Loss Curves

The normalized curves in the CSD88584Q5DC data sheet provide guidance on the power loss and SOA adjustments based on application specific needs. These curves show how the power loss and SOA temperature boundaries will adjust for different operation conditions. The primary Y-axis is the normalized change in power loss while the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the typical power loss. The change in SOA temperature is subtracted from the SOA curve.

6.6 Design Example – Regulate Current to Maintain Safe Operation

If the case and board temperature of the power block are known, the SOA can be used to determine the maximum allowed current that will maintain operation within the safe operating area of the device. The following procedure outlines how to determine the RMS current limit while maintaining operation within the confines of the SOA, assuming the temperatures of the top of the package and PCB directly underneath the part are known.

1. Start at the maximum current of the device on the Y-axis and draw a line from this point at the known top case temperature to the known PCB temperature.
2. Observe where this point intersects the T_X line.
3. At this intersection with the T_X line, draw vertical line until you hit the SOA current limit. This intercept is the maximum allowed current at the corresponding power block PCB and case temperatures.

In the example below, we show how to achieve this for the temperatures T_C = 124°C and T_B = 120°C. First we draw from 50 A on the Y-axis at 124°C to 120°C on the X-axis. Then, we draw a line up from where this line crosses the T_X line to see that this line intercepts the SOA at 39 A. Thus we can assume if we are measuring a PCB temperature of 124°C, and a top case temperature of 120°C, the power block can handle 39-A RMS, at the normalized conditions. At conditions that differ from those in 图 5-1, the user may be required to make an SOA temperature adjustment on the T_X line, as shown in the next section.

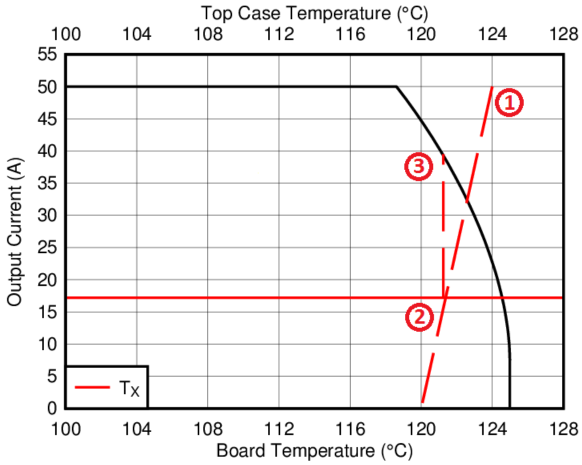

图 6-4. Regulating Current to Maintain Safe Operation

6.7 Design Example – Regulate Board and Case Temperature to Maintain Safe Operation

In the previous example we showed how given the PCB and case temperature, the current of the power block could be limited to ensure operation within the SOA. Conversely, if the current and other application conditions are known, one can determine from the SOA what board or case temperature the user will need to limit their design to. The user can estimate product loss and SOA boundaries by arithmetic means (see *节 6.7.1* section). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

6.7.1 Operating Conditions

- Winding output current (I_{OUT}) = 40 A
- Input voltage (V_{IN}) = 32 V
- Switching frequency (F_{SW}) = 40 kHz
- Duty cycle (D.C.) = 95%

6.7.2 Calculating Power Loss

- Power loss at 40 A ≈ 4.7 W (图 5-1)
- Normalized power loss for switching frequency ≈ 1.24 (图 5-4)
- Normalized power loss for input voltage ≈ 1.09 (图 5-5)
- Normalized power loss for duty cycle ≈ 1.06 (图 5-6)
- **Final calculated power loss = 4.7 W × 1.24 × 1.09 × 1.06 ≈ 6.7 W**

6.7.3 Calculating SOA Adjustments

- SOA adjustment for switching frequency ≈ 1.7°C (图 5-4)
- SOA adjustment for input voltage ≈ 0.6°C (图 5-5)
- SOA adjustment for duty cycle ≈ 0.4°C (图 5-6)
- **Final calculated SOA adjustment = 1.7 + 0.6 + 0.4 ≈ 2.7°C**

In the *节 6.6* section above, the estimated power loss of the CSD88584Q5DC would increase to 6.7 W. In addition, the maximum allowable board temperature would have to increase by 2.7°C. In 图 6-5, the SOA graph was adjusted accordingly.

1. Start by drawing a horizontal line from the application current (40 A) to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the T_X line.
3. Adjust the intersection point by subtracting the temperature adjustment value.

In this design example, the SOA board/ambient temperature adjustment yields a decrease of allowed junction temperature of 2.7°C from 121.0°C to 118.3°C. Now it is known that the intersection of the case and PCB temperatures on the T_X line must stay below this point. For instance, if the power block case is observed operating at 124°C, the PCB temperature must in turn be kept under 115°C to maintain this crossover point.

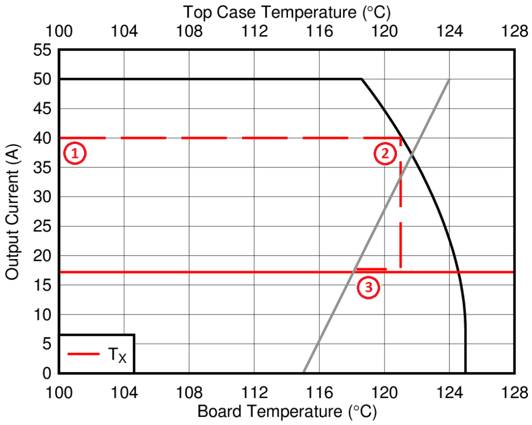

图 6-5. Regulate Temperature to Maintain Safe Operation

7 Layout

The two key system-level parameters that can be optimized with proper PCB design are electrical and thermal performance. A proper PCB layout will yield maximum performance in both areas. Below are some tips for how to address each.

7.1 Layout Guidelines

7.1.1 Electrical Performance

The CSD88584Q5DC power block has the ability to switch at voltage rates greater than 1 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors; high-current, high dI/dT switching path; current shunt resistors; and GND return planes. As with any high-power inverter operated in hard switching mode, there will be voltage ringing present on the switch nodes U, V, and W. Switch-node ringing appears mainly at the HS FET turnon commutation with positive winding current direction. The U, V, and W phase connections to the BLDC motor can be usually excluded from the ringing behavior since they are subjected to high-peak currents but low dI/dT slew-rates. However, a compact PCB design with short and low-parasitic loop inductances is critical to achieve low ringing and compliance with EMI specifications.

For safe and reliable operation of the three-phase inverter, motor phase currents have to be accurately monitored and reported to the system microcontroller. One current sensor needs to be connected on each motor phase winding U, V, and W. This sensing method is best for current sensing as it provides good accuracy over a wide range of duty cycles, motor torque, and winding currents. Using current sensors is recommended because it is less intrusive to the V_{IN} and GND connections.

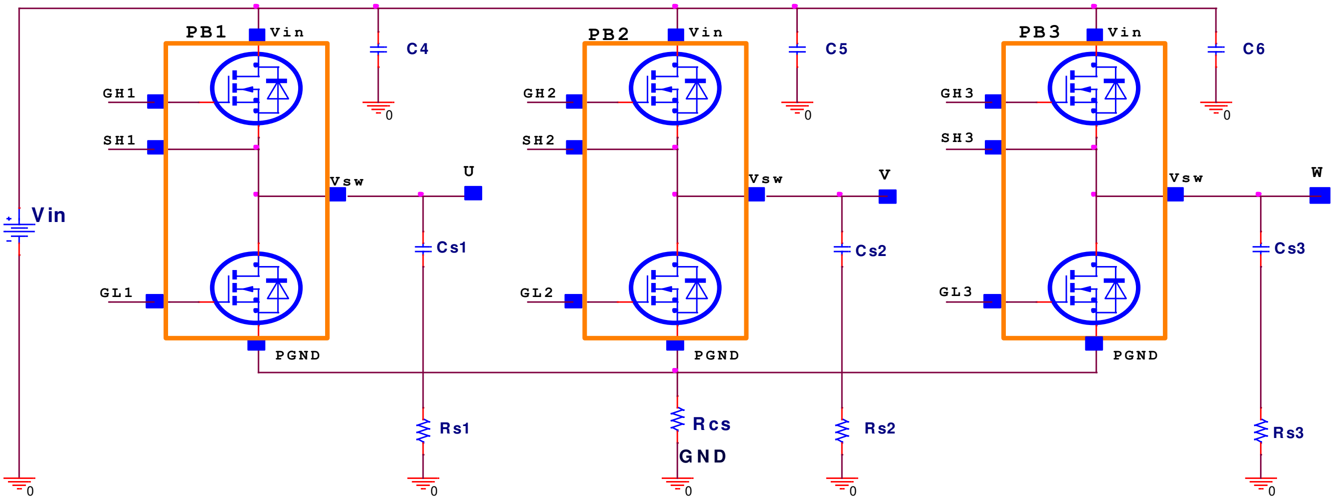

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图 7-1. Recommended Ringing Reduction Components

However, for cost sensitive applications, current sensors are generally replaced with current sense resistors.

- For designs using the 60-V three-phase smart gate driver DRV8320SRHBR, current sense resistor R_{CS} can be placed between common source terminals for all 3 power block devices CSD88584Q5DC to P_{GND} and measured using an external current sense amplifier as depicted in 图 7-1 above.
- For designs using the 60-V three-phase gate driver DRV8323RSRGZT, three current sense resistors R_{CS1}, R_{CS2} and R_{CS3} can be used between each CSD88584Q5DC source terminal to GND and measured by the included DRV8323 current sense amplifiers. The three-phase driver IC should be placed as close as possible to the power block gate GL and GH terminals.

Breaking the high-current flow path from the source terminals of the power block to GND by introducing the R_{CS} current shunt resistors introduces parasitic PCB inductance. In the event the switch node waveforms exhibits peak ringing that reaches undesirable levels, the ringing can be reduced by using the following ringing reduction components:

- The use of a high-side gate resistor in series with the GH pin is one effective way to reduce peak ringing. The recommended HS FET gate resistor value will range between 4.7 Ω to 10 Ω depending on the driver IC output characteristics used in conjunction with the power block device. The low-side FET gate pin GL should connect directly to the driver IC output to avoid any parasitic cdV/dT turnon effect.
- Low inductance MLCC caps C4, C5, and C6 can be used across each power block device from V_{IN} to the source terminal P_{GND}. MLCC 10 nF, 100 V, ±10%, X7S, 0402, PN: C1005X7S2A103K050BB are recommended.
- Ringing can be reduced via the implementation of RC snubbers from each switch node U, V, and W to GND. Recommended snubber component values are as follows:
  - Snubber resistors Rs1, Rs2, Rs3: 2.21 Ω, 1%, 0.125 W, 0805, PN: CRCW08052R21FKEA
  - Snubber caps Cs1, Cs2, and Cs3: MLCC 4.7 nF, 100 V, X7S, 0402, PN: C1005X7S2A472M050BB

With a switching frequency of 20 kHz on the three-phase inverter, the power dissipation on the RC snubber resistor is 80 mW per channel. As a result, 0805 package size for resistors Rs1, Rs2, and Rs3 is adequate.

7.1.2 Thermal Considerations

The CSD88584Q5DC power block device has the ability to utilize the PCB copper planes as the primary thermal path. As such, the use of thermal vias included in the footprint is an effective way to pull away heat from the device and into the system board. Concerns regarding solder voids and manufacturability issues can be addressed through the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from one another to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed by the design. The example in 图 7-2 uses vias with a 10-mil drill hole and a 16-mil solder pad.
- Tent the opposite side of the via with solder-mask. Ultimately the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

To take advantage of the DualCool thermally enhanced package, an external heatsink can be applied on top of the power block devices. For low EMI, the heatsink is usually connected to GND through the mounting screws to the PCB. Gap pad insulators with good thermal conductivity should be used between the top of the package and the heatsink. The Bergquist Sil-Pad 980 is recommended which provides excellent thermal impedance of 1.07°C/W at 50 psi.

7.2 Layout Example

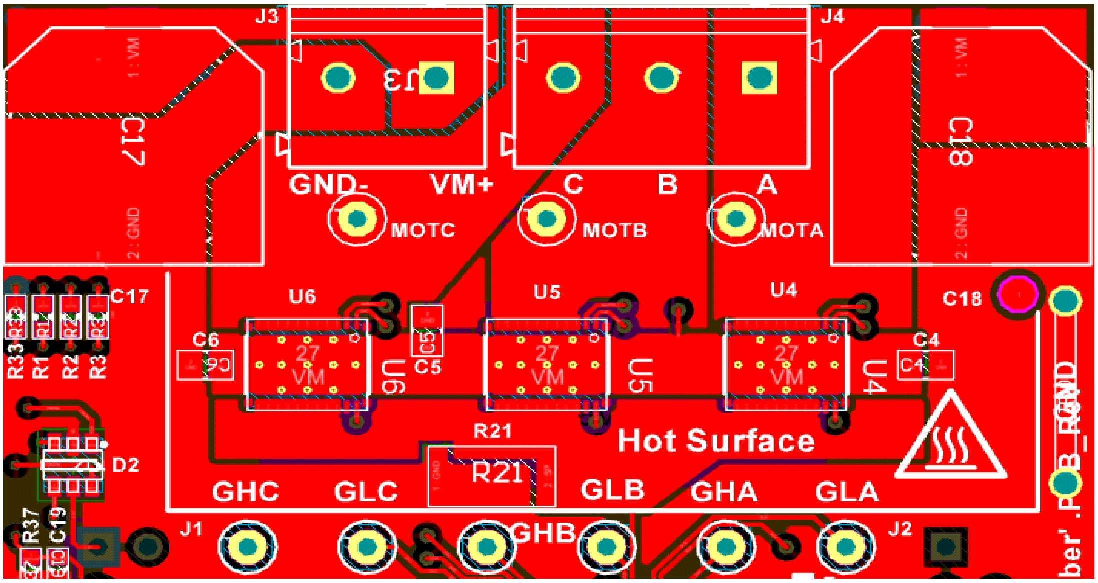

图 7-2. Top Layer

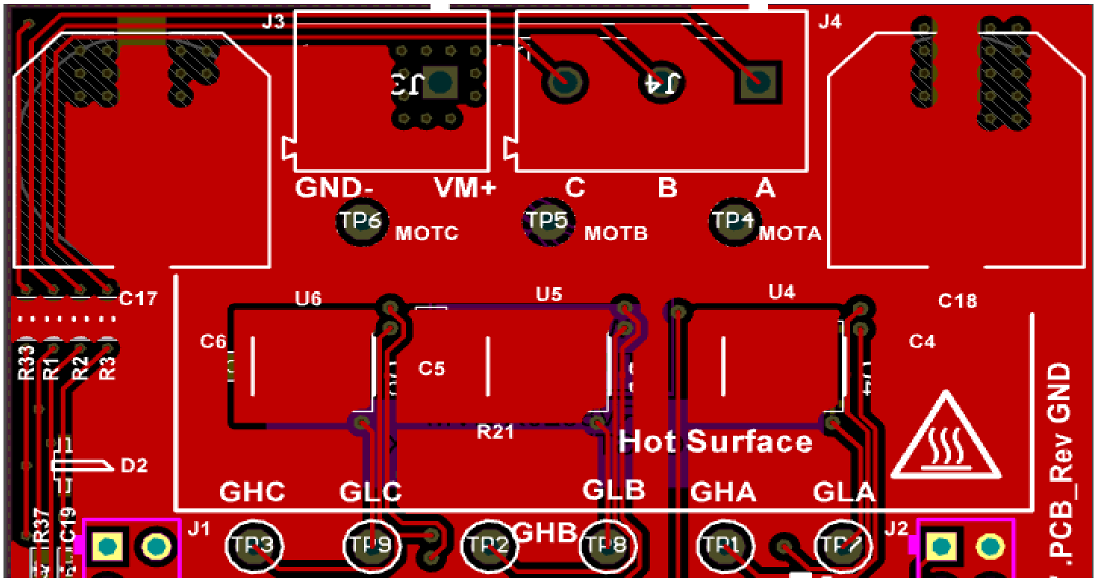

图 7-3. Bottom Layer

The placement of the input capacitors C4, C5, and C6 relative to V_{IN} and P_{GND} pins of CSD88584Q5DC device should have the highest priority during the component placement routine. It is critical to minimize the V_{IN} to GND parasitic loop inductance. A shunt resistor R21 is used between all three U4, U5, and U6 power block source terminals to the input supply GND return pin.

Input RMS current filtering is achieved via two bulk caps C17 and C18. Based on the RMS current ratings, the recommended part number for input bulk is CAP AL, 330 µF, 63 V, ±20%, PN: EMVA630ADA331MKG5S.

8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

表 9-1. Pin Configuration Table

POSITION	PIN NAME	DESCRIPTION
1	GH	High Side Gate
2	SH	High Side Gate Return
3-11	V_{SW}	Switch Node
12-20	P_{GND}	Power Ground
21	NC	No Connect
22	GL	Low Side Gate
23-26	NC	No Connect
27	V_{IN}	Input Voltage

重要声明和免责声明

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88584Q5DC	ACTIVE	VSON-CLIP	DMM	22	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	88584	Samples
CSD88584Q5DCT	ACTIVE	VSON-CLIP	DMM	22	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	88584	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
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OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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