

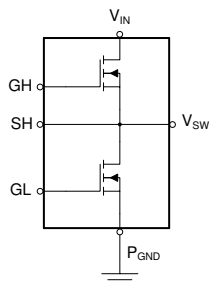
## CSD88584Q5DC 40V 半桥 NexFET™ 电源块

### 1 特性

- 半桥电源块
- 高密度 SON 5mm × 6mm 封装
- 低  $R_{DS(ON)}$ ，可更大限度地降低传导损耗
  - 在 35A 下， $P_{Loss}$  为 2.4W
- DualCool™ 散热增强型封装
- 超低电感封装
- 符合 RoHS
- 无卤素
- 无铅端子镀层

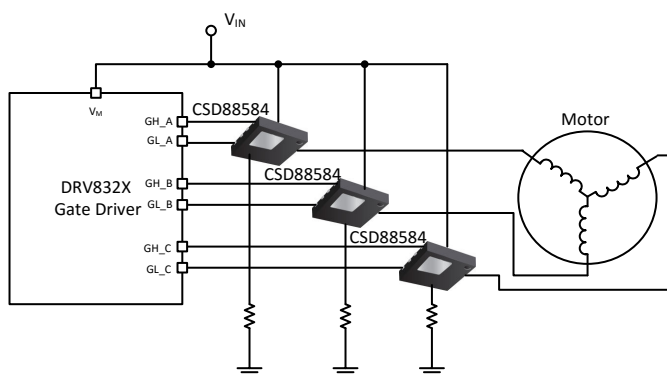
### 2 应用

- 用于无刷直流电机控制的三相桥
- 具有多达 8 节串联电池的电动工具
- 其他半桥和全桥拓扑



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### 电源块原理图

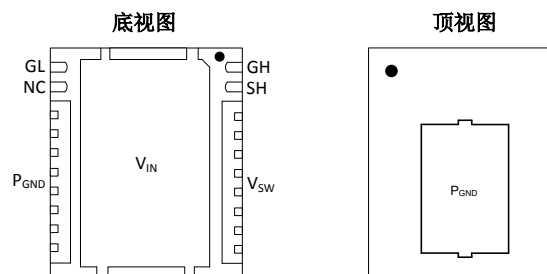


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### 典型电路

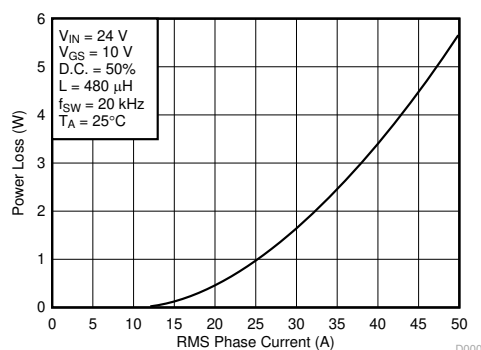
### 3 说明

CSD88584Q5DC 40V 电源块是一款针对手持设备、无绳园艺工具和电动工具等高电流电机控制应用进行了优化的设计。该器件利用 TI 获得专利的堆叠裸片技术来最大限度地减小寄生电感，同时采用节省空间的热增强型 DualCool™ 5mm × 6mm 封装，提供完整的半桥。利用外露的金属顶部，该电源块器件允许简单散热应用通过封装顶部散发 PCB 热量，从而在许多电机控制应用所要求的较高电流下，实现出色的热性能。



### 器件信息

器件	数量	介质	封装	运输
CSD88584Q5DC	2500	13 英寸卷带	SON 5.00mm × 6.00mm 塑料封装	卷带包装
CSD88584Q5DCT	250	7 英寸卷带		



功率损耗与输出电流

D000



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## 4 Specifications

### 4.1 Absolute Maximum Ratings

$T_J = 25^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voltage	$V_{IN}$ to $P_{GND}$	- 0.8	40	V
	$V_{SW}$ to $P_{GND}$	- 0.3	40	
	GH to SH	- 20	20	
	GL to $P_{GND}$	- 20	20	
Pulsed current rating, $I_{DM}$ <sup>(2)</sup>			400	A
Power dissipation, $P_D$			12	W
Avalanche energy, $E_{AS}$	High-side FET, $I_D = 103\text{A}$ , $L = 0.1\text{mH}$		525	mJ
	Low-side FET, $I_D = 103\text{A}$ , $L = 0.1\text{mH}$		525	
Operating junction temperature, $T_J$		- 55	150	$^\circ\text{C}$
Storage temperature, $T_{stg}$		- 55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Single FET conduction, max  $R_{\theta JC} = 1.1^\circ\text{C/W}$ , pulse duration  $\leq 100 \mu\text{s}$ , single pulse.

### 4.2 Recommended Operating Conditions

$T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{GS}$ Gate drive voltage		4.5	16	V
$V_{IN}$ Input supply voltage <sup>(1)</sup>			36	V
$f_{SW}$ Switching frequency	$C_{BST} = 0.1\mu\text{F}$ (min)	5	50	kHz
$I_{OUT}$ RMS motor winding current			50	A
$T_J$ Operating temperature			125	$^\circ\text{C}$

- (1) Up to 32V input use one capacitor per phase, MLCC 10nF, 100V, X7S, 0402, PN: C1005X7S2A103K050BB from  $V_{IN}$  to GND return. Between 32V to 36V input operation, add RC switch-node snubber as described in the [# 6.1.1](#) section of this data sheet.

### 4.3 Power Block Performance

$T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$P_{LOSS}$ Power loss <sup>(1)</sup>	$V_{IN} = 24\text{V}$ , $V_{GS} = 10\text{V}$ , $I_{OUT} = 35\text{A}$ , $f_{SW} = 20\text{kHz}$ , $T_J = 25^\circ\text{C}$ , duty cycle = 50%, $L = 480\mu\text{H}$		2.4		W
$P_{LOSS}$ Power loss	$V_{IN} = 24\text{V}$ , $V_{GS} = 10\text{V}$ , $I_{OUT} = 35\text{A}$ , $f_{SW} = 20\text{kHz}$ , $T_J = 125^\circ\text{C}$ , duty cycle = 50%, $L = 480\mu\text{H}$		3.5		W

- (1) Measurement made with eight 10 $\mu\text{F}$ , 50V,  $\pm 10\%$  X5R (TDK C3225X5R1H106K250AB or equivalent) ceramic capacitors placed across  $V_{IN}$  to  $P_{GND}$  pins and using UCC27210DDAR 100V, 4A driver IC.

## 4.4 Thermal Information

$T_J = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu) <sup>(2)</sup>			125	$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance (max Cu) <sup>(2) (1)</sup>			50	
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package) <sup>(2)</sup>			2.1	$^\circ\text{C/W}$
	Junction-to-case thermal resistance ( $V_{IN}$ pin) <sup>(2)</sup>			1.1	

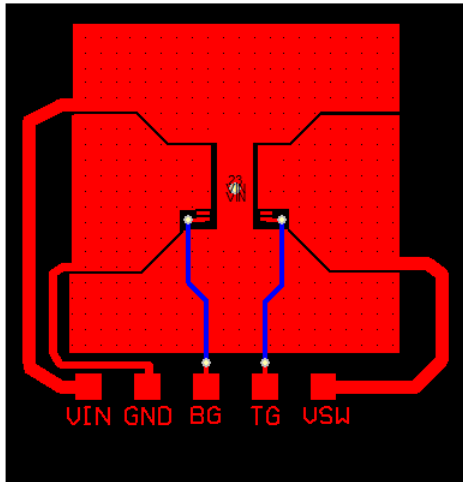
(1) Device mounted on FR4 material with  $1\text{in}^2$  ( $6.45\text{cm}^2$ ) Cu.

(2)  $R_{\theta JC}$  is determined with the device mounted on a  $1\text{in}^2$  ( $6.45\text{cm}^2$ ), 2oz (0.071mm) thick Cu pad on a  $1.5\text{in} \times 1.5\text{in}$  ( $3.81\text{cm} \times 3.81\text{cm}$ ), 0.06in (1.52mm) thick FR4 board.  $R_{\theta JC}$  is specified by design while  $R_{\theta JA}$  is determined by the user's board design.

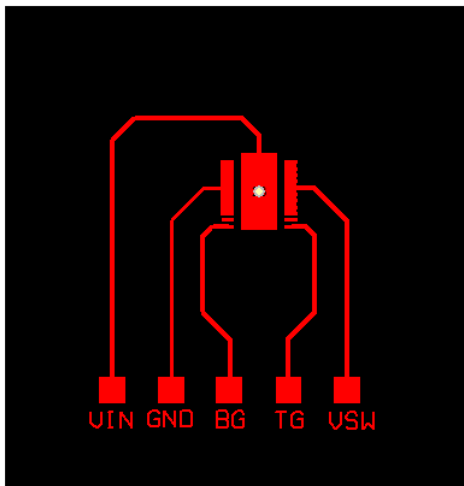
## 4.5 Electrical Characteristics

$T_J = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{V}$ , $I_{DS} = 250\mu\text{A}$	40			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{V}$ , $V_{DS} = 32\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{V}$ , $V_{GS} = 20\text{V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$ , $I_{DS} = 250\mu\text{A}$	1.2	1.7	2.3	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 4.5\text{V}$ , $I_{DS} = 30\text{A}$		1.0	1.5	m $\Omega$
		$V_{GS} = 10\text{V}$ , $I_{DS} = 30\text{A}$		0.68	0.95	
$g_{fs}$	Transconductance	$V_{DS} = 4\text{V}$ , $I_{DS} = 30\text{A}$		149		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{ISS}$	Input capacitance			9540	12400	pF
$C_{OSS}$	Output capacitance	$V_{GS} = 0\text{V}$ , $V_{DS} = 20\text{V}$ , $f = 1\text{MHz}$		957	1240	pF
$C_{RSS}$	Reverse transfer capacitance			474	616	pF
$R_G$	Series gate resistance			1.0	2.0	$\Omega$
$Q_g$	Gate charge total (4.5 V)			68	88	nC
$Q_g$	Gate charge total (10 V)			137	178	nC
$Q_{gd}$	Gate charge gate-to-drain	$V_{DS} = 20\text{V}$ , $I_{DS} = 30\text{A}$		26		nC
$Q_{gs}$	Gate charge gate-to-source			24		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			16		nC
$Q_{OSS}$	Output charge	$V_{DS} = 20\text{V}$ , $V_{GS} = 0\text{V}$		42		nC
$t_{d(on)}$	Turnon delay time			11		ns
$t_r$	Rise time	$V_{DS} = 20\text{V}$ , $V_{GS} = 10\text{V}$ , $I_{DS} = 30\text{A}$ , $R_G = 0\Omega$		24		ns
$t_{d(off)}$	Turnoff delay time			53		ns
$t_f$	Fall time			17		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{DS} = 30\text{A}$ , $V_{GS} = 0\text{V}$		0.75	1.0	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 20\text{V}$ , $I_F = 30\text{A}$ , $di/dt = 300\text{A}/\mu\text{s}$		34		nC
$t_{rr}$	Reverse recovery time			24		ns



Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$  when mounted on  $1\text{in}^2$  ( $6.45\text{cm}^2$ ) of 2oz ( $0.071\text{mm}$ ) thick Cu.



Max  $R_{\theta JA} = 125^{\circ}\text{C/W}$  when mounted on minimum pad area of 2oz ( $0.071\text{mm}$ ) thick Cu.

### 4.6 Typical Power Block Device Characteristics

The typical power block system characteristic curves (图 4-1 through 图 4-6) are based on measurements made on a PCB design with dimensions of 4in (W) × 3.5in (L) × 0.062in (H) and 6 copper layers of 2oz copper thickness. See 节 5 section for detailed explanation.  $T_J = 125^\circ\text{C}$ , unless stated otherwise.

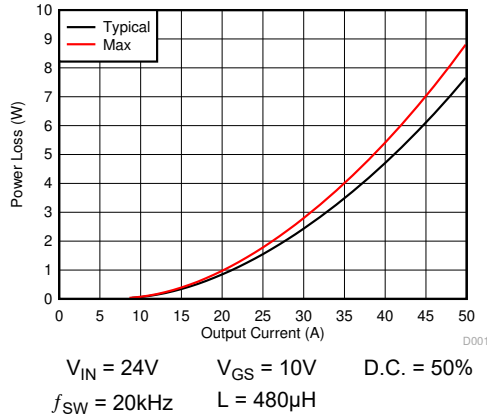


图 4-1. Power Loss vs Output Current

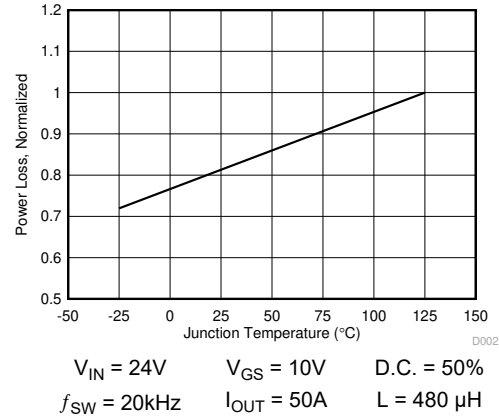


图 4-2. Power Loss vs Temperature

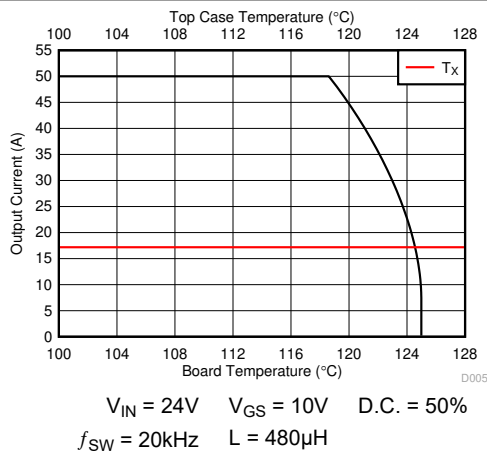


图 4-3. Typical Safe Operating Area

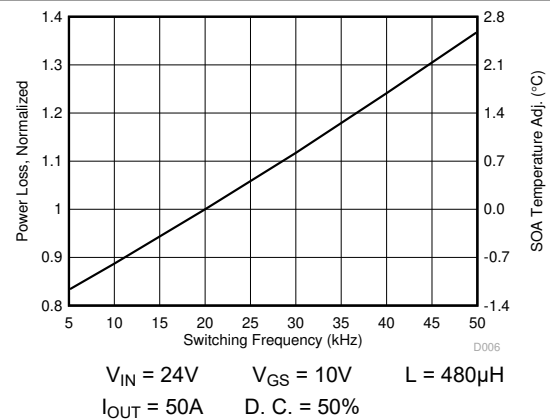


图 4-4. Normalized Power Loss vs Switching Frequency

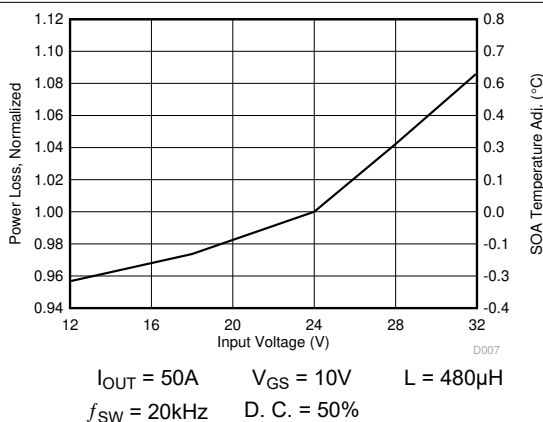


图 4-5. Normalized Power Loss vs Input Voltage

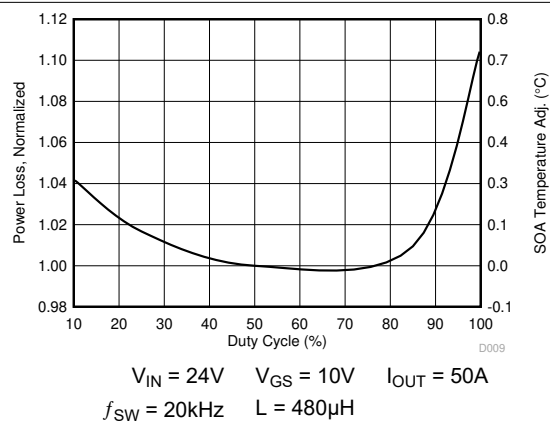


图 4-6. Normalized Power Loss vs Duty Cycle

### 4.7 Typical Power Block MOSFET Characteristics

$T_J = 25^\circ\text{C}$ , unless stated otherwise.

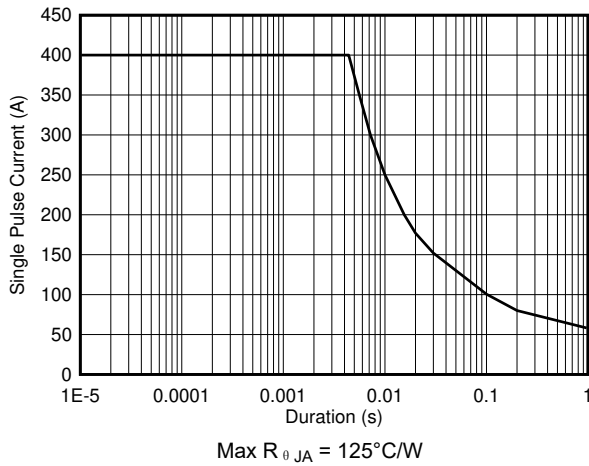


图 4-7. Single Pulse Current vs Pulse Duration

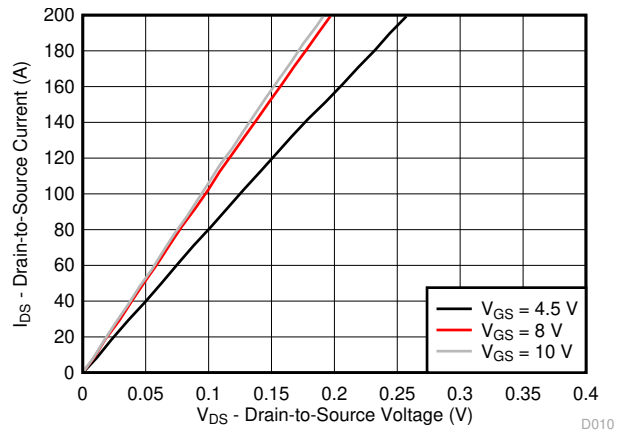


图 4-8. MOSFET Saturation Characteristics

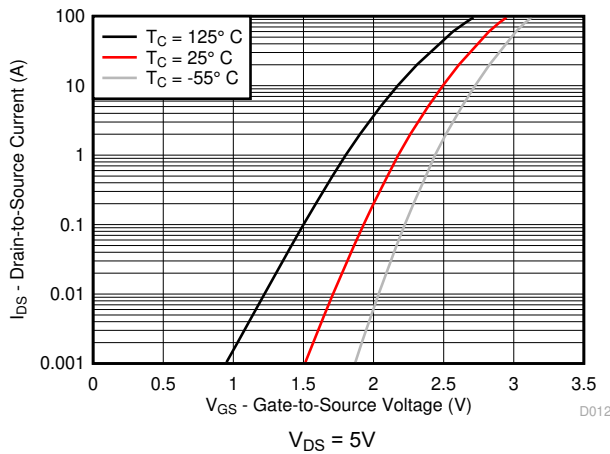


图 4-9. MOSFET Transfer Characteristics

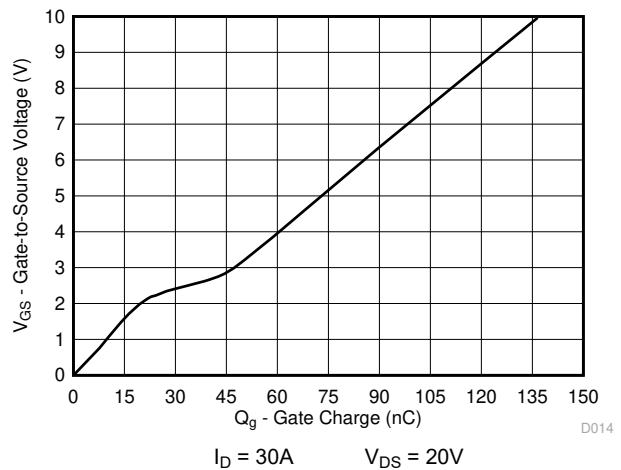


图 4-10. MOSFET Gate Charge

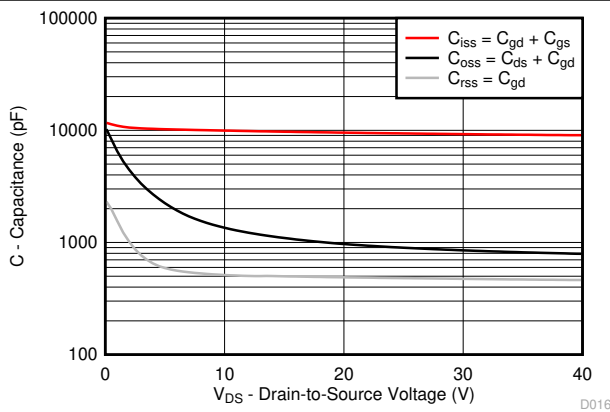


图 4-11. MOSFET Capacitance

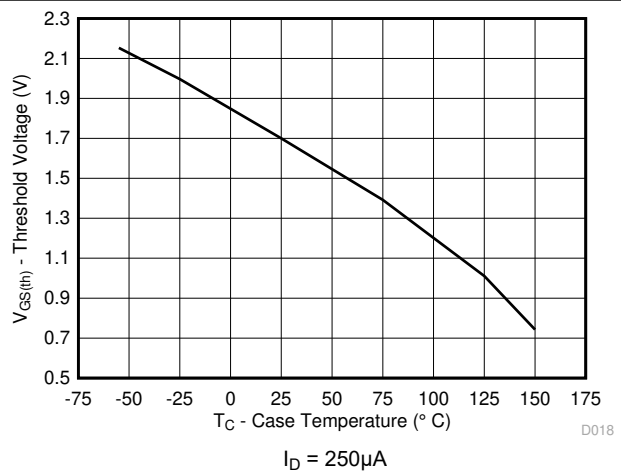


图 4-12. Threshold Voltage vs Temperature

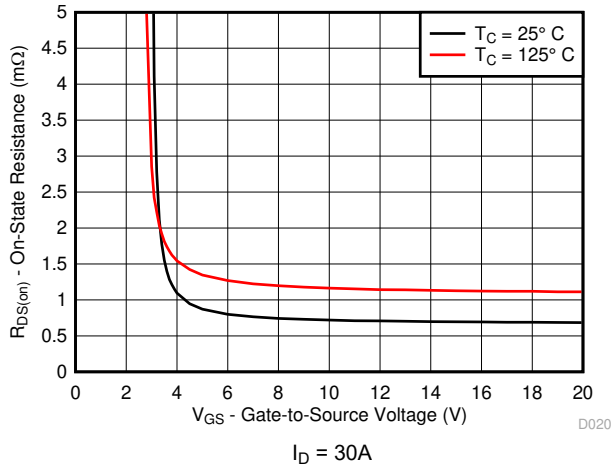


图 4-13. MOSFET  $R_{DS(on)}$  vs  $V_{GS}$

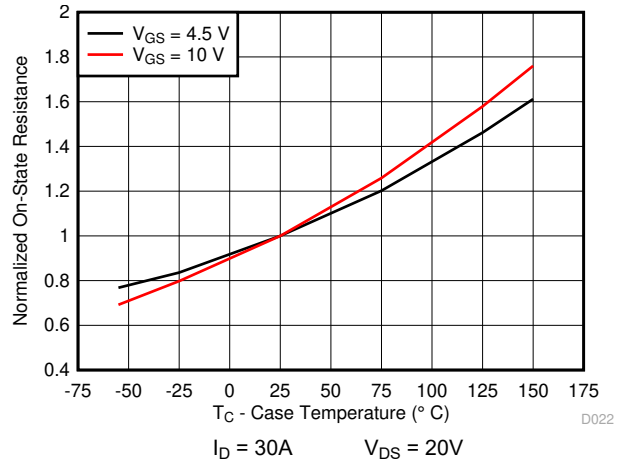


图 4-14. MOSFET Normalized  $R_{DS(on)}$  vs Temperature

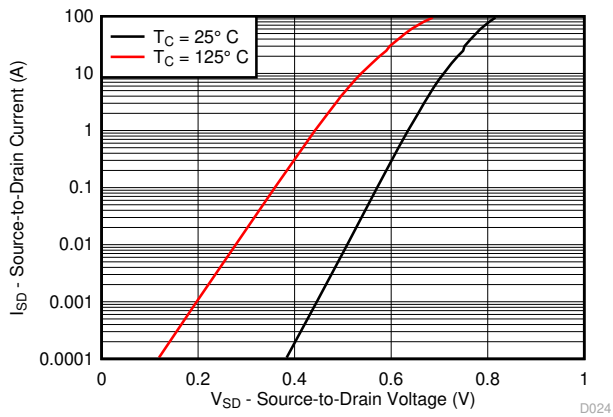


图 4-15. MOSFET Body Diode Forward Voltage

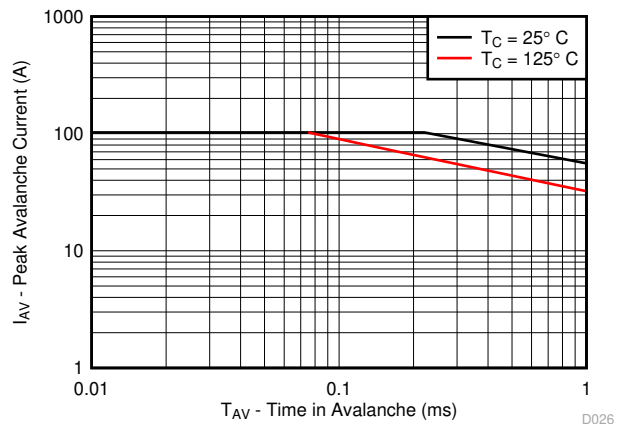


图 4-16. MOSFET Single Pulse Unclamped Inductive Switching



## 5 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

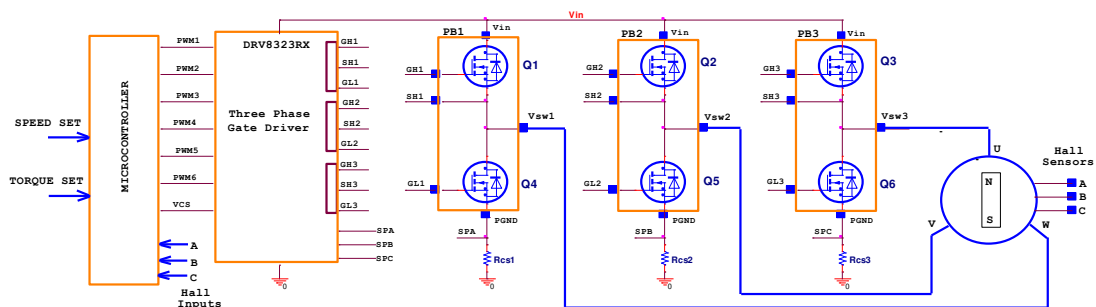
### 5.1 Application Information

Historically, battery powered tools have favored brushed DC configurations to spin their primary motors, but more recently, the advantages offered by brushless DC operation (BLDC) operation have brought about the advent of popular designs that favor the latter. Those advantages include, but are not limited to higher efficiency and therefore longer battery life, superior reliability, greater peak torque capability, and smooth operation over a wider range of speeds. However, BLDC designs put increased demand for higher power density and current handling capabilities on the power stage responsible for driving the motor.

The CSD88584Q5DC is part of TI's power block product family and is a highly optimized product designed explicitly for the purpose driving higher current DC motors in power and gardening tools. It incorporates TI's latest generation silicon which has been optimized for low resistance to minimize conduction losses and offer excellent thermal performance. The power block utilizes TI's stacked die technology to offer one complete half bridge vertically integrated into a single 5mm × 6mm package with a DualCool exposed metal case. This feature allows the designer to apply a heatsink to the top of the package and pull heat away from the PCB, thus maximizing the power density while reducing the power stage footprint by up to 50%.

### 5.2 Brushless DC Motor With Trapezoidal Control

The trapezoidal commutation control is simple and has fewer switching losses compared to sinusoidal control.



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图 5-1. Functional Block Diagram

The block diagram shown in 图 5-1 offers a simple instruction of what is required to drive a BLDC motor: one microcontroller, one three-phase driver IC, 3 power blocks (historically 6 power MOSFETs) and 3 Hall effect sensors. The microcontroller responsible for block commutation must always know the rotor orientation or its position relative to the stator coils. This is easily achieved with a brushed DC motor due to the fixed geometry and position of the rotor windings, shaft and commutator.

A three-phase BLDC motor requires three Hall effect sensors or a rotary encoder to detect the rotor position in relation to stator armature windings. Combining these three Hall effect sensors output signals, the microcontroller can determine the proper commutation sequence. The three Hall sensors named A, B, and C are mounted on the stator core at 120° intervals and the stator phase windings are implemented in a star configuration. For every 60° of motor rotation, one Hall sensor changes its state. Based on the Hall sensor outputs code, at the end of each block commutation interval the ampere conductors are commutated to the next position. There are 6 steps needed to complete a full electrical cycle. The number of block commutation cycles to complete a full mechanical rotation is determined by the number of rotor pole pairs.

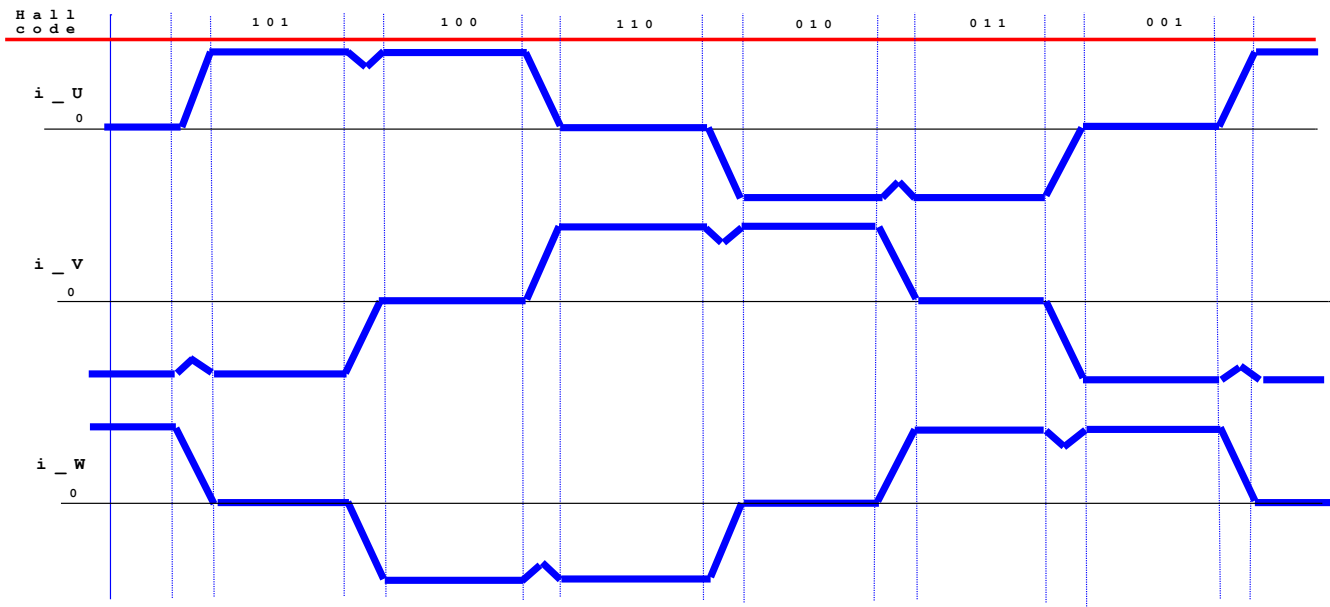


图 5-2. Winding Current Waveforms on a BLDC Motor

图 5-2 上方显示了三个相电机绕组电流  $i_U$ 、 $i_V$  和  $i_W$  在 100% 占空比下运行时的波形。

梯形换相控制提供以下优势：

- 在任何时候，只有两个绕组串联承载相绕组电流，而第三个绕组是开路的。
- 对于所有三个绕组 U、V 和 W，只需要一个电流传感器。
- 传感器的位置允许使用低成本分流电阻。

然而，梯形换相控制具有换相转矩纹波这一缺点。在三相逆变器中的电流检测可以配置为使用单个分流或三个不同的检测电阻。对于成本敏感的应用，特别是针对无传感器控制，三个霍尔效应传感器可以被 BEMF 电压反馈分压器取代。

为了获得更快的电机转速和更高的每分钟转速 (RPM)，需要更短的周期和更高的  $V_{IN}$  电压。相反，为了降低电机的转速，有必要降低施加在定子绕组上的 RMS 电压。这可以通过调制占空比来实现，同时保持恒定的开关频率。三相逆变器的频率通常选择在 10kHz 到 50kHz 之间，以减少绕组损耗并避免 audible noise。

### 5.3 Power Loss Curves

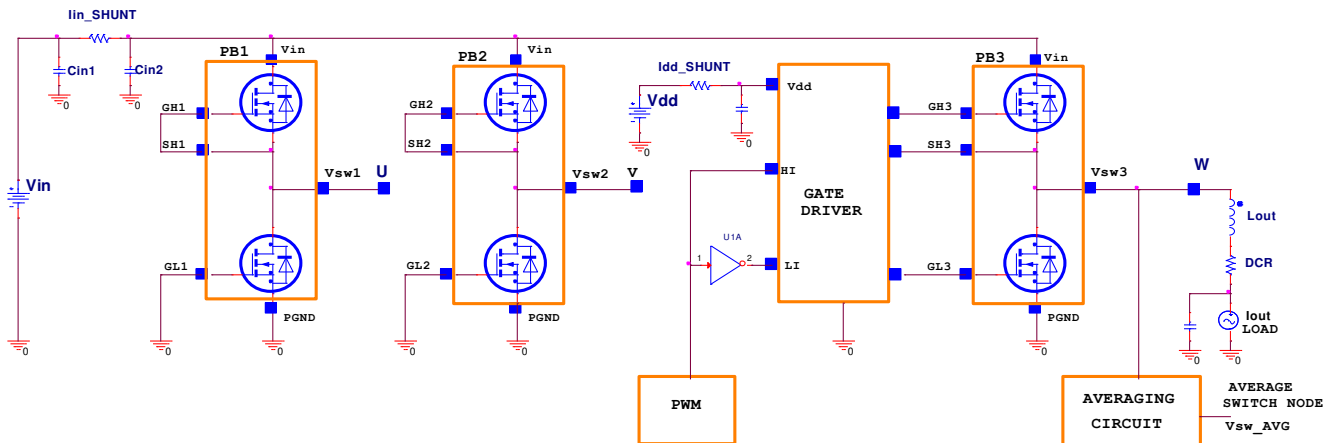
CSD88584Q5DC was designed to operate up to 7-cell Li-Ion battery voltage applications ranging from 18V to 32V, typical 24V. For 8s, input voltages between 32V to 36V, RC snubbers are required for each switch-node U, V, and W. To reduce ringing, refer to the 节 6.1.1 section. In an effort to simplify the design process, Texas Instruments has provided measured power loss performance curves over a variety of typical conditions.

图 4-1 plots the CSD88584Q5DC power loss as a function of load current. The measured power loss includes both input conversion loss and gate drive loss.

方程式 1 is used to generate the power loss curve:

$$\text{Power loss (W)} = (V_{IN} \times I_{IN\_SHUNT}) + (V_{DD} \times I_{DD\_SHUNT}) - (V_{SW\_AVG} \times I_{OUT}) \quad (1)$$

The power loss measurements were made on the circuit shown in 图 5-3, power block devices for legs U and V, PB1 and PB2 were disabled by shorting the CSD88584Q5DC high-side and low-side FETs gate-to-source terminals. Current shunt  $I_{in\_shunt}$  provides Input current and  $I_{dd\_SHUNT}$  provides driver supply current measurements. The winding current is measured from the DC load. An averaging circuit provides switch node W equivalent RMS voltage.



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图 5-3. Power Loss Test Circuit

The RMS current on the CSD88584Q5DC device depends on the motor winding current. For trapezoidal control, the MOSFET RMS current is calculated using 方程式 2.

$$I_{RMS} = I_{OUT} \times \sqrt{2} \quad (2)$$

Taking into consideration system tolerances with the current measurement scheme, the inverter design needs to withstand a 20% overload current.

表 5-1. RMS and Overload Current Calculations

Winding RMS Current (A)	CSD88584Q5DC $I_{RMS}$ (A)	Overload 120% $\times I_{RMS}$ (A)
30	42	51
40	56	68
50	70	85

## 5.4 Safe Operating Area (SOA) Curve

The SOA curve in 图 4-3 provide guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. This curve outlines the board and case temperatures required for a given load current. The area under the curve dictates the safe operating area. This curve is based on measurements made on a PCB design with dimensions of 4in (W) × 3.5in (L) × 0.062in (H) and 6 copper layers of 2oz copper thickness.

## 5.5 Normalized Power Loss Curves

The normalized curves in the CSD88584Q5DC data sheet provide guidance on the power loss and SOA adjustments based on application specific needs. These curves show how the power loss and SOA temperature boundaries will adjust for different operation conditions. The primary Y-axis is the normalized change in power loss while the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the typical power loss. The change in SOA temperature is subtracted from the SOA curve.

## 5.6 Design Example – Regulate Current to Maintain Safe Operation

If the case and board temperature of the power block are known, the SOA can be used to determine the maximum allowed current that will maintain operation within the safe operating area of the device. The following procedure outlines how to determine the RMS current limit while maintaining operation within the confines of the SOA, assuming the temperatures of the top of the package and PCB directly underneath the part are known.

1. Start at the maximum current of the device on the Y-axis and draw a line from this point at the known top case temperature to the known PCB temperature.
2. Observe where this point intersects the  $T_{\chi}$  line.
3. At this intersection with the  $T_{\chi}$  line, draw vertical line until you hit the SOA current limit. This intercept is the maximum allowed current at the corresponding power block PCB and case temperatures.

In the example below, we show how to achieve this for the temperatures  $T_C = 124^{\circ}\text{C}$  and  $T_B = 120^{\circ}\text{C}$ . First we draw from 50 A on the Y-axis at  $124^{\circ}\text{C}$  to  $120^{\circ}\text{C}$  on the X-axis. Then, we draw a line up from where this line crosses the  $T_{\chi}$  line to see that this line intercepts the SOA at 39A. Thus we can assume if we are measuring a PCB temperature of  $124^{\circ}\text{C}$ , and a top case temperature of  $120^{\circ}\text{C}$ , the power block can handle 39A RMS, at the normalized conditions. At conditions that differ from those in 图 4-1, the user may be required to make an SOA temperature adjustment on the  $T_{\chi}$  line, as shown in the next section.

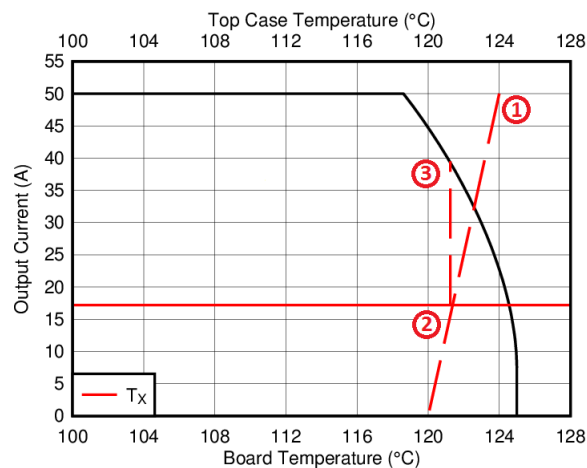


图 5-4. Regulating Current to Maintain Safe Operation

## 5.7 Design Example – Regulate Board and Case Temperature to Maintain Safe Operation

In the previous example we showed how given the PCB and case temperature, the current of the power block could be limited to ensure operation within the SOA. Conversely, if the current and other application conditions are known, one can determine from the SOA what board or case temperature the user will need to limit their design to. The user can estimate product loss and SOA boundaries by arithmetic means (see [§ 5.7.1](#) section). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

### 5.7.1 Operating Conditions

- Winding output current ( $I_{OUT}$ ) = 40A
- Input voltage ( $V_{IN}$ ) = 32V
- Switching frequency ( $F_{SW}$ ) = 40kHz
- Duty cycle (D.C.) = 95%

### 5.7.2 Calculating Power Loss

- Power loss at 40A  $\approx$  4.7W ([图 4-1](#))
- Normalized power loss for switching frequency  $\approx$  1.24 ([图 4-4](#))
- Normalized power loss for input voltage  $\approx$  1.09 ([图 4-5](#))
- Normalized power loss for duty cycle  $\approx$  1.06 ([图 4-6](#))
- **Final calculated power loss = 4.7W  $\times$  1.24  $\times$  1.09  $\times$  1.06  $\approx$  6.7W**

### 5.7.3 Calculating SOA Adjustments

- SOA adjustment for switching frequency  $\approx$  1.7°C ([图 4-4](#))
- SOA adjustment for input voltage  $\approx$  0.6°C ([图 4-5](#))
- SOA adjustment for duty cycle  $\approx$  0.4°C ([图 4-6](#))
- **Final calculated SOA adjustment = 1.7 + 0.6 + 0.4  $\approx$  2.7°C**

In the [§ 5.6](#) section above, the estimated power loss of the CSD88584Q5DC would increase to 6.7W. In addition, the maximum allowable board temperature would have to increase by 2.7°C. In [图 5-5](#), the SOA graph was adjusted accordingly.

1. Start by drawing a horizontal line from the application current (40A) to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the  $T_X$  line.
3. Adjust the intersection point by subtracting the temperature adjustment value.

In this design example, the SOA board/ambient temperature adjustment yields a decrease of allowed junction temperature of 2.7°C from 121.0°C to 118.3°C. Now it is known that the intersection of the case and PCB temperatures on the  $T_X$  line must stay below this point. For instance, if the power block case is observed operating at 124°C, the PCB temperature must in turn be kept under 115°C to maintain this crossover point.

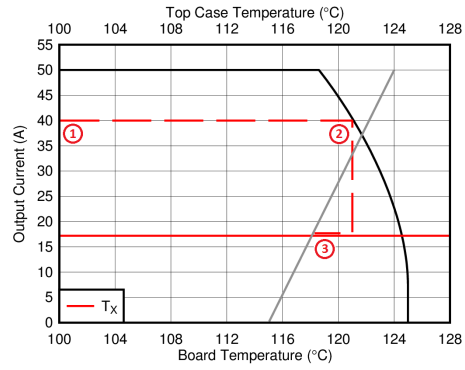


图 5-5. Regulate Temperature to Maintain Safe Operation

## 6 Layout

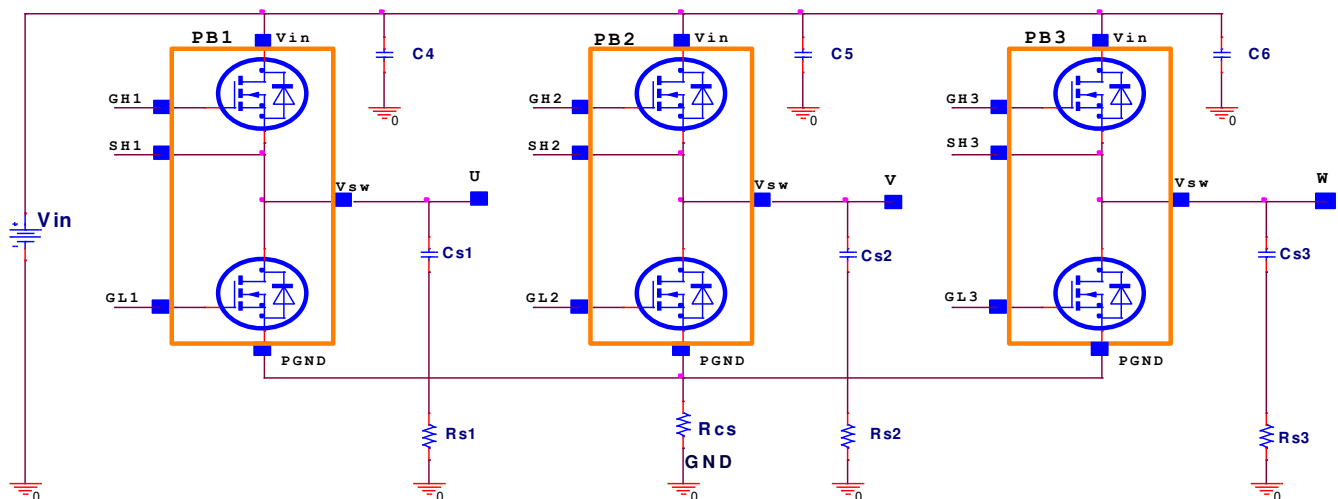
The two key system-level parameters that can be optimized with proper PCB design are electrical and thermal performance. A proper PCB layout will yield maximum performance in both areas. Below are some tips for how to address each.

### 6.1 Layout Guidelines

#### 6.1.1 Electrical Performance

The CSD88584Q5DC power block has the ability to switch at voltage rates greater than  $1\text{kV}/\mu\text{s}$ . Special care must be then taken with the PCB layout design and placement of the input capacitors; high-current, high  $dI/dT$  switching path; current shunt resistors; and GND return planes. As with any high-power inverter operated in hard switching mode, there will be voltage ringing present on the switch nodes U, V, and W. Switch-node ringing appears mainly at the HS FET turnon commutation with positive winding current direction. The U, V, and W phase connections to the BLDC motor can be usually excluded from the ringing behavior since they are subjected to high-peak currents but low  $dI/dT$  slew-rates. However, a compact PCB design with short and low-parasitic loop inductances is critical to achieve low ringing and compliance with EMI specifications.

For safe and reliable operation of the three-phase inverter, motor phase currents have to be accurately monitored and reported to the system microcontroller. One current sensor needs to be connected on each motor phase winding U, V, and W. This sensing method is best for current sensing as it provides good accuracy over a wide range of duty cycles, motor torque, and winding currents. Using current sensors is recommended because it is less intrusive to the  $V_{IN}$  and GND connections.



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图 6-1. Recommended Ringing Reduction Components

However, for cost sensitive applications, current sensors are generally replaced with current sense resistors.

- For designs using the 60V three-phase smart gate driver DRV8320SRHBR, current sense resistor  $R_{CS}$  can be placed between common source terminals for all 3 power block devices CSD88584Q5DC to  $P_{GND}$  and measured using an external current sense amplifier as depicted in 图 6-1 above.
- For designs using the 60V three-phase gate driver DRV8323RSRGZT, three current sense resistors  $R_{CS1}$ ,  $R_{CS2}$  and  $R_{CS3}$  can be used between each CSD88584Q5DC source terminal to GND and measured by the included DRV8323 current sense amplifiers. The three-phase driver IC should be placed as close as possible to the power block gate GL and GH terminals.

Breaking the high-current flow path from the source terminals of the power block to GND by introducing the  $R_{CS}$  current shunt resistors introduces parasitic PCB inductance. In the event the switch node waveforms exhibit peak ringing that reaches undesirable levels, the ringing can be reduced by using the following ringing reduction components:

- The use of a high-side gate resistor in series with the GH pin is one effective way to reduce peak ringing. The recommended HS FET gate resistor value will range between  $4.7\Omega$  to  $10\Omega$  depending on the driver IC output characteristics used in conjunction with the power block device. The low-side FET gate pin GL should connect directly to the driver IC output to avoid any parasitic  $cdV/dT$  turnon effect.
- Low inductance MLCC caps C4, C5, and C6 can be used across each power block device from  $V_{IN}$  to the source terminal  $P_{GND}$ . MLCC 10nF, 100V,  $\pm 10\%$ , X7S, 0402, PN: C1005X7S2A103K050BB are recommended.
- Ringing can be reduced via the implementation of RC snubbers from each switch node U, V, and W to GND. Recommended snubber component values are as follows:
  - Snubber resistors  $R_{s1}$ ,  $R_{s2}$ ,  $R_{s3}$ :  $2.21\Omega$ , 1%, 0.125W, 0805, PN: CRCW08052R21FKEA
  - Snubber caps  $C_{s1}$ ,  $C_{s2}$ , and  $C_{s3}$ : MLCC 4.7nF, 100V, X7S, 0402, PN: C1005X7S2A472M050BB

With a switching frequency of 20kHz on the three-phase inverter, the power dissipation on the RC snubber resistor is 80mW per channel. As a result, 0805 package size for resistors  $R_{s1}$ ,  $R_{s2}$ , and  $R_{s3}$  is adequate.

### 6.1.2 Thermal Considerations

The CSD88584Q5DC power block device has the ability to utilize the PCB copper planes as the primary thermal path. As such, the use of thermal vias included in the footprint is an effective way to pull away heat from the device and into the system board. Concerns regarding solder voids and manufacturability issues can be addressed through the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from one another to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed by the design. The example in [图 6-2](#) uses vias with a 10mil drill hole and a 16mil solder pad.
- Tent the opposite side of the via with solder-mask. Ultimately the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

To take advantage of the DualCool thermally enhanced package, an external heatsink can be applied on top of the power block devices. For low EMI, the heatsink is usually connected to GND through the mounting screws to the PCB. Gap pad insulators with good thermal conductivity should be used between the top of the package and the heatsink. The Bergquist Sil-Pad 980 is recommended which provides excellent thermal impedance of  $1.07^\circ\text{C/W}$  at 50psi.



## 6.2 Layout Example

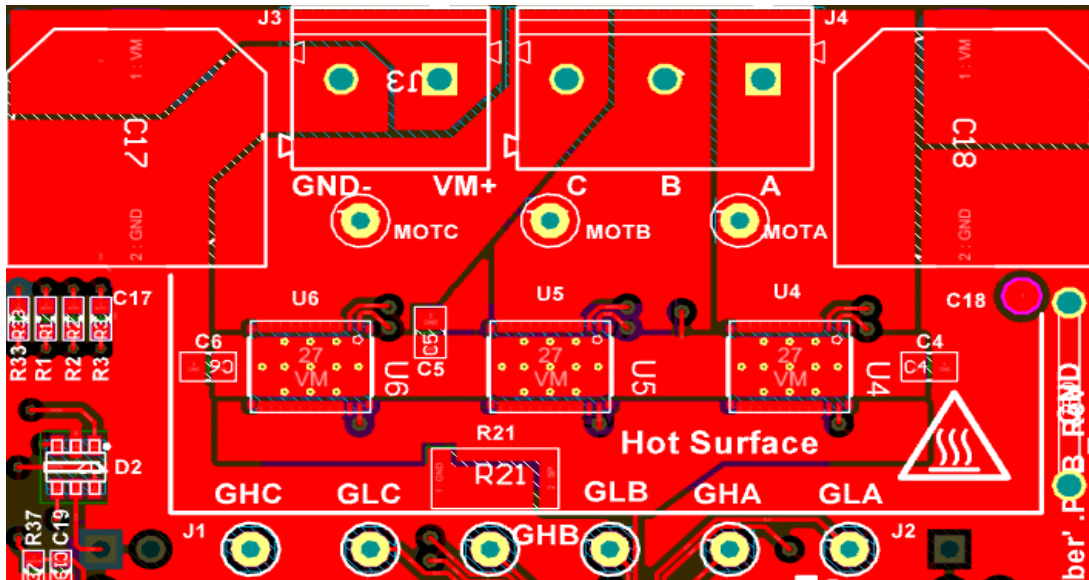


图 6-2. Top Layer

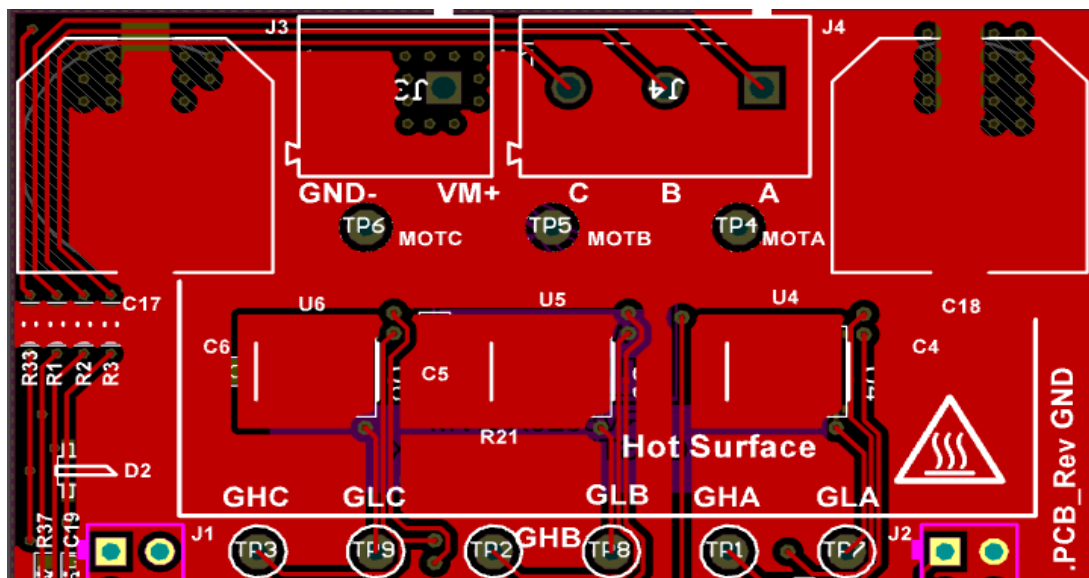


图 6-3. Bottom Layer

The placement of the input capacitors C4, C5, and C6 relative to  $V_{IN}$  and  $P_{GND}$  pins of CSD88584Q5DC device should have the highest priority during the component placement routine. It is critical to minimize the  $V_{IN}$  to GND parasitic loop inductance. A shunt resistor R21 is used between all three U4, U5, and U6 power block source terminals to the input supply GND return pin.

Input RMS current filtering is achieved via two bulk caps C17 and C18. Based on the RMS current ratings, the recommended part number for input bulk is CAP AL, 330 $\mu$ F, 63V,  $\pm$ 20%, PN: EMVA630ADA331MKG5S.

## 7 Device and Documentation Support

### 7.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 7.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 7.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 8 Revision History

<b>Changes from Revision D (December 2018) to Revision E (June 2024)</b>	<b>Page</b>
• 通篇更新了表格、图和交叉参考的编号格式.....	1
• 向“顶视图”引脚排列图中添加了 PGND.....	1
<b>Changes from Revision C (January 2018) to Revision D (December 2018)</b>	<b>Page</b>
• Updated current sense resistor description in applications section .....	15
<b>Changes from Revision B (September 2017) to Revision C (January 2018)</b>	<b>Page</b>
• 将 <i>功率损耗与输出电流</i> <i>功率损耗与输出电流</i> 图表上的 $V_{DD} = 10V$ 改为 $V_{GS} = 10V$ .....	1
• Changed $V_{DD}$ to $V_{GS}$ in sections <i>Recommended Operating Conditions</i> , <i>Block Performance</i> , and <i>Typical Power Block Device Characteristics</i> .....	3
• Changed $I_{DSS}$ test condition from 20V to 32V in the <i>Electrical Characteristics</i> table.....	4
<b>Changes from Revision A (May 2017) to Revision B (September 2017)</b>	<b>Page</b>
• Updated <a href="#">图 4-3</a> to extend to 50A.....	6
<b>Changes from Revision * (May 2017) to Revision A (May 2017)</b>	<b>Page</b>
• 更新了 <i>典型电路</i> 图中的栅极驱动器器件型号.....	1

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

表 9-1. Pin Configuration Table

POSITION	PIN NAME	DESCRIPTION
1	GH	High Side Gate
2	SH	High Side Gate Return
3-11	V <sub>SW</sub>	Switch Node
12-20	P <sub>GND</sub>	Power Ground
21	NC	No Connect
22	GL	Low Side Gate
23-26	NC	No Connect
27	V <sub>IN</sub>	Input Voltage

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88584Q5DC	ACTIVE	VSON-CLIP	DMM	22	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	88584	<a href="#">Samples</a>
CSD88584Q5DCT	ACTIVE	VSON-CLIP	DMM	22	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	88584	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD88584Q5DC	VSON-CLIP	DMM	22	2500	330.0	15.4	6.3	5.3	1.2	8.0	12.0	Q2
CSD88584Q5DCT	VSON-CLIP	DMM	22	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD88584Q5DC	VSON-CLIP	DMM	22	2500	333.2	345.9	28.6
CSD88584Q5DCT	VSON-CLIP	DMM	22	250	180.0	180.0	79.0



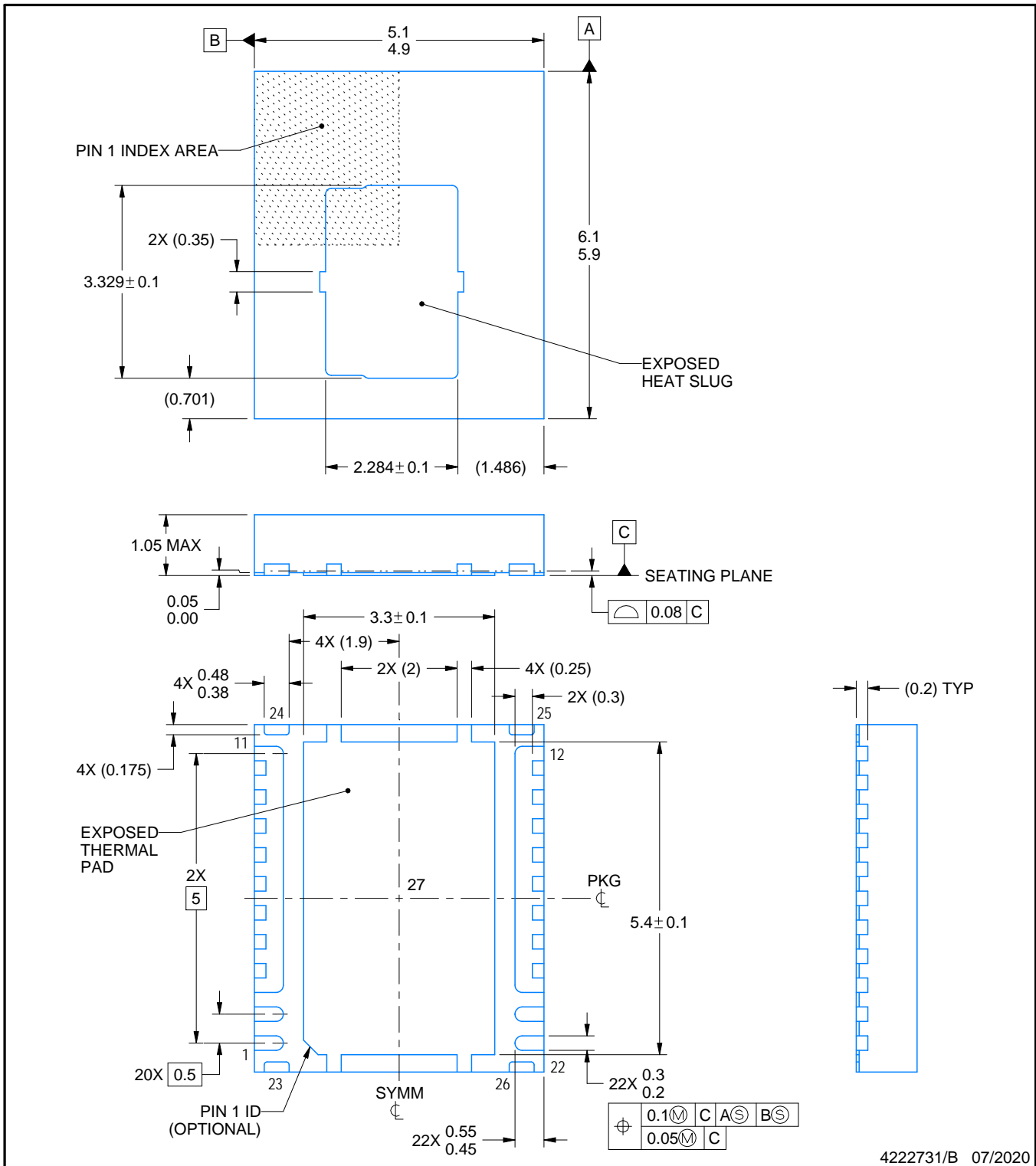
# DMM0022A



# PACKAGE OUTLINE

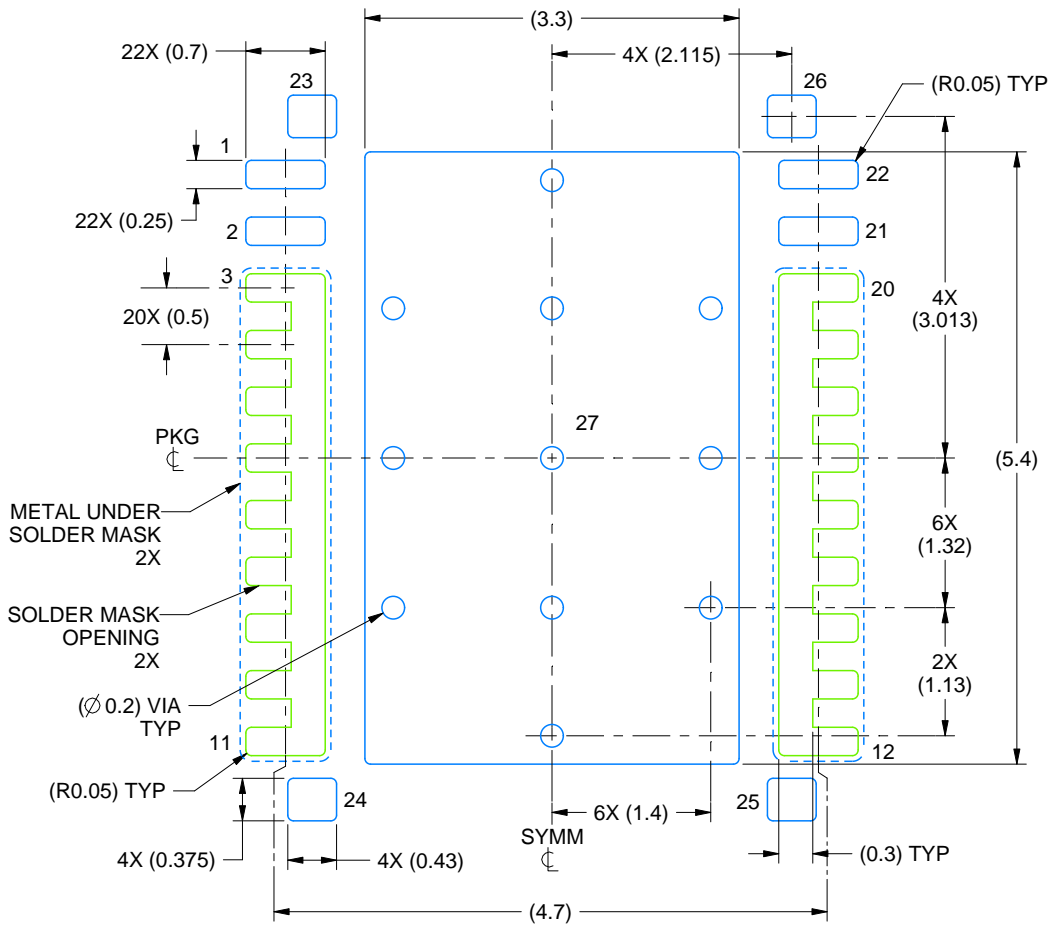
## LSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

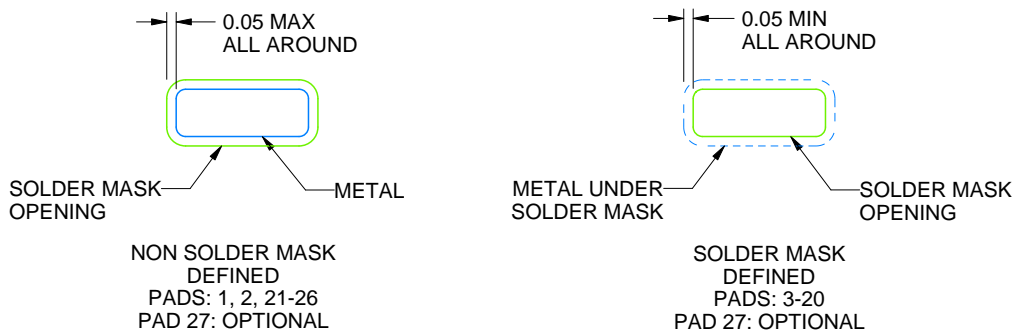


### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Tie bar size and position may vary.



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4222731/B 07/2020

NOTES: (continued)

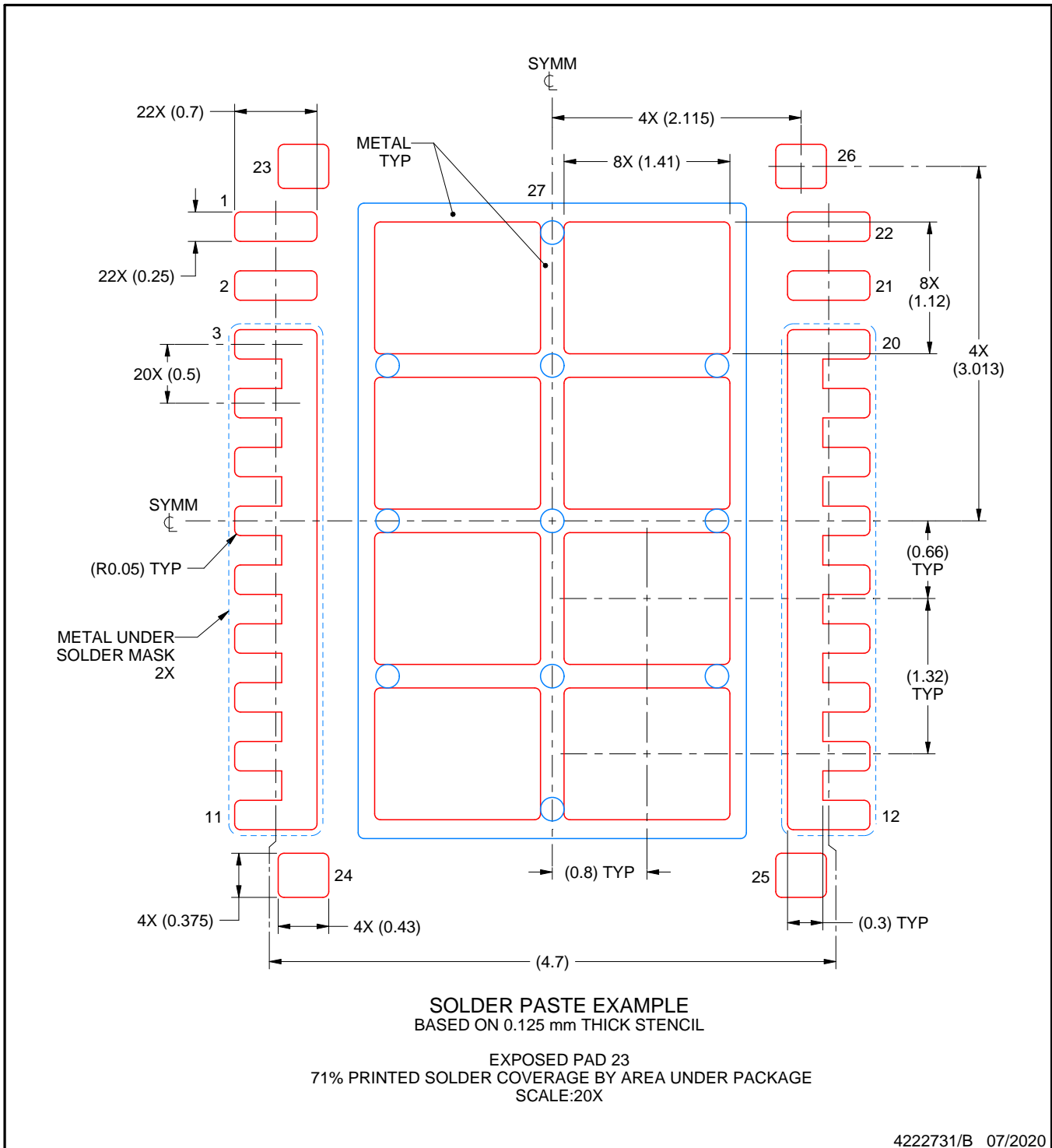
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DMM0022A

LSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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