# DS91M040 125 MHz Quad M-LVDS Transceiver

**Check for Samples: DS91M040**

## FEATURES

- **DC - 125 MHz / 250 Mbps Low Jitter, Low Skew, Low Power Operation**
- **Wide Input Common Mode Voltage Range Allows up to ±1V of GND Noise**
- **Conforms to TIA/EIA-899 M-LVDS Standard**
- **Pin Selectable M-LVDS Receiver Type (1 or 2)**
- **Controlled Transition Times (2.0 ns typ) Minimize Reflections**
- **8 kV ESD on M-LVDS I/O pins protects adjoining components**
- **Flow-Through Pinout Simplifies PCB Layout**
- **Small 5 mm x 5 mm WQFN-32 Space Saving Package**

## APPLICATIONS

- **Multidrop / Multipoint Clock and Data Distribution**
- **High-Speed, Low Power, Short-Reach Alternative to TIA/EIA-485/422**
- **Clock Distribution in AdvancedTCA (ATCA) and MicroTCA (µTCA, uTCA) Backplanes**

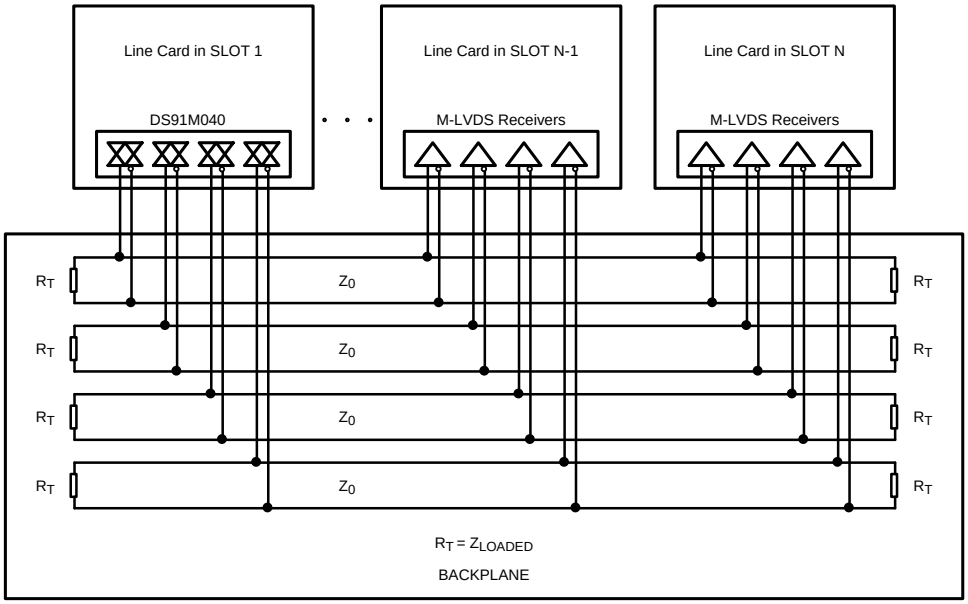
## DESCRIPTION

The DS91M040 is a quad M-LVDS transceiver designed for driving / receiving clock or data signals to / from up to four multipoint networks.

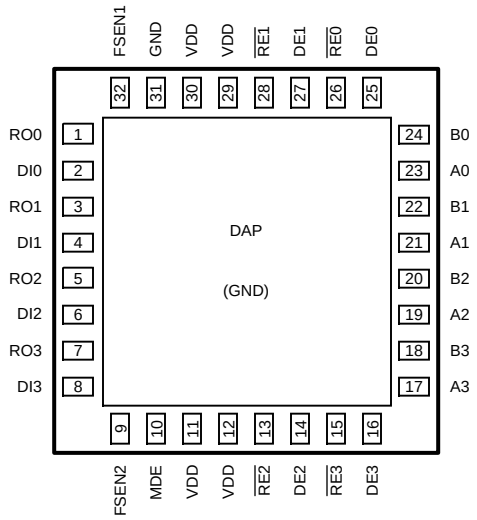
M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multi-point applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs. M-LVDS devices also have a very large input common mode voltage range for additional noise margin in heavily loaded and noisy backplane environments.

A single DS91M040 channel is a half-duplex transceiver that accepts LVTTL/LVCMOS signals at the driver inputs and converts them to differential M-LVDS signal levels. The receiver inputs accept low voltage differential signals (LVDS, BLVDS, M-LVDS, LVPECL and CML) and convert them to 3V LVCMOS signals. The DS91M040 supports both M-LVDS type 1 and type 2 receiver inputs.

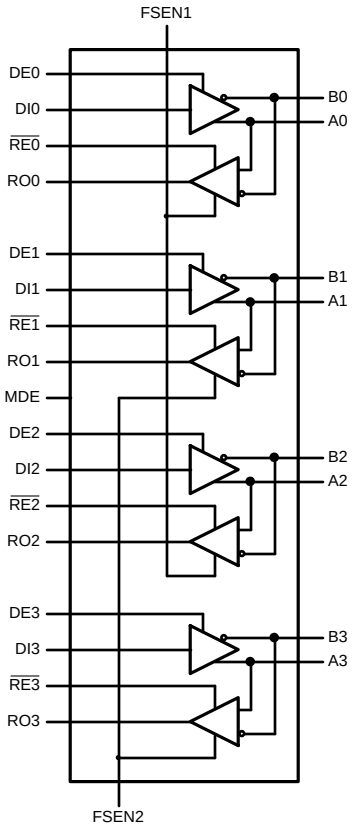
### System Diagram



## Connection Diagram




## Logic Diagram



**PIN DESCRIPTIONS**

| Number | Name | I/O, Type | Description |
|---|---|---|---|
| 1, 3, 5, 7 | RO | O, LVCMOS | Receiver output pin. |
| 26, 28, 13, 15 | $\overline{RE}$ | I, LVCMOS | Receiver enable pin: When $\overline{RE}$ is high, the receiver is disabled. When $\overline{RE}$ is low, the receiver is enabled. There is a 300 kΩ pullup resistor on this pin. |
| 25, 27, 14, 16 | DE | I, LVCMOS | Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled. There is a 300 kΩ pulldown resistor on this pin. |
| 2, 4, 6, 8 | DI | I, LVCMOS | Driver input pin. |
| 31, DAP | GND | Power | Ground pin and pad. |
| 17, 19, 21, 23 | A | I/O, M-LVDS | Non-inverting driver output pin/Non-inverting receiver input pin |
| 18, 20, 22, 24 | B | I/O, M-LVDS | Inverting driver output pin/Inverting receiver input pin |
| 11, 12, 29, 30 | $V_{DD}$ | Power | Power supply pin, +3.3V ± 0.3V |
| 32 | FSEN1 | I, LVCMOS | Failsafe enable pin with a 300 kΩ pullup resistor. This pin enables Type 2 receiver on inputs 0 and 2.<br>FSEN1 = L --> Type 1 receiver inputs<br>FSEN1 = H --> Type 2 receiver inputs |
| 9 | FSEN2 | I, LVCMOS | Failsafe enable pin with a 300 kΩ pullup resistor. This pin enables Type 2 receiver on inputs 1 and 3.<br>FSEN2 = L --> Type 1 receiver inputs<br>FSEN2 = H --> Type 2 receiver inputs |
| 10 | MDE | I, LVCMOS | Master enable pin. When MDE is H, the device is powered up. When MDE is L, the device overrides all other control and powers down. |

## M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater then $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.

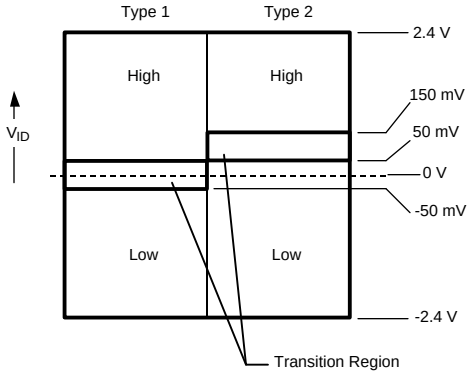



**Figure 1. M-LVDS Receiver Input Thresholds**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1][2]

| | | |
|---|---|---|
| Power Supply Voltage | | −0.3V to +4V |
| LVCMOS Input Voltage | | −0.3V to ($V_{DD}$ + 0.3V) |
| LVCMOS Output Voltage | | −0.3V to ($V_{DD}$ + 0.3V) |
| M-LVDS I/O Voltage | | −1.9V to +5.5V |
| M-LVDS Output Short Circuit Current Duration | | Continuous |
| Junction Temperature | | +140°C |
| Storage Temperature Range | | −65°C to +150°C |
| Lead Temperature Range Soldering (4 sec.) | | +260°C |
| Maximum Package Power Dissipation @ +25°C | RTV Package | 3.91W |
| | Derate RTV Package | 34 mW/°C above +25°C |
| Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC) | $\theta_{JA}$ | +29.4°C/W |
| | $\theta_{JC}$ | +2.8°C/W |
| ESD Susceptibility | HBM[3] | ≥8 kV |
| | MM[4] | ≥250V |
| | CDM[5] | ≥1250V |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

## Recommended Operating Conditions

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Supply Voltage, $V_{DD}$ | 3.0 | 3.3 | 3.6 | V |
| Voltage at Any Bus Terminal (Separate or Common-Mode) | −1.4 | | +3.8 | V |
| Differential Input Voltage $V_{ID}$ | | | 2.4 | V |
| LVTTL Input Voltage High $V_{IH}$ | 2.0 | | $V_{DD}$ | V |
| LVTTL Input Voltage Low $V_{IL}$ | 0 | | 0.8 | V |
| Operating Free Air Temperature $T_A$ | −40 | +25 | +85 | °C |

## DC Electrical Characteristics[1][2][3][4]

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **M-LVDS Driver** | | | | | | | |
| $\|V_{AB}\|$ | Differential output voltage magnitude | $R_L$ = 50Ω, $C_L$ = 5 pF | | 480 | | 650 | mV |
| $\Delta V_{AB}$ | Change in differential output voltage magnitude between logic states | Figure 2<br>Figure 4 | | −50 | 0 | +50 | mV |
| $V_{OS(SS)}$ | Steady-state common-mode output voltage | $R_L$ = 50Ω, $C_L$ = 5 pF | | 0.3 | 1.6 | 2.1 | V |
| $\|\Delta V_{OS(SS)}\|$ | Change in steady-state common-mode output voltage between logic states | Figure 2<br>Figure 3 | | 0 | | +50 | mV |
| $V_{A(OC)}$ | Maximum steady-state open-circuit output voltage | Figure 5 | | 0 | | 2.4 | V |
| $V_{B(OC)}$ | Maximum steady-state open-circuit output voltage | | | 0 | | 2.4 | V |
| $V_{P(H)}$ | Voltage overshoot, low-to-high level output[5] | $R_L$ = 50Ω, $C_L$ = 5pF,$C_D$ = 0.5 pF<br>Figure 7<br>Figure 8 | | | | $1.2V_{SS}$ | V |
| $V_{P(L)}$ | Voltage overshoot, high-to-low level output[5] | | | $-0.2V_{SS}$ | | | V |
| $I_{IH}$ | High-level input current (LVTTL inputs) | $V_{IH}$ = 3.6V | | -15 | | 15 | µA |
| $I_{IL}$ | Low-level input current (LVTTL inputs) | $V_{IL}$ = 0.0V | | -15 | | 15 | µA |
| $V_{CL}$ | Input Clamp Voltage (LVTTL inputs) | $I_{IN}$ = -18 mA | | -1.5 | | | V |
| $I_{OS}$ | Differential short-circuit output current[6] | Figure 6 | | -43 | | 43 | mA |
| **M-LVDS Receiver** | | | | | | | |
| $V_{IT+}$ | Positive-going differential input voltage threshold | See Truth Tables | Type 1 | | 16 | 50 | mV |
| | | | Type 2 | | 100 | 150 | mV |
| $V_{IT-}$ | Negative-going differential input voltage threshold | See Truth Tables | Type 1 | −50 | 20 | | mV |
| | | | Type 2 | 50 | 94 | | mV |
| $V_{OH}$ | High-level output voltage (LVTTL output) | $I_{OH}$ = −8mA | | 2.4 | 2.7 | | V |
| $V_{OL}$ | Low-level output voltage (LVTTL output) | $I_{OL}$ = 8mA | | | 0.28 | 0.4 | V |
| $I_{OZ}$ | TRI-STATE output current | $V_O$ = 0V or 3.6V | | −10 | | 10 | µA |
| $I_{OSR}$ | Short-circuit receiver output current (LVTTL output) | $V_O$ = 0V | | | -50 | -90 | mA |

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except $V_{OD}$ and $\Delta V_{OD}$.
(3) Typical values represent most likely parametric norms for $V_{DD}$ = +3.3V and $T_A$ = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not specified.
(4) $C_L$ includes fixture capacitance and $C_D$ includes probe capacitance.
(5) Specification is ensured by characterization and is not tested in production.
(6) Output short circuit current ($I_{OS}$) is specified as magnitude only, minus sign indicates direction only.

## DC Electrical Characteristics[1][2][3][4] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **M-LVDS Bus (Input and Output) Pins** | | | | | | |
| $I_A$ | Transceiver input/output current | $V_A$ = 3.8V, $V_B$ = 1.2V | | | 32 | µA |
| | | $V_A$ = 0V or 2.4V, $V_B$ = 1.2V | −20 | | +20 | µA |
| | | $V_A$ = −1.4V, $V_B$ = 1.2V | −32 | | | µA |
| $I_B$ | Transceiver input/output current | $V_B$ = 3.8V, $V_A$ = 1.2V | | | 32 | µA |
| | | $V_B$ = 0V or 2.4V, $V_A$ = 1.2V | −20 | | +20 | µA |
| | | $V_B$ = −1.4V, $V_A$ = 1.2V | −32 | | | µA |
| $I_{AB}$ | Transceiver input/output differential current ($I_A$ − $I_B$) | $V_A$ = $V_B$, −1.4V ≤ V ≤ 3.8V | −4 | | +4 | µA |
| $I_{A(OFF)}$ | Transceiver input/output power-off current | $V_A$ = 3.8V, $V_B$ = 1.2V, DE = 0V, 0V ≤ $V_{DD}$ ≤ 1.5V | | | 32 | µA |
| | | $V_A$ = 0V or 2.4V, $V_B$ = 1.2V, DE = 0V, 0V ≤ $V_{DD}$ ≤ 1.5V | −20 | | +20 | µA |
| | | $V_A$ = −1.4V, $V_B$ = 1.2V, DE = 0V, 0V ≤ $V_{DD}$ ≤ 1.5V | −32 | | | µA |
| $I_{B(OFF)}$ | Transceiver input/output power-off current | $V_B$ = 3.8V, $V_A$ = 1.2V, DE = 0V, 0V ≤ $V_{DD}$ ≤ 1.5V | | | 32 | µA |
| | | $V_B$ = 0V or 2.4V, $V_A$ = 1.2V, DE = 0V, 0V ≤ $V_{DD}$ ≤ 1.5V | −20 | | +20 | µA |
| | | $V_B$ = −1.4V, $V_A$ = 1.2V, DE = 0V, 0V ≤ $V_{DD}$ ≤ 1.5V | −32 | | | µA |
| $I_{AB(OFF)}$ | Transceiver input/output power-off differential current ($I_{A(OFF)}$ − $I_{B(OFF)}$) | $V_A$ = $V_B$, −1.4V ≤ V ≤ 3.8V, DE = 0V, 0V ≤ $V_{DD}$ ≤ 1.5V | −4 | | +4 | µA |
| $C_A$ | Transceiver input/output capacitance | $V_{DD}$ = OPEN | | 7.8 | | pF |
| $C_B$ | Transceiver input/output capacitance | | | 7.8 | | pF |
| $C_{AB}$ | Transceiver input/output differential capacitance | | | 3 | | pF |
| $C_{A/B}$ | Transceiver input/output capacitance balance ($C_A$/$C_B$) | | | 1 | | |
| **SUPPLY CURRENT ($V_{CC}$)** | | | | | | |
| $I_{CCD}$ | Driver Supply Current | $R_L$ = 50Ω, DE = H, $\overline{RE}$ = H | | 67 | 75 | mA |
| $I_{CCZ}$ | TRI-STATE Supply Current | DE = L, $\overline{RE}$ = H | | 22 | 26 | mA |
| $I_{CCR}$ | Receiver Supply Current | DE = L, $\overline{RE}$ = L | | 32 | 38 | mA |
| $I_{CCPD}$ | Power Down Supply Current | MDE = L | | 3 | 5 | mA |

## Switching Characteristics[1][2][3]

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DRIVER AC SPECIFICATIONS** | | | | | | |
| $t_{PLH}$ | Differential Propagation Delay Low to High | $R_L$ = 50Ω, $C_L$ = 5 pF, | 1.5 | 3.3 | 5.5 | ns |
| $t_{PHL}$ | Differential Propagation Delay High to Low | $C_D$ = 0.5 pF | 1.5 | 3.3 | 5.5 | ns |
| $t_{SKD1}$ | Pulse Skew[4][5] | Figure 7<br>Figure 8 | | 30 | 125 | ps |
| $t_{SKD2}$ | Channel-to-Channel Skew[4][6] | | | 100 | 200 | ps |
| $t_{SKD3}$ | Part-to-Part Skew[4][7] | | | 0.8 | 1.6 | ns |
| $t_{SKD4}$ | Part-to-Part Skew[4][8] | | | | 4 | ns |
| $t_{TLH}$ | Rise Time[4] | | 1.2 | 2.0 | 3.0 | ns |
| $t_{THL}$ | Fall Time[4] | | 1.2 | 2.0 | 3.0 | ns |
| $t_{PZH}$ | Enable Time (Z to Active High) | $R_L$ = 50Ω, $C_L$ = 5 pF, | | 7.5 | 11.5 | ns |
| $t_{PZL}$ | Enable Time (Z to Active Low ) | $C_D$ = 0.5 pF | | 8.0 | 11.5 | ns |
| $t_{PLZ}$ | Disable Time (Active Low to Z) | Figure 9<br>Figure 10 | | 7.0 | 11.5 | ns |
| $t_{PHZ}$ | Disable Time (Active High to Z) | | | 7.0 | 11.5 | ns |
| **RECEIVER AC SPECIFICATIONS** | | | | | | |
| $t_{PLH}$ | Propagation Delay Low to High | $C_L$ = 15 pF | 1.5 | 3.0 | 4.5 | ns |
| $t_{PHL}$ | Propagation Delay High to Low | Figure 11<br>Figure 12<br>Figure 13 | 1.5 | 3.1 | 4.5 | ns |
| $t_{SKD1A}$ | Pulse Skew (Receiver Type 1)[4][5] | | | 55 | 325 | ps |
| $t_{SKD1B}$ | Pulse Skew (Receiver Type 2)[4][5] | | | 475 | 800 | ps |
| $t_{SKD2}$ | Channel-to-Channel Skew[4][6] | | | 60 | 300 | ps |
| $t_{SKD3}$ | Part-to-Part Skew[4][7] | | | 0.6 | 1.2 | ns |
| $t_{SKD4}$ | Part-to-Part Skew[8] | | | | 3 | ns |
| $t_{TLH}$ | Rise Time[4] | | 0.3 | 1.1 | 1.6 | ns |
| $t_{THL}$ | Fall Time[4] | | 0.3 | 0.65 | 1.6 | ns |
| $t_{PZH}$ | Enable Time (Z to Active High) | $R_L$ = 500Ω, $C_L$ = 15 pF | | 3 | 5.5 | ns |
| $t_{PZL}$ | Enable Time (Z to Active Low) | Figure 14<br>Figure 15 | | 3 | 5.5 | ns |
| $t_{PLZ}$ | Disable Time (Active Low to Z) | | | 3.5 | 5.5 | ns |
| $t_{PHZ}$ | Disable Time (Active High to Z) | | | 3.5 | 5.5 | ns |
| **GENERIC AC SPECIFICATIONS** | | | | | | |
| $t_{WKUP}$ | Wake Up Time[4]<br>(Master Device Enable (MDE) time) | | | | 500 | ms |
| $f_{MAX}$ | Maximum Operating Frequency[4] | | 125 | | | MHz |

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms for $V_{DD}$ = +3.3V and $T_A$ = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not specified.
(3) $C_L$ includes fixture capacitance and $C_D$ includes probe capacitance.
(4) Specification is ensured by characterization and is not tested in production.
(5) $t_{SKD1}$, $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(6) $t_{SKD2}$, Channel-to-Channel Skew, is the difference in propagation delay ($t_{PLHD}$ or $t_{PHLD}$) among all output channels.
(7) $t_{SKD3}$, Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same $V_{DD}$ and within 5°C of each other within the operating temperature range.
(8) $t_{SKD4}$, Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{SKD4}$ is defined as |Max − Min| differential propagation delay.

## Test Circuits and Waveforms

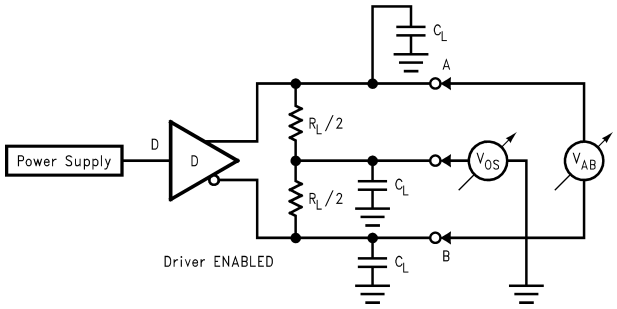



**Figure 2. Differential Driver Test Circuit**

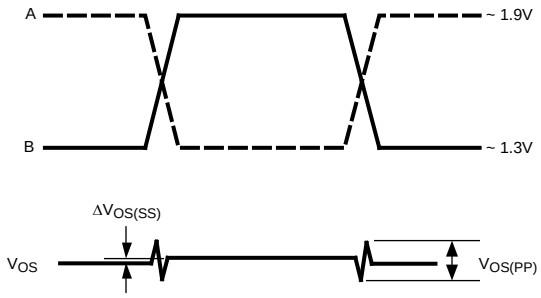



**Figure 3. Differential Driver Waveforms**

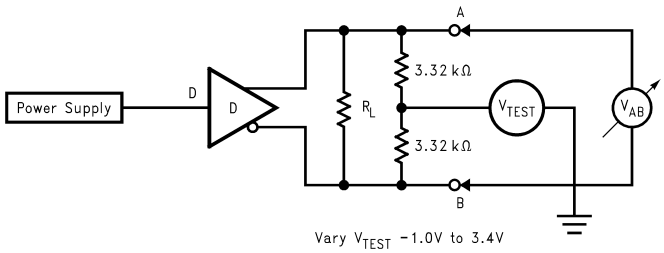



**Figure 4. Differential Driver Full Load Test Circuit**

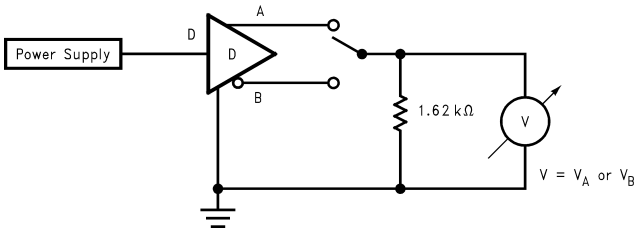



**Figure 5. Differential Driver DC Open Test Circuit**

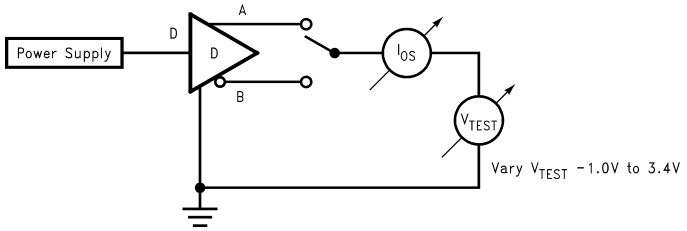



**Figure 6. Differential Driver Short-Circuit Test Circuit**

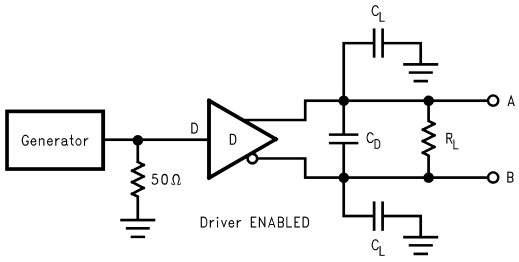



**Figure 7. Driver Propagation Delay and Transition Time Test Circuit**

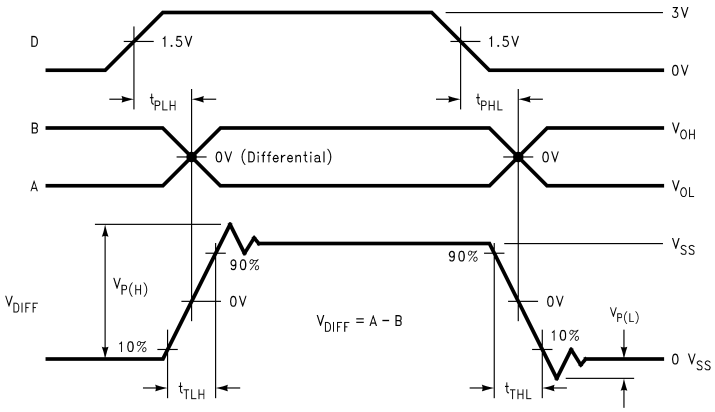



**Figure 8. Driver Propagation Delays and Transition Time Waveforms**

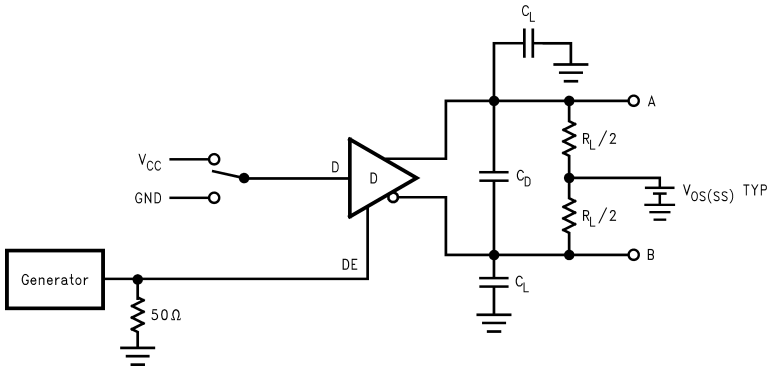



**Figure 9. Driver TRI-STATE Delay Test Circuit**

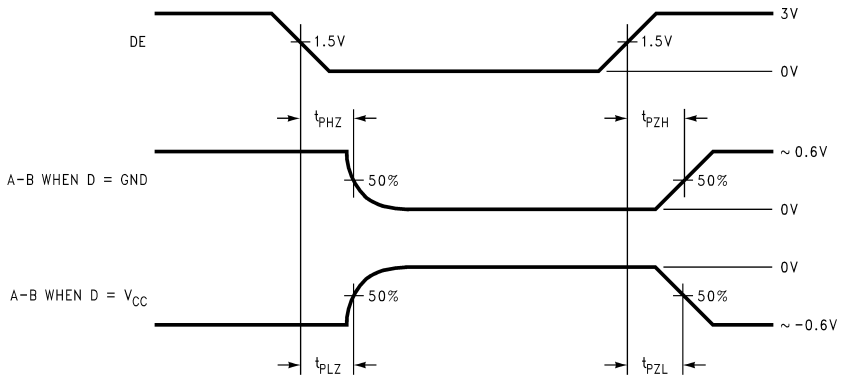



**Figure 10. Driver TRI-STATE Delay Waveforms**

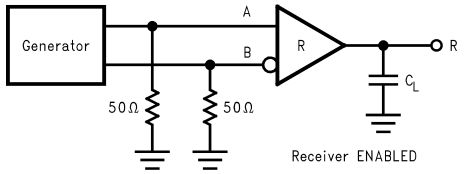



**Figure 11. Receiver Propagation Delay and Transition Time Test Circuit**

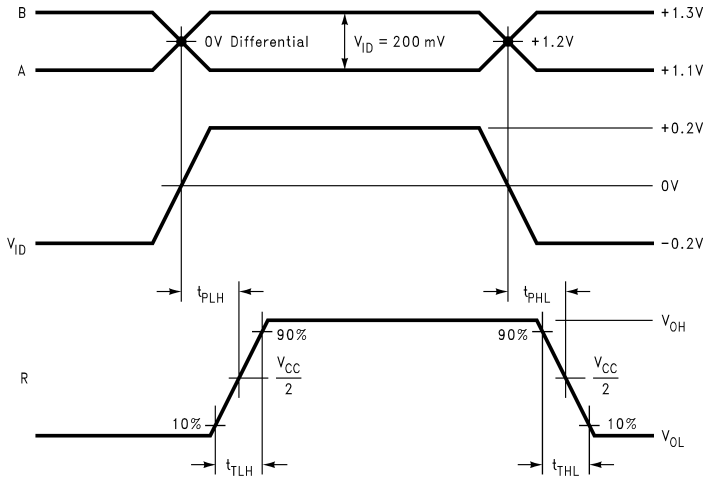



**Figure 12. Type 1 Receiver Propagation Delay and Transition Time Waveforms**

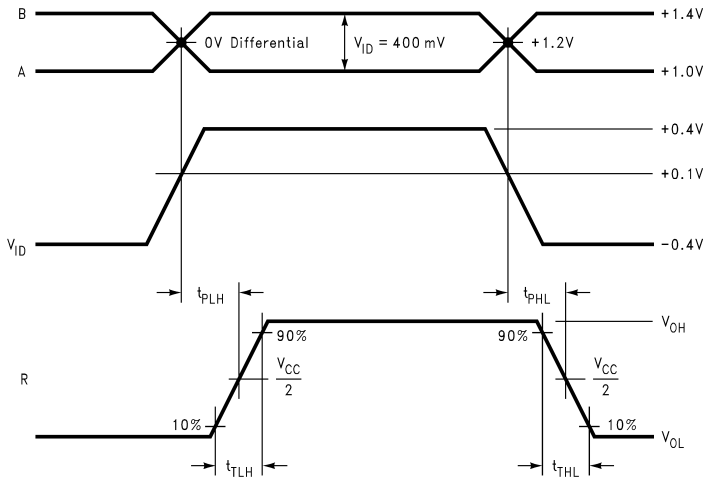



**Figure 13. Type 2 Receiver Propagation Delay and Transition Time Waveforms**

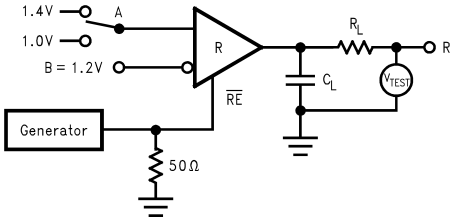



**Figure 14. Receiver TRI-STATE Delay Test Circuit**

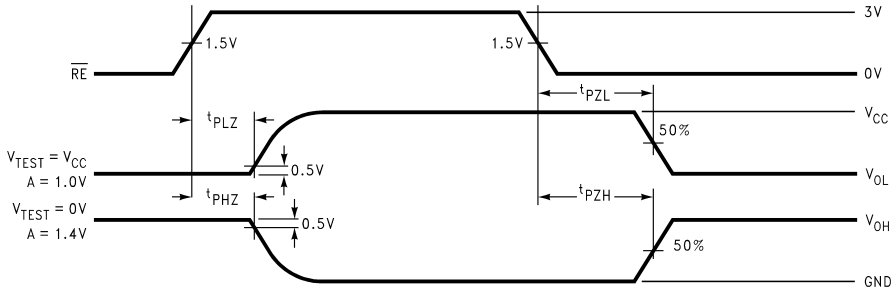



**Figure 15. Receiver TRI-STATE Delay Waveforms**

## TRUTH TABLES

### DS91M040 Transmitting[1]

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{RE}$ | DE | DI | B | A |
| X | H | H | L | H |
| X | H | L | H | L |
| X | L | X | Z | Z |

(1) X — Don't care condition
Z — High impedance state

## DS91M040 as Type 1 Receiving(1)

| Inputs | | | | Output |
|---|---|---|---|---|
| FSEN | $\overline{RE}$ | DE | A − B | RO |
| L | L | X | ≥ +0.05V | H |
| L | L | X | ≤ −0.05V | L |
| L | L | X | −0.05V ≤ A-B ≤ +0.05V | Undefined |
| L | H | X | X | Z |

(1) X — Don't care condition
Z — High impedance state

## DS91M040 as Type 2 Receiving(1)

| Inputs | | | | Output |
|---|---|---|---|---|
| FSEN | $\overline{RE}$ | DE | A − B | RO |
| H | L | X | ≥ +0.15V | H |
| H | L | X | ≤ +0.05V | L |
| H | L | X | +0.05V ≤ A-B ≤ +0.15V | Undefined |
| H | H | X | X | Z |

(1) X — Don't care condition
Z — High impedance state

## DS91M040 Type 1 Receiver Input Threshold Test Voltages(1)

| Applied Voltages | | Resulting Differential Input Voltage | Resulting Common-Mode Input Voltage | Receiver Output |
|---|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{ICM}$ | R |
| 2.400V | 0.000V | 2.400V | 1.200V | H |
| 0.000V | 2.400V | −2.400V | 1.200V | L |
| 3.800V | 3.750V | 0.050V | 3.775V | H |
| 3.750V | 3.800V | −0.050V | 3.775V | L |
| −1.350V | −1.400V | 0.050V | −1.375V | H |
| −1.400V | −1.350V | −0.050V | −1.375V | L |

(1) H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

## DS91M040 Type 2 Receiver Input Threshold Test Voltages(1)

| Applied Voltages | | Resulting Differential Input Voltage | Resulting Common-Mode Input Voltage | Receiver Output |
|---|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ | R |
| 2.400V | 0.000V | 2.400V | 1.200V | H |
| 0.000V | 2.400V | −2.400V | 1.200V | L |
| 3.800V | 3.650V | 0.150V | 3.725V | H |
| 3.800V | 3.750V | 0.050V | 3.775V | L |
| −1.250V | −1.400V | 0.150V | −1.325V | H |
| −1.350V | −1.400V | 0.050V | −1.375V | L |

(1) H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

## Typical Performance Characteristics

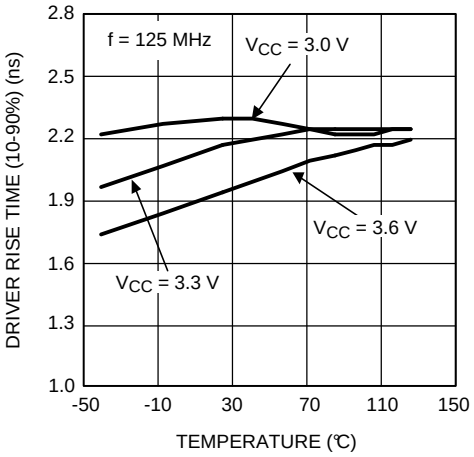



**Figure 16. Driver Rise Time as a Function of Temperature**

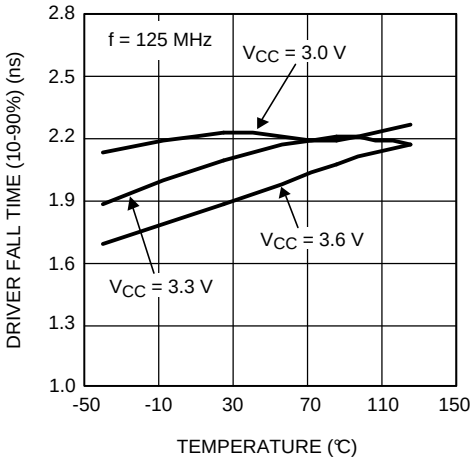



**Figure 17. Driver Fall Time as a Function of Temperature**

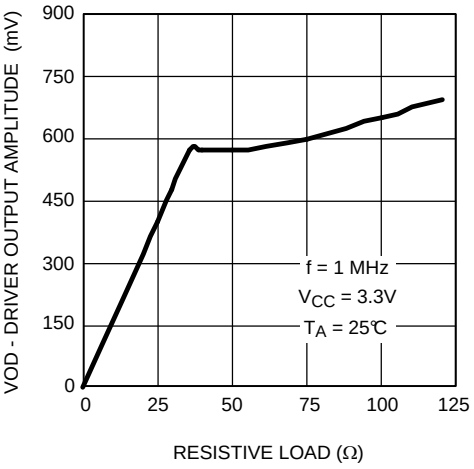



**Figure 18. Driver Output Signal Amplitude as a Function of Resistive Load**

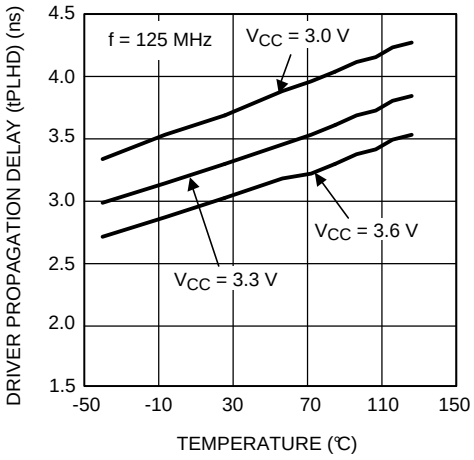



**Figure 19. Driver Propagation Delay (tPLHD) as a Function of Temperature**

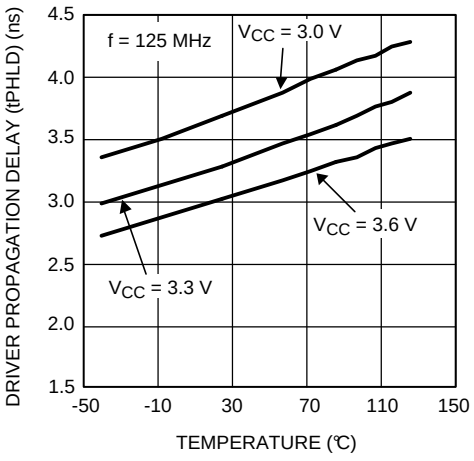



**Figure 20. Driver Propagation Delay (tPHLD) as a Function of Temperature**

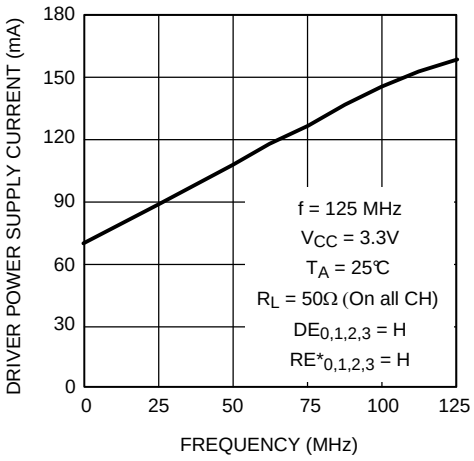



**Figure 21. Driver Power Supply Current as a Function of Frequency**

## Typical Performance Characteristics (continued)

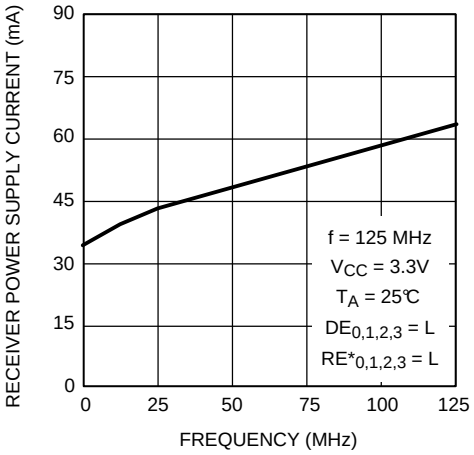



**Figure 22. Receiver Power Supply Current as a Function of Frequency**

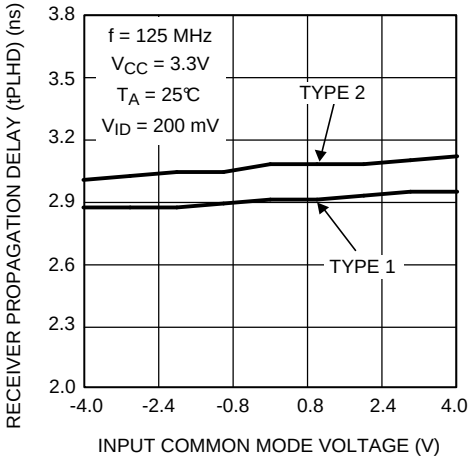



**Figure 23. Receiver Propagation Delay (tPLHD) as a Function of Input Common Mode Voltage**

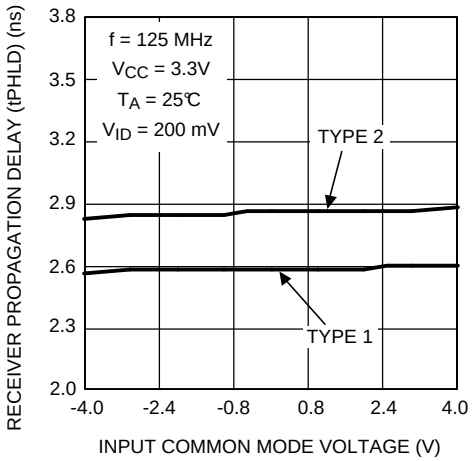



**Figure 24. Receiver Propagation Delay (tPHLD) as a Function of Input Common Mode Voltage**

## REVISION HISTORY

| Changes from Revision L (April 2013) to Revision M | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 14 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DS91M040TSQ/NOPB | ACTIVE | WQFN | RTV | 32 | 1000 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | M040TS | Samples |
| DS91M040TSQE/NOPB | ACTIVE | WQFN | RTV | 32 | 250 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | M040TS | Samples |
| DS91M040TSQX/NOPB | ACTIVE | WQFN | RTV | 32 | 4500 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | M040TS | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

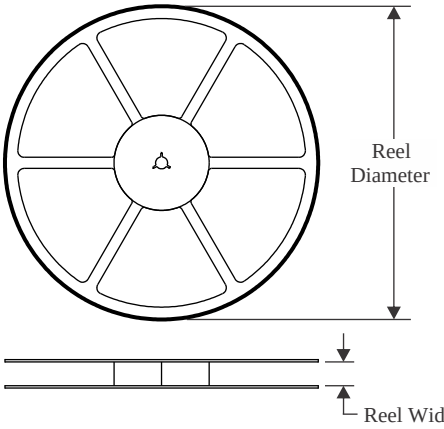
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

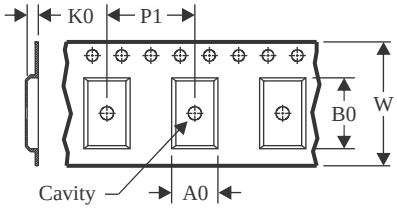
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

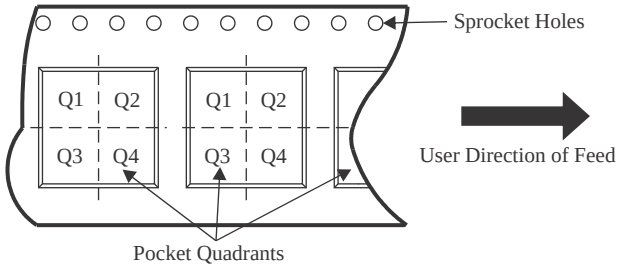



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

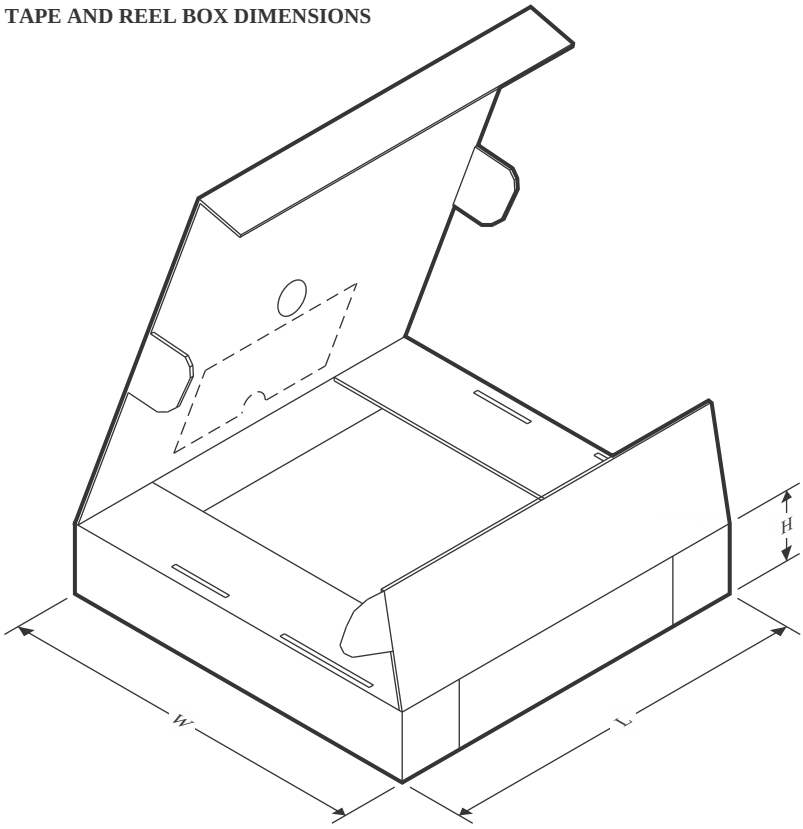
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS91M040TSQ/NOPB | WQFN | RTV | 32 | 1000 | 178.0 | 12.4 | 5.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| DS91M040TSQE/NOPB | WQFN | RTV | 32 | 250 | 178.0 | 12.4 | 5.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| DS91M040TSQX/NOPB | WQFN | RTV | 32 | 4500 | 330.0 | 12.4 | 5.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

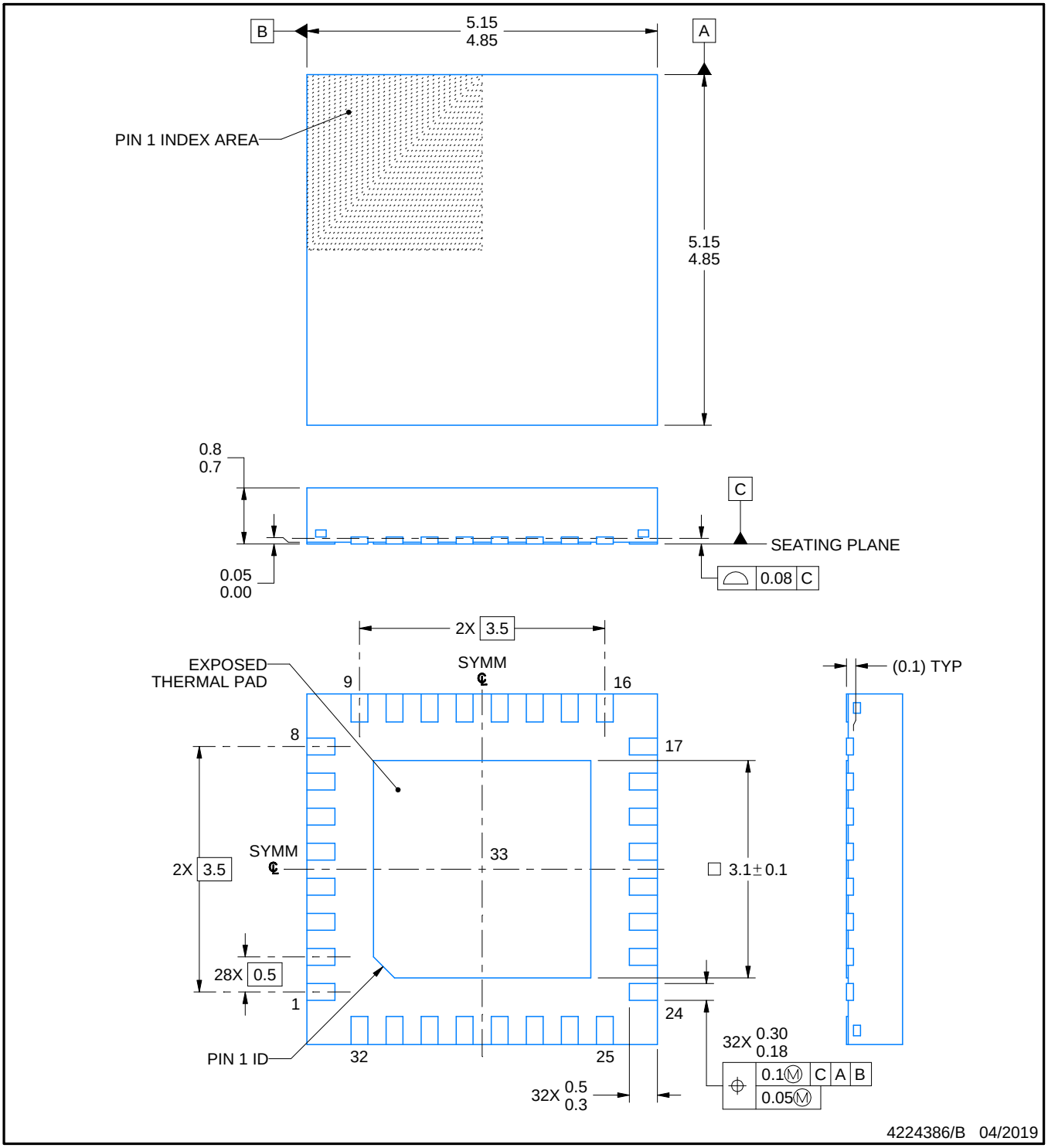
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS91M040TSQ/NOPB | WQFN | RTV | 32 | 1000 | 208.0 | 191.0 | 35.0 |
| DS91M040TSQE/NOPB | WQFN | RTV | 32 | 250 | 208.0 | 191.0 | 35.0 |
| DS91M040TSQX/NOPB | WQFN | RTV | 32 | 4500 | 356.0 | 356.0 | 36.0 |

# PACKAGE OUTLINE

## RTV0032A

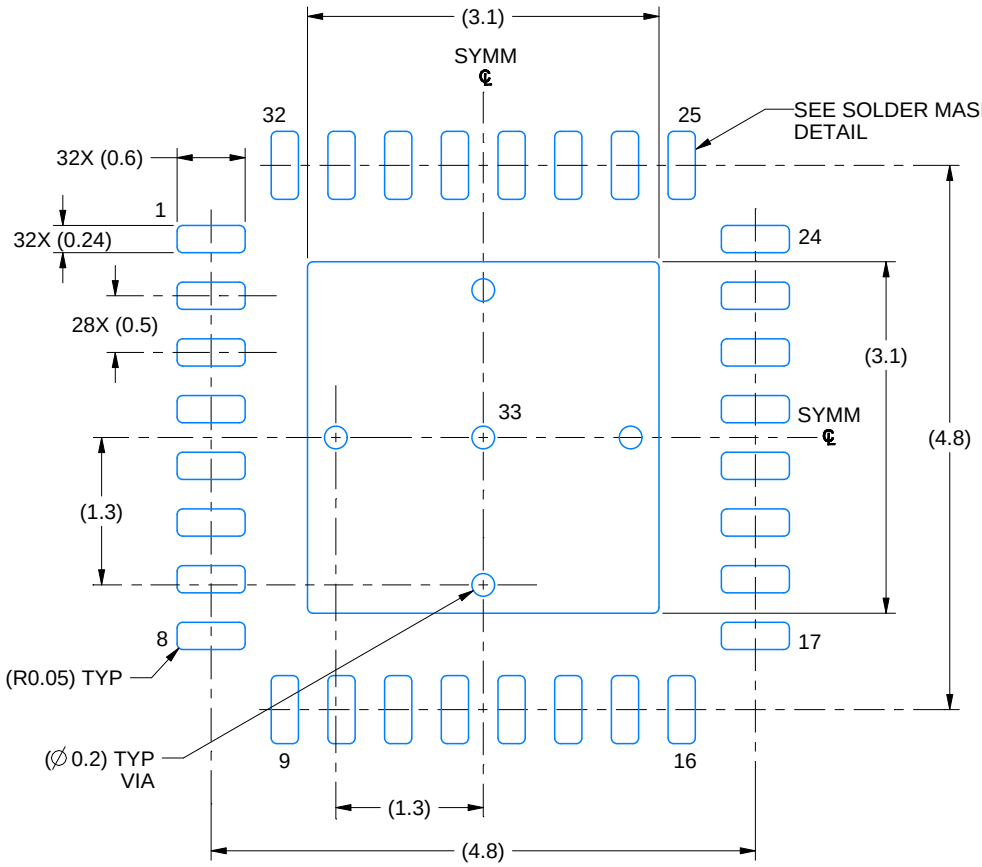
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

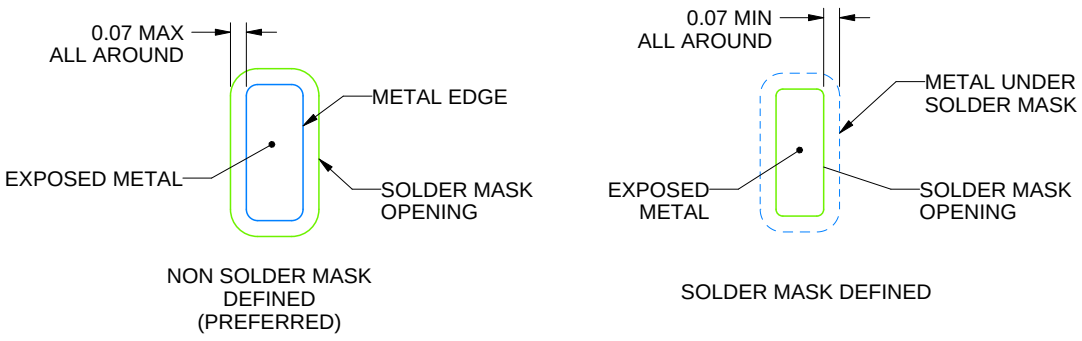



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

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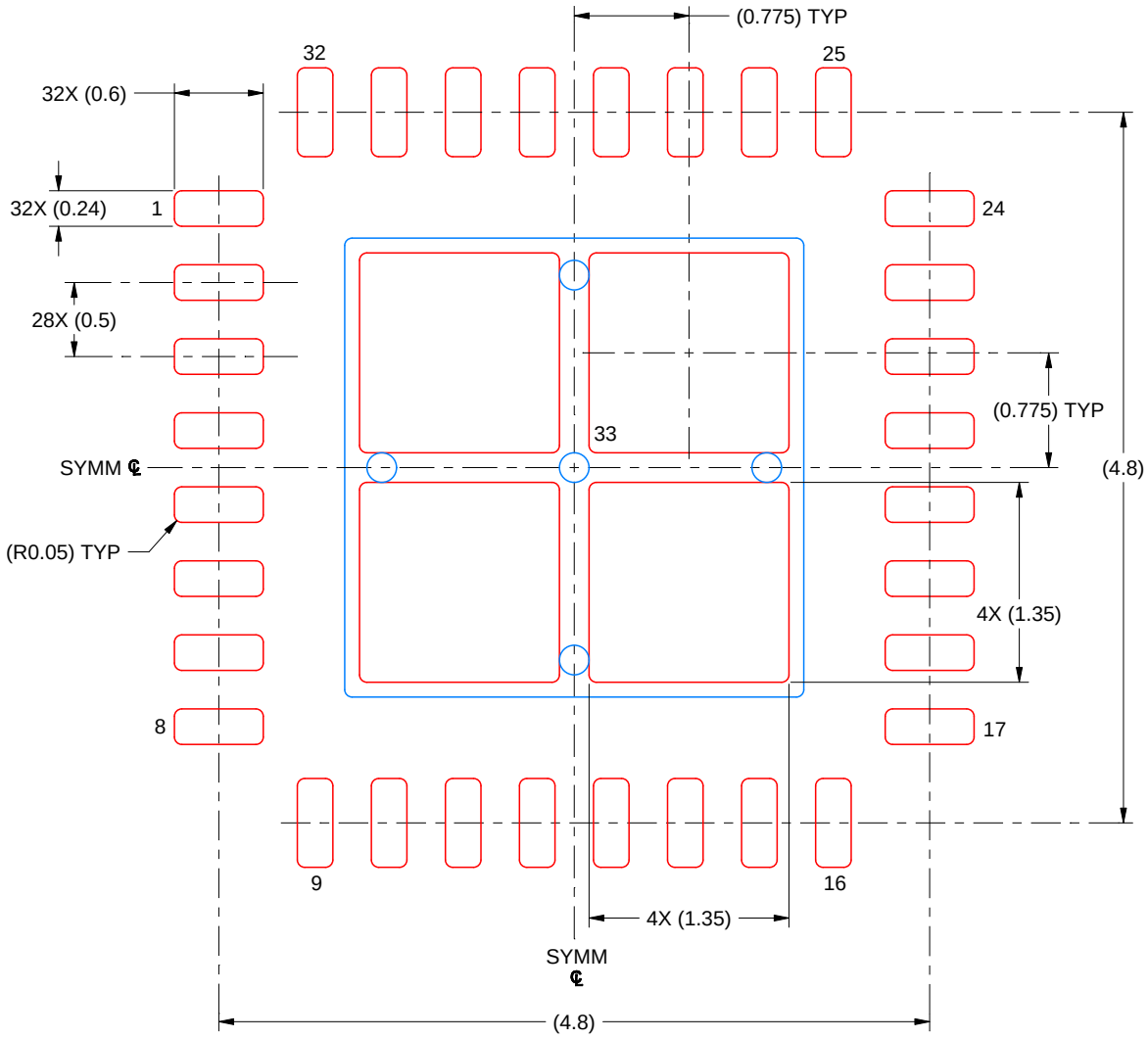
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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