

## FDC2x1x-Q1 适用于电容式感应应用的多通道、高分辨率、电容数字转换器

### 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 +125°C 环境温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C5
- 抗 EMI 架构
- 最大输出速率（一个运行通道）：
  - 13.3kSPS (FDC2112-Q1、FDC2114-Q1)
  - 4.08kSPS (FDC2212-Q1、FDC2214-Q1)
- 最大输入电容：250nF（在 10kHz 下，使用 1mH 电感器）
- 传感器激励频率：10kHz 至 10MHz
- 通道数量：2、4
- 分辨率：高达 28 位
- RMS 噪声：在 100SPS 和  $f_{\text{SENSOR}} = 5\text{MHz}$  时为 0.3fF
- 电源电压：2.7V 至 3.6V
- 功耗：（运行）2.1mA
- 低功耗睡眠模式：35 $\mu$ A
- 关断：200nA
- 接口：I<sup>2</sup>C
- 温度范围：-40°C 至 +125°C

### 2 应用

- 接近传感器
- 手势识别
- 汽车车门/脚踢传感器
- 导电液体液位传感器

### 3 说明

电容式感应是一种具有低功耗、高分辨率的非接触式感应技术，适用于接近检测和手势识别等各类应用。电容式感应系统中的传感器可以采用任意金属或导体，因此可实现高度灵活的系统设计。

电容式感应应用灵敏度的主要限制因素在于传感器的噪声敏感性。FDC2x1x-Q1 采用谐振感应架构，即使在荧光环境中也能使性能保持不变。

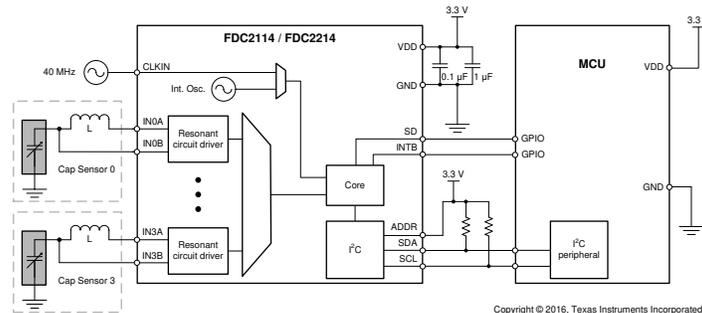
FDC2x1x-Q1 是多通道系列高分辨率、高速电容数字转换器，用于实施电容式感应解决方案。该系列器件采用基于窄带的创新型架构，可对噪声进行高度抑制，同时在高速条件下提供高分辨率。该系列器件支持宽激励频率范围，可为系统设计带来灵活性。

#### 封装信息

| 器件型号       | 封装 <sup>(1)</sup> | 封装尺寸 <sup>(2)</sup> |
|------------|-------------------|---------------------|
| FDC2112-Q1 | DNT (WSON, 12)    | 4mm × 4mm           |
| FDC2114-Q1 | RGH (WQFN, 16)    | 4mm × 4mm           |
| FDC2212-Q1 | DNT (WSON, 12)    | 4mm × 4mm           |
| FDC2214-Q1 | RGH (WQFN, 16)    | 4mm × 4mm           |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化原理图



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## 4 Pin Configuration and Functions

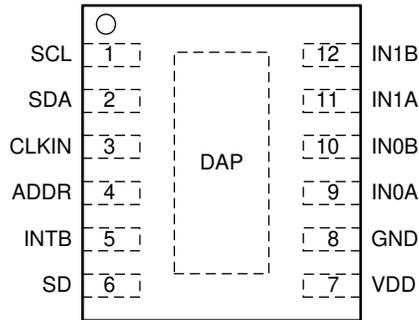


图 4-1. FDC2112/FDC2212 DNT Package 12-Pin WSON Top View

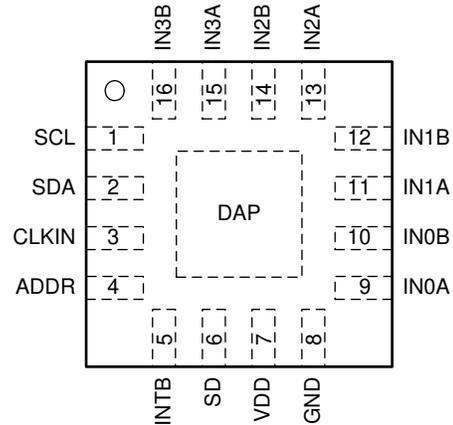


图 4-2. FDC2114/FDC2214 RGH Package 16-Pin WQFN Top View

表 4-1. Pin Functions

| PIN |                    | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-----|--------------------|---------------------|---|
| NO. | NAME               |                     |   |
| 1   | SCL                | I                   | I <sup>2</sup> C clock input  |
| 2   | SDA                | I/O                 | I <sup>2</sup> C data input/output  |
| 3   | CLKIN              | I                   | Controller Clock input. Tie this pin to GND if internal oscillator is selected  |
| 4   | ADDR               | I                   | I <sup>2</sup> C Address selection pin: when ADDR=L, I <sup>2</sup> C address = 0x2A, when ADDR=H, I <sup>2</sup> C address = 0x2B. |
| 5   | INTB               | O                   | Configurable Interrupt output pin   |
| 6   | SD                 | I                   | Shutdown input  |
| 7   | VDD                | P                   | Power Supply  |
| 8   | GND                | G                   | Ground  |
| 9   | IN0A               | A                   | Capacitive sensor input 0   |
| 10  | IN0B               | A                   | Capacitive sensor input 0   |
| 11  | IN1A               | A                   | Capacitive sensor input 1   |
| 12  | IN1B               | A                   | Capacitive sensor input 1   |
| 13  | IN2A               | A                   | Capacitive sensor input 2 (FDC2114 / FDC2214 only)  |
| 14  | IN2B               | A                   | Capacitive sensor input 2 (FDC2114 / FDC2214 only)  |
| 15  | IN3A               | A                   | Capacitive sensor input 3 (FDC2114 / FDC2214 only)  |
| 16  | IN3B               | A                   | Capacitive sensor input 3 (FDC2114 / FDC2214 only)  |
| DAP | DAP <sup>(2)</sup> | N/A                 | Connect to ground   |

(1) I = Input, O = Output, P=Power, G=Ground, A=Analog

(2) There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the GND pin of the device. Although the DAP can be left floating, connect the DAP to the same potential as the GND pin of the device for best performance. Do not use the DAP as the primary ground for the device. The device GND pin must always be connected to ground.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |  | MIN   | MAX       | UNIT |
|------------------|--|-------|-----------|------|
| VDD              | Supply voltage                           |       | 5         | V    |
| V <sub>i</sub>   | Voltage on any pin                       | - 0.3 | VDD + 0.3 | V    |
| I <sub>A</sub>   | Input current on any I <sub>Nx</sub> pin | - 8   | 8         | mA   |
| I <sub>D</sub>   | Input current on any digital pin         | - 5   | 5         | mA   |
| T <sub>J</sub>   | Junction temperature                     | - 55  | 150       | °C   |
| T <sub>stg</sub> | Storage temperature                      | - 65  | 150       | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

|                    |                         | VALUE   | UNIT  |
|--------------------|-------------------------|---|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2000 |
|                    |                         | Charged-device model (CDM), per AEC Q100-011            | ±750  |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

Unless otherwise specified, all limits ensured for T<sub>A</sub> = 25°C, VDD = 3.3V

|                |                       | MIN  | NOM | MAX | UNIT |
|----------------|-----------------------|------|-----|-----|------|
| VDD            | Supply voltage        | 2.7  |     | 3.6 | V    |
| T <sub>A</sub> | Operating temperature | - 40 |     | 125 | °C   |

### 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | FDC2112 / FDC2212 | FDC2214 / FDC2214 | UNIT |
|-------------------------------|--|-------------------|-------------------|------|
|                               |  | DNT (WSON)        | RGH (WQFN)        |      |
|                               |  | 12 PINS           | 16 PINS           |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 36.7              | 35.6              | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 36.2              | 36.2              | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 14                | 13.4              | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.4               | 0.4               | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 14.2              | 13.4              | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 3.5               | 3.5               | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}^{(1)}$

| PARAMETER                |  | TEST CONDITIONS <sup>(2)</sup>  | MIN <sup>(3)</sup> | TYP <sup>(4)</sup> | MAX <sup>(3)</sup> | UNIT          |
|--------------------------|--|---|--------------------|--------------------|--------------------|---------------|
| <b>POWER</b>             |  |   |                    |                    |                    |               |
| $V_{DD}$                 | Supply voltage   | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$                              | 2.7                |                    | 3.6                | V             |
| $I_{DD}$                 | Supply current (not including sensor current) <sup>(5)</sup> | CLKIN = 10MHz <sup>(6)</sup>  |                    | 2.1                |                    | mA            |
| $I_{DDSL}$               | Sleep mode supply current <sup>(5)</sup>                     |   |                    | 35                 | 60                 | $\mu\text{A}$ |
| $I_{SD}$                 | Shutdown mode supply current <sup>(5)</sup>                  |   |                    | 0.2                | 1                  | $\mu\text{A}$ |
| <b>CAPACITIVE SENSOR</b> |  |   |                    |                    |                    |               |
| $C_{\text{SENSORMAX}}$   | Maximum sensor capacitance                                   | 1-mH inductor, 10kHz oscillation  |                    | 250                |                    | nF            |
| $C_{\text{IN}}$          | Sensor pin parasitic capacitance                             |   |                    | 4                  |                    | pF            |
| $N_{\text{BITS}}$        | Number of bits   | FDC2112, FDC2114<br>RCOUNT $\geq$ 0x0400                                      |                    |                    | 12                 | bits          |
|                          |  | FDC2212, FDC2214<br>RCOUNT = 0xFFFF   |                    |                    | 28                 | bits          |
| $f_{\text{CS}}$          | Maximum channel sample rate                                  | FDC2112, FDC2114<br>single active channel continuous conversion, SCL = 400kHz |                    |                    | 13.3               | kSPS          |
|                          |  | FDC2212, FDC2214<br>single active channel continuous conversion, SCL = 400kHz |                    |                    | 4.08               | kSPS          |
| <b>EXCITATION</b>        |  |   |                    |                    |                    |               |
| $f_{\text{SENSOR}}$      | Sensor excitation frequency                                  | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$                              | 0.01               |                    | 10                 | MHz           |
| $V_{\text{SENSORMIN}}$   | Minimum sensor oscillation amplitude (pk) <sup>(7)</sup>     |   |                    | 1.2                |                    | V             |
| $V_{\text{SENSORMAX}}$   | Maximum sensor oscillation amplitude (pk)                    |   |                    | 1.8                |                    | V             |
| $I_{\text{SENSORMAX}}$   | Sensor maximum current drive                                 | HIGH_CURRENT_DRV = b0<br>DRIVE_CURRENT_CH0 = 0xF800                           |                    | 1.5                |                    | mA            |
|                          |  | HIGH_CURRENT_DRV = b1<br>DRIVE_CURRENT_CH0 = 0xF800<br>Channel 0 only         |                    | 6                  |                    | mA            |

Unless otherwise specified, all limits ensured for  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}^{(1)}$

| PARAMETER                         |   | TEST CONDITIONS <sup>(2)</sup>                   | MIN <sup>(3)</sup>         | TYP <sup>(4)</sup> | MAX <sup>(3)</sup> | UNIT                  |
|-----------------------------------|---|--|----------------------------|--------------------|--------------------|-----------------------|
| <b>CONTROLLER CLOCK</b>           |   |  |                            |                    |                    |                       |
| $f_{\text{CLKIN}}$                | External controller clock input frequency (CLKIN)               | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ | 2                          |                    | 40                 | MHz                   |
| $\text{CLKIN}_{\text{DUTY\_MIN}}$ | External controller clock minimum acceptable duty cycle (CLKIN) |  |                            | 40%                |                    |                       |
| $\text{CLKIN}_{\text{DUTY\_MAX}}$ | External controller clock maximum acceptable duty cycle (CLKIN) |  |                            | 60%                |                    |                       |
| $V_{\text{CLKIN\_LO}}$            | CLKIN low voltage threshold                                     |  |                            |                    | $0.3V_{\text{DD}}$ | V                     |
| $V_{\text{CLKIN\_HI}}$            | CLKIN high voltage threshold                                    |  | $0.7 \times V_{\text{DD}}$ |                    |                    | V                     |
| $f_{\text{INTCLK}}$               | Internal controller clock frequency range                       |  | 35                         | 43.4               | 55                 | MHz                   |
| $T_{\text{Cf\_int\_}\mu}$         | Internal controller clock temperature coefficient mean          |  |                            | - 13               |                    | ppm/ $^\circ\text{C}$ |

- (1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device can be permanently degraded, either mechanically or electrically.
- (2) Register values are represented as either binary (b is the prefix to the digits), or hexadecimal (0x is the prefix to the digits). Decimal values have no prefix.
- (3) Limits are specified by testing, design, or statistical analysis at  $25^\circ\text{C}$ . Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values can vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (5) I<sup>2</sup>C read/write communication and pullup resistors current through SCL, SDA not included.
- (6) Sensor capacitor: 1 layer,  $20.9 \times 13.9\text{mm}$ , Bourns CMH322522-180KL sensor inductor with  $L=18\mu\text{H}$  and  $33\text{pF}$  1% COG/NP0 Target: Grounded aluminum plate ( $176 \times 123\text{mm}$ ), Channel = Channel 0 (continuous mode)  $\text{CLKIN} = 40\text{MHz}$ ,  $\text{CHx\_FIN\_SEL} = \text{b}10$ ,  $\text{CHx\_FREF\_DIVIDER} = \text{b}00\ 0000\ 0001$   $\text{CH0\_RCOUNT} = 0\text{x}FFFF$ ,  $\text{SETTLECOUNT\_CH0} = 0\text{x}0100$ ,  $\text{DRIVE\_CURRENT\_CH0} = 0\text{x}7800$ .
- (7) Lower  $V_{\text{SENSORMIN}}$  oscillation amplitudes can be used, but will result in lower SNR.

## 5.6 Timing Requirements

|  |   | MIN | NOM | MAX  | UNIT          |
|--|---|-----|-----|------|---------------|
| $t_{\text{SDWAKEUP}}$                        | Wake-up time from SD high-low transition to I <sup>2</sup> C readback                       |     |     | 2    | ms            |
| $t_{\text{SLEEPWAKEUP}}$                     | Wake-up time from sleep mode  |     |     | 0.05 | ms            |
| $t_{\text{WD-TIMEOUT}}$                      | Sensor recovery time (after watchdog timeout)   |     | 5.2 |      | ms            |
| <b>I<sup>2</sup>C TIMING CHARACTERISTICS</b> |   |     |     |      |               |
| $f_{\text{SCL}}$                             | Clock frequency   | 10  |     | 400  | kHz           |
| $t_{\text{LOW}}$                             | Clock low time  | 1.3 |     |      | $\mu\text{s}$ |
| $t_{\text{HIGH}}$                            | Clock high time   | 0.6 |     |      | $\mu\text{s}$ |
| $t_{\text{HD;STA}}$                          | Hold time (repeated) START condition: after this period, the first clock pulse is generated | 0.6 |     |      | $\mu\text{s}$ |
| $t_{\text{SU;STA}}$                          | Setup time for a repeated START condition   | 0.6 |     |      | $\mu\text{s}$ |
| $t_{\text{HD;DAT}}$                          | Data hold time  | 0   |     |      | $\mu\text{s}$ |
| $t_{\text{SU;DAT}}$                          | Data setup time   | 100 |     |      | ns            |
| $t_{\text{SU;STO}}$                          | Setup time for STOP condition   | 0.6 |     |      | $\mu\text{s}$ |
| $t_{\text{BUF}}$                             | Bus free time between a STOP and START condition  | 1.3 |     |      | $\mu\text{s}$ |
| $t_{\text{VD;DAT}}$                          | Data valid time   |     |     | 0.9  | $\mu\text{s}$ |
| $t_{\text{VD;ACK}}$                          | Data valid acknowledge time   |     |     | 0.9  | $\mu\text{s}$ |

|                 |  | MIN | NOM | MAX | UNIT |
|-----------------|--|-----|-----|-----|------|
| t <sub>SP</sub> | Pulse width of spikes that must be suppressed by the input filter <sup>(1)</sup> |     |     | 50  | ns   |

## 5.7 Switching Characteristics - I<sup>2</sup>C

Unless otherwise specified, all limits ensured for T<sub>A</sub> = 25°C, V<sub>DD</sub> = 3.3V

| PARAMETER             | TEST CONDITIONS                       | MIN                   | TYP                   | MAX                   | UNIT |
|-----------------------|---------------------------------------|-----------------------|-----------------------|-----------------------|------|
| <b>VOLTAGE LEVELS</b> |                                       |                       |                       |                       |      |
| V <sub>IH</sub>       | Input high voltage                    | 0.7 × V <sub>DD</sub> |                       |                       | V    |
| V <sub>IL</sub>       | Input low voltage                     |                       |                       | 0.3 × V <sub>DD</sub> | V    |
| V <sub>OL</sub>       | Output low voltage (3mA sink current) |                       |                       | 0.4                   | V    |
| HYS                   | Hysteresis                            |                       | 0.1 × V <sub>DD</sub> |                       | V    |

(1) This parameter is specified by design and/or characterization and is not tested in production.

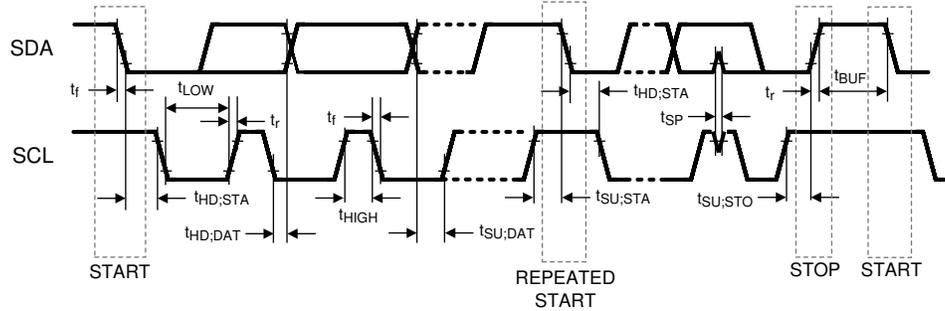
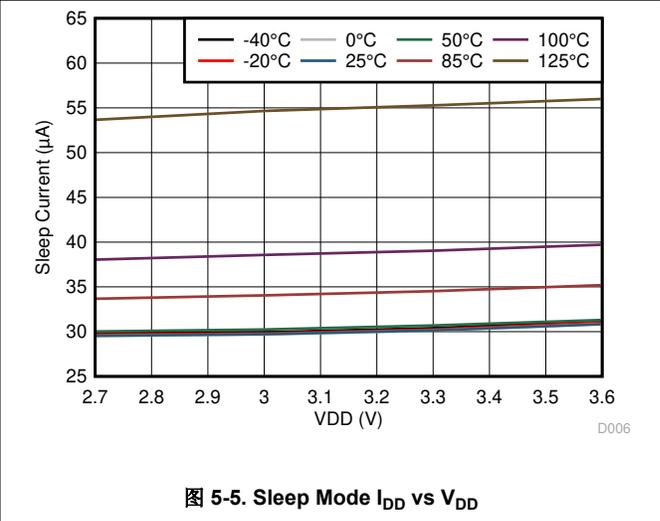
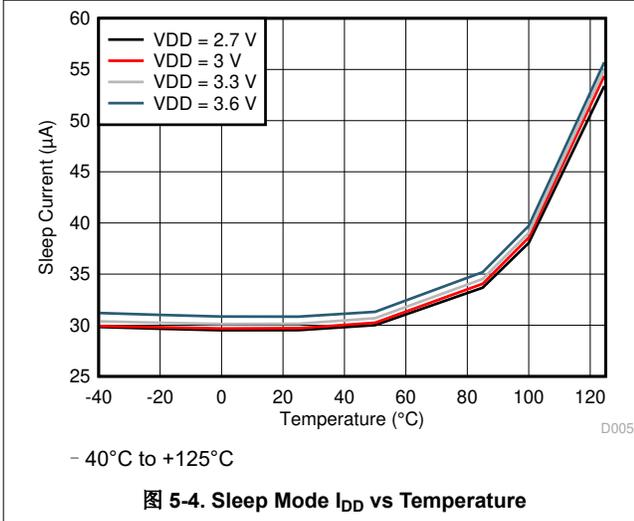
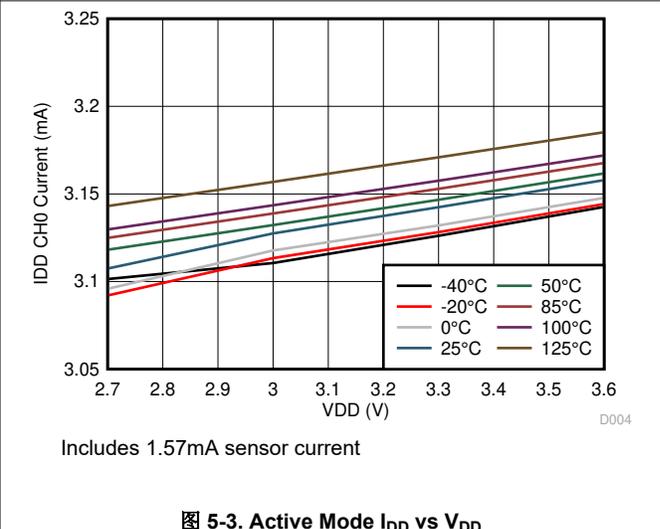
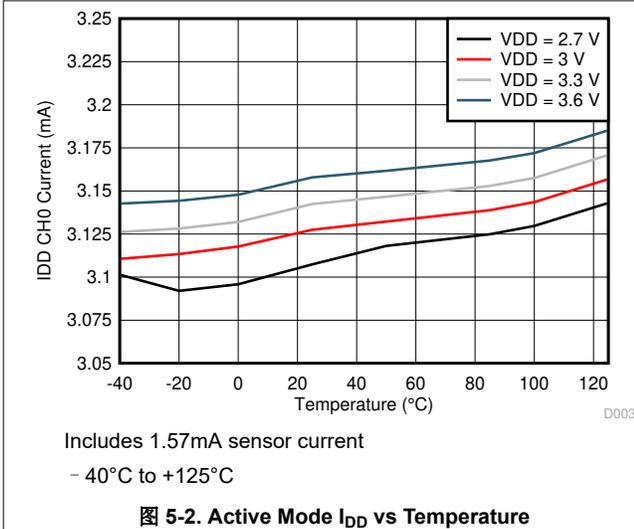


图 5-1. I<sup>2</sup>C Timing

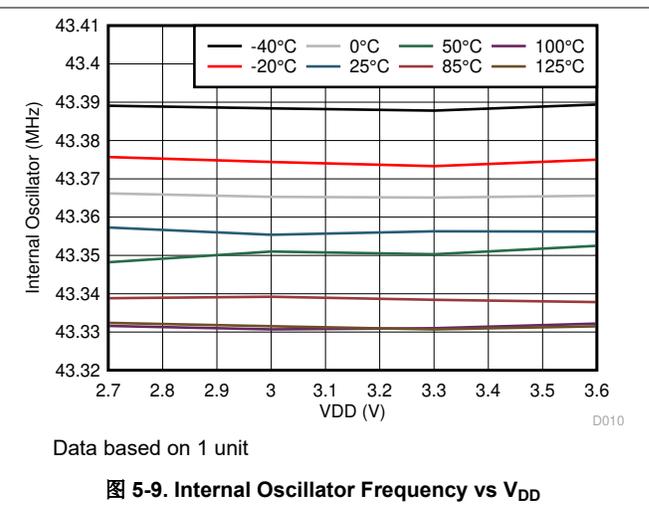
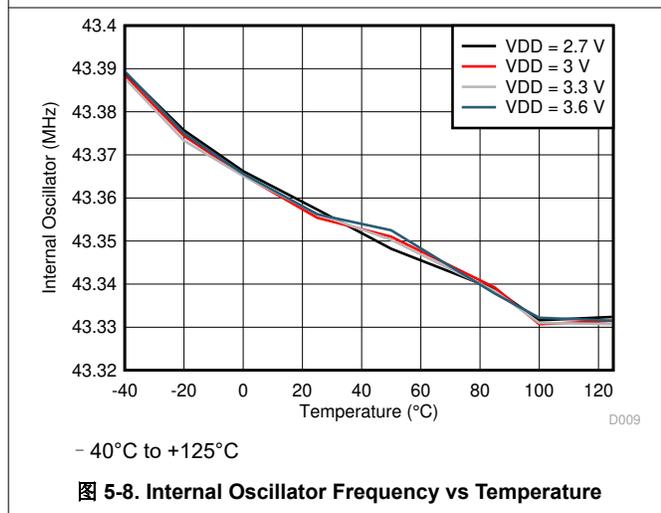
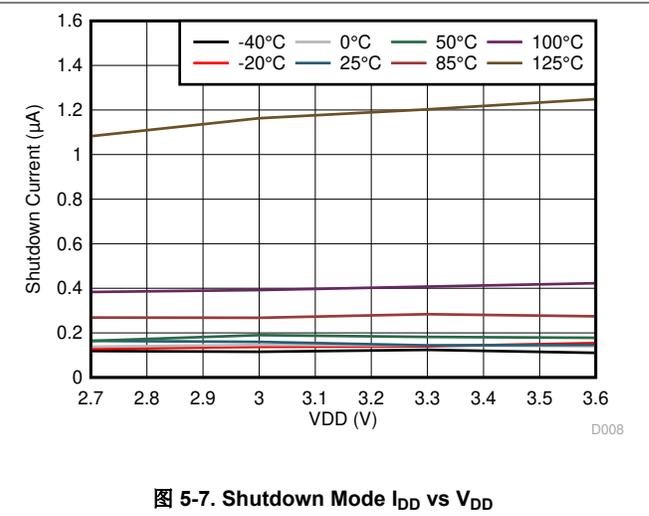
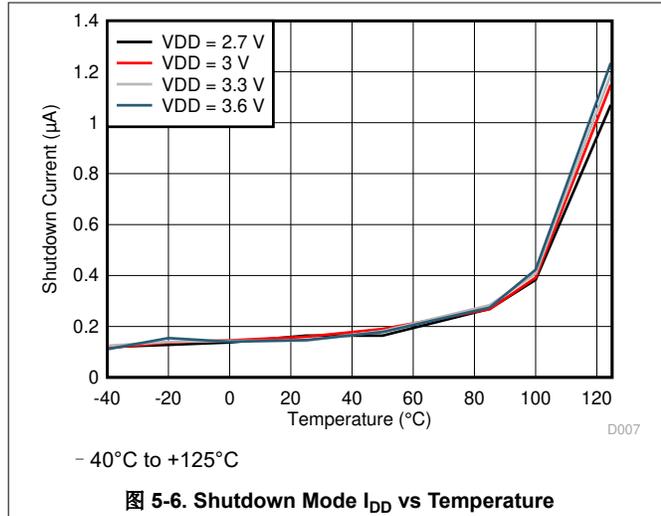
## 5.8 Typical Characteristics

Common test conditions (unless specified otherwise): Sensor capacitor: 1 layer, 20.9mm × 13.9mm, Bourns CMH322522-180KL sensor inductor with L = 18μH and 33pF 1% COG/NP0 Target: Grounded aluminum plate (176mm × 123mm), Channel = Channel 0 (continuous mode) CLKIN = 40MHz, CHx\_FIN\_SEL = b01, CHx\_FREF\_DIVIDER = b00 0000 0001 CH0\_RCOUNT = 0xFFFF, SETTLECOUNT\_CH0 = 0x0100, DRIVE\_CURRENT\_CH0 = 0x7800.



## 5.8 Typical Characteristics (continued)

*Common test conditions (unless specified otherwise):* Sensor capacitor: 1 layer, 20.9mm × 13.9mm, Bourns CMH322522-180KL sensor inductor with L = 18μH and 33pF 1% COG/NP0 Target: Grounded aluminum plate (176mm × 123mm), Channel = Channel 0 (continuous mode) CLKIN = 40MHz, CHx\_FIN\_SEL = b01, CHx\_FREF\_DIVIDER = b00 0000 0001 CH0\_RCOUNT = 0xFFFF, SETTLECOUNT\_CH0 = 0x0100, DRIVE\_CURRENT\_CH0 = 0x7800.



## 6 Detailed Description

### 6.1 Overview

The FDC2112, FDC2114, FDC2212, and FDC2214 are high-resolution, multichannel capacitance-to-digital converters for implementing capacitive sensing solutions. In contrast to traditional switched-capacitance architectures, the FDC2112, FDC2114, FDC2212, and FDC2214 employ an L-C resonator, also known as L-C tank, as a sensor. The narrow-band architecture allows unprecedented EMI immunity and greatly reduced noise floor when compared to other capacitive sensing solutions.

Using this approach, a change in capacitance of the L-C tank can be observed as a shift in the resonant frequency. Using this principle, the FDC is a capacitance-to-digital converter (FDC) that measures the oscillation frequency of an LC resonator. The device outputs a digital value that is proportional to frequency. This frequency measurement can be converted to an equivalent capacitance

### 6.2 Functional Block Diagrams

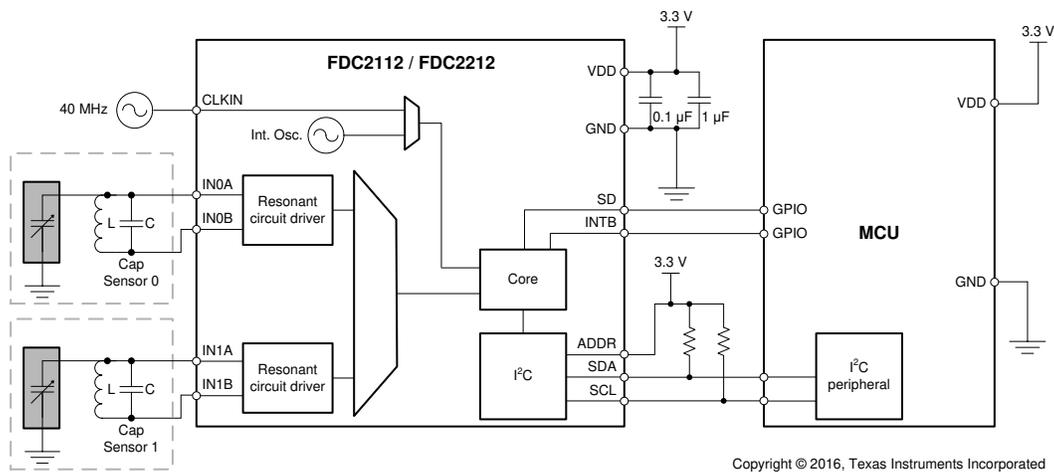


图 6-1. Block Diagram for the FDC2112 and FDC2212

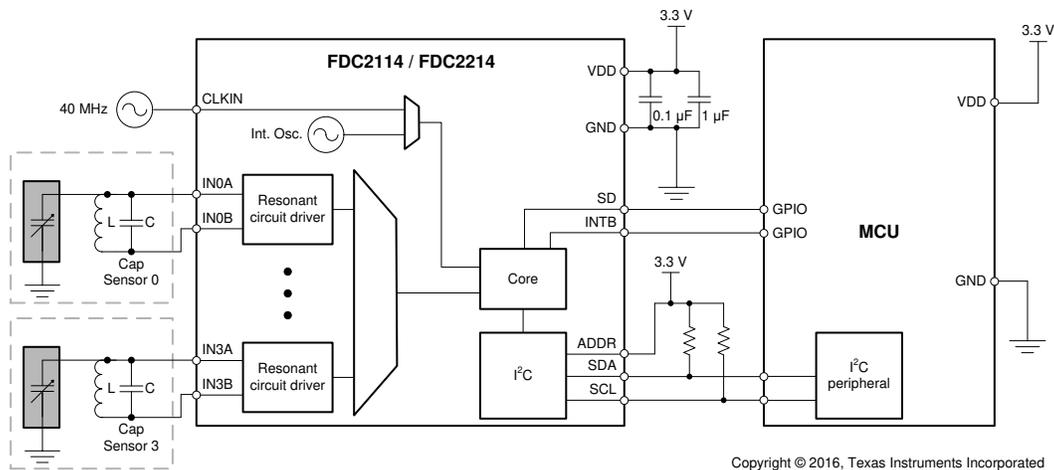


图 6-2. Block Diagram for the FDC2114 and FDC2214

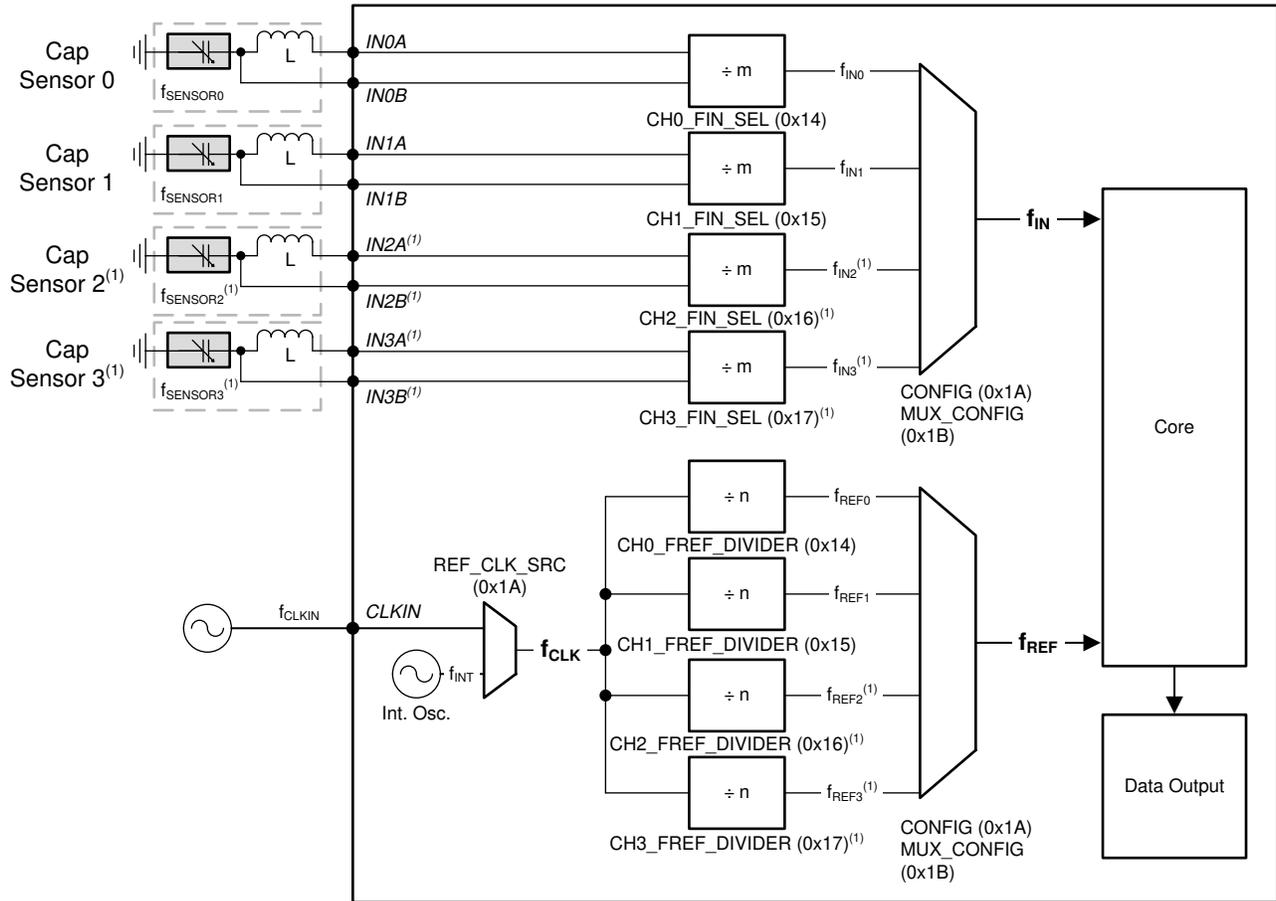
The FDC is composed of front-end resonant circuit drivers, followed by a multiplexer that sequences through the active channels, connecting them to the core that measures and digitizes the sensor frequency ( $f_{\text{SENSOR}}$ ). The core uses a reference frequency ( $f_{\text{REF}}$ ) to measure the sensor frequency.  $f_{\text{REF}}$  is derived from either an internal reference clock (oscillator), or an externally supplied clock. The digitized output for each channel is proportional to the ratio of  $f_{\text{SENSOR}}/f_{\text{REF}}$ . The I<sup>2</sup>C interface is used to support device configuration and to transmit the digitized

frequency values to a host processor. The FDC can be placed in shutdown mode, saving current, using the SD pin. The INTB pin may be configured to notify the host of changes in system status.

### 6.3 Feature Description

#### 6.3.1 Clocking Architecture

图 6-3 shows the clock dividers and multiplexers of the FDC.



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A. FDC2114 / FDC2214 only

图 6-3. Clocking Diagram

In 图 6-3, the key clocks are  $f_{IN}$ ,  $f_{REF}$ , and  $f_{CLK}$ .  $f_{CLK}$  is selected from either the internal clock source or external clock source (CLKIN). The frequency measurement reference clock,  $f_{REF}$ , is derived from the  $f_{CLK}$  source. TI recommends that precision applications use an external controller clock that offers the stability and accuracy requirements needed for the application. The internal oscillator may be used in applications that require low cost and do not require high precision. The  $f_{INx}$  clock is derived from sensor frequency for a channel  $x$ ,  $f_{SENSORx}$ .  $f_{REFx}$  and  $f_{INx}$  must meet the requirements listed in 表 6-1, depending on whether  $f_{CLK}$  (controller clock) is the internal or external clock.

表 6-1. Clock Configuration Requirements

| MODE <sup>(1)</sup> | CLKIN SOURCE                | VALID $f_{REFx}$ RANGE (MHz) | VALID $f_{INx}$ RANGE | SET CHx_FIN_SEL to <sup>(2)</sup>   | SET CHx_SETTLECO UNT to | SET CHx_RCOUNT to |
|---------------------|-----------------------------|------------------------------|-----------------------|---|-------------------------|-------------------|
| Multi-channel       | Internal                    | $f_{REFx} \leq 55$           | $< f_{REFx} / 4$      | Differential sensor configuration:<br>b01: 0.01MHz to 8.75MHz (divide by 1)<br>b10: 5MHz to 10MHz (divide by 2)<br>Single-ended sensor configuration<br>b10: 0.01MHz to 10MHz (divide by 2) | $> 3$                   | $> 8$             |
|                     | External                    | $f_{REFx} \leq 40$           |                       |   |                         |                   |
| Single-channel      | Either external or internal | $f_{REFx} \leq 35$           |                       |   |                         |                   |

(1) Channels 2 and 3 are only available for FDC2114 and FDC2214.

(2) Refer to [Sensor Configuration](#) for information on differential and single-ended sensor configurations.

表 6-2 shows the clock configuration registers for all channels.

表 6-2. Clock Configuration Registers

| CHANNEL <sup>(1)</sup> | CLOCK                               | REGISTER                      | FIELD [ BIT(S) ]       | VALUE  |
|------------------------|-------------------------------------|-------------------------------|------------------------|--|
| All                    | $f_{CLK}$ = Controller Clock Source | CONFIG, addr 0x1A             | REF_CLK_SRC [9]        | b0 = internal oscillator is used as the controller clock<br>b1 = external clock source is used as the controller clock |
| 0                      | $f_{REF0}$                          | CLOCK_DIVIDERS_CH0, addr 0x14 | CH0_FREF_DIVIDER [9:0] | $f_{REF0} = f_{CLK} / CH0\_FREF\_DIVIDER$  |
| 1                      | $f_{REF1}$                          | CLOCK_DIVIDERS_CH1, addr 0x15 | CH1_FREF_DIVIDER [9:0] | $f_{REF1} = f_{CLK} / CH1\_FREF\_DIVIDER$  |
| 2                      | $f_{REF2}$                          | CLOCK_DIVIDERS_CH2, addr 0x16 | CH2_FREF_DIVIDER [9:0] | $f_{REF2} = f_{CLK} / CH2\_FREF\_DIVIDER$  |
| 3                      | $f_{REF3}$                          | CLOCK_DIVIDERS_CH3, addr 0x17 | CH3_FREF_DIVIDER [9:0] | $f_{REF3} = f_{CLK} / CH3\_FREF\_DIVIDER$  |
| 0                      | $f_{IN0}$                           | CLOCK_DIVIDERS_CH0, addr 0x14 | CH0_FIN_SEL [13:12]    | $f_{IN0} = f_{SENSOR0} / CH0\_FIN\_SEL$  |
| 1                      | $f_{IN1}$                           | CLOCK_DIVIDERS_CH1, addr 0x15 | CH1_FIN_SEL [13:12]    | $f_{IN1} = f_{SENSOR1} / CH1\_FIN\_SEL$  |
| 2                      | $f_{IN2}$                           | CLOCK_DIVIDERS_CH2, addr 0x16 | CH2_FIN_SEL [13:12]    | $f_{IN2} = f_{SENSOR2} / CH2\_FIN\_SEL$  |
| 3                      | $f_{IN3}$                           | CLOCK_DIVIDERS_CH3, addr 0x17 | CH3_FIN_SEL [13:12]    | $f_{IN3} = f_{SENSOR3} / CH3\_FIN\_SEL$  |

(1) Channels 2 and 3 are only available for FDC2114 and FDC2214

### 6.3.2 Multi-Channel and Single-Channel Operation

The multi-channel package of the FDC enables the user to save board space and support flexible system design. For example, temperature drift can often cause a shift in component values, resulting in a shift in resonant frequency of the sensor. Using a second sensor as a reference provides the capability to cancel out a temperature shift. When operated in multi-channel mode, the FDC sequentially samples the active channels. In single-channel mode, the FDC samples a single channel, which is selectable. 表 6-3 shows the registers and values that are used to configure either multi-channel or single-channel modes.

**表 6-3. Single- and Multi-Channel Configuration Registers**

| MODE           | REGISTER             | FIELD [ BIT(S) ]    | VALUE   |
|----------------|----------------------|---------------------|---|
| Single channel | CONFIG, addr 0x1A    | ACTIVE_CHAN [15:14] | 00 = chan 0   |
|                |                      |                     | 01 = chan 1   |
|                |                      |                     | 10 = chan 2   |
|                |                      |                     | 11 = chan 3   |
|                | MUX_CONFIG addr 0x1B | AUTOSCAN_EN [15]    | 0 = continuous conversion on a single channel (default) |
| Multi-channel  | MUX_CONFIG addr 0x1B | AUTOSCAN_EN [15]    | 1 = continuous conversion on multiple channels          |
|                | MUX_CONFIG addr 0x1B | RR_SEQUENCE [14:13] | 00 = Ch0, Ch 1  |
|                |                      |                     | 01 = Ch0, Ch 1, Ch 2                                    |
|                |                      |                     | 10 = Ch0, CH1, Ch2, Ch3                                 |

The digitized sensor measurement for each channel (DATA<sub>x</sub>) represents the ratio of the sensor frequency to the reference frequency.

The data output (DATA<sub>x</sub>) of the FDC2112 and FDC2114 is expressed as the 12 MSBs of a 16-bit result:

$$DATA_x = \frac{f_{SENSORx} * 2^{12}}{f_{REFx}} \quad (1)$$

The data output (DATA<sub>x</sub>) of the FDC2212 and FDC2214 is expressed as:

$$DATA_x = \frac{f_{SENSORx} * 2^{28}}{f_{REFx}} \quad (2)$$

表 6-4 lists the registers that contain the fixed point sample values for each channel.

**表 6-4. Sample Data Registers**

| CHANNEL <sup>(2)</sup> | REGISTER <sup>(1)</sup> | FIELD NAME [ BITS(S) ] AND VALUE (FDC2112, FDC2114)  | FIELD NAME [ BITS(S) ] AND VALUE (FDC2212, FDC2214) <sup>(3) (4)</sup> |
|------------------------|-------------------------|--|--|
| 0                      | DATA_CH0, addr 0x00     | DATA0 [11:0]:<br>12 bits of the 16 bit conversion result.<br>0x000 = under range<br>0xfff = over range | DATA0 [27:16]:<br>12 MSBs of the 28 bit conversion result              |
|                        | DATA_LSB_CH0, addr 0x01 | Not applicable   | DATA0 [15:0]:<br>16 LSBs of the 28 bit conversion result               |
| 1                      | DATA_CH1, addr 0x02     | DATA1 [11:0]:<br>12 bits of the 16 bit conversion result.<br>0x000 = under range<br>0xfff = over range | DATA1 [27:16]:<br>12 MSBs of the 28 bit conversion result              |
|                        | DATA_LSB_CH1, addr 0x03 | Not applicable   | DATA1 [15:0]:<br>16 LSBs of the 28 bit conversion result               |
| 2                      | DATA_CH2, addr 0x04     | DATA2 [11:0]:<br>12 bits of the 16 bit conversion result.<br>0x000 = under range<br>0xfff = over range | DATA2 [27:16]:<br>12 MSBs of the 28 bit conversion result              |
|                        | DATA_LSB_CH2, addr 0x05 | Not applicable   | DATA2 [15:0]:<br>16 LSBs of the 28 bit conversion result               |

表 6-4. Sample Data Registers (续)

| CHANNEL <sup>(2)</sup> | REGISTER <sup>(1)</sup> | FIELD NAME [ BITS(S) ] AND VALUE (FDC2112, FDC2114)  | FIELD NAME [ BITS(S) ] AND VALUE (FDC2212, FDC2214) <sup>(3) (4)</sup> |
|------------------------|-------------------------|--|--|
| 3                      | DATA_CH3, addr 0x06     | DATA3 [11:0]:<br>12 bits of the 16 bit conversion result.<br>0x000 = under range<br>0xfff = over range | DATA3 [27:16]:<br>12 MSBs of the 28 bit conversion result              |
|                        | DATA_LSB_CH3, addr 0x07 | Not applicable   | DATA3 [15:0]:<br>16 LSBs of the 28 bit conversion result               |

- (1) The DATA\_CHx.DATAx register must always be read first, followed by the DATA\_LSB\_CHx.DATAx register of the same channel to ensure data coherency.
- (2) Channels 2 and 3 are only available for FDC2114 and FDC2214.
- (3) A DATA value of 0x0000000 = under range for FDC2212/FDC2214.
- (4) A DATA value of 0xFFFFFFF = over range for FDC2212/FDC2214.

When the FDC sequences through the channels in multi-channel mode, the dwell time interval for each channel is the sum of three parts:

1. sensor activation time
2. conversion time
3. channel switch delay

The sensor activation time is the amount of settling time required for the sensor oscillation to stabilize, as shown in 图 6-4. The settling wait time is programmable, and TI recommends setting the wait time to a value that is long enough to allow stable oscillation. The settling wait time for channel x is given by:

$$t_{Sx} = (CHX\_SETTLECOUNT \times 16) / f_{REFx} \quad (3)$$

表 6-5 illustrates the registers and values for configuring the settling time for each channel.

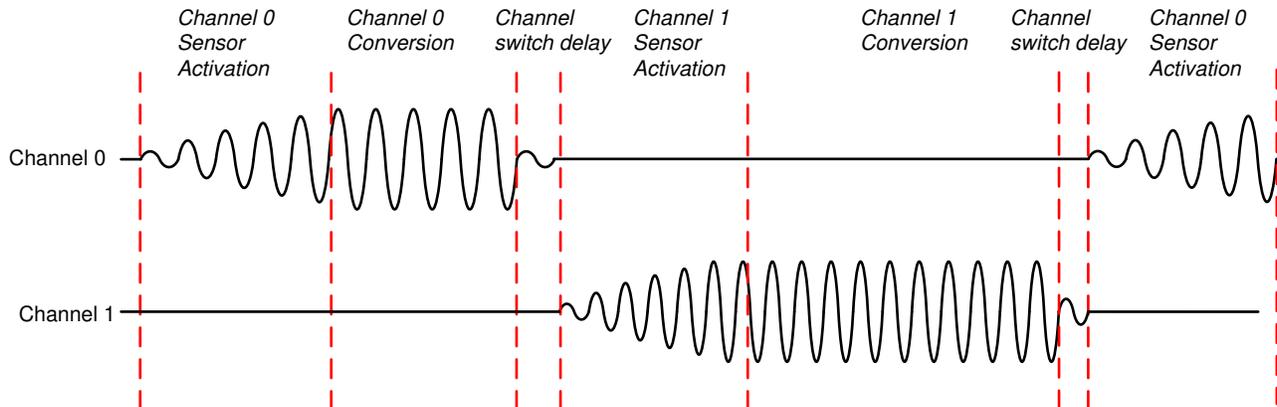


图 6-4. Multi-Channel Mode Sequencing

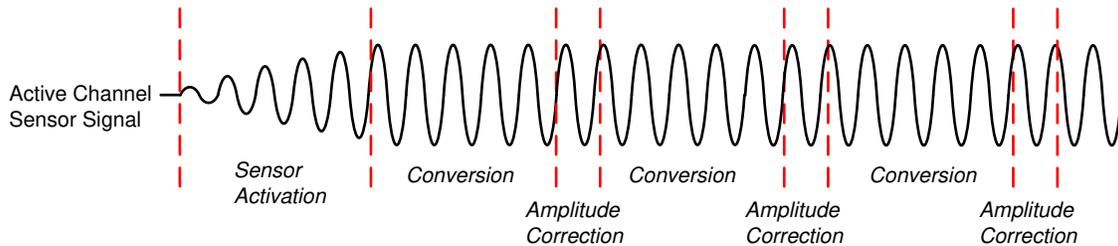


图 6-5. Single-Channel Mode Sequencing

**表 6-5. Settling Time Register Configuration**

| CHANNEL <sup>(1)</sup> | REGISTER                   | FIELD                  | CONVERSION TIME <sup>(2)</sup>         |
|------------------------|----------------------------|------------------------|--|
| 0                      | SETTLECOUNT_CH0, addr 0x10 | CH0_SETTLECOUNT [15:0] | (CH0_SETTLECOUNT*16)/f <sub>REF0</sub> |
| 1                      | SETTLECOUNT_CH1, addr 0x11 | CH1_SETTLECOUNT [15:0] | (CH1_SETTLECOUNT*16)/f <sub>REF1</sub> |
| 2                      | SETTLECOUNT_CH2, addr 0x12 | CH2_SETTLECOUNT [15:0] | (CH2_SETTLECOUNT*16)/f <sub>REF2</sub> |
| 3                      | SETTLECOUNT_CH3, addr 0x13 | CH3_SETTLECOUNT [15:0] | (CH3_SETTLECOUNT*16)/f <sub>REF3</sub> |

(1) Channels 2 and 3 are available only in the FDC2114 and FDC2214.

(2) f<sub>REFx</sub> is the reference frequency configured for the channel.

The SETTLECOUNT for any channel x must satisfy:

$$\bullet \text{ CHx\_SETTLECOUNT} > V_{pk} \times f_{REFx} \times C \times \pi^2 / (32 \times \text{IDRIVE}_x) \quad (4)$$

- - where
  - V<sub>pk</sub> = Peak oscillation amplitude at the programmed IDRIVE setting
  - f<sub>REFx</sub> = Reference frequency for Channel x
  - C = sensor capacitance including parasitic PCB capacitance
  - IDRIVE<sub>x</sub> = setting programmed into the IDRIVE register in amps
- Round the result to the next highest integer (for example, if 方程式 4 recommends a minimum value of 6.08, program the register to 7 or higher).
- The conversion time represents the number of reference clock cycles used to measure the sensor frequency and is set by the CHx\_RCOUNT register for the channel. The conversion time for any channel x is:

$$\bullet t_{Cx} = (\text{CHx\_RCOUNT} \times 16 + 4) / f_{REFx} \quad (5)$$

- The reference count value must be chosen to support the required number of effective bits (ENOB). For example, if an ENOB of 13 bits is required, then a minimum conversion time of 2<sup>13</sup> = 8192 clock cycles is required. 8192 clock cycles correspond to a CHx\_RCOUNT value of 0x0200.

**表 6-6. Conversion Time Configuration Registers, Channels 0 - 3<sup>(1)</sup>**

| CHANNEL | REGISTER              | FIELD [ BIT(S) ]  | CONVERSION TIME                     |
|---------|-----------------------|-------------------|-------------------------------------|
| 0       | RCOUNT_CH0, addr 0x08 | CH0_RCOUNT [15:0] | (CH0_RCOUNT × 16)/f <sub>REF0</sub> |
| 1       | RCOUNT_CH1, addr 0x09 | CH1_RCOUNT [15:0] | (CH1_RCOUNT × 16)/f <sub>REF1</sub> |
| 2       | RCOUNT_CH2, addr 0x0A | CH2_RCOUNT [15:0] | (CH2_RCOUNT × 16)/f <sub>REF2</sub> |
| 3       | RCOUNT_CH3, addr 0x0B | CH3_RCOUNT [15:0] | (CH3_RCOUNT × 16)/f <sub>REF3</sub> |

(1) Channels 2 and 3 are available only for FDC2114 and FDC2214.

The typical channel switch delay time between the end of conversion and the beginning of sensor activation of the subsequent channel is:

$$\text{Channel Switch Delay} = 692\text{ns} + 5 / f_{ref} \quad (6)$$

The deterministic conversion time of the FDC allows data polling at a fixed interval. For example, if the programmed SETTLECOUNT is 128 F<sub>REF</sub> cycles (SETTLECOUNT = 0x0008) and RCOUNT is 512 F<sub>REF</sub> cycles (RCOUNT=0x0020), then one conversion takes 3.2ms (sensor-activation time) + 12.8ms (conversion time) + 0.8μs (channel-switch delay) = 16.0ms per channel. If the FDC is configured for dual-channel operation by setting AUTOSCAN\_EN = 1 and RR\_SEQUENCE = 00, then one full set of conversion results is available from the data registers every 32ms.

A data ready flag (DRDY) is also available for interrupt driven system designs (see the STATUS register description in [Register Maps](#)).

### 6.3.3 Current Drive Control Registers

The registers listed in 表 6-7 are used to control the sensor drive current. Follow the recommendations listed in the last column of the table.

**表 6-7. Current Drive Control Registers**

| CHANNEL <sup>(1)</sup> | REGISTER                     | FIELD [ BIT(S) ]         | VALUE   |
|------------------------|------------------------------|--------------------------|---|
| All                    | CONFIG, addr 0x1A            | SENSOR_ACTIVATE_SEL [11] | Sets current drive for sensor activation. Recommended value is b0 (full current mode).  |
| 0                      | CONFIG, addr 0x1A            | HIGH_CURRENT_DRV [6]     | b0 = normal current drive (1.5mA)<br>b1 = Increased current drive (> 1.5mA) for Ch 0 in single channel mode only. Cannot be used in multi-channel mode. |
| 0                      | DRIVE_CURRENT_CH0, addr 0x1E | CH0_IDRIVE [15:11]       | Drive current used during the settling and conversion time for Ch. 0. Set such that $1.2V \leq$ sensor oscillation amplitude (pk) $\leq 1.8V$           |
| 1                      | DRIVE_CURRENT_CH1, addr 0x1F | CH1_IDRIVE [15:11]       | Drive current used during the settling and conversion time for Ch. 1. Set such that $1.2V \leq$ sensor oscillation amplitude (pk) $\leq 1.8V$           |
| 2                      | DRIVE_CURRENT_CH2, addr 0x20 | CH2_IDRIVE [15:11]       | Drive current used during the settling and conversion time for Ch. 2. Set such that $1.2V \leq$ sensor oscillation amplitude (pk) $\leq 1.8V$           |
| 3                      | DRIVE_CURRENT_CH3, addr 0x21 | CH3_IDRIVE [15:11]       | Drive current used during the settling and conversion time for Ch. 3. Set such that $1.2V \leq$ sensor oscillation amplitude (pk) $\leq 1.8V$           |

(1) Channels 2 and 3 are available for FDC2114 and FDC2214 only.

Program the CH<sub>x</sub>\_IDRIVE field such that the sensor oscillates at an amplitude between 1.2Vpk ( $V_{\text{SENSORMIN}}$ ) and 1.8Vpk ( $V_{\text{SENSORMAX}}$ ). An IDRIVE value of 00000 corresponds to 16 $\mu$ A, and IDRIVE = b11111 corresponds to 1563 $\mu$ A.

A high sensor current drive mode can be enabled to drive sensor coils with > 1.5mA on channel 0, only in single channel mode. This feature can be used when the sensor minimum recommended oscillation amplitude of 1.2V cannot be achieved with the highest IDRIVE setting. Set the HIGH\_CURRENT\_DRV register bit to b1 to enable this mode.

### 6.3.4 Device Status Registers

The registers listed in 表 6-8 may be used to read device status.

**表 6-8. Status Registers**

| CHANNEL <sup>(1)</sup> | REGISTER                 | FIELDS [ BIT(S) ]  | VALUES   |
|------------------------|--------------------------|--|--|
| All                    | STATUS, addr 0x18        | 12 fields are available that contain various status bits [ 15:0 ]            | Refer to <a href="#">Register Maps</a> for a description of the individual status bits.              |
| All                    | STATUS_CONFIG, addr 0x19 | 12 fields are available that are used to configure status reporting [ 15:0 ] | Refer to <a href="#">Register Maps</a> for a description of the individual error configuration bits. |

(1) Channels 2 and 3 are available for FDC2114 and FDC2114 only.

See the STATUS and STATUS\_CONFIG register description in [Register Maps](#). These registers can be configured to trigger an interrupt on the INTB pin for certain events. The following conditions must be met:

1. The error or status register must be unmasked by enabling the appropriate register bit in the STATUS\_CONFIG register
2. The INTB function must be enabled by setting CONFIG.INTB\_DIS to 0

When a bit field in the STATUS register is set, the entire STATUS register content is held until read or until the DATA\_CHx register is read. Reading also deasserts INTB.

Interrupts are cleared by one of the following events:

1. Entering sleep mode
2. Power-on reset (POR)
3. Device enters shutdown mode (SD is asserted)
4. S/W reset
5. I<sup>2</sup>C read of the STATUS register: Reading the STATUS register clears any error status bit set in STATUS along with the ERR\_CHAN field and deassert INTB

Setting register CONFIG.INTB\_DIS to b1 disables the INTB function and holds the INTB pin high.

### 6.3.5 Input Deglitch Filter

The input deglitch filter suppresses EMI and ringing above the sensor frequency. The input deglitch filter does not impact the conversion result as long as its bandwidth is configured to be above the maximum sensor frequency. The input deglitch filter can be configured in MUX\_CONFIG.DEGLITCH register field as shown in 表 6-9. For optimal performance, TI recommends selection of the lowest setting that exceeds the sensor oscillation frequency. For example, if the maximum sensor frequency is 2MHz, choose MUX\_CONFIG.DEGLITCH = b100 (3.3MHz).

表 6-9. Input Deglitch Filter Register

| CHANNEL <sup>(1)</sup> | MUX_CONFIG.DEGLITCH (addr 0x1B) REGISTER VALUE | DEGLITCH FREQUENCY |
|------------------------|--|--------------------|
| ALL                    | 001  | 1MHz               |
| ALL                    | 100  | 3.3MHz             |
| ALL                    | 101  | 10MHz              |
| ALL                    | 011  | 33MHz              |

(1) Channels 2 and 3 are available for FDC2114 / FDC2214 only.

## 6.4 Device Functional Modes

### 6.4.1 Start-Up Mode

When the FDC powers up, the FDC enters sleep mode and waits for configuration. When the device is configured, exit sleep mode by setting CONFIG.SLEEP\_MODE\_EN to b0.

TI recommends configuring the FDC while in sleep mode. If a setting on the FDC needs to be changed, return the device to sleep mode, change the appropriate register, and then exit sleep mode.

### 6.4.2 Normal (Conversion) Mode

When operating in the normal (conversion) mode, the FDC is periodically sampling the frequency of the sensor(s) and generating sample outputs for the active channel(s).

### 6.4.3 Sleep Mode

Sleep mode is entered by setting the CONFIG.SLEEP\_MODE\_EN register field to 1. While in this mode, the device configuration is maintained. To exit sleep mode, set the CONFIG.SLEEP\_MODE\_EN register field to 0. After setting CONFIG.SLEEP\_MODE\_EN to b0, sensor activation for the first conversion begins after 16,384 f<sub>INT</sub> clock cycles. While in sleep mode the I<sup>2</sup>C interface is functional so that register reads and writes can be performed. While in sleep mode, no conversions are performed. In addition, entering sleep mode clears conversion results, any error condition, and deassert the INTB pin.

### 6.4.4 Shutdown Mode

When the SD pin is set to high, the FDC enters shutdown mode. Shutdown mode is the lowest power state. To exit shutdown mode, set the SD pin to low. Entering shutdown mode returns all registers to their default state.

While in shutdown mode, no conversions are performed. In addition, entering shutdown mode clears any error condition and deasserts the INTB pin. While the device is in shutdown mode, it is not possible to read to or write from the device via the I<sup>2</sup>C interface.

#### 6.4.4.1 Reset

The FDC can be reset by writing to RESET\_DEV.RESET\_DEV. Any active conversion stops, and all register values return to their default value. This register bit always returns 0b when read.

## 6.5 Programming

The FDC device uses an I<sup>2</sup>C interface to access control and data registers.

### 6.5.1 I<sup>2</sup>C Interface Specifications

The FDC uses an extended start sequence with I<sup>2</sup>C for register access. The maximum speed of the I<sup>2</sup>C interface is 400 kbit/s. This sequence follows the standard I<sup>2</sup>C 7-bit target address followed by an 8-bit pointer register byte to set the register address. When the ADDR pin is set low, the FDC I<sup>2</sup>C address is 0x2A; when the ADDR pin is set high, the FDC I<sup>2</sup>C address is 0x2B. The ADDR pin must not change state after the FDC exits Shutdown Mode.

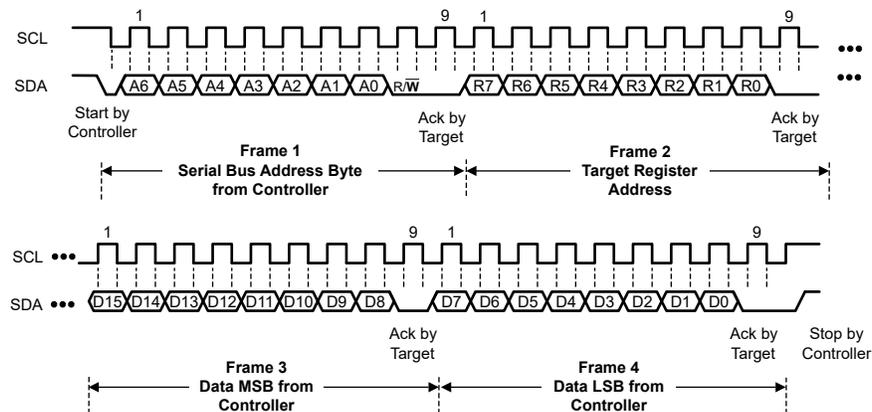


图 6-6. I<sup>2</sup>C Write Register Sequence

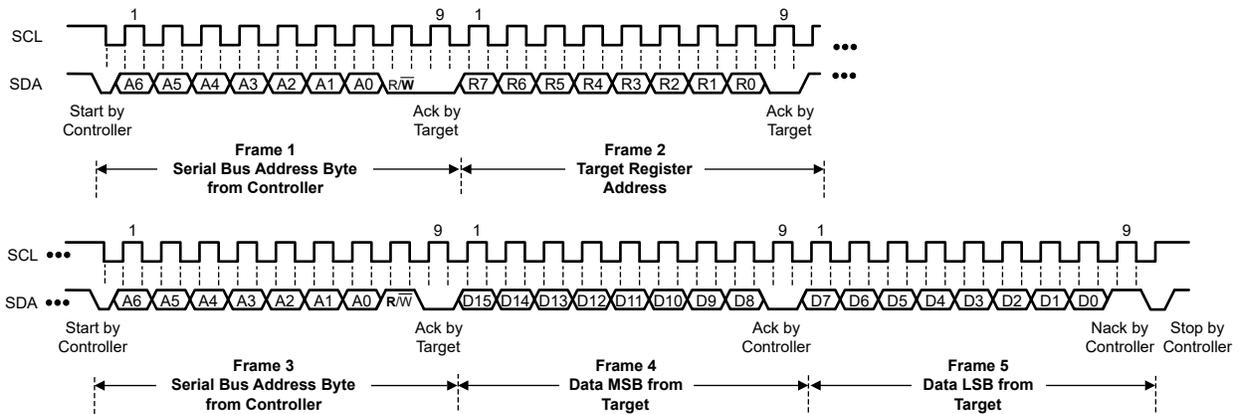


图 6-7. I<sup>2</sup>C Read Register Sequence

## 6.6 Register Maps

### 6.6.1 Register List

Fields indicated with Reserved must be written only with indicated values, otherwise improper device operation may occur. The R/W column indicates the Read-Write status of the corresponding field. A 'R/W' entry indicates read and write capability, a 'R' indicates read-only, and a 'W' indicates write-only.

图 6-8. Register List

| ADDRESS | NAME               | DEFAULT VALUE | DESCRIPTION   |
|---------|--------------------|---------------|---|
| 0x00    | DATA_CH0           | 0x0000        | Channel 0 Conversion Result and status ( <b>FDC2112 / FDC2114 only</b> )                                    |
|         |                    | 0x0000        | Channel 0 MSB Conversion Result and status ( <b>FDC2212 / FDC2214 only</b> )                                |
| 0x01    | DATA_LSB_CH0       | 0x0000        | Channel 0 LSB Conversion Result. Must be read after Register address 0x00 ( <b>FDC2212 / FDC2214 only</b> ) |
| 0x02    | DATA_CH1           | 0x0000        | Channel 1 Conversion Result and status ( <b>FDC2112 / FDC2114 only</b> )                                    |
|         |                    | 0x0000        | Channel 1 MSB Conversion Result and status ( <b>FDC2212 / FDC2214 only</b> )                                |
| 0x03    | DATA_LSB_CH1       | 0x0000        | Channel 1 LSB Conversion Result. Must be read after Register address 0x02 ( <b>FDC2212 / FDC2214 only</b> ) |
| 0x04    | DATA_CH2           | 0x0000        | Channel 2 Conversion Result and status ( <b>FDC2114 only</b> )  |
|         |                    | 0x0000        | Channel 2 MSB Conversion Result and status ( <b>FDC2214 only</b> )  |
| 0x05    | DATA_LSB_CH2       | 0x0000        | Channel 2 LSB Conversion Result. Must be read after Register address 0x04 ( <b>FDC2214 only</b> )           |
| 0x06    | DATA_CH3           | 0x0000        | Channel 3 Conversion Result and status ( <b>FDC2114 only</b> )  |
|         |                    | 0x0000        | Channel 3 MSB Conversion Result and status ( <b>FDC2214 only</b> )  |
| 0x07    | DATA_LSB_CH3       | 0x0000        | Channel 3 LSB Conversion Result. Must be read after Register address 0x06 ( <b>FDC2214 only</b> )           |
| 0x08    | RCOUNT_CH0         | 0x0080        | Reference Count setting for Channel 0   |
| 0x09    | RCOUNT_CH1         | 0x0080        | Reference Count setting for Channel 1   |
| 0x0A    | RCOUNT_CH2         | 0x0080        | Reference Count setting for Channel 2 ( <b>FDC2114 / FDC2214 only</b> )                                     |
| 0x0B    | RCOUNT_CH3         | 0x0080        | Reference Count setting for Channel 3 ( <b>FDC2114 / FDC2214 only</b> )                                     |
| 0x0C    | OFFSET_CH0         | 0x0000        | Offset value for Channel 0 ( <b>FDC2112 / FDC2114 only</b> )  |
| 0x0D    | OFFSET_CH1         | 0x0000        | Offset value for Channel 1 ( <b>FDC2112 / FDC2114 only</b> )  |
| 0x0E    | OFFSET_CH2         | 0x0000        | Offset value for Channel 2 ( <b>FDC2114 only</b> )  |
| 0x0F    | OFFSET_CH3         | 0x0000        | Offset value for Channel 3 ( <b>FDC2114 only</b> )  |
| 0x10    | SETTLECOUNT_CH0    | 0x0000        | Channel 0 Settling Reference Count  |
| 0x11    | SETTLECOUNT_CH1    | 0x0000        | Channel 1 Settling Reference Count  |
| 0x12    | SETTLECOUNT_CH2    | 0x0000        | Channel 2 Settling Reference Count ( <b>FDC2114 / FDC2214 only</b> )  |
| 0x13    | SETTLECOUNT_CH3    | 0x0000        | Channel 3 Settling Reference Count ( <b>FDC2114 / FDC2214 only</b> )  |
| 0x14    | CLOCK_DIVIDERS_CH0 | 0x0000        | Reference divider settings for Channel 0  |
| 0x15    | CLOCK_DIVIDERS_CH1 | 0x0000        | Reference divider settings for Channel 1  |
| 0x16    | CLOCK_DIVIDERS_CH2 | 0x0000        | Reference divider settings for Channel 2 ( <b>FDC2114 / FDC2214 only</b> )                                  |
| 0x17    | CLOCK_DIVIDERS_CH3 | 0x0000        | Reference divider settings for Channel 3 ( <b>FDC2114 / FDC2214 only</b> )                                  |
| 0x18    | STATUS             | 0x0000        | Device Status Reporting   |
| 0x19    | STATUS_CONFIG      | 0x0000        | Device Status Reporting Configuration   |
| 0x1A    | CONFIG             | 0x2801        | Conversion Configuration  |
| 0x1B    | MUX_CONFIG         | 0x020F        | Channel Multiplexing Configuration  |
| 0x1C    | RESET_DEV          | 0x0000        | Reset Device  |
| 0x1E    | DRIVE_CURRENT_CH0  | 0x0000        | Channel 0 sensor current drive configuration  |
| 0x1F    | DRIVE_CURRENT_CH1  | 0x0000        | Channel 1 sensor current drive configuration  |
| 0x20    | DRIVE_CURRENT_CH2  | 0x0000        | Channel 2 sensor current drive configuration ( <b>FDC2114 / FDC2214 only</b> )                              |

图 6-8. Register List (续)

| ADDRESS | NAME              | DEFAULT VALUE | DESCRIPTION   |
|---------|-------------------|---------------|---|
| 0x21    | DRIVE_CURRENT_CH3 | 0x0000        | Channel 3 sensor current drive configuration (FDC2114 / FDC2214 only) |
| 0x7E    | MANUFACTURER_ID   | 0x5449        | Manufacturer ID   |
| 0x7F    | DEVICE_ID         | 0x3054        | Device ID (FDC2112, FDC2114 only)                                     |
|         |                   | 0x3055        | Device ID (FDC2212, FDC2214 only)                                     |

### 6.6.2 Address 0x00, DATA\_CH0

图 6-9. Address 0x00, DATA\_CH0

|          |    |            |            |       |    |   |   |
|----------|----|------------|------------|-------|----|---|---|
| 15       | 14 | 13         | 12         | 11    | 10 | 9 | 8 |
| RESERVED |    | CH0_ERR_WD | CH0_ERR_AW | DATA0 |    |   |   |
| 7        | 6  | 5          | 4          | 3     | 2  | 1 | 0 |
| DATA0    |    |            |            |       |    |   |   |

表 6-10. Address 0x00, DATA\_CH0 Field Descriptions

| Bit   | Field                                 | Type | Reset             | Description   |
|-------|---------------------------------------|------|-------------------|---|
| 15:14 | RESERVED                              | R    | 00                | Reserved.   |
| 13    | CH0_ERR_WD                            | R    | 0                 | Channel 0 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit. |
| 12    | CH0_ERR_AW                            | R    | 0                 | Channel 0 Amplitude Warning. Cleared by reading the bit.                      |
| 11:0  | DATA0 (FDC2112 / FDC2114 only)        | R    | 0000 0000<br>0000 | Channel 0 Conversion Result   |
|       | DATA0[27:16] (FDC2212 / FDC2214 only) |      |                   |   |

### 6.6.3 Address 0x01, DATA\_LSB\_CH0 (FDC2212 / FDC2214 only)

图 6-10. Address 0x01, DATA\_LSB\_CH0

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA0 |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DATA0 |    |    |    |    |    |   |   |

表 6-11. Address 0x01, DATA\_CH0 Field Descriptions

| Bit  | Field       | Type | Reset             | Description                 |
|------|-------------|------|-------------------|-----------------------------|
| 15:0 | DATA0[15:0] | R    | 0000 0000<br>0000 | Channel 0 Conversion Result |

### 6.6.4 Address 0x02, DATA\_CH1

图 6-11. Address 0x02, DATA\_CH1

|          |    |            |            |       |    |   |   |
|----------|----|------------|------------|-------|----|---|---|
| 15       | 14 | 13         | 12         | 11    | 10 | 9 | 8 |
| RESERVED |    | CH1_ERR_WD | CH1_ERR_AW | DATA1 |    |   |   |
| 7        | 6  | 5          | 4          | 3     | 2  | 1 | 0 |
| DATA1    |    |            |            |       |    |   |   |

表 6-12. Address 0x02, DATA\_CH1 Field Descriptions

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 15:14 | RESERVED | R    | 00    | Reserved.   |

表 6-12. Address 0x02, DATA\_CH1 Field Descriptions (续)

| Bit  | Field                                 | Type | Reset             | Description   |
|------|---------------------------------------|------|-------------------|---|
| 13   | CH1_ERR_WD                            | R    | 0                 | Channel 1 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit. |
| 12   | CH1_ERR_AW                            | R    | 0                 | Channel 1 Amplitude Warning. Cleared by reading the bit.                      |
| 11:0 | DATA1 (FDC2112 / FDC2114 only)        | R    | 0000 0000<br>0000 | Channel 1 Conversion Result   |
|      | DATA1[27:16] (FDC2212 / FDC2214 only) |      |                   |   |

6.6.5 Address 0x03, DATA\_LSB\_CH1 (FDC2212 / FDC2214 only)

图 6-12. Address 0x03, DATA\_LSB\_CH1

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA1 |    |    |    |    |    |   |   |
|       |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DATA1 |    |    |    |    |    |   |   |
|       |    |    |    |    |    |   |   |

表 6-13. Address 0x03, DATA\_CH1 Field Descriptions

| Bit  | Field       | Type | Reset             | Description                 |
|------|-------------|------|-------------------|-----------------------------|
| 15:0 | DATA1[15:0] | R    | 0000 0000<br>0000 | Channel 1 Conversion Result |

6.6.6 Address 0x04, DATA\_CH2 (FDC2114, FDC2214 only)

图 6-13. Address 0x04, DATA\_CH2

|          |    |            |            |       |    |   |   |
|----------|----|------------|------------|-------|----|---|---|
| 15       | 14 | 13         | 12         | 11    | 10 | 9 | 8 |
| RESERVED |    | CH2_ERR_WD | CH2_ERR_AW | DATA2 |    |   |   |
|          |    |            |            |       |    |   |   |
| 7        | 6  | 5          | 4          | 3     | 2  | 1 | 0 |
| DATA2    |    |            |            |       |    |   |   |
|          |    |            |            |       |    |   |   |

表 6-14. Address 0x04, DATA\_CH2 Field Descriptions

| Bit   | Field                                 | Type | Reset             | Description   |
|-------|---------------------------------------|------|-------------------|---|
| 15:14 | RESERVED                              | R    | 00                | Reserved.   |
| 13    | CH2_ERR_WD                            | R    | 0                 | Channel 2 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit. |
| 12    | CH2_ERR_AW                            | R    | 0                 | Channel 2 Amplitude Warning. Cleared by reading the bit.                      |
| 11:0  | DATA2 (FDC2112 / FDC2114 only)        | R    | 0000 0000<br>0000 | Channel 2 Conversion Result   |
|       | DATA2[27:16] (FDC2212 / FDC2214 only) |      |                   |   |

6.6.7 Address 0x05, DATA\_LSB\_CH2 (FDC2214 only)

图 6-14. Address 0x05, DATA\_LSB\_CH2

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA2 |    |    |    |    |    |   |   |
|       |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DATA2 |    |    |    |    |    |   |   |
|       |    |    |    |    |    |   |   |

表 6-15. Address 0x05, DATA\_CH2 Field Descriptions

| Bit  | Field       | Type | Reset             | Description                 |
|------|-------------|------|-------------------|-----------------------------|
| 15:0 | DATA2[15:0] | R    | 0000 0000<br>0000 | Channel 2 Conversion Result |

6.6.8 Address 0x06, DATA\_CH3 (FDC2114, FDC2214 only)

图 6-15. Address 0x06, DATA\_CH3

|          |    |            |            |       |    |   |   |
|----------|----|------------|------------|-------|----|---|---|
| 15       | 14 | 13         | 12         | 11    | 10 | 9 | 8 |
| RESERVED |    | CH3_ERR_WD | CH3_ERR_AW | DATA3 |    |   |   |
| 7        | 6  | 5          | 4          | 3     | 2  | 1 | 0 |
| DATA3    |    |            |            |       |    |   |   |

表 6-16. Address 0x06, DATA\_CH3 Field Descriptions

| Bit   | Field   | Type | Reset             | Description   |
|-------|---|------|-------------------|---|
| 15:14 | RESERVED  | R    | 00                | Reserved.   |
| 13    | CH3_ERR_WD  | R    | 0                 | Channel 3 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit. |
| 12    | CH3_ERR_AW  | R    | 0                 | Channel 3 Amplitude Warning. Cleared by reading the bit.                      |
| 11:0  | DATA3 (FDC2112 / FDC2114 only)<br>DATA3[27:16] (FDC2212 / FDC2214 only) | R    | 0000 0000<br>0000 | Channel 3 Conversion Result   |

6.6.9 Address 0x07, DATA\_LSB\_CH3 (FDC2214 only)

图 6-16. Address 0x07, DATA\_LSB\_CH3

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA3 |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DATA3 |    |    |    |    |    |   |   |

表 6-17. Address 0x07, DATA\_CH3 Field Descriptions

| Bit  | Field       | Type | Reset             | Description                 |
|------|-------------|------|-------------------|-----------------------------|
| 15:0 | DATA3[15:0] | R    | 0000 0000<br>0000 | Channel 3 Conversion Result |

6.6.10 Address 0x08, RCOUNT\_CH0

图 6-17. Address 0x08, RCOUNT\_CH0

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH0_RCOUNT |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH0_RCOUNT |    |    |    |    |    |   |   |

表 6-18. Address 0x08, RCOUNT\_CH0 Field Descriptions

| Bit  | Field      | Type | Reset                  | Description   |
|------|------------|------|------------------------|---|
| 15:0 | CH0_RCOUNT | R/W  | 0000 0000<br>1000 0000 | Channel 0 Reference Count Conversion Interval Time<br>0x0000-0x00FF: Reserved<br>0x0100-0xFFFF: Conversion Time ( $t_{C0}$ ) = (CH0_RCOUNT*16)/<br>$f_{REF0}$ |

6.6.11 Address 0x09, RCOUNT\_CH1

图 6-18. Address 0x09, RCOUNT\_CH1

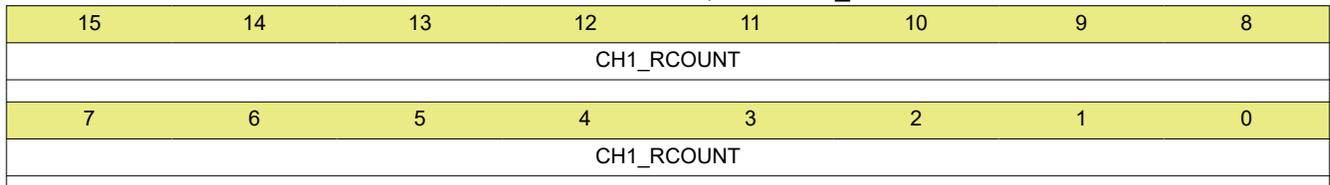


表 6-19. Address 0x09, RCOUNT\_CH1 Field Descriptions

| Bit  | Field      | Type | Reset                  | Description   |
|------|------------|------|------------------------|---|
| 15:0 | CH1_RCOUNT | R/W  | 0000 0000<br>1000 0000 | Channel 1 Reference Count Conversion Interval Time<br>0x0000-0x00FF: Reserved<br>0x0100-0xFFFF: Conversion Time ( $t_{C1}$ ) = (CH1_RCOUNT*16)/<br>$f_{REF1}$ |

6.6.12 Address 0x0A, RCOUNT\_CH2 (FDC2114, FDC2214 only)

图 6-19. Address 0x0A, RCOUNT\_CH2

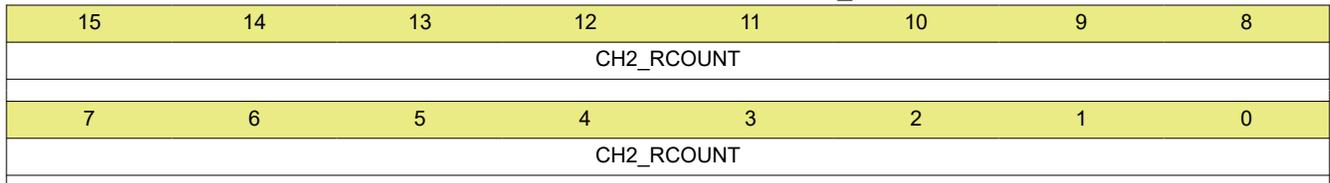


表 6-20. Address 0x0A, RCOUNT\_CH2 Field Descriptions

| Bit  | Field      | Type | Reset                  | Description   |
|------|------------|------|------------------------|---|
| 15:0 | CH2_RCOUNT | R/W  | 0000 0000<br>1000 0000 | Channel 2 Reference Count Conversion Interval Time<br>0x0000-0x00FF: Reserved<br>0x0100-0xFFFF: Conversion Time ( $t_{C2}$ ) = (CH2_RCOUNT*16)/<br>$f_{REF2}$ |

6.6.13 Address 0x0B, RCOUNT\_CH3 (FDC2114, FDC2214 only)

图 6-20. Address 0x0B, RCOUNT\_CH3

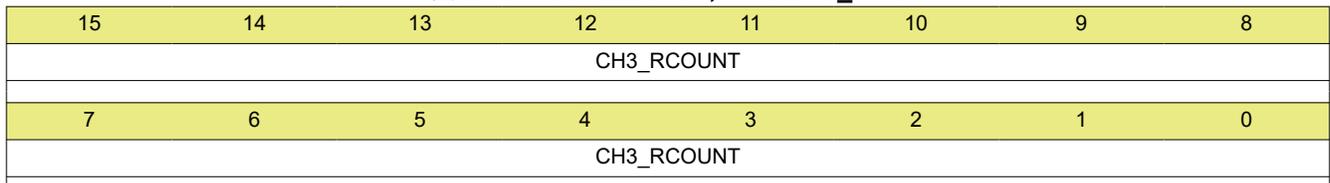


表 6-21. Address 0x0B, RCOUNT\_CH3 Field Descriptions

| Bit  | Field      | Type | Reset                  | Description   |
|------|------------|------|------------------------|---|
| 15:0 | CH3_RCOUNT | R/W  | 0000 0000<br>1000 0000 | Channel 3 Reference Count Conversion Interval Time<br>0x0000-0x00FF: Reserved<br>0x0100-0xFFFF: Conversion Time ( $t_{C3}$ ) = (CH3_RCOUNT*16)/<br>$f_{REF3}$ |

**6.6.14 Address 0x0C, OFFSET\_CH0 (FDC21112 / FDC2114 only)**

**图 6-21. Address 0x0C, CH0\_OFFSET**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH0_OFFSET |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH0_OFFSET |    |    |    |    |    |   |   |

**表 6-22. CH0\_OFFSET Field Descriptions**

| Bit  | Field      | Type | Reset                  | Description  |
|------|------------|------|------------------------|--|
| 15:0 | CH0_OFFSET | R/W  | 0000 0000<br>0000 0000 | Channel 0 Conversion Offset. $f_{\text{OFFSET}_0} = (\text{CH0\_OFFSET} / 2^{16}) * f_{\text{REF0}}$ |

**6.6.15 Address 0x0D, OFFSET\_CH1 (FDC21112 / FDC2114 only)**

**图 6-22. Address 0x0D, OFFSET\_CH1**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH1_OFFSET |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH1_OFFSET |    |    |    |    |    |   |   |

**表 6-23. Address 0x0D, OFFSET\_CH1 Field Descriptions**

| Bit  | Field      | Type | Reset                  | Description  |
|------|------------|------|------------------------|--|
| 15:0 | CH1_OFFSET | R/W  | 0000 0000<br>0000 0000 | Channel 1 Conversion Offset. $f_{\text{OFFSET}_1} = (\text{CH1\_OFFSET} / 2^{16}) * f_{\text{REF1}}$ |

**6.6.16 Address 0x0E, OFFSET\_CH2 (FDC2114 only)**

**图 6-23. Address 0x0E, OFFSET\_CH2**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH2_OFFSET |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH2_OFFSET |    |    |    |    |    |   |   |

**表 6-24. Address 0x0E, OFFSET\_CH2 Field Descriptions**

| Bit  | Field      | Type | Reset                  | Description  |
|------|------------|------|------------------------|--|
| 15:0 | CH2_OFFSET | R/W  | 0000 0000<br>0000 0000 | Channel 2 Conversion Offset. $f_{\text{OFFSET}_2} = (\text{CH2\_OFFSET} / 2^{16}) * f_{\text{REF2}}$ |

6.6.17 Address 0x0F, OFFSET\_CH3 (FDC2114 only)

图 6-24. Address 0x0F, OFFSET\_CH3

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH3_OFFSET |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH3_OFFSET |    |    |    |    |    |   |   |

表 6-25. Address 0x0F, OFFSET\_CH3 Field Descriptions

| Bit  | Field      | Type | Reset                  | Description  |
|------|------------|------|------------------------|--|
| 15:0 | CH3_OFFSET | R/W  | 0000 0000<br>0000 0000 | Channel 3 Conversion Offset. $f_{\text{OFFSET}_3} = (\text{CH3\_OFFSET} / 2^{16}) * f_{\text{REF3}}$ |

6.6.18 Address 0x10, SETTLECOUNT\_CH0

图 6-25. Address 0x10, SETTLECOUNT\_CH0

|                 |    |    |    |    |    |   |   |
|-----------------|----|----|----|----|----|---|---|
| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH0_SETTLECOUNT |    |    |    |    |    |   |   |
| 7               | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH0_SETTLECOUNT |    |    |    |    |    |   |   |

表 6-26. Address 0x11, SETTLECOUNT\_CH0 Field Descriptions

| Bit  | Field           | Type | Reset                  | Description  |
|------|-----------------|------|------------------------|--|
| 15:0 | CH0_SETTLECOUNT | R/W  | 0000 0000<br>0000 0000 | Channel 0 Conversion Settling<br>The FDC uses this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 0. If the amplitude has not settled prior to the conversion start, an Amplitude warning is generated if reporting of this type of warning is enabled.<br>0x0000: Settle Time ( $t_{s0}$ )= 32 ÷ $f_{\text{REF0}}$<br>0x0001: Settle Time ( $t_{s0}$ )= 32 ÷ $f_{\text{REF0}}$<br>0x0002 - 0xFFFF: Settle Time ( $t_{s0}$ )= (CH0_SETTLECOUNT×16) ÷ $f_{\text{REF0}}$ |

6.6.19 Address 0x11, SETTLECOUNT\_CH1

图 6-26. Address 0x11, SETTLECOUNT\_CH1

|                 |    |    |    |    |    |   |   |
|-----------------|----|----|----|----|----|---|---|
| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH1_SETTLECOUNT |    |    |    |    |    |   |   |
| 7               | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH1_SETTLECOUNT |    |    |    |    |    |   |   |

表 6-27. Address 0x12, SETTLECOUNT\_CH1 Field Descriptions

| Bit  | Field           | Type | Reset                  | Description   |
|------|-----------------|------|------------------------|---|
| 15:0 | CH1_SETTLECOUNT | R/W  | 0000 0000<br>0000 0000 | Channel 1 Conversion Settling<br>The FDC uses this settling time to allow the LC sensor to stabilize before initiation of a conversion on a Channel 1. If the amplitude has not settled prior to the conversion start, an Amplitude warning is generated if reporting of this type of warning is enabled.<br>0x0000: Settle Time ( $t_{S1}$ ) = $32 \div f_{REF1}$<br>0x0001: Settle Time ( $t_{S1}$ ) = $32 \div f_{REF1}$<br>0x0002 - 0xFFFF: Settle Time ( $t_{S1}$ ) = $(CH1\_SETTLECOUNT \times 16) \div f_{REF1}$ |

6.6.20 Address 0x12, SETTLECOUNT\_CH2 (FDC2114, FDC2214 only)

图 6-27. Address 0x12, SETTLECOUNT\_CH2

|                 |    |    |    |    |    |   |   |
|-----------------|----|----|----|----|----|---|---|
| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH2_SETTLECOUNT |    |    |    |    |    |   |   |
| 7               | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH2_SETTLECOUNT |    |    |    |    |    |   |   |

表 6-28. Address 0x12, SETTLECOUNT\_CH2 Field Descriptions

| Bit  | Field           | Type | Reset                  | Description   |
|------|-----------------|------|------------------------|---|
| 15:0 | CH2_SETTLECOUNT | R/W  | 0000 0000<br>0000 0000 | Channel 2 Conversion Settling<br>The FDC uses this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 2. If the amplitude has not settled prior to the conversion start, an Amplitude warning is generated if reporting of this type of warning is enabled.<br>0x0000: Settle Time ( $t_{S2}$ ) = $32 \div f_{REF2}$<br>0x0001: Settle Time ( $t_{S2}$ ) = $32 \div f_{REF2}$<br>0x0002 - 0xFFFF: Settle Time ( $t_{S2}$ ) = $(CH2\_SETTLECOUNT \times 16) \div f_{REF2}$ |

6.6.21 Address 0x13, SETTLECOUNT\_CH3 (FDC2114, FDC2214 only)

图 6-28. Address 0x13, SETTLECOUNT\_CH3

|                 |    |    |    |    |    |   |   |
|-----------------|----|----|----|----|----|---|---|
| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CH3_SETTLECOUNT |    |    |    |    |    |   |   |
| 7               | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CH3_SETTLECOUNT |    |    |    |    |    |   |   |

表 6-29. Address 0x13, SETTLECOUNT\_CH3 Field Descriptions

| Bit  | Field           | Type | Reset                  | Description  |
|------|-----------------|------|------------------------|--|
| 15:0 | CH3_SETTLECOUNT | R/W  | 0000 0000<br>0000 0000 | Channel 3 Conversion Settling<br>The FDC uses this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 3. If the amplitude has not settled prior to the conversion start, an Amplitude warning is generated if reporting of this type of warning is enabled<br>0x0000: Settle Time ( $t_{S3}$ ) = $32 \div f_{REF3}$<br>0x0001: Settle Time ( $t_{S3}$ ) = $32 \div f_{REF3}$<br>0x0002 - 0xFFFF: Settle Time ( $t_{S3}$ ) = $(CH3\_SETTLECOUNT \times 16) \div f_{REF3}$ |

### 6.6.22 Address 0x14, CLOCK\_DIVIDERS\_CH0

图 6-29. Address 0x14, CLOCK\_DIVIDERS\_CH0

|                  |    |             |    |          |    |                  |   |
|------------------|----|-------------|----|----------|----|------------------|---|
| 15               | 14 | 13          | 12 | 11       | 10 | 9                | 8 |
| RESERVED         |    | CH0_FIN_SEL |    | RESERVED |    | CH0_FREF_DIVIDER |   |
| 7                | 6  | 5           | 4  | 3        | 2  | 1                | 0 |
| CH0_FREF_DIVIDER |    |             |    |          |    |                  |   |

表 6-30. Address 0x14, CLOCK\_DIVIDERS\_CH0 Field Descriptions

| Bit   | Field            | Type | Reset           | Description  |
|-------|------------------|------|-----------------|--|
| 15:14 | RESERVED         | R/W  | 00              | Reserved. Set to b00.  |
| 13:12 | CH0_FIN_SEL      | R/W  | 00              | Channel 0 Sensor frequency select for differential sensor configuration:<br>b01: divide by 1. Choose for sensor frequencies between 0.01MHz and 8.75MHz<br>b10: divide by 2. Choose for sensor frequencies between 5MHz and 10MHz<br>for single-ended sensor configuration:<br>b10: divide by 2. Choose for sensor frequencies between 0.01MHz and 10MHz |
| 11:10 | RESERVED         | R/W  | 00              | Reserved. Set to b00.  |
| 9:0   | CH0_FREF_DIVIDER | R/W  | 00 0000<br>0000 | Channel 0 Reference Divider<br>Sets the divider for Channel 0 reference. Use this to scale the maximum conversion frequency.<br>b00' 0000' 0000: Reserved. Do not use.<br>CH0_FREF_DIVIDER ≥ b00' 0000' 0001: $f_{REF0} = f_{CLK} / CH0\_FREF\_DIVIDER$  |

### 6.6.23 Address 0x15, CLOCK\_DIVIDERS\_CH1

图 6-30. Address 0x15, CLOCK\_DIVIDERS\_CH1

|                  |    |             |    |          |    |                  |   |
|------------------|----|-------------|----|----------|----|------------------|---|
| 15               | 14 | 13          | 12 | 11       | 10 | 9                | 8 |
| RESERVED         |    | CH1_FIN_SEL |    | RESERVED |    | CH1_FREF_DIVIDER |   |
| 7                | 6  | 5           | 4  | 3        | 2  | 1                | 0 |
| CH1_FREF_DIVIDER |    |             |    |          |    |                  |   |

表 6-31. Address 0x15, CLOCK\_DIVIDERS\_CH1 Field Descriptions

| Bit   | Field       | Type | Reset | Description  |
|-------|-------------|------|-------|--|
| 15:14 | RESERVED    | R/W  | 00    | Reserved. Set to b00.  |
| 13:12 | CH1_FIN_SEL | R/W  | 0000  | Channel 1 Sensor frequency select for differential sensor configuration:<br>b01: divide by 1. Choose for sensor frequencies between 0.01MHz and 8.75MHz<br>b10: divide by 2. Choose for sensor frequencies between 5MHz and 10MHz<br>for single-ended sensor configuration:<br>b10: divide by 2. Choose for sensor frequencies between 0.01MHz and 10MHz |
| 11:10 | RESERVED    | R/W  | 00    | Reserved. Set to b00.  |

**表 6-31. Address 0x15, CLOCK\_DIVIDERS\_CH1 Field Descriptions (续)**

| Bit | Field            | Type | Reset           | Description   |
|-----|------------------|------|-----------------|---|
| 9:0 | CH1_FREF_DIVIDER | R/W  | 00 0000<br>0000 | Channel 1 Reference Divider<br>Sets the divider for Channel 1 reference. Use this to scale the maximum conversion frequency.<br>b00' 0000' 0000: Reserved. Do not use.<br>CH1_FREF_DIVIDER ≥ b00' 0000' 0001: $f_{REF1} = f_{CLK} / CH1\_FREF\_DIVIDER$ |

6.6.24 Address 0x16, CLOCK\_DIVIDERS\_CH2 (FDC2114, FDC2214 only)

图 6-31. Address 0x16, CLOCK\_DIVIDERS\_CH2

|                  |    |             |    |          |    |                  |   |
|------------------|----|-------------|----|----------|----|------------------|---|
| 15               | 14 | 13          | 12 | 11       | 10 | 9                | 8 |
| RESERVED         |    | CH2_FIN_SEL |    | RESERVED |    | CH2_FREF_DIVIDER |   |
| 7                | 6  | 5           | 4  | 3        | 2  | 1                | 0 |
| CH2_FREF_DIVIDER |    |             |    |          |    |                  |   |

表 6-32. Address 0x16, CLOCK\_DIVIDERS\_CH2 Field Descriptions

| Bit   | Field            | Type | Reset           | Description  |
|-------|------------------|------|-----------------|--|
| 15:14 | RESERVED         | R/W  | 00              | Reserved. Set to b00.  |
| 13:12 | CH2_FIN_SEL      | R/W  | 0000            | Channel 2 Sensor frequency select for differential sensor configuration:<br>b01: divide by 1. Choose for sensor frequencies between 0.01MHz and 8.75MHz<br>b10: divide by 2. Choose for sensor frequencies between 5MHz and 10MHz<br>for single-ended sensor configuration:<br>b10: divide by 2. Choose for sensor frequencies between 0.01MHz and 10MHz |
| 11:10 | RESERVED         | R/W  | 00              | Reserved. Set to b00.  |
| 9:0   | CH2_FREF_DIVIDER | R/W  | 00 0000<br>0000 | Channel 2 Reference Divider<br>Sets the divider for Channel 2 reference. Use this to scale the maximum conversion frequency.<br>b00' 0000' 0000: Reserved. Do not use.<br>$CH2\_FREF\_DIVIDER \geq b00' 0000' 0001: f_{REF2} = f_{CLK} / CH2\_FREF\_DIVIDER$   |

6.6.25 Address 0x17, CLOCK\_DIVIDERS\_CH3 (FDC2114, FDC2214 only)

图 6-32. Address 0x17, CLOCK\_DIVIDERS\_CH3

|                  |    |             |    |          |    |                  |   |
|------------------|----|-------------|----|----------|----|------------------|---|
| 15               | 14 | 13          | 12 | 11       | 10 | 9                | 8 |
| RESERVED         |    | CH3_FIN_SEL |    | RESERVED |    | CH3_FREF_DIVIDER |   |
| 7                | 6  | 5           | 4  | 3        | 2  | 1                | 0 |
| CH3_FREF_DIVIDER |    |             |    |          |    |                  |   |

表 6-33. Address 0x17, CLOCK\_DIVIDERS\_CH3

| Bit   | Field       | Type | Reset | Description  |
|-------|-------------|------|-------|--|
| 15:14 | RESERVED    | R/W  | 00    | Reserved. Set to b00.  |
| 13:12 | CH3_FIN_SEL | R/W  | 0000  | Channel 3 Sensor frequency select for differential sensor configuration:<br>b01: divide by 1. Choose for sensor frequencies between 0.01MHz and 8.75MHz<br>b10: divide by 2. Choose for sensor frequencies between 5MHz and 10MHz<br>for single-ended sensor configuration:<br>b10: divide by 2. Choose for sensor frequencies between 0.01MHz and 10MHz |
| 11:10 | RESERVED    | R/W  | 00    | Reserved. Set to b00.  |

**表 6-33. Address 0x17, CLOCK\_DIVIDERS\_CH3 (续)**

| Bit | Field            | Type | Reset           | Description   |
|-----|------------------|------|-----------------|---|
| 9:0 | CH3_FREF_DIVIDER | R/W  | 00 0000<br>0000 | Channel 3 Reference Divider<br>Sets the divider for Channel 3 reference. Use this to scale the maximum conversion frequency.<br>b00' 0000' 0000: reserved<br>$CH3\_FREF\_DIVIDER \geq b00' 0000' 0001: f_{REF3} = f_{CLK} / CH3\_FREF\_DIVIDER$ |

6.6.26 Address 0x18, STATUS

图 6-33. Address 0x18, STATUS

|          |      |          |    |                |                |                |                |
|----------|------|----------|----|----------------|----------------|----------------|----------------|
| 15       | 14   | 13       | 12 | 11             | 10             | 9              | 8              |
| ERR_CHAN |      | RESERVED |    | ERR_WD         | RESERVED       |                |                |
| 7        | 6    | 5        | 4  | 3              | 2              | 1              | 0              |
| RESERVED | DRDY | RESERVED |    | CH0_UNREADCONV | CH1_UNREADCONV | CH2_UNREADCONV | CH3_UNREADCONV |

表 6-34. Address 0x18, STATUS Field Descriptions

| Bit   | Field          | Type | Reset | Description  |
|-------|----------------|------|-------|--|
| 15:14 | ERR_CHAN       | R    | 00    | Error Channel<br>Indicates which channel has generated a Flag or Error. When flagged, any reported error is latched and maintained until either the STATUS register or the DATA_CHx register corresponding to the Error Channel is read.<br>b00: Channel 0 is source of flag or error.<br>b01: Channel 1 is source of flag or error.<br>b10: Channel 2 is source of flag or error (FDC2114, FDC2214 only).<br>b11: Channel 3 is source of flag or error (FDC2114, FDC2214 only). |
| 13:12 | RESERVED       | R    | 00    | Reserved   |
| 11    | ERR_WD         | R    | 0     | Watchdog Timeout Error<br>b0: No Watchdog Timeout error was recorded since the last read of the STATUS register.<br>b1: An active channel has generated a Watchdog Timeout error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.   |
| 10    | ERR_AHW        | R    | 0     | Amplitude High Warning<br>b0: No Amplitude High warning was recorded since the last read of the STATUS register.<br>b1: An active channel has generated an Amplitude High warning. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this warning.  |
| 9     | ERR_ALW        | R    | 0     | Amplitude Low Warning<br>b0: No Amplitude Low warning was recorded since the last read of the STATUS register.<br>b1: An active channel has generated an Amplitude Low warning. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this warning.   |
| 8:7   | RESERVED       | R    | 00    | Reserved   |
| 6     | DRDY           | R    | 0     | Data Ready Flag.<br>b0: No new conversion result was recorded in the STATUS register.<br>b1: A new conversion result is ready. When in Single Channel Conversion, this indicates a single conversion is available. When in sequential mode, this indicates that a new conversion result for all active channels is now available.  |
| 3     | CH0_UNREADCONV | R    | 0     | Channel 0 Unread Conversion b0: No unread conversion is present for Channel 0.<br>b1: An unread conversion is present for Channel 0.<br>Read Register DATA_CH0 to retrieve conversion results.   |
| 2     | CH1_UNREADCONV | R    | 0     | Channel 1 Unread Conversion b0: No unread conversion is present for Channel 1.<br>b1: An unread conversion is present for Channel 1.<br>Read Register DATA_CH1 to retrieve conversion results.   |
| 1     | CH2_UNREADCONV | R    | 0     | Channel 2 Unread Conversion b0: No unread conversion is present for Channel 2.<br>b1: An unread conversion is present for Channel 2.<br>Read Register DATA_CH2 to retrieve conversion results (FDC2114, FDC2214 only)  |
| 0     | CH3_UNREADCONV | R    | 0     | Channel 3 Unread Conversion<br>b0: No unread conversion is present for Channel 3.<br>b1: An unread conversion is present for Channel 3.<br>Read Register DATA_CH3 to retrieve conversion results (FDC2114, FDC2214 only)   |

### 6.6.27 Address 0x19, ERROR\_CONFIG

图 6-34. Address 0x19, ERROR\_CONFIG

|          |    |            |             |             |          |   |           |
|----------|----|------------|-------------|-------------|----------|---|-----------|
| 15       | 14 | 13         | 12          | 11          | 10       | 9 | 8         |
| RESERVED |    | WD_ERR2OUT | AH_WARN2OUT | AL_WARN2OUT | RESERVED |   |           |
| 7        | 6  | 5          | 4           | 3           | 2        | 1 | 0         |
| RESERVED |    | WD_ERR2INT | RESERVED    |             |          |   | DRDY_2INT |

表 6-35. Address 0x19, ERROR\_CONFIG

| Bit   | Field       | Type | Reset  | Description  |
|-------|-------------|------|--------|--|
| 15:14 | RESERVED    | R/W  | 00     | Reserved (set to b000)   |
| 13    | WD_ERR2OUT  | R/W  | 0      | Watchdog Timeout Error to Output Register<br>b0: Do not report Watchdog Timeout errors in the DATA_CHx registers.<br>b1: Report Watchdog Timeout errors in the DATA_CHx.CHx_ERR_WD register field corresponding to the channel that generated the error.   |
| 12    | AH_WARN2OUT | R/W  | 0      | Amplitude High Warning to Output Register<br>b0: Do not report Amplitude High warnings in the DATA_CHx registers.<br>b1: Report Amplitude High warnings in the DATA_CHx.CHx_ERR_AW register field corresponding to the channel that generated the warning. |
| 11    | AL_WARN2OUT | R/W  | 0      | Amplitude Low Warning to Output Register<br>b0: Do not report Amplitude Low warnings in the DATA_CHx registers.<br>b1: Report Amplitude High warnings in the DATA_CHx.CHx_ERR_AW register field corresponding to the channel that generated the warning.   |
| 10:6  | RESERVED    | R/W  | 0 0000 | Reserved (set to b0 0000)  |
| 5     | WD_ERR2INT  | R/W  | 0      | Watchdog Timeout Error to INTB b0: Do not report Under-range errors by asserting INTB pin and STATUS register.<br>b1: Report Watchdog Timeout errors by asserting INTB pin and updating STATUS.ERR_WD register field.                                      |
| 4:1   | Reserved    | R/W  | 0000   | Reserved (set to b000)   |
| 0     | DRDY_2INT   | R/W  | 0      | Data Ready Flag to INTB b0: Do not report Data Ready Flag by asserting INTB pin and STATUS register.<br>b1: Report Data Ready Flag by asserting INTB pin and updating STATUS.DRDY register field.  |

6.6.28 Address 0x1A, CONFIG

图 6-35. Address 0x1A, CONFIG

|             |                  |               |          |                     |          |             |          |
|-------------|------------------|---------------|----------|---------------------|----------|-------------|----------|
| 15          | 14               | 13            | 12       | 11                  | 10       | 9           | 8        |
| ACTIVE_CHAN |                  | SLEEP_MODE_EN | RESERVED | SENSOR_ACTIVATE_SEL | RESERVED | REF_CLK_SRC | RESERVED |
| 7           | 6                | 5             | 4        | 3                   | 2        | 1           | 0        |
| INTB_DIS    | HIGH_CURRENT_DRV | RESERVED      |          |                     |          |             |          |

表 6-36. Address 0x1A, CONFIG Field Descriptions

| Bit   | Field               | Type | Reset   | Description   |
|-------|---------------------|------|---------|---|
| 15:14 | ACTIVE_CHAN         | R/W  | 00      | Active channel selection<br>Selects channel for continuous conversions when MUX_CONFIG.SEQUENTIAL is 0.<br>b00: Perform continuous conversions on Channel 0<br>b01: Perform continuous conversions on Channel 1<br>b10: Perform continuous conversions on Channel 2 (FDC2114, FDC2214 only)<br>b11: Perform continuous conversions on Channel 3 (FDC2114, FDC2214 only) |
| 13    | SLEEP_MODE_EN       | R/W  | 1       | Sleep mode enable<br>Enter or exit low power sleep mode.<br>b0: Device is active.<br>b1: Device is in sleep mode.   |
| 12    | RESERVED            | R/W  | 0       | Reserved. <b>Set to b1.</b>   |
| 11    | SENSOR_ACTIVATE_SEL | R/W  | 1       | Sensor activation mode selection.<br>Set the mode for sensor initialization.<br>b0: Full current activation mode - the FDC drives the maximum sensor current for a shorter sensor activation time.<br>b1: Low power activation mode - the FDC uses the value programmed in DRIVE_CURRENT_CHx during sensor activation to minimize power consumption.                    |
| 10    | RESERVED            | R/W  | 0       | Reserved. <b>Set to b1.</b>   |
| 9     | REF_CLK_SRC         | R/W  | 0       | Select Reference Frequency Source<br>b0: Use Internal oscillator as reference frequency<br>b1: Reference frequency is provided from CLKIN pin.  |
| 8     | RESERVED            | R/W  | 0       | Reserved. Set to b0.  |
| 7     | INTB_DIS            | R/W  | 0       | INTB Disable<br>b0: Asserts INTB pin when status register updates.<br>b1: Does not assert INTB pin when status register updates   |
| 6     | HIGH_CURRENT_DRV    | R/W  | 0       | High Current Sensor Drive<br>b0: The FDC drives all channels with normal sensor current (1.5mA maximum).<br>b1: The FDC drives channel 0 with current >1.5mA.<br>This mode is not supported if AUTOSCAN_EN = b1 (multi-channel mode)  |
| 5:0   | RESERVED            | R/W  | 00 0001 | Reserved Set to b00' 0001   |

### 6.6.29 Address 0x1B, MUX\_CONFIG

图 6-36. Address 0x1B, MUX\_CONFIG

|             |             |    |          |    |          |   |   |
|-------------|-------------|----|----------|----|----------|---|---|
| 15          | 14          | 13 | 12       | 11 | 10       | 9 | 8 |
| AUTOSCAN_EN | RR_SEQUENCE |    | RESERVED |    |          |   |   |
| 7           | 6           | 5  | 4        | 3  | 2        | 1 | 0 |
| RESERVED    |             |    |          |    | DEGLITCH |   |   |

表 6-37. Address 0x1B, MUX\_CONFIG Field Descriptions

| Bit   | Field       | Type | Reset        | Description  |
|-------|-------------|------|--------------|--|
| 15    | AUTOSCAN_EN | R/W  | 0            | Auto-Scan mode enable<br>b0: Continuous conversion on the single channel selected by CONFIG.ACTIVE_CHAN register field.<br>b1: Auto-Scan conversions as selected by MUX_CONFIG.RR_SEQUENCE register field.   |
| 14:13 | RR_SEQUENCE | R/W  | 00           | Auto-Scan sequence configuration<br>Configure multiplexing channel sequence. The FDC performs a single conversion on each channel in the sequence selected, and then restart the sequence continuously.<br>b00: Ch0, Ch1<br>b01: Ch0, Ch1, Ch2 (FDC2114, FDC2214 only)<br>b10: Ch0, Ch1, Ch2, Ch3 (FDC2114, FDC2214 only)<br>b11: Ch0, Ch1 |
| 12:3  | RESERVED    | R/W  | 00 0100 0001 | Reserved. Must be set to 00 0100 0001  |
| 2:0   | DEGLITCH    | R/W  | 111          | Input deglitch filter bandwidth.<br>Select the lowest setting that exceeds the oscillation tank oscillation frequency.<br>b001: 1MHz<br>b100: 3.3MHz<br>b101: 10MHz<br>b111: 33MHz   |

### 6.6.30 Address 0x1C, RESET\_DEV

图 6-37. Address 0x1C, RESET\_DEV

|           |          |    |    |    |             |   |          |
|-----------|----------|----|----|----|-------------|---|----------|
| 15        | 14       | 13 | 12 | 11 | 10          | 9 | 8        |
| RESET_DEV | RESERVED |    |    |    | OUTPUT_GAIN |   | RESERVED |
| 7         | 6        | 5  | 4  | 3  | 2           | 1 | 0        |
| RESERVED  |          |    |    |    |             |   |          |

表 6-38. Address 0x1C, RESET\_DEV Field Descriptions

| Bit   | Field       | Type | Reset       | Description  |
|-------|-------------|------|-------------|--|
| 15    | RESET_DEV   | R/W  | 0           | Device Reset<br>Write b1 to reset the device. Will always readback 0.  |
| 14:11 | RESERVED    | R/W  | 0000        | Reserved. Set to b0000   |
| 10:9  | OUTPUT_GAIN | R/W  | 00          | Output gain control (FDC2112, FDC2114 only)<br>00: Gain = 1 (0 bits shift)<br>01: Gain = 4 (2 bits shift)<br>10: Gain = 8 (3 bits shift)<br>11: Gain = 16 (4 bits shift) |
| 8:0   | RESERVED    | R/W  | 0 0000 0000 | Reserved, Set to b0 0000 0000  |

6.6.31 Address 0x1E, DRIVE\_CURRENT\_CH0

图 6-38. Address 0x1E, DRIVE\_CURRENT\_CH0

|            |    |    |    |    |          |   |   |
|------------|----|----|----|----|----------|---|---|
| 15         | 14 | 13 | 12 | 11 | 10       | 9 | 8 |
| CH0_IDRIVE |    |    |    |    | RESERVED |   |   |
| 7          | 6  | 5  | 4  | 3  | 2        | 1 | 0 |
| RESERVED   |    |    |    |    |          |   |   |

表 6-39. Address 0x1E, DRIVE\_CURRENT\_CH0 Field Descriptions

| Bit   | Field      | Type | Reset            | Description   |
|-------|------------|------|------------------|---|
| 15:11 | CH0_IDRIVE | R/W  | 0000 0           | Channel 0 Sensor drive current<br>This field defines the Drive Current used during the settling + conversion time of Channel 0 sensor clock. Set such that $1.2V \leq \text{sensor oscillation amplitude (pk)} \leq 1.8V$<br>00000: 0.016mA<br>00001: 0.018mA<br>00010: 0.021mA<br>00011: 0.025mA<br>00100: 0.028mA<br>00101: 0.033mA<br>00110: 0.038mA<br>00111: 0.044mA<br>01000: 0.052mA<br>01001: 0.060mA<br>01010: 0.069mA<br>01011: 0.081mA<br>01100: 0.093mA<br>01101: 0.108mA<br>01110: 0.126mA<br>01111: 0.146mA<br>10000: 0.169mA<br>10001: 0.196mA<br>10010: 0.228mA<br>10011: 0.264mA<br>10100: 0.307mA<br>10101: 0.356mA<br>10110: 0.413mA<br>10111: 0.479mA<br>11000: 0.555mA<br>11001: 0.644mA<br>11010: 0.747mA<br>11011: 0.867mA<br>11100: 1.006mA<br>11101: 1.167mA<br>11110: 1.354mA<br>11111: 1.571mA |
| 10:0  | RESERVED   | -    | 000 0000<br>0000 | Reserved  |

### 6.6.32 Address 0x1F, DRIVE\_CURRENT\_CH1

图 6-39. Address 0x1F, DRIVE\_CURRENT\_CH1

|            |    |    |    |    |    |          |   |
|------------|----|----|----|----|----|----------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9        | 8 |
| CH1_IDRIVE |    |    |    |    |    | RESERVED |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1        | 0 |
| RESERVED   |    |    |    |    |    |          |   |

表 6-40. Address 0x1F, DRIVE\_CURRENT\_CH1 Field Descriptions

| Bit   | Field      | Type | Reset            | Description  |
|-------|------------|------|------------------|--|
| 15:11 | CH1_IDRIVE | R/W  | 0000 0           | Channel 1 Sensor drive current<br>This field defines the drive current used during the settling + conversion time of Channel 1 sensor clock. Set such that $1.2V \leq \text{sensor oscillation amplitude (pk)} \leq 1.8V$<br>00000: 0.016mA<br>00001: 0.018mA<br>00010: 0.021mA<br>...<br>11111: 1.571mA |
| 10:0  | RESERVED   | -    | 000 0000<br>0000 | Reserved   |

### 6.6.33 Address 0x20, DRIVE\_CURRENT\_CH2 (FDC2114 / FDC2214 only)

图 6-40. Address 0x20, DRIVE\_CURRENT\_CH2

|            |    |    |    |    |    |          |   |
|------------|----|----|----|----|----|----------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9        | 8 |
| CH2_IDRIVE |    |    |    |    |    | RESERVED |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1        | 0 |
| RESERVED   |    |    |    |    |    |          |   |

表 6-41. Address 0x20, DRIVE\_CURRENT\_CH2 Field Descriptions

| Bit   | Field      | Type | Reset            | Description  |
|-------|------------|------|------------------|--|
| 15:11 | CH2_IDRIVE | R/W  | 0000 0           | Channel 2 Sensor drive current<br>This field defines the drive current to be used during the settling + conversion time of Channel 2 sensor clock. Set such that $1.2V \leq \text{sensor oscillation amplitude (pk)} \leq 1.8V$<br>00000: 0.016mA<br>00001: 0.018mA<br>00010: 0.021mA<br>...<br>11111: 1.571mA |
| 10:0  | RESERVED   | -    | 000 0000<br>0000 | Reserved   |

6.6.34 Address 0x21, DRIVE\_CURRENT\_CH3 (FDC2114 / FDC2214 only)

图 6-41. Address 0x21, DRIVE\_CURRENT\_CH3

|            |    |    |    |    |    |          |   |
|------------|----|----|----|----|----|----------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9        | 8 |
| CH3_IDRIVE |    |    |    |    |    | RESERVED |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1        | 0 |
| RESERVED   |    |    |    |    |    |          |   |

表 6-42. DRIVE\_CURRENT\_CH3 Field Descriptions

| Bit   | Field      | Type | Reset            | Description  |
|-------|------------|------|------------------|--|
| 15:11 | CH3_IDRIVE | R/W  | 0000 0           | Channel 3 Sensor drive current<br>This field defines the drive current to be used during the settling + conversion time of Channel 3 sensor clock. Set such that $1.2V \leq \text{sensor oscillation amplitude (pk)} \leq 1.8V$<br>00000: 0.016mA<br>00001: 0.018mA<br>00010: 0.021mA<br>...<br>11111: 1.571mA |
| 10:0  | RESERVED   | -    | 000 0000<br>0000 | Reserved   |

6.6.35 Address 0x7E, MANUFACTURER\_ID

图 6-42. Address 0x7E, MANUFACTURER\_ID

|                 |    |    |    |    |    |   |   |
|-----------------|----|----|----|----|----|---|---|
| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MANUFACTURER_ID |    |    |    |    |    |   |   |
| 7               | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| MANUFACTURER_ID |    |    |    |    |    |   |   |

表 6-43. Address 0x7E, MANUFACTURER\_ID Field Descriptions

| Bit  | Field           | Type | Reset                  | Description              |
|------|-----------------|------|------------------------|--------------------------|
| 15:0 | MANUFACTURER_ID | R    | 0101 0100<br>0100 1001 | Manufacturer ID = 0x5449 |

6.6.36 Address 0x7F, DEVICE\_ID

图 6-43. Address 0x7F, DEVICE\_ID

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEVICE_ID |   |   |   |   |   |   |   |

表 6-44. Address 0x7F, DEVICE\_ID Field Descriptions

| Bit | Field     | Type | Reset                  | Description   |
|-----|-----------|------|------------------------|---|
| 7:0 | DEVICE_ID | R    | 0011 0000<br>0101 0100 | Device ID<br>0x3054 (FDC2112, FDC2114 only)<br>0x3055 (FDC2212, FDC2214 only) |

## 7 Application and Implementation

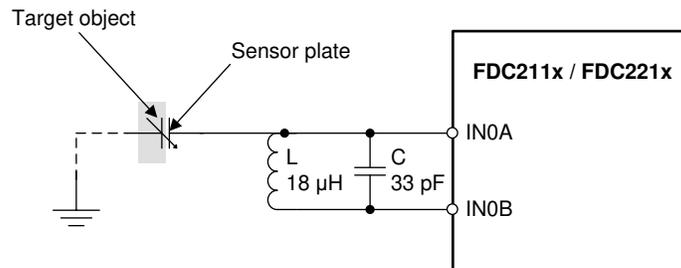
### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 7.1 Application Information

#### 7.1.1 Sensor Configuration

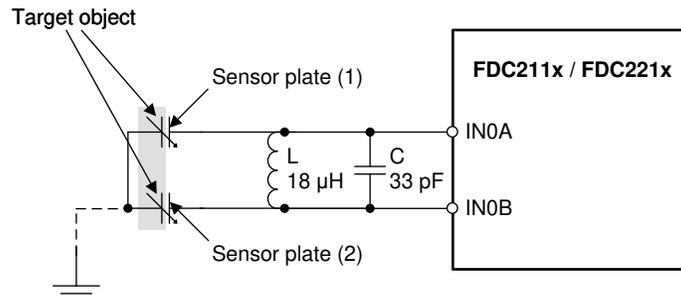
The FDC supports two sensor configurations. Both configurations use an LC tank to set the frequency of oscillation. A typical choice is an 18- $\mu$ H shielded SMD inductor in parallel with a 33pF capacitor, which result in a 6.5MHz oscillation frequency. In the single-ended configuration in 图 7-1, a conductive plate is connected IN0A. Together with a target object, the conductive plate forms a variable capacitor.



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图 7-1. Single-Ended Sensor Configuration

In the differential sensor configuration in 图 7-2, one conductive plate is connected to IN0A, and a second conductive plate is connected to IN0B. Together, they form a variable capacitor. When using an single-ended sensor configuration, set CHx\_FIN\_SEL to b10 (divide by 2).



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图 7-2. Differential Sensor Configuration

The single-ended configuration allows higher sensing range than the differential configuration for a given total sensor plate area. In applications in which high sensitivity at close proximity is desired, the differential configuration performs better than the single-ended configuration.

### 7.1.2 Shield

in order to minimize interference from external objects, some applications require an additional plate which acts as a shield. The shield can either be:

- actively driven shield: The shield is a buffered signal of the INxA pin. The signal is buffered by an external amplifier with a gain of 1.
- passive shield: The shield is connected to GND. Adding a passive shield decreases sensitivity of the sensor, but is dependent on the distance between the sensing plate and the shield. Adjust the distance between the sensing plate and the shield to achieve the required sensitivity.

### 7.1.3 Power-Cycled Applications

For applications which do not require high sample rates or maximum conversion resolution, the total active conversion time of the FDC can be minimized to reduce power consumption. This can be done by either by using sleep mode or shutdown mode during times in which conversions are not required (see [Device Functional Modes](#)).

As an example, for an application which only needs 10 samples per second with a resolution of 16 bits can utilize the low-power modes. The sensor requires SETTLECOUNT = 16 and IDRIVE of 01111b (0.146mA). Given FREF = 40MHz and RCOUNT = 4096 will provide the resolution required. This corresponds to  $4096 \times 16 \times 10 / 40\text{MHz} \rightarrow 16.4\text{ms}$  of active conversion time per second. Start-up time and channel switch delay account for an additional 0.34ms. For the remainder of the time, the device can be in sleep mode: Therefore, the average current is  $19.4\text{ms} \times 3.6\text{mA}$  active current +  $980.6\text{ms}$  of  $35\mu\text{A}$  of sleep current, which is approximately  $104.6\mu\text{A}$  of average supply current. Sleep mode retains register settings and therefore requires less I<sup>2</sup>C writes to wake up the FDC than shutdown mode.

Greater current savings can be realized by use of shutdown mode during inactive periods. In shutdown mode, device configuration is not retained, so the device must be configured for each sample. For this example, configuring each sample takes approximately 1.2ms (13 registers  $\times$  92.5  $\mu\text{s}$  per register). The total active time is 20.6ms. The average current is  $20\text{ms} \times 3.6\text{mA}$  active current +  $980\text{ms} \times 2\mu\text{A}$  of shutdown current, which is approximately  $75\mu\text{A}$  of average supply current.

For further information on power-cycled applications, refer to [Power Reduction Techniques for the FDC2214/2212/2114/2112 in Capacitive Sensing Applications](#).

### 7.1.4 Inductor Self-Resonant Frequency

Every inductor has a distributed parasitic capacitance, which is dependent on construction and geometry. At the self-resonant frequency (SRF), the reactance of the inductor cancels the reactance of the parasitic capacitance. Above the SRF, the inductor electrically appears to be a capacitor. The parasitic capacitance is not well-controlled or stable, therefore TI recommends  $f_{\text{SENSOR}} < 0.8 \times f_{\text{SR}}$ .

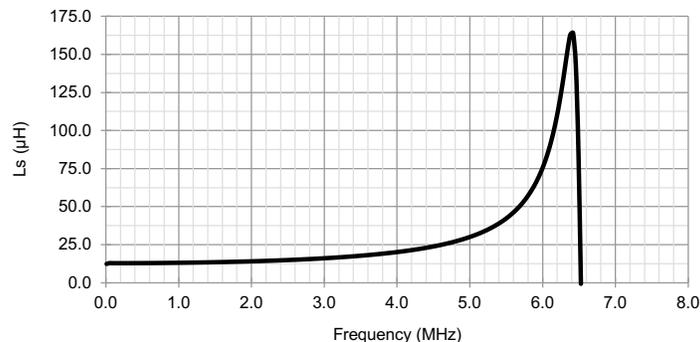


图 7-3. Example Coil Inductance vs Frequency

The example inductor in 图 7-3, has a SRF at 6.38MHz; therefore, the inductor must not be operated above  $0.8 \times 6.38\text{MHz}$ , or 5.1MHz.

### 7.1.5 Application Curves for Proximity Sensing

*Common test conditions (unless specified otherwise):* Sensor capacitor: 1 layer, 20.9 × 13.9mm, Bourns CMH322522-180KL sensor inductor with L=18μH and 33pF 1% COG/NP0 Target: Grounded aluminum plate (176 × 123mm), Channel = Channel 0 (continuous mode) CLKIN = 40MHz, CHx\_FIN\_SEL = b10, CHx\_FREF\_DIVIDER = b00 0000 0001 CH0\_RCOUNT = 0xFFFF, SETTLECOUNT\_CH0 = 0x0100, DRIVE\_CURRENT\_CH0 = 0x7800

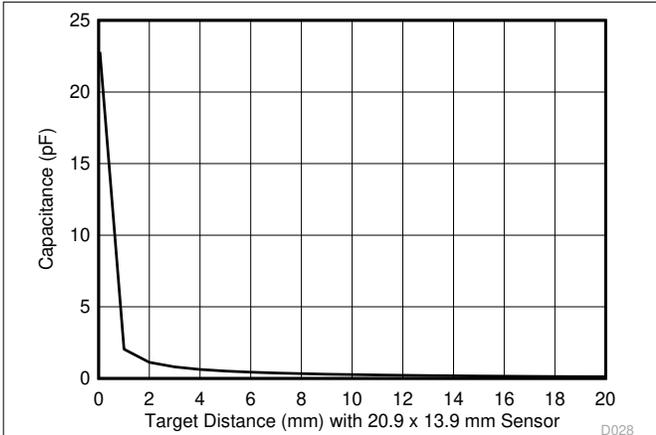


图 7-4. FDC2212 / FDC2214: Capacitance vs Target Distance (0mm to 20mm)

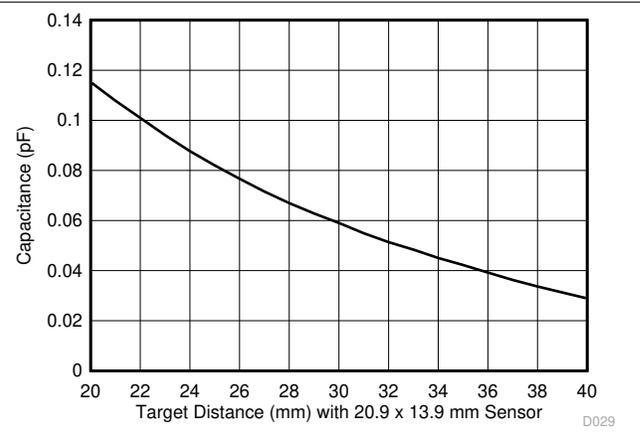


图 7-5. FDC2112 / FDC2114: Capacitance vs Target Distance (20mm to 40mm)

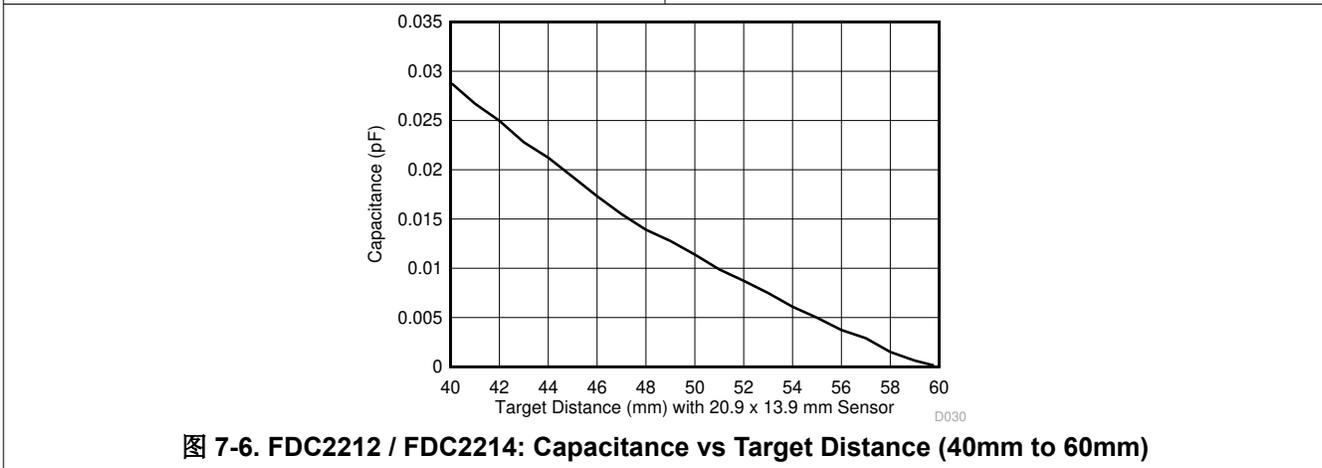


图 7-6. FDC2212 / FDC2214: Capacitance vs Target Distance (40mm to 60mm)

## 7.2 Typical Application

The FDC can be used to measure liquid level in non-conductive containers. Due to very high excitation rate capability, the FDC is able to measure soapy water, ink, soap, and other conductive liquids. Capacitive sensors can be attached to the outside of the container or be located remotely from the container, allowing for contactless measurements.

The working principle is based on a ratiometric measurement; 图 7-7 shows a possible system implementation which uses three electrodes. The level electrode provides a capacitance value proportional to the liquid level. The reference environmental electrode and the reference liquid electrode are used as references. The reference liquid electrode accounts for the liquid dielectric constant and its variation, while the reference environmental electrode is used to compensate for any other environmental variations that are not due to the liquid itself. Note that the reference environmental electrode and the reference liquid electrode are the same physical size (hREF).

For this application, single-ended measurements on the active channels are appropriate, as the tank is grounded. Use 方程式 7 to determine the liquid level from the measured capacitances:

$$Level = h_{ref} \frac{C_{Lev} - C_{Lev}(0)}{C_{RL} - C_{RE}} \quad (7)$$

where

- $C_{RE}$  is the capacitance of the reference environmental electrode,
- $C_{RL}$  is the capacitance of the reference liquid electrode,
- $C_{Lev}$  is the current value of the capacitance measured at the level electrode sensor,
- $C_{Lev}(0)$  is the capacitance of the Level electrode when the container is empty, and
- $h_{REF}$  is the height in the desired units of the container or liquid reference electrodes.

The ratio between the capacitance of the level and the reference electrodes allows simple calculation of the liquid level inside the container itself. Very high sensitivity values (that is, many LSB/mm) can be obtained due to the high resolution of the FDC2x1x, even when the sensors are located remotely from the container. Note that this approach assumes that the container has a uniform cross section from top to bottom, so that each incremental increase or decrease in the liquid represents a change in volume that is directly related to the height of the liquid.

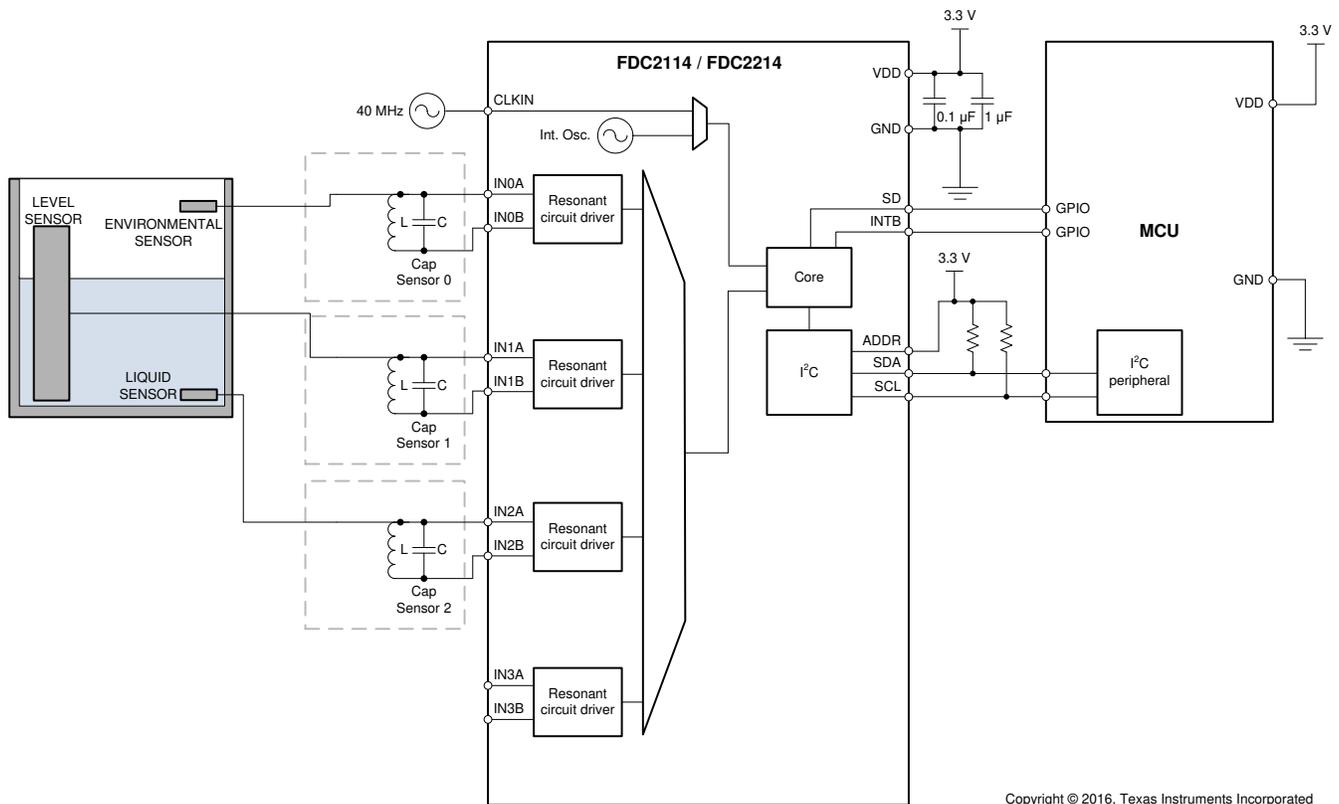


图 7-7. FDC (Liquid Level Measurement)

### 7.2.1 Design Requirements

Make sure the liquid level measurement is independent of the liquid, which can be achieved using the 3-electrode design described above. Moreover, isolate the sensor from environmental interferences such as a human body, other objects, or EMI.

## 7.2.2 Detailed Design Procedure

In capacitive sensing systems, the design of the sensor plays an important role in determining system performance and capabilities. In most cases the sensor is simply a metal plate that can be designed on the PCB.

The sensor used in this example is implemented with a two-layer PCB. On the top layer, which faces the tank, there are the 3 electrodes (reference environmental, reference liquid, and level) with a ground plane surrounding the electrodes.

Depending on the shape of the container, the FDC can be located on the sensor PCB to minimize the length of the traces between the input channels and the sensors. In case the shape of the container or other mechanical constraints do not allow having the sensors and the FDC on the same PCB, the traces which connect the channels to the sensor need to be shielded with the appropriate shield.

### 7.2.2.1 Recommended Initial Register Configuration Values

The application requires 100SPS ( $T_{\text{SAMPLE}} = 10\text{ms}$ ). A sensor with an 18- $\mu\text{H}$  inductor and a 33pF capacitor is used. Additional pin, trace, and wire capacitance accounts for 20pF, so the total capacitance is 53pF.

Using L and C,  $f_{\text{SENSOR}} = 1/2 \pi \sqrt{LC} = 1/2 \pi \sqrt{(18 \times 10^{-6} \times 50 \times 10^{-12})} = 5.15\text{MHz}$ . This represents the maximum sensor frequency. When the sensor capacitance is added, the frequency decreases.

Using a system controller clock of 40MHz applied to the CLKIN pin allows flexibility for setting the internal clock frequencies. The sensor coils are connected to channel 0 (IN0A and IN0B pins), channel 1 (IN1A and IN1B pins), and channel 2 (IN2A and IN2B pins).

After powering on the FDC, the FDC enters into Sleep Mode. Program the registers as follows (example sets registers for channel 0 only; channel 1 and channel 2 registers can use equivalent configuration):

1. Set the dividers for channel 0.
  - a. The sensor is in a single-ended configuration, therefore set the sensor frequency select register to 2, which means setting field CH0\_FIN\_SEL to b10.
  - b. The design constraint for  $f_{\text{REF0}}$  is  $> 4 \times f_{\text{SENSOR}}$ . To satisfy this constraint,  $f_{\text{REF0}}$  must be greater than 20.6MHz, so set the reference divider to 1. This is done by setting the CH0\_FREF\_DIVIDER field to 0x01.
  - c. The combined value for Chan. 0 divider register (0x14) is 0x2001.
2. Sensor drive current: to ensure that the oscillation amplitude is between 1.2V and 1.8V, measure the oscillation amplitude on an oscilloscope and adjust the IDRIVE value, or use the integrated FDC GUI feature to determine the optimal setting. In this case, set the IDRIVE value to 15 (decimal), which results in an oscillation amplitude of 1.68V(pk). Set the INIT\_DRIVE current field to 0x00. The combined value for the DRIVE\_CURRENT\_CH0 register (addr 0x1E) is 0x7C00.
3. Program the settling time for Channel 0 (see [Multi-Channel and Single-Channel Operation](#)).
  - a.  $\text{CH}_x\text{ SETTLECOUNT} > V_{\text{pk}} \times f_{\text{REFx}} \times C \times \pi^2 / (32 \times \text{IDRIVE}_x) \rightarrow 7.5$ , rounded up to 8. To provide margin to account for system tolerances, a higher value of 10 is chosen.
  - b. Program Register 0x10 to a minimum of 10.
  - c. The settle time is:  $(10 \times 16)/40,000,000 = 4\mu\text{s}$
  - d. The value for Channel 0 SETTLECOUNT register (0x10) is 0x000A.
4. The channel switching delay is approximately  $1 \mu\text{s}$  for  $f_{\text{REF}} = 40\text{MHz}$  (see [Multi-Channel and Single-Channel Operation](#))
5. Set the conversion time by programming the reference count for Channel 0. The budget for the conversion time is:  $1/N \times (T_{\text{SAMPLE}} - \text{settling time} - \text{channel switching delay}) = 1/3 (10,000 - 4 - 1) = 3.33\text{ms}$ 
  - a. To determine the conversion time register value, use the following equation and solve for CH0\_RCOUNT: Conversion Time ( $t_{\text{C0}}$ ) =  $(\text{CH0\_RCOUNT} \times 16)/f_{\text{REF0}}$ .
  - b. This results in CH0\_RCOUNT having a value of 8329 decimal (rounded down). Note that this yields an ENOB > 13 bits.

- c. Set the CH0\_RCOUNT register (0x08) to 0x2089.
6. Use the default values for the ERROR\_CONFIG register (address 0x19). By default, no interrupts are enabled
7. Program the MUX\_CONFIG register
  - a. Set the AUTOSCAN\_EN to b1 bit to enable sequential mode
  - b. Set RR\_SEQUENCE to b10 to enable data conversion on three channels (channel 0, channel 1, channel 2)
  - c. Set DEGLITCH to b101 to set the input deglitch filter bandwidth to 10MHz, the lowest setting that exceeds the oscillation tank frequency.
  - d. The combined value for the MUX\_CONFIG register (address 0x1B) is 0xC20D
8. Finally, program the CONFIG register as follows:
  - a. Set the ACTIVE\_CHAN field to b00 to select channel 0.
  - b. Set SLEEP\_MODE\_EN field to b0 to enable conversion.
  - c. Set SENSOR\_ACTIVATE\_SEL = b0, for full current drive during sensor activation
  - d. Set the REF\_CLK\_SRC field to b1 to use the external clock source.
  - e. Set the other fields to their default values.
  - f. The combined value for the CONFIG register (address 0x1A) is 0x1601.

We then read the conversion results for channel 0 to channel 2 every 10ms from register addresses 0x00 to 0x05.

Based on the example configuration above, TI recommends the following register write sequence is recommended:

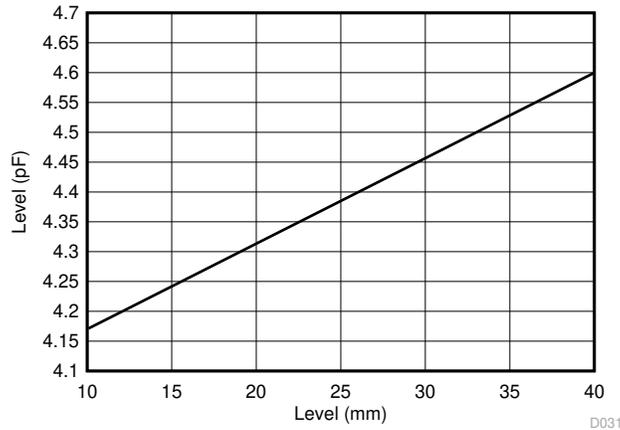
**表 7-1. Recommended Initial Register Configuration Values (Multi-Channel Operation)**

| ADDRESS | VALUE  | REGISTER NAME     | COMMENTS   |
|---------|--------|-------------------|--|
| 0x08    | 0x8329 | RCOUNT_CH0        | Reference count calculated from timing requirements (100SPS) and resolution requirements   |
| 0x09    | 0x8329 | RCOUNT_CH1        | Reference count calculated from timing requirements (100SPS) and resolution requirements   |
| 0x0A    | 0x8329 | RCOUNT_CH2        | Reference count calculated from timing requirements (100SPS) and resolution requirements   |
| 0x10    | 0x000A | SETTLECOUNT_CH0   | Minimum settling time for chosen sensor  |
| 0x11    | 0x000A | SETTLECOUNT_CH1   | Minimum settling time for chosen sensor  |
| 0x12    | 0x000A | SETTLECOUNT_CH2   | Minimum settling time for chosen sensor  |
| 0x14    | 0x2002 | CLOCK_DIVIDER_CH0 | CH0_FIN_DIVIDER = 1, CH0_FREF_DIVIDER = 2  |
| 0x15    | 0x2002 | CLOCK_DIVIDER_CH1 | CH1_FIN_DIVIDER = 1, CH1_FREF_DIVIDER = 2  |
| 0x16    | 0x2002 | CLOCK_DIVIDER_CH2 | CH1_FIN_DIVIDER = 1, CH1_FREF_DIVIDER = 2  |
| 0x19    | 0x0000 | ERROR_CONFIG      | Can be changed from default to report status and error conditions  |
| 0x1B    | 0xC20D | MUX_CONFIG        | Enable Ch 0, Ch 1, and Ch 2 (sequential mode), set Input deglitch bandwidth to 10MHz   |
| 0x1E    | 0x7C00 | DRIVE_CURRENT_CH0 | Sets sensor drive current on ch 0  |
| 0x1F    | 0x7C00 | DRIVE_CURRENT_CH1 | Sets sensor drive current on ch 1  |
| 0x20    | 0x7C00 | DRIVE_CURRENT_CH2 | Sets sensor drive current on ch 2  |
| 0x1A    | 0x1601 | CONFIG            | Enable full current drive during sensor activation, select external clock source, wake up device to start conversion. This register write must occur last because device configuration is not permitted while the FDC is in active mode. |

### 7.2.3 Application Curve

A liquid level sensor with 3 electrodes like the one shown in the schematic was connected to the EVM. The plot shows the capacitance measured by Level sensor at different levels of liquid in the tank. The capacitance of the

Reference Liquid and Reference Environmental sensors have a steady value because they experience consistent exposure to liquid and air, while the capacitance of the level sensor (Level) increases linearly with the height of the liquid in the tank.



**图 7-8. Electrode Capacitance vs Liquid Level**

### 7.3 Best Design Practices

- Do leave a small gap between sensor plates in differential configurations. TI recommends a 2mm to 3mm minimum separation.
- The FDC does not support hot-swapping of the sensors. Do not hot-swap sensors, for example by using external multiplexers.

### 7.4 Power Supply Recommendations

The FDC requires a voltage supply within 2.7V and 3.6V. TI recommends multilayer ceramic bypass X7R capacitors of 0.1  $\mu$ F and 1  $\mu$ F between the VDD and GND pins. If the supply is located more than a few inches from the FDC, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10  $\mu$ F is a typical choice.

The optimum placement is closest to the VDD and GND pins of the device. Take care to minimize the loop area formed by the bypass capacitor connection, the VDD pin, and the GND pin of the device. See [图 7-9](#) and [图 7-12](#) for layout examples.

### 7.5 Layout

#### 7.5.1 Layout Guidelines

- Avoid long traces to connect the sensor to the FDC. Short traces reduce parasitic capacitances between sensor inductor and offer higher system performance.
- Systems that require matched channel response need to have matched trace length on all active channels.

#### 7.5.2 Layout Examples

[图 7-9](#) to [图 7-12](#) show the FDC2114 / FDC2214 evaluation module (EVM) layout.

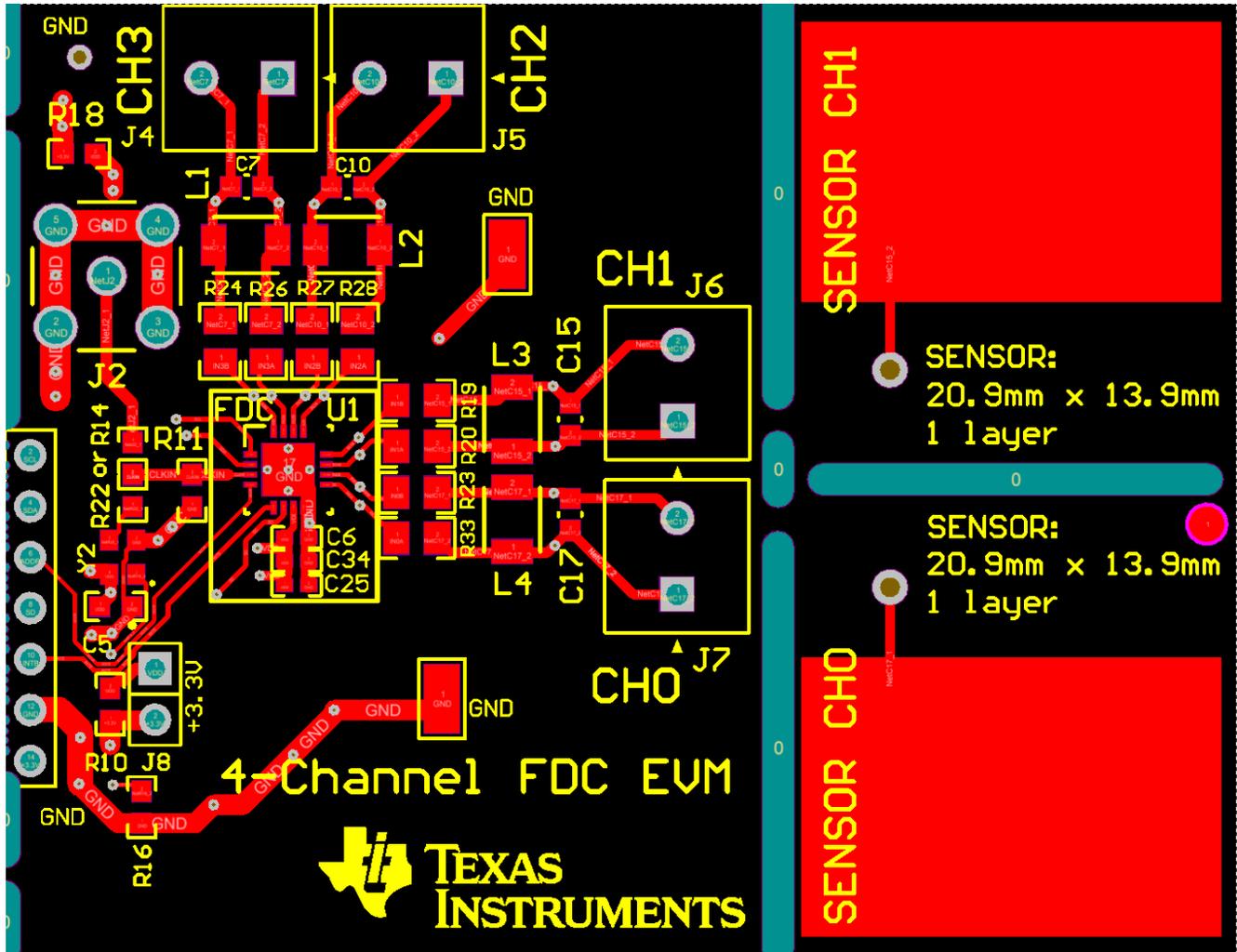


图 7-9. Example PCB Layout: Top Layer (Signal)

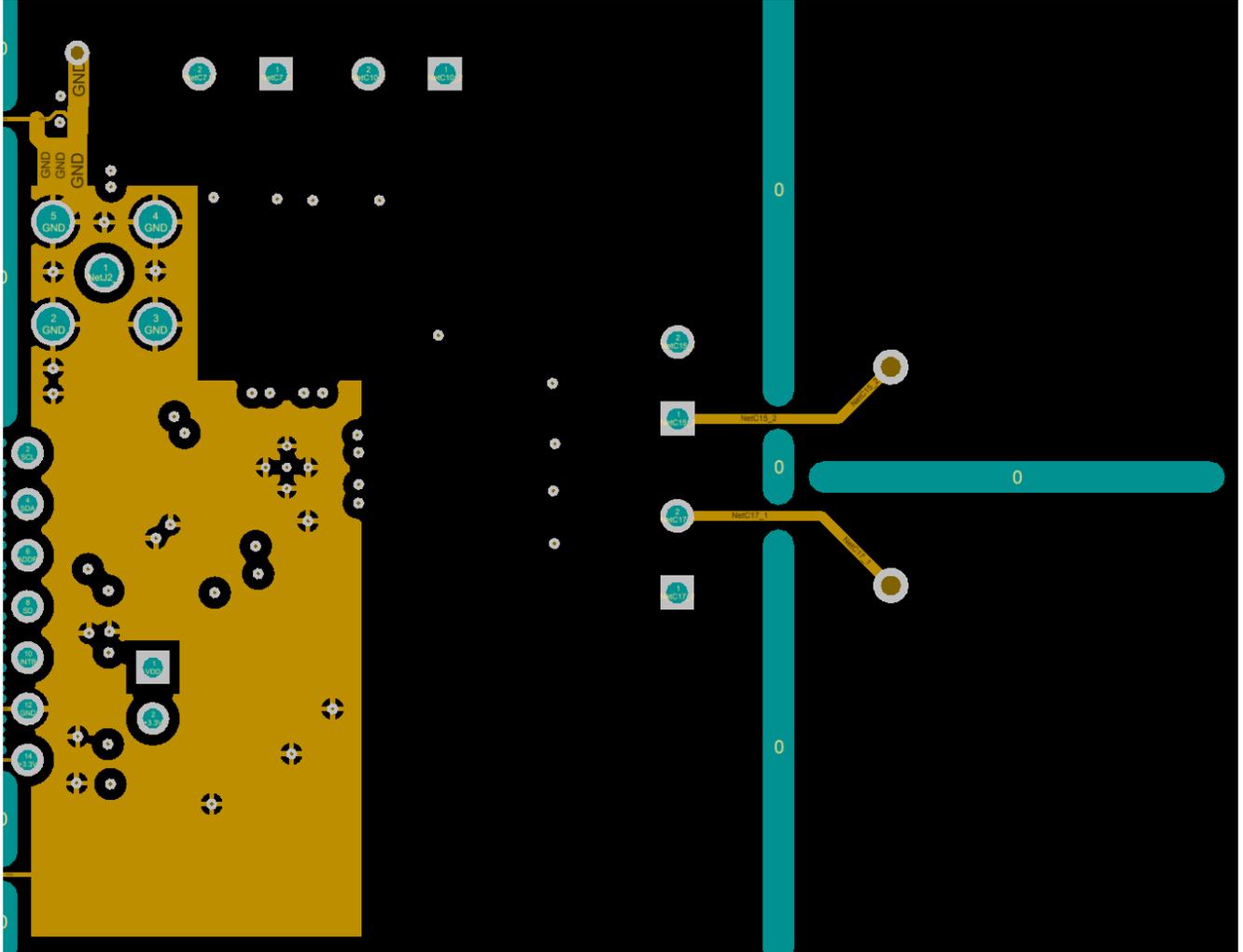


图 7-10. Example PCB Layout: Mid-Layer 1 (GND)

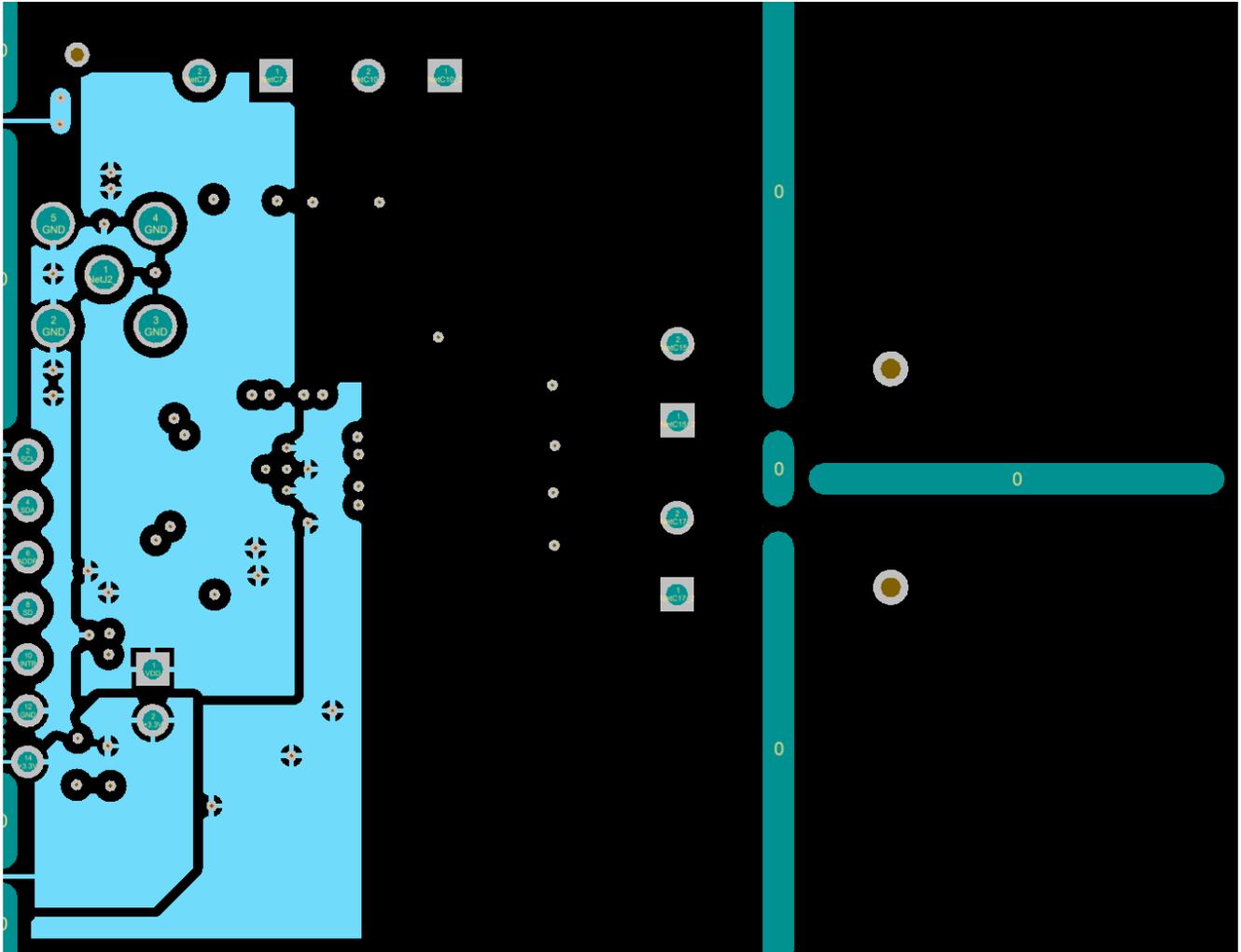


图 7-11. Example PCB Layout: Mid-Layer 2 (Power)



## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 Development Support

For related links, see the following:

Texas Instruments' WEBENCH® tool: <http://www.ti.com/webench>

### 8.2 Documentation Support

#### 8.2.1 Related Documentation

For related documentation, refer to the following:

For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953)

### 8.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

### Changes from Revision \* (May 2016) to Revision A (October 2024)

Page

|  |   |
|--|---|
| • 将数据表标题从“FDC2112-Q1、FDC2114-Q1、FDC2212-Q1、FDC2214-Q1 适用于电容式感应的多通道 12 位或 28 位电容数字转换器 (FDC)”更改为“FDC2x1x-Q1 适用于电容式感应应用的多通道、高分辨率、电容数字转换器” ..... | 1 |
| • 更新了整个文档中的表格、图和交叉参考的编号格式.....   | 1 |
| • 将提到 I <sup>2</sup> C 的旧术语实例通篇更改为控制器和目标.....  | 1 |
| • 将 <a href="#">器件信息</a> 表更改为 <a href="#">封装信息</a> .....   | 1 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">FDC2112QDNTRQ1</a> | Active        | Production           | WSON (DNT)   12 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | FDC2112<br>Q1       |
| FDC2112QDNTRQ1.B               | Active        | Production           | WSON (DNT)   12 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | FDC2112<br>Q1       |
| <a href="#">FDC2114QRGHRQ1</a> | Active        | Production           | WQFN (RGH)   16 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | FC2114Q             |
| FDC2114QRGHRQ1.B               | Active        | Production           | WQFN (RGH)   16 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | FC2114Q             |
| <a href="#">FDC2114QRGHTQ1</a> | Obsolete      | Production           | WQFN (RGH)   16 | -                     | -           | Call TI                              | Call TI                           | -40 to 125   | FC2114Q             |
| <a href="#">FDC2212QDNTRQ1</a> | Active        | Production           | WSON (DNT)   12 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | FDC2212<br>Q1       |
| FDC2212QDNTRQ1.B               | Active        | Production           | WSON (DNT)   12 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | FDC2212<br>Q1       |
| <a href="#">FDC2212QDNTRQ1</a> | Obsolete      | Production           | WSON (DNT)   12 | -                     | -           | Call TI                              | Call TI                           | -40 to 125   | FDC2212<br>Q1       |
| <a href="#">FDC2214QRGHRQ1</a> | Active        | Production           | WQFN (RGH)   16 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | FC2214Q             |
| FDC2214QRGHRQ1.B               | Active        | Production           | WQFN (RGH)   16 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | FC2214Q             |
| <a href="#">FDC2214QRGHTQ1</a> | Obsolete      | Production           | WQFN (RGH)   16 | -                     | -           | Call TI                              | Call TI                           | -40 to 125   | FC2214Q             |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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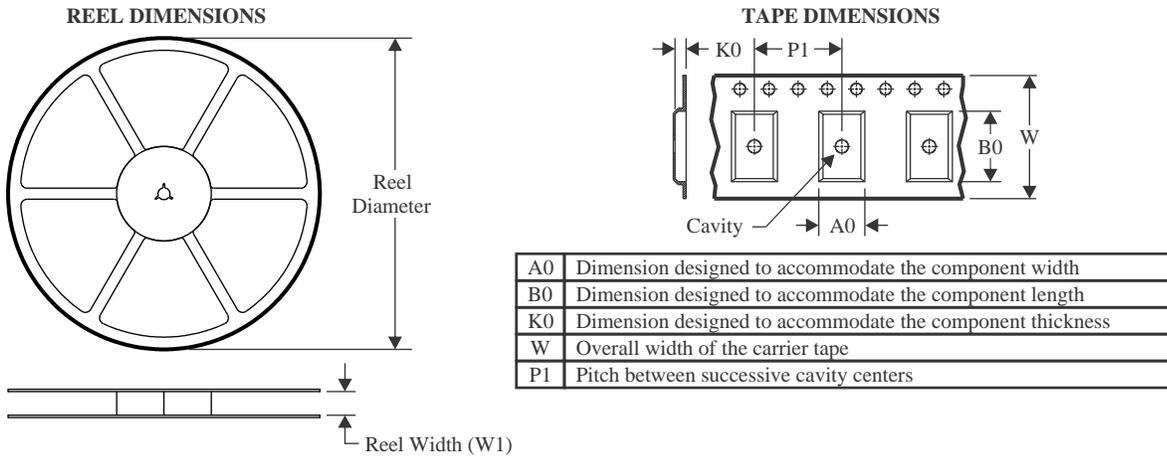
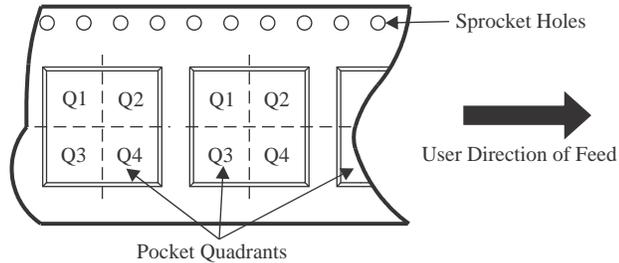
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF FDC2112-Q1, FDC2114-Q1, FDC2212-Q1, FDC2214-Q1 :**

- Catalog : [FDC2112](#), [FDC2114](#), [FDC2212](#), [FDC2214](#)

NOTE: Qualified Version Definitions:

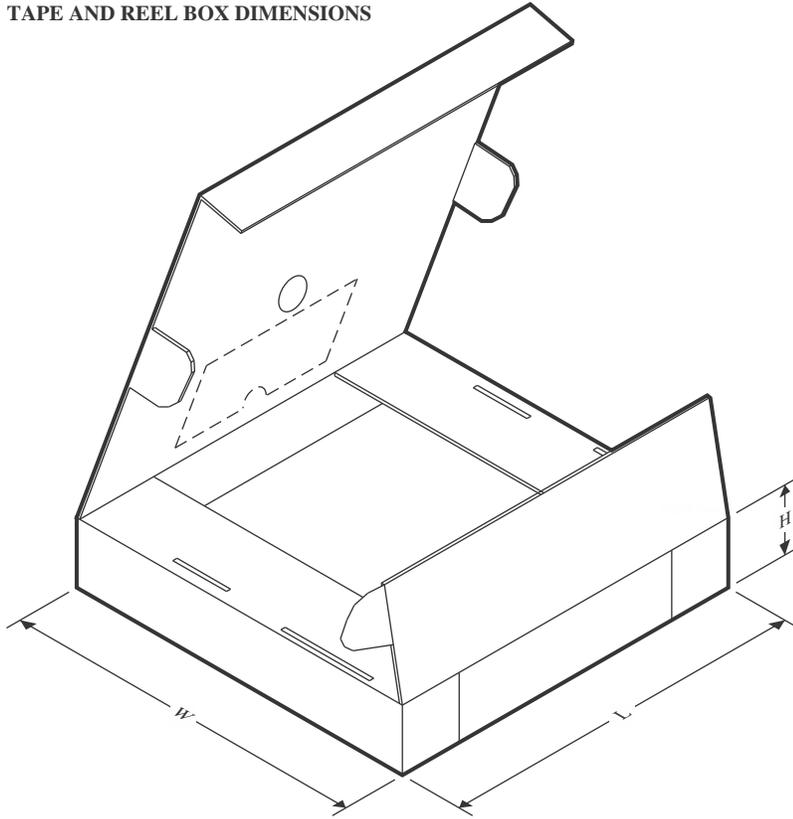
- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| FDC2112QDNTRQ1 | WSON         | DNT             | 12   | 4500 | 330.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |
| FDC2114QRGHRQ1 | WQFN         | RGH             | 16   | 4500 | 330.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |
| FDC2212QDNTRQ1 | WSON         | DNT             | 12   | 4500 | 330.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |
| FDC2214QRGHRQ1 | WQFN         | RGH             | 16   | 4500 | 330.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |

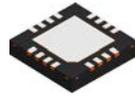
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| FDC2112QDNTRQ1 | WSON         | DNT             | 12   | 4500 | 356.0       | 356.0      | 36.0        |
| FDC2114QRGHRQ1 | WQFN         | RGH             | 16   | 4500 | 356.0       | 356.0      | 36.0        |
| FDC2212QDNTRQ1 | WSON         | DNT             | 12   | 4500 | 356.0       | 356.0      | 36.0        |
| FDC2214QRGHRQ1 | WQFN         | RGH             | 16   | 4500 | 356.0       | 356.0      | 36.0        |

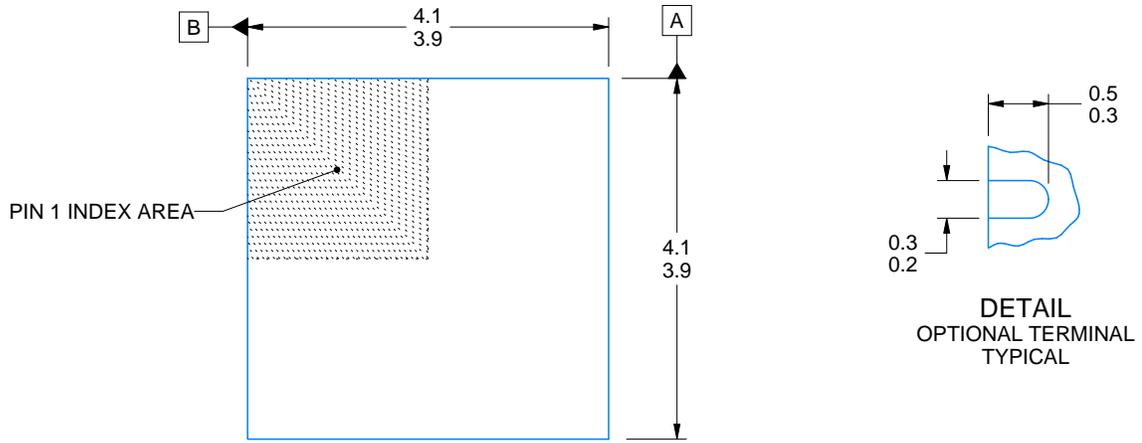
# RGH0016A



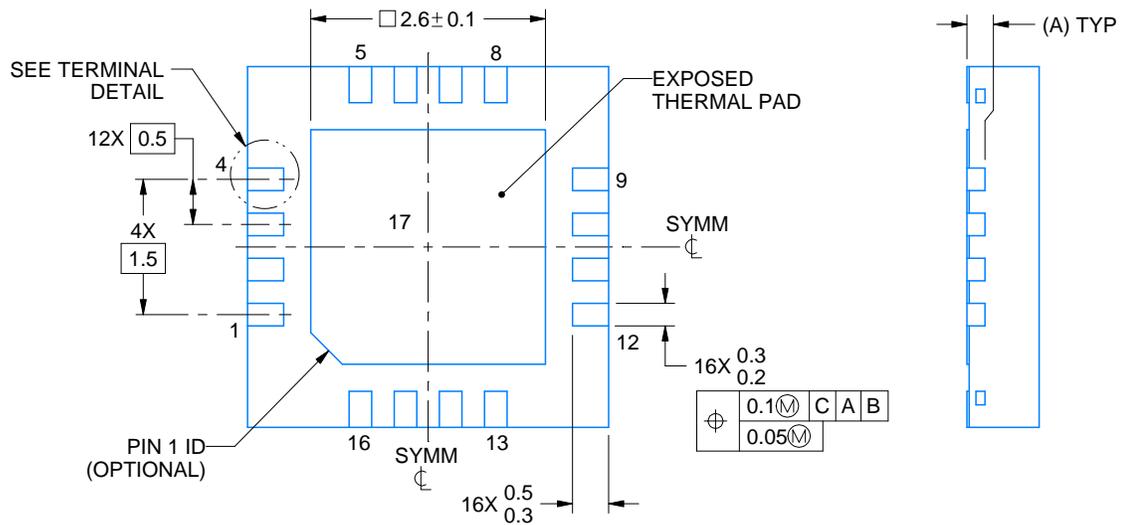
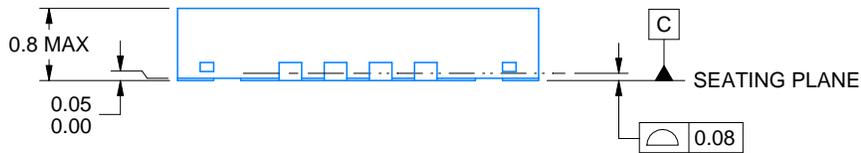
# PACKAGE OUTLINE

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



| DIM A |       |
|-------|-------|
| OPT 1 | OPT 1 |
| (0.1) | (0.2) |



4214978/B 01/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

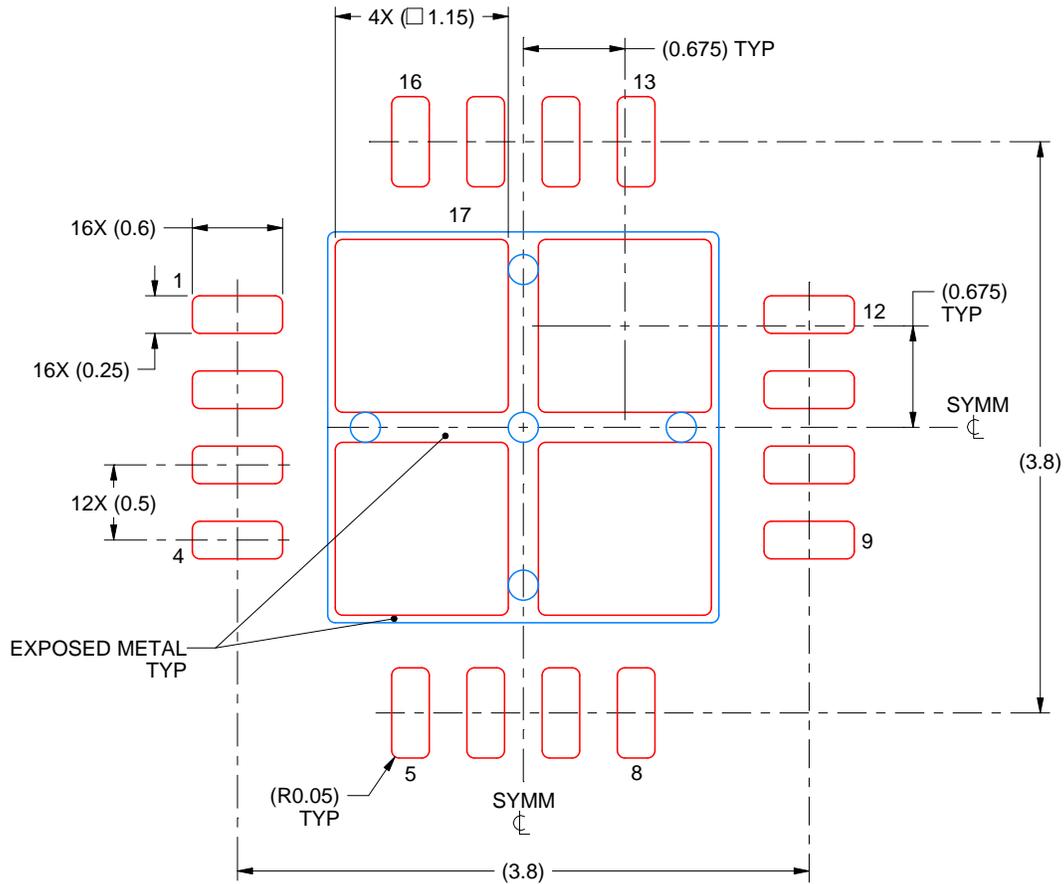


# EXAMPLE STENCIL DESIGN

RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

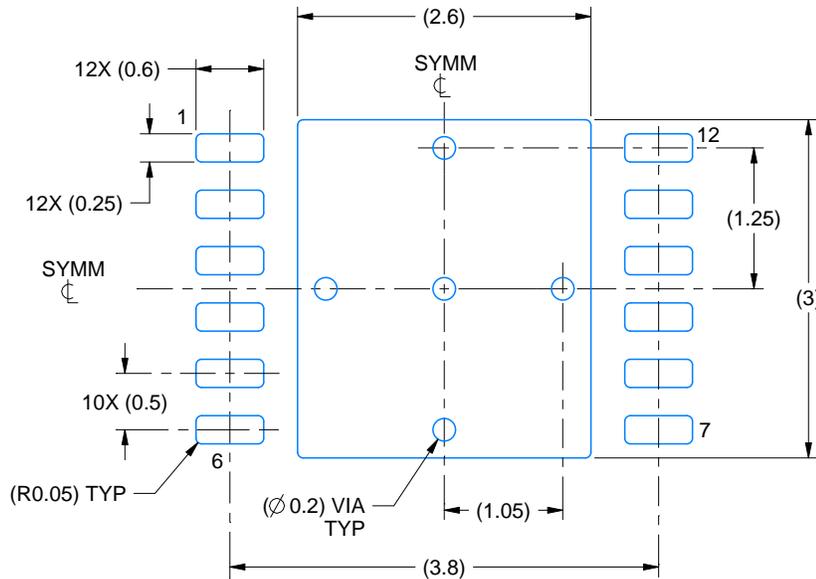


# EXAMPLE BOARD LAYOUT

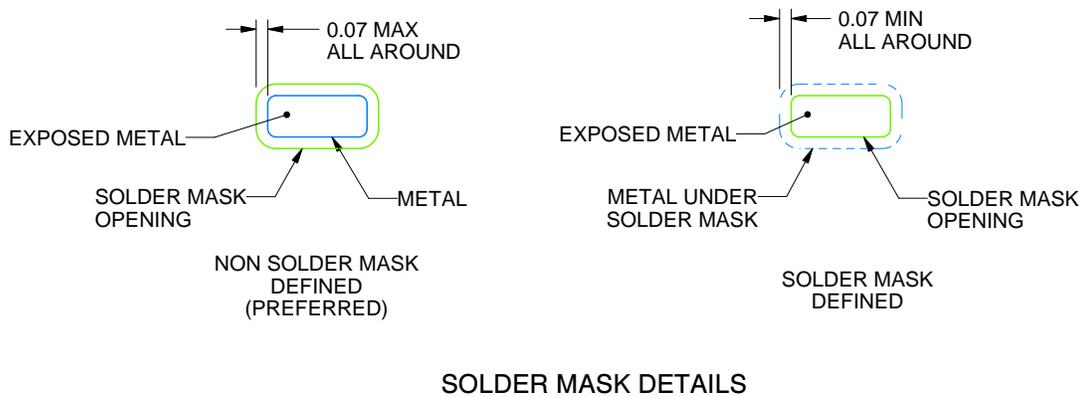
DNT0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

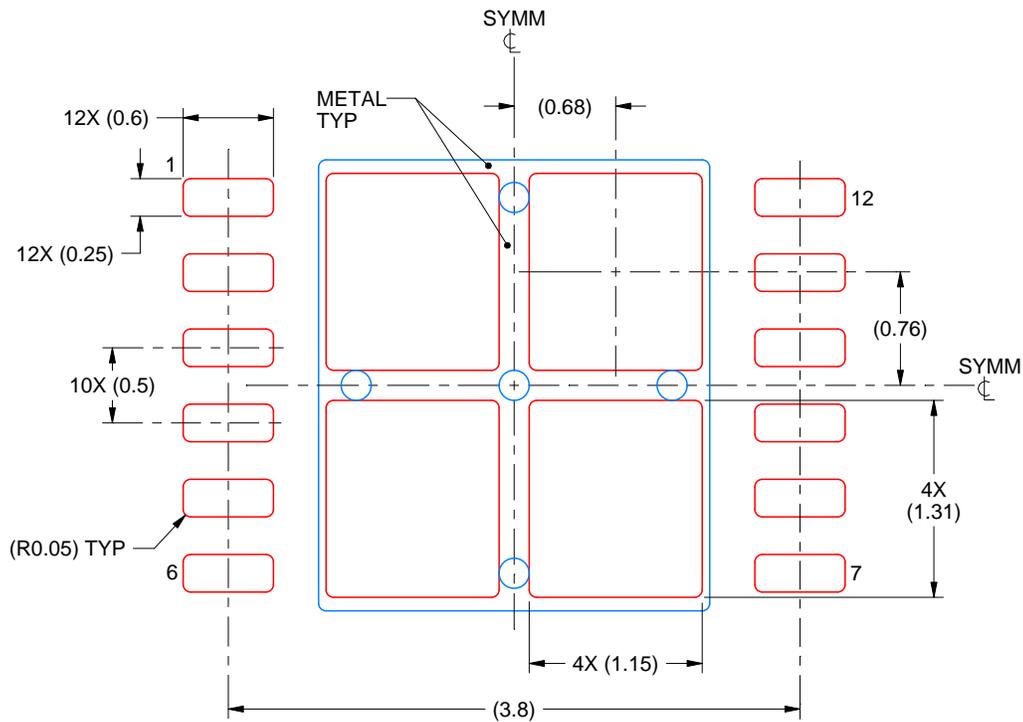
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DNT0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
77% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月