INA132 低功耗单电源差分放大器

1 特性

- 宽电源电压范围：
  - 单电源：2.7V 至 36V
  - 双电源：±1.35V 至 ±18V
- 直流精度性能：
  - 低增益误差：±0.075%（最大值）
  - 低非线性：0.001%（最大值）
  - 高共模抑制：90dB（典型值）
- 低静态电流：175μA

2 应用

- 光学模块
- 楼宇安全网关
- 交流模拟输入模块
- 质谱仪
- CPU（PLC 控制器）
- 实验室和现场仪表

3 说明

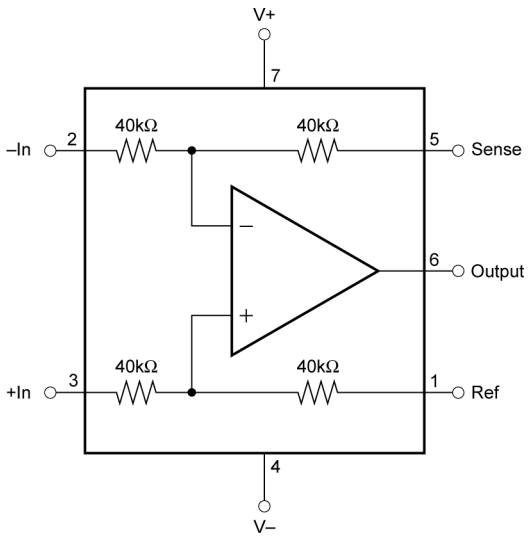
INA132 器件是一款低功耗、单位增益差分放大器，由精密运算放大器和精密电阻器网络组成。片上电阻器经过激光微调，可实现准确增益和高共模抑制。电阻器的出色 TCR 跟踪在全温度范围内保持增益精度和共模抑制。内部运算放大器共模范围可扩展至负电源，这是单电源应用的理想选择。INA132 采用单电源（2.7V 至 36V）或双电源（±1.35V 至 ±18V）运行。

差分放大器是许多常用电路的基础。INA132 提供此电路功能，而无需使用昂贵的精密电阻器网络。INA132 采用 SO-8 表面贴装型封装，工业温度范围为 –40°C 至 +85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
INA132	D（SOIC，8）	4.9mm × 6mm

(1) 如需更多信息，请参阅节 9。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



功能图

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4 Pin Configuration and Functions

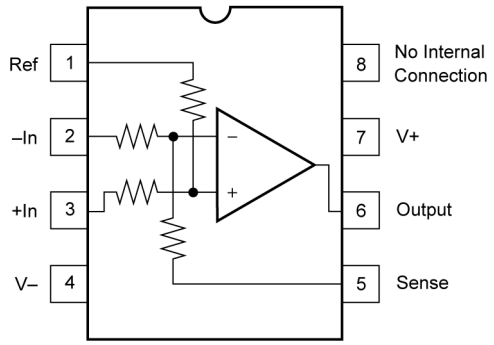


图 4-1. D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
– In	2	Input	Negative (inverting) input
+In	3	Input	Positive (noninverting) input
No Internal Connection	8	—	No internal connection. Leave unconnected.
Output	6	Output	Output
Ref	1	—	Reference input. Drive this pin with a low impedance source. Interchanging pin 1 and 3 degrade CMR.
Sense	5	—	Sense input. Drive this pin with a low impedance source. Interchanging pin 2 and 5 degrade CMR.
V –	4	Input	Negative supply
V+	7	Input	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, V_S = (V+) – (V–)		±18	V
		Single supply, V_S = (V+) – 0V		36	
	Input voltage range			±80	V
	Output short-circuit to (V_S / 2)		Continuous		
T_A	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	125	°C
	Lead temperature (soldering, 10s)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±750	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single-supply	2.7	36	V
		Dual-supply	±1.35	±18	
T_A	Specified temperature		–40	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		INA132 D (SOIC) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	150	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics: V_S = ±15V

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ, V_{REF} = 0V, V_{CM} = V_S/2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage(1)	RTO	INA132		±75	±250	µV
			INA132A		±75	±500	
	Offset voltage drift(1)	RTO, T_A = –40°C to +85°C	INA132		±1	±5	µV/°C
			INA132A		±1	±10(4)	
	Long-term stability(1)				±0.3		µV/mo
PSRR	Power-supply rejection ratio(1)	RTO, V_S = ±1.35V to ±18V			±5	±30	µV/V
V_{CM}	Common-mode voltage	V_O = 0V		(V–)		2(V+) – 2	V
CMRR	Common-mode rejection	V_{CM} = –15V to +28V, R_S = 0Ω	INA132	76	90		dB
			INA132A	70	90		dB
	Differential input impedance(2)				80		kΩ
	Common-mode input impedance(2)				80		kΩ
NOISE							
e_N	Voltage noise(3)	RTO, f_B = 0.1Hz to 10Hz			1.6		μV_{PP}
		RTO, f = 1kHz			75		nV/√Hz
GAIN							
	Gain				1		V/V
GE	Gain error	V_O = –14V to +13.5V	INA132		±0.01	±0.075	%
			INA132A		±0.01	±0.1	
	Gain error drift(4)	T_A = –40°C to +85°C			±1	±10	ppm/°C
	Gain nonlinearity	V_O = –14V to +13.5V	INA132		±0.0001	±0.001	% of FSR
			INA132A		±0.0001	±0.002	
OUTPUT							
	Positive output voltage swing	R_L = 100kΩ		(V+) – 1	(V+) – 0.8		V
		R_L = 10kΩ		(V+) – 1.5	(V+) – 0.8		
	Negative output voltage swing	R_L = 100kΩ		(V–) + 0.5	(V–) + 0.15		V
		R_L = 10kΩ		(V–) + 1	(V–) + 0.25		
C_L	Load capacitance	Stable operation			10000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2			+6/–15		mA
FREQUENCY RESPONSE							
BW	Small signal bandwidth, –3dB				300		kHz
SR	Slew rate				0.1		V/µs
t_S	Settling time	V_O = 10V step	0.1%		85		µs
			0.01%		88		
	Overload recovery time	50% input overdrive			7		µs
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0V			±175	±230	µA

(1) Includes effects of amplifier input bias and offset currents.
(2) 40kΩ resistors are ratio matched but have ±20% absolute value.
(3) Includes effects of amplifier input current noise and thermal noise contribution of resistor network.
(4) Specified by wafer test to 95% confidence level.

5.6 Electrical Characteristics: V_S = 5V

at T_A = 25°C, V_S = +5V, R_L = 10kΩ connected to V_S/2, V_{REF} = V_S/2, V_{CM} = V_S/2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage(1)	RTO	INA132		±150	±500	µV
			INA132A		±150	±750	
	Offset voltage drift(1)	RTO, T_A = –40°C to +85°C			±2		µV/°C
V_{CM}	Common-mode voltage	V_O = 0V		(V–)		2(V+) – 2	V
CMRR	Common-mode rejection	V_{CM} = 0V to 8V, R_S = 0Ω	INA132	76	90		dB
			INA132A	70	90		
OUTPUT							
	Positive output voltage swing	R_L = 100kΩ		(V+) – 1	(V+) – 0.75		V
		R_L = 10kΩ		(V+) – 1	(V+) – 0.8		
	Negative output voltage swing	R_L = 100kΩ		(V–) + 0.25	(V–) + 0.06		V
		R_L = 10kΩ		(V–) + 0.25	(V–) + 0.12		
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0V			±175	±230	µA

(1) Includes effects of amplifier input bias and offset currents.

5.7 Typical Characteristics

at T_A = +25°C and V_S = ±15V (unless otherwise noted)

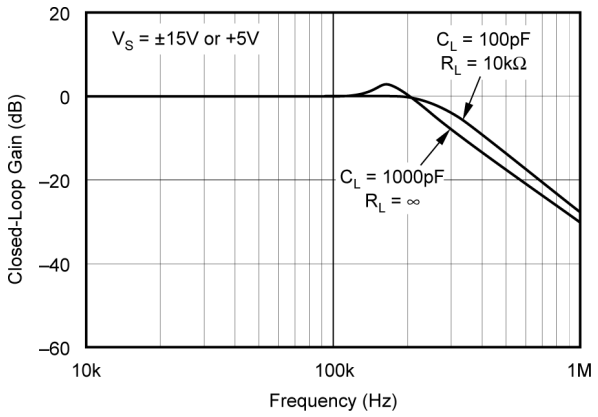


图 5-1. Gain vs Frequency

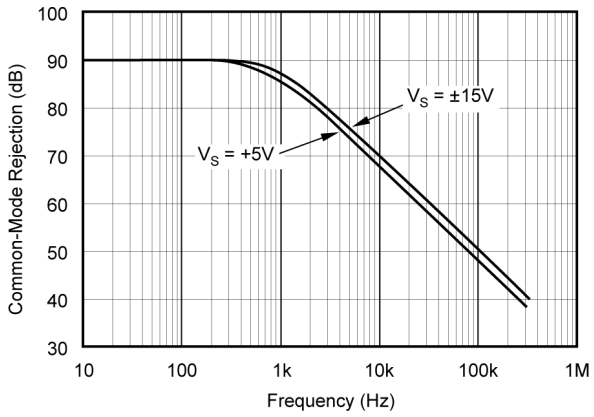


图 5-2. Common-Mode Rejection vs Frequency

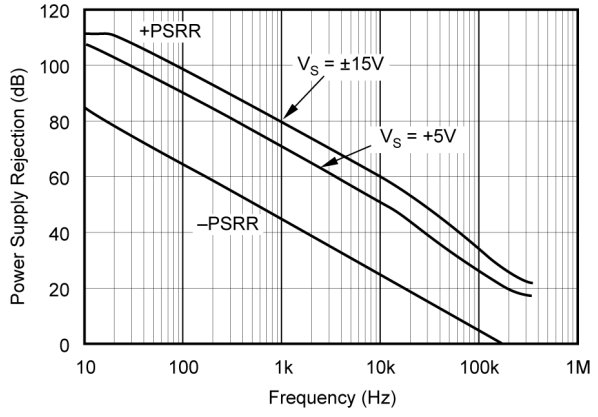


图 5-3. Power Supply Rejection vs Frequency

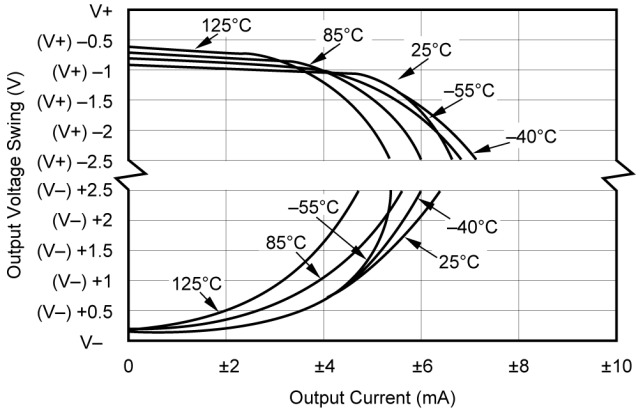


图 5-4. Output Voltage Swing vs Output Current

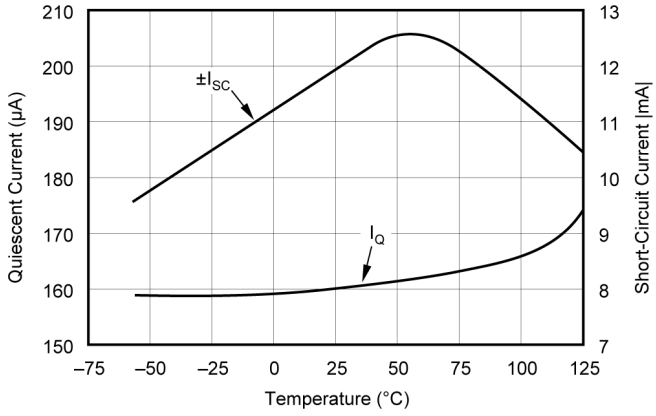


图 5-5. Quiescent and Short-Circuit Current vs Temperature

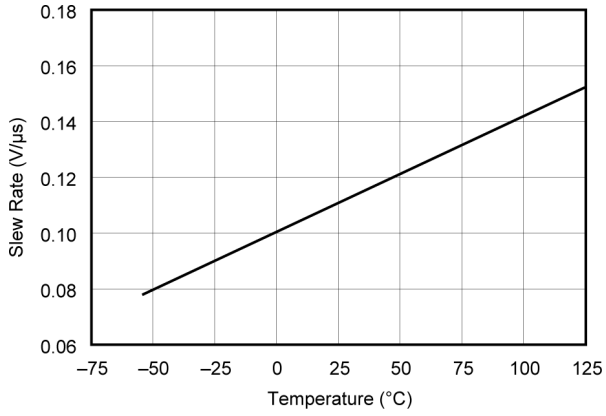


图 5-6. Slew Rate vs Temperature

5.7 Typical Characteristics (continued)

at T_A = +25°C and V_S = ±15V (unless otherwise noted)

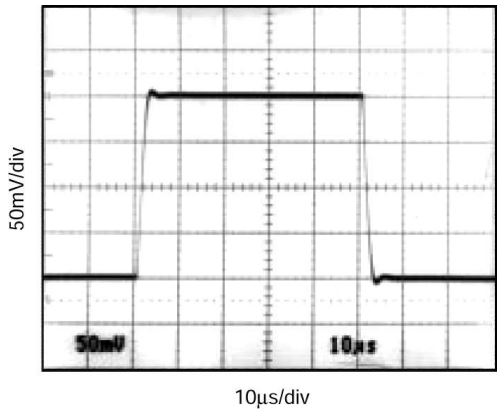


图 5-7. Small-Signal Step Response

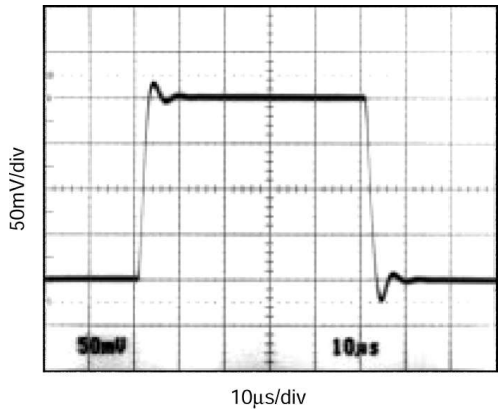


图 5-8. Small-Signal Step Response

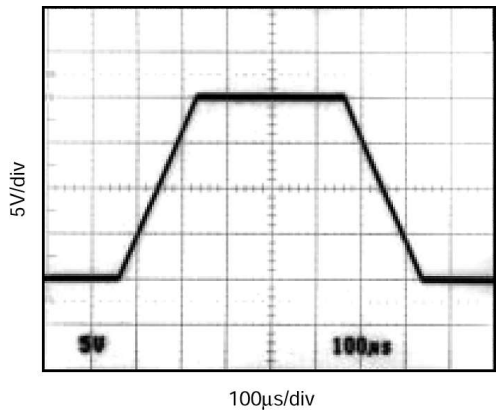


图 5-9. Large-Signal Step Response

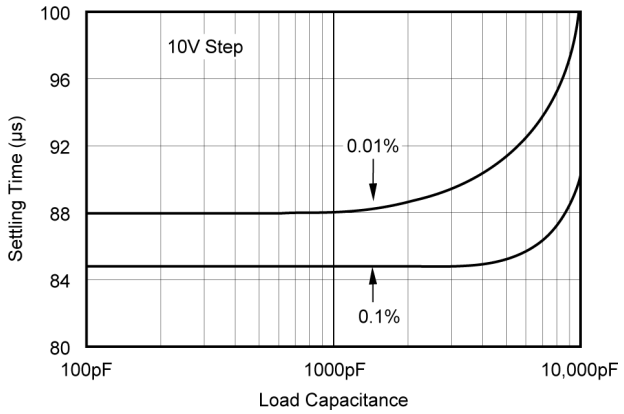


图 5-10. Settling Time vs Load Capacitance

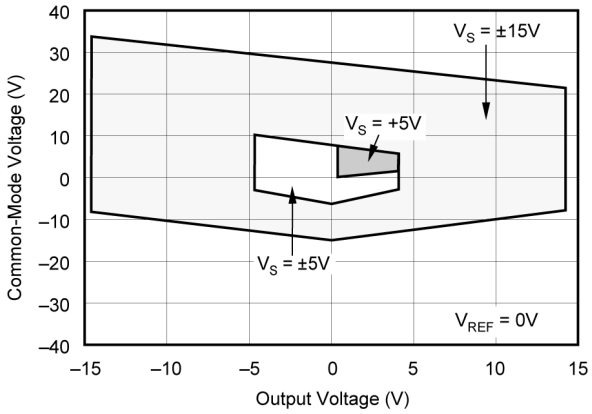


图 5-11. Input Common-mode Voltage Range vs Output Voltage

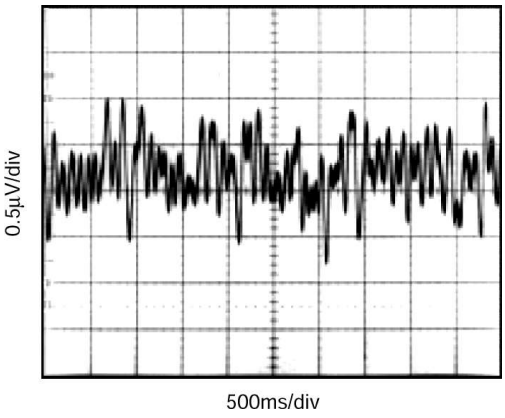


图 5-12. 0.1-Hz to 10-Hz Peak-to-Peak Voltage Noise

5.7 Typical Characteristics (continued)

at T_A = +25°C and V_S = ±15V (unless otherwise noted)

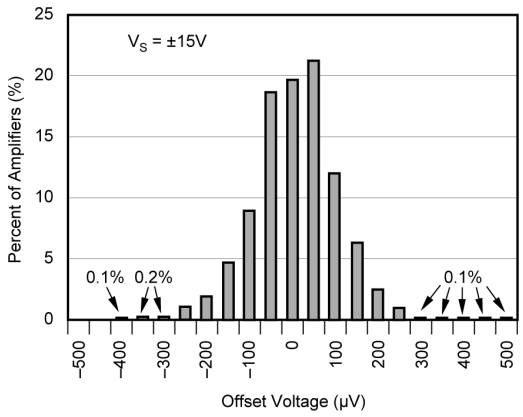


图 5-13. Offset Voltage Production Distribution

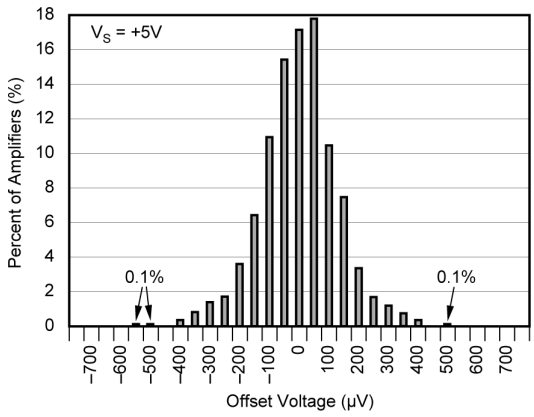


图 5-14. Offset Voltage Production Distribution

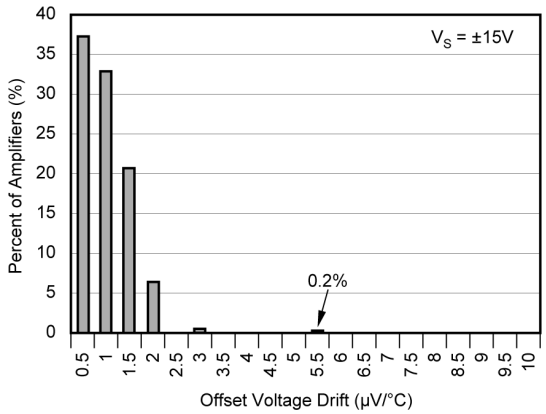


图 5-15. Offset Voltage Drift Production Distribution

6 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

6.1 Applications Information

图 6-1 shows the basic connections required for operation of the INA132. Connect power-supply bypass capacitors close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. Ensure that the source impedances connected to the inputs are nearly equal to maintain good common-mode rejection. An 8Ω mismatch in source impedance degrades the common-mode rejection of a typical device to approximately 80dB. Gain accuracy is also slightly affected. If the source has a known impedance mismatch, use an additional resistor in series with one input to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins does not provide specified performance. Sense measurements at the load, as in 图 6-1.

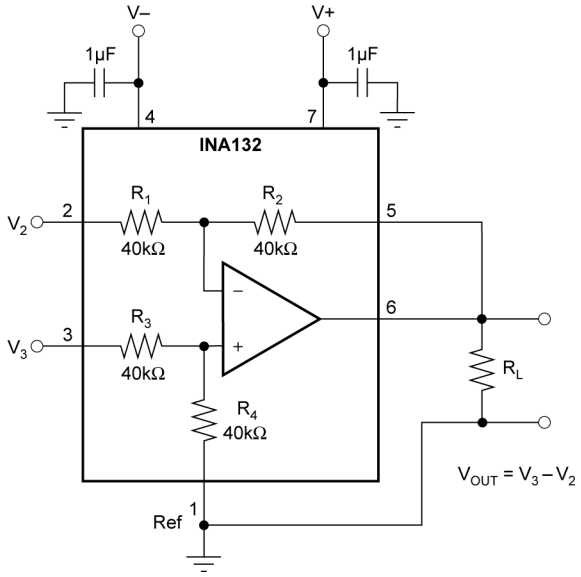


图 6-1. Basic Power Supply and Signal Connections

6.1.1 Operating Voltage

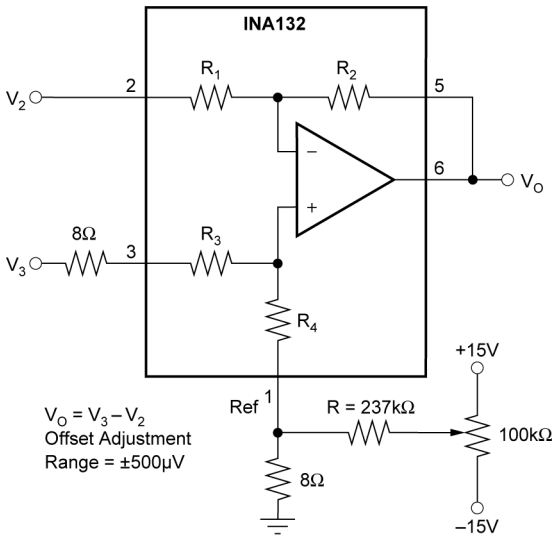
The INA132 operates from single (2.7V to 36V) or dual (±1.35V to ±18V) supplies with excellent performance. Specifications are production tested with +5V and ±15V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the *Typical Characteristics*.

The internal op amp in the INA132 is a single-supply design. This design allows linear operation with the op-amp common-mode voltage equal to, or slightly below V – (or single supply ground). Although input voltages on pins 2 and 3 that are less than the negative supply voltage do not damage the device, operation in this region is not recommended. Transient conditions at the inverting input terminal less than the negative supply can cause a positive feedback condition that can lock the INA132 output to the negative rail.

The INA132 can accurately measure differential signals that are greater than the positive power supply. The linear common-mode range extends to nearly twice the positive power supply voltage — see typical characteristics curve, *Common-Mode Range vs Output Voltage*.

6.1.2 Offset Voltage Trim

The INA132 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. 图 6-2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal is summed with the output signal, and can be used to null offset voltage. Ensure that the source impedance of a signal applied to the Ref terminal is less than 8Ω to maintain good common-mode rejection. To maintain low impedance at the Ref terminal, the trim voltage can be buffered with an op amp, such as the OPA177.



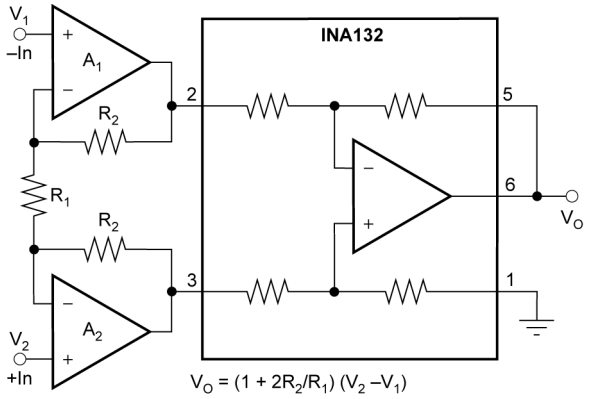
NOTE: For ±750µV range, R = 158kΩ.

图 6-2. Offset Adjustment.

6.1.3 Capacitive Load Drive Capability

The INA132 drives large capacitive loads, even at low supplies. The device is stable with a 10,000-pF load. See the *Small-Signal Step Response* and *Settling Time vs Load Capacitance* typical characteristics.

6.2 Typical Applications



The INA132 can be combined with op amps to form a complete instrumentation amplifier with specialized performance characteristics. Burr-Brown offers many complete high performance IAs. Products with related performances are shown at the right.

A_1, A_2	FEATURE	SIMILIAR COMPLETE BURR-BROWN IA
OPA27	Low Noise	INA103
OPA129	Ultra Low Bias Current (fA)	INA116
OPA177	Low Offset Drift, Low Noise	INA114,INA128
OPA2130	Low Power, FET-Input (pA)	INA111
OPA2234	Single Supply, Precision, Low Power	INA122(1), INA118
OPA2237	Single Supply, Low Power, MSOP-8	INA122(1), INA126(1)

NOTE: (1) Available 1Q'97.

图 6-3. Precision Instrumentation Amplifier

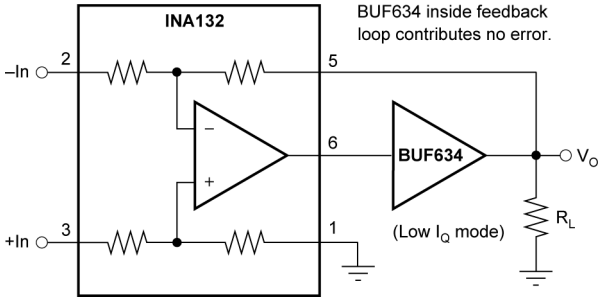


图 6-4. Low Power, High Output Current Precision Difference Amplifier

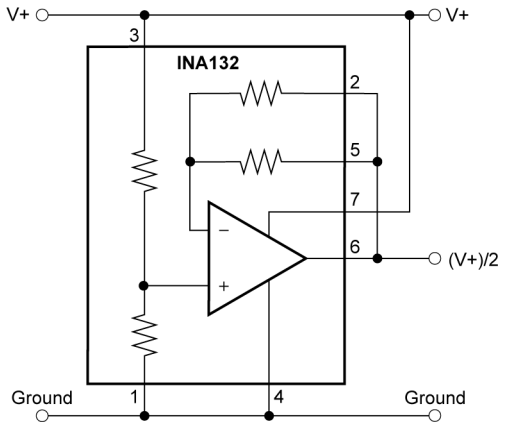


图 6-5. Pseudoground Generator

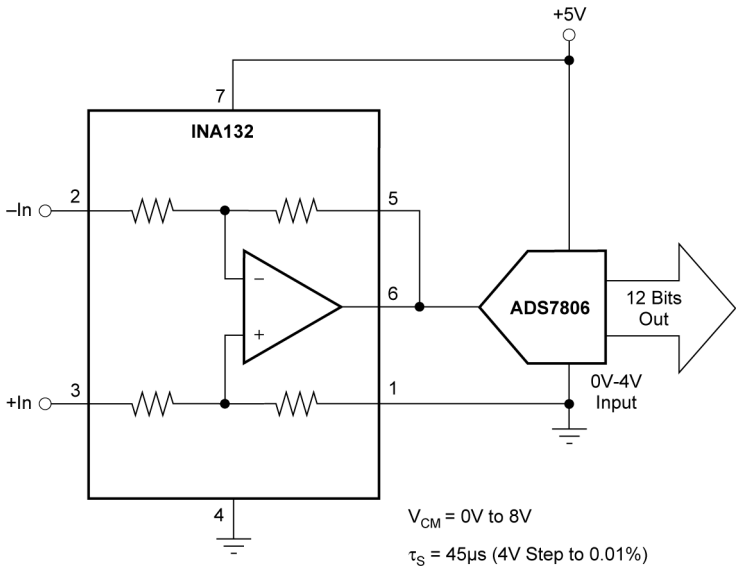


图 6-6. Differential Input Data Acquisition

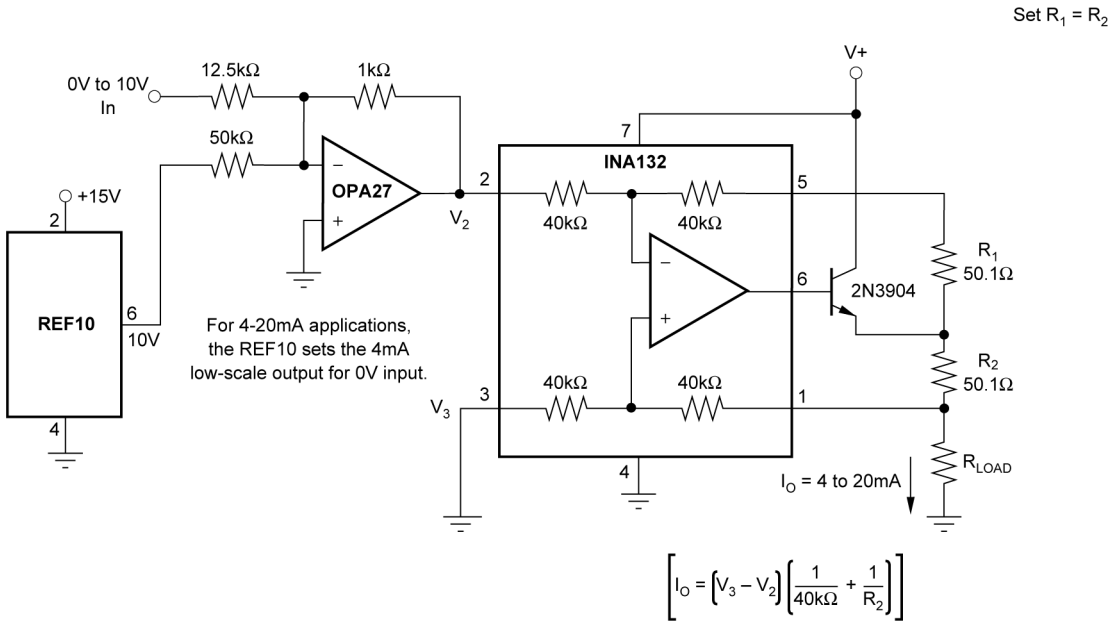


图 6-7. Precision Voltage-to-Current Conversion

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet for additional applications ideas, including:

- Current receiver with compliance to rails
- Precision unity-gain inverting amplifier
- ±10-V precision voltage reference
- ±5-V precision voltage reference
- Precision unity-gain buffer
- Precision average value amplifier
- Precision G = 2 amplifier
- Precision summing amplifier
- Precision G = 1/2 amplifier
- Precision bipolar offsetting
- Precision summing amplifier with gain
- Instrumentation amplifier guard drive generator
- Precision summing instrumentation amplifier
- Precision absolute value buffer
- Precision voltage-to-current converter with differential inputs
- Differential input voltage-to-current converter for low I_{OUT}
- Isolating current source
- Differential output difference amplifier
- Isolating current source with buffering amplifier for greater accuracy
- Window comparator with window span and window center inputs
- Precision voltage-controlled current source with buffered differential inputs and gain
- Digitally controlled gain of ±1 amplifier

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (November 1996) to Revision A (February 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 添加了 *ESD 等级*、*建议运行条件*、*热性能信息*、*应用和实施*、*典型应用*、*器件和文档支持* 以及*机械、封装和可订购信息* 部分	1
• 从数据表中删除了 DIP 封装和相关内容	1
• 更新了*特性* 要点	1
• 更新了*应用* 要点	1
• Added *Pin Functions* table	2
• Added dual supply specification to *Absolute Maximum Ratings*	3
• Changed output short-circuit from "ground" to "V_S / 2" in *Absolute Maximum Ratings*	3
• Added V_{REF} = 0V, V_{CM} = V_S / 2, and G = 1 to test conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity	4
• Changed "Offset Voltage vs Temperature" to "Offset voltage drift" and added T_A = –40℃ to +85℃ test condition for clarity	4
• Changed "Offset Voltage vs Time" to "Long-term stability" for clarity	4
• Changed "Offset Voltage vs Power Supply" to Power-supply rejection ratio for clarity	4
• Changed voltage noise typical value at 1kHz from 65nV/ √Hz to 75nV/ √Hz	4
• Changed "Gain Error vs Temperature" to "Gain error drift" and added T_A = –40℃ to +85℃ test condition for clarity	4

- Changed "Voltage, Positive" to "Positive output voltage swing" and from "Voltage, Negative" to "Negative output voltage swing"....4
- Added test condition of "Continuous to V_S / 2" to short-circuit current for clarity....4
- Changed short-circuit current typical value from ±12mA to +6mA/ – 15mA....4
- Deleted power supply voltage range typical value of ±15V....4
- Moved voltage range, operating temperature range, and thermal resistance from *Electrical Characteristics* to *Recommended Operating Conditions* and *Thermal Information* 4
- Changed quiescent current typical value from ±160µA to ±175µA and maximum value from ±185µA to ±230µA....4
- Added V_{REF} = V_S / 2, V_{CM} = V_S / 2, and G = 1 to test conditions in *Electrical Characteristics: V_S = 5V* for clarity....5
- Changed "Offset Voltage vs Temperature" to "Offset voltage drift" and added T_A = – 40℃ to +85℃ test condition for clarity....5
- Added (V –) to negative output voltage swing minimum and typical values....5
- Deleted power supply voltage range typical value of +5V....5
- Moved voltage range from *Electrical Characteristics: V_S = 5V* to *Recommended Operating Conditions* 5
- Changed quiescent current typical value from ±155µA to ±175µA and maximum value from ±185µA to ±230µA....5

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA132U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI		INA 132U	
INA132U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 132U	Samples
INA132UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	INA 132U A	
INA132UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 132U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

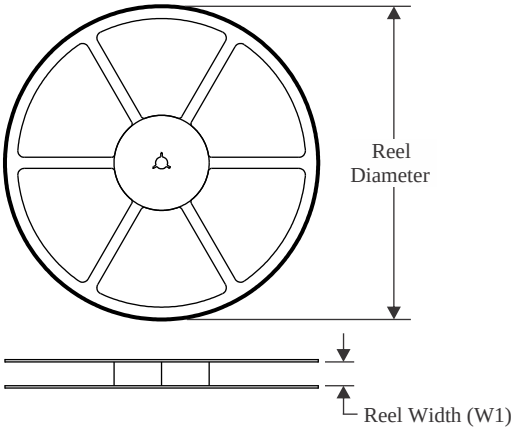
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

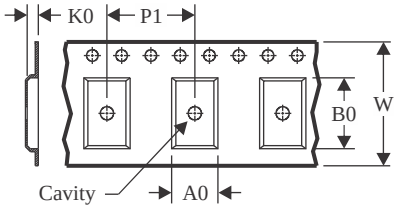
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

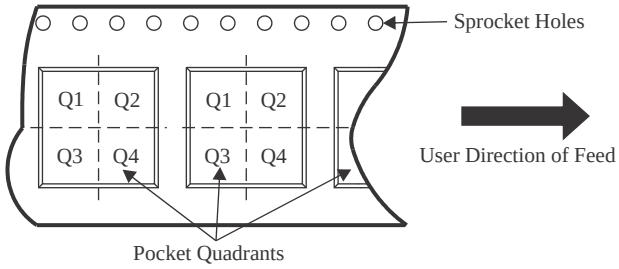


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

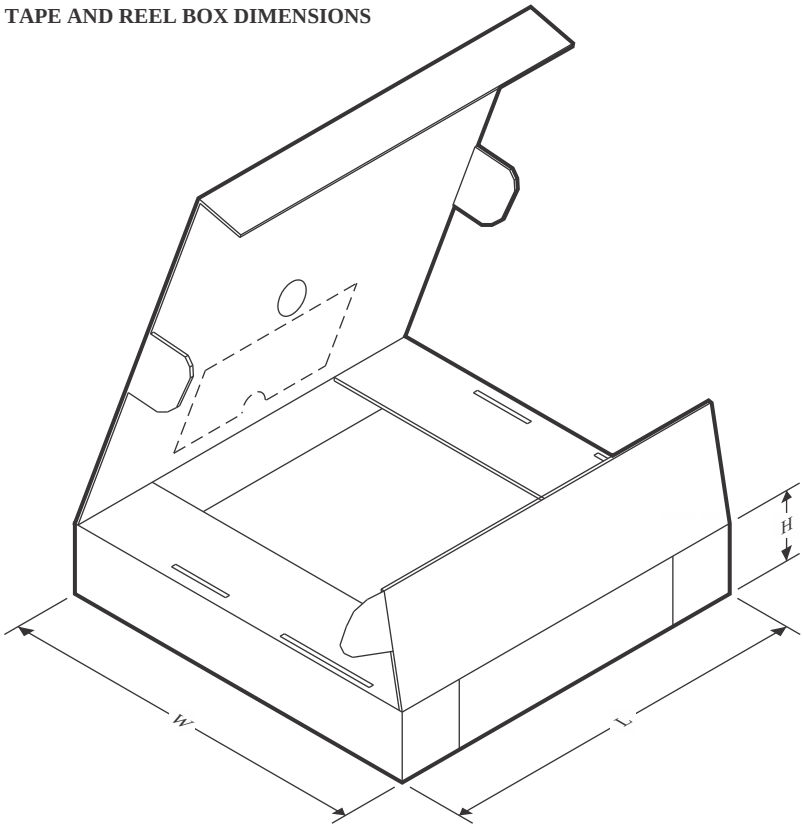
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA132U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA132U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA132UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA132UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

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