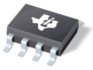


高共模电压差动放大器

特性

- 共模电压范围： **±275 V**
- 最小 **CMRR**： **–40°C** 至 **125°C** 时为 **90 dB**
- **DC** 规范
  - 最大偏移电压： **1100 μV**
  - 最大偏移电压漂移**: 15 μV/°C**
  - 最大增益误差**: 0.02%**
  - 最大增益漂移误差**: 10 ppm/°C**
  - 最大增益非线性值**: 0.001% FSR**
- **AC** 性能：
  - 带宽： **500 kHz**
  - 典型转换率： **5 V/μs**
- 宽电源电压范围： **±2.0 V** 至 **±18 V**
  - 最大静态电流**: 900 μA**
  - **±15-V** 电源的输出摆幅**: ±13.5 V**
- 输入保护
  - 共模电压**: ±500 V**
  - 差分电压**: ±500 V**

应用

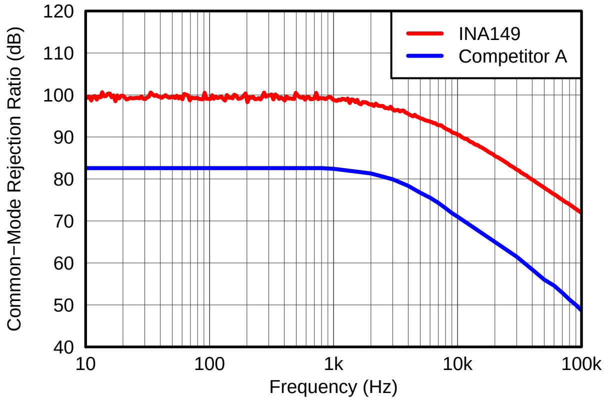
- 高压电流感应
- 电池电压监视
- 电源电流监视
- 电机控制
- 隔离电路的替代产品

说明

INA149 是一款高精度单位增益差动放大器，此放大器具有很高的输入共模电压范围。 它是一款包含有高精度运算放大器和集成薄膜电阻器网路的单一单片器件。 在共模信号电压高达 ±275 V时，INA149 可以准确测量较小的差分电压。INA149 输入受到最高 500 V 的瞬时共模电压或者的差分负载的保护。

在很多无需电流隔离的应用中，INA149 可以取代隔离放大器。 此功能可以省去昂贵的隔离的输入端电源并去除相关纹波、噪音和静态电流。 INA149 出色的 0.0005% 非线性和 500-kHz 带宽特性使之优于传统隔离放大器。

INA149 与 INA117-和 INA148-类型高共模电压放大器引脚兼容并且提供优于上述两设备的性能。 INA149 采用 SOIC-8 封装，额定拓展工业工作温度范围为 –40°C 至 +125°C。



English Data Sheet: SBOS579

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA149	SOIC-8	D	INA149A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		INA149	UNIT
Supply voltage	(V+) – (V–)	40	V
Input voltage range	Continuous	300	V
Common-mode and differential, 10 s		500	V
Maximum Voltage on REF_A and REF_B		(V–) – 0.3 to (V+) + 0.3	V
Input current on any input pin(2)		10	mA
Output short-circuit current duration		Indefinite	
Operating temperature range		–55 to +150	°C
Storage temperature range		–65 to +150	°C
Junction temperature		+150	°C
ESD rating	Human body model (HBM)	1500	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	100	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) REF_A and REF_B are diode clamped to the power-supply rails. Signals applied to these pins that can swing more than 0.3 V beyond the supply rails should be limited to 10 mA or less.

ELECTRICAL CHARACTERISTICS: V+ = +15 V and V– = –15 V

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_{CM} = REF_A = REF_B = GND, unless otherwise noted.

PARAMETER	TEST CONDITIONS	INA149 MIN	INA149 TYP	INA149 MAX	UNIT
GAIN					
Initial	V_{OUT} = ±10.0 V		1		V/V
Gain error	V_{OUT} = ±10.0 V		±0.005	±0.02	%FSR
Gain	vs temperature, T_A = –40°C to +125°C		±1.5	±10	ppm/°C
Nonlinearity			±0.0005	±0.001	%FSR
OFFSET VOLTAGE					
Initial offset			350	1100	µV
	vs temperature, T_A = –40°C to +125°C		3	15	µV/°C
	vs supply (PSRR), V_S = ±2 V to ±18 V	90	120		dB
INPUT					
Impedance	Differential		800		kΩ
	Common-mode		200		kΩ
Voltage range	Differential	–13.5		13.5	V
	Common-mode	–275		275	V
Common-mode rejection (CMRR)	At dc, V_{CM} = ±275 V	90	100		dB
	vs temperature, T_A = –40°C to +125°C, at dc	90			dB
	At ac, 500 Hz, V_{CM} = 500 V_{PP}	90			dB
	At ac, 1 kHz, V_{CM} = 500 V_{PP}		90		dB
OUTPUT					
Voltage range		–13.5		13.5	V
Short-circuit current			±25		mA
Capacitive load drive	No sustained oscillations		10		nF
OUTPUT NOISE VOLTAGE					
0.01 Hz to 10 Hz			20		μV_{PP}
10 kHz			550		$nV/\sqrt{Hz}$
DYNAMIC RESPONSE					
Small-signal bandwidth			500		kHz
Slew rate	V_{OUT} = ±10-V step	1.7	5		V/µs
Full-power bandwidth	V_{OUT} = 20 V_{PP}		32		kHz
Settling time	0.01%, V_{OUT} = 10-V step		7		µs
POWER SUPPLY					
Voltage range		±2		±18	V
Quiescent current	V_S = ±18 V, V_{OUT} = 0 V		810	900	µA
	vs temperature, T_A = –40°C to +125°C			1.1	mA
TEMPERATURE RANGE					
Specified		–40		+125	°C
Operating		–55		+150	°C
Storage		–65		+150	°C

ELECTRICAL CHARACTERISTICS: V+ = 5 V and V– = 0 V

At T_A = +25°C, R_L = 2 kΩ connected to 2.5 V, and V_{CM}= REF_A = REF_B = 2.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA149 MIN	INA149 TYP	INA149 MAX	UNIT
GAIN						
	Initial	V_{OUT} = 1.5 V to 3.5 V		1		V/V
	Gain error	V_{OUT} = 1.5 V to 3.5 V		±0.005		%FSR
	Gain	vs temperature, T_A = –40°C to +125°C		±1.5		ppm/°C
	Nonlinearity			±0.0005		%FSR
OFFSET VOLTAGE						
	Initial offset			350		µV
		vs temperature, T_A = –40°C to +125°C		3		µV/°C
		vs supply (PSRR), V_S = 4 V to 5 V		120		dB
INPUT						
	Impedance	Differential		800		kΩ
		Common-mode		200		kΩ
	Voltage range	Differential	1.5		3.5	V
		Common-mode	–20		25	V
	Common-mode rejection	At dc, V_{CM} = –20 V to 25 V		100		dB
		vs temperature, T_A = –40°C to +125°C, at dc		100		dB
		At ac, 500 Hz, V_{CM} = 49 V_{PP}		100		dB
		At ac, 1 kHz, V_{CM} = 49 V_{PP}		90		dB
OUTPUT						
	Voltage range		1.5		3.5	V
	Short-circuit current			±15		mA
	Capacitive load drive	No sustained oscillations		10		nF
OUTPUT NOISE VOLTAGE						
	0.01 Hz to 10 Hz			20		μV_{PP}
	10 kHz			550		nV/√Hz
DYNAMIC RESPONSE						
	Small-signal bandwidth			500		kHz
	Slew rate	V_{OUT} = 2 V_{PP} step		5		V/µs
	Full-power bandwidth	V_{OUT} = 2 V_{PP}		32		kHz
	Settling time	0.01%, V_{OUT} = 2 V_{PP} step		7		µs
POWER SUPPLY						
	Voltage range			5		V
	Quiescent current	V_S = 5 V		810		µA
		vs temperature, T_A = –40°C to +125°C		1		mA

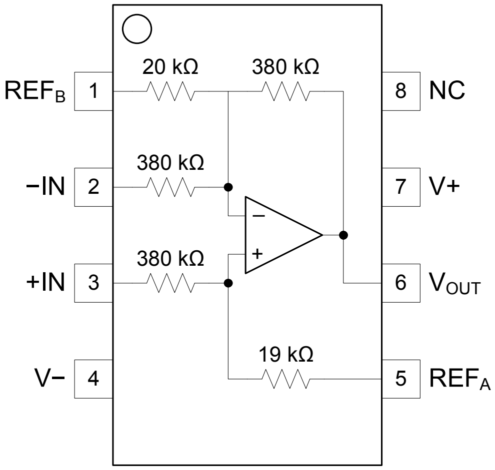
THERMAL INFORMATION

THERMAL METRIC[1]		INA149 D (SOIC) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	110	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	57	
θ_{JB}	Junction-to-board thermal resistance	54	
ψ_{JT}	Junction-to-top characterization parameter	11	
ψ_{JB}	Junction-to-board characterization parameter	53	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATION

D PACKAGE
SOIC-8
(TOP VIEW)



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
–IN	2	Inverting input
+IN	3	Noninverting input
NC	8	No internal connection
REF_A	5	Reference input
REF_B	1	Reference input
V–	4	Negative power supply
V+	7	Positive power supply[1]
V_{OUT}	6	Output

(1) In this document, (V+) – (V–) is referred to as V_S.

TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

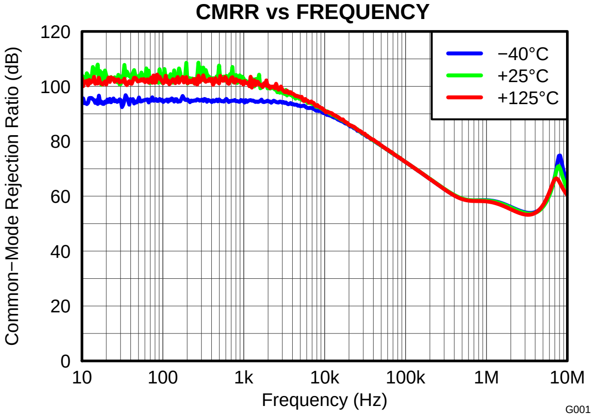

CMRR vs FREQUENCY

Figure 1.

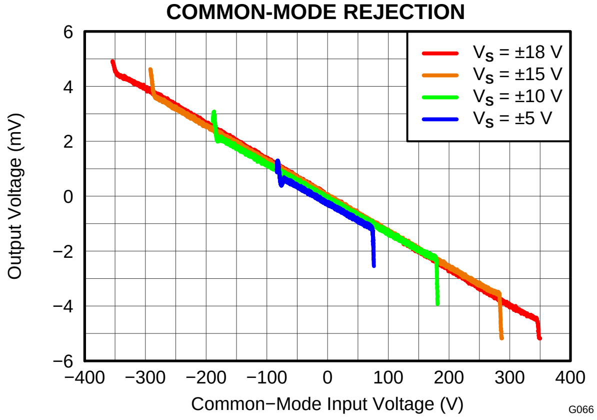

COMMON-MODE REJECTION

Figure 2.

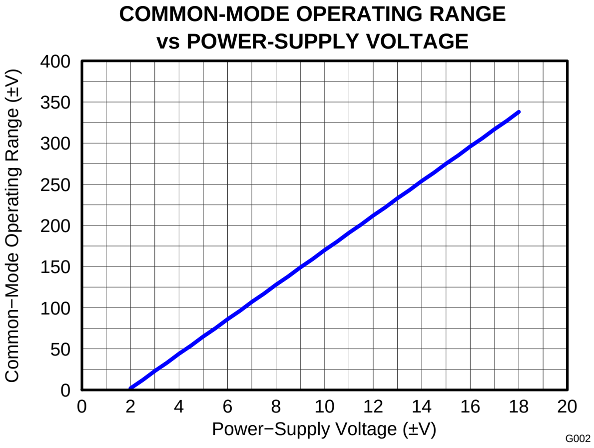

COMMON-MODE OPERATING RANGE vs POWER-SUPPLY VOLTAGE

Figure 3.

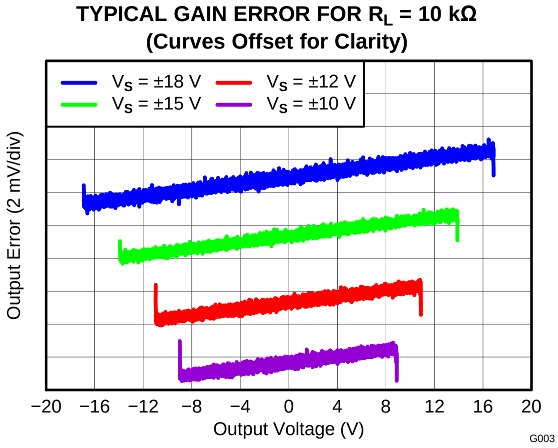

TYPICAL GAIN ERROR FOR R_L = 10 kΩ (Curves Offset for Clarity)

Figure 4.

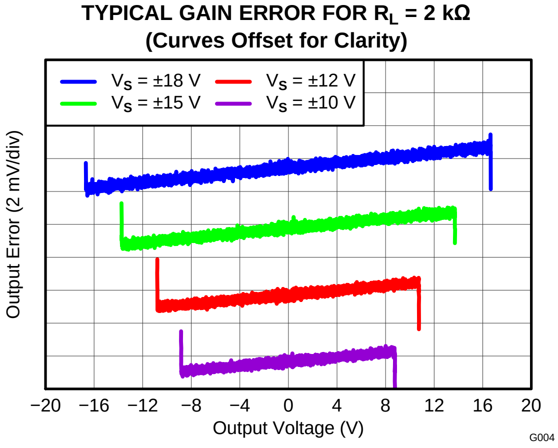

TYPICAL GAIN ERROR FOR R_L = 2 kΩ (Curves Offset for Clarity)

Figure 5.

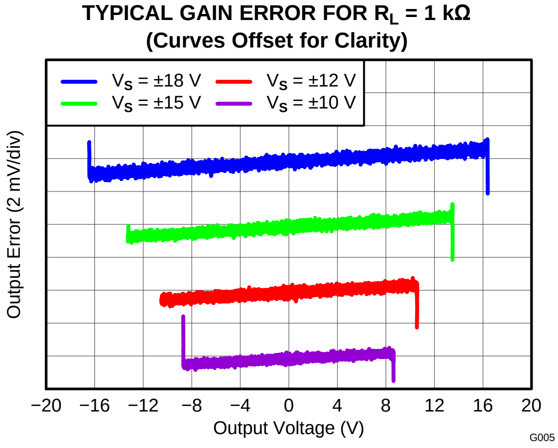

TYPICAL GAIN ERROR FOR R_L = 1 kΩ (Curves Offset for Clarity)

Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

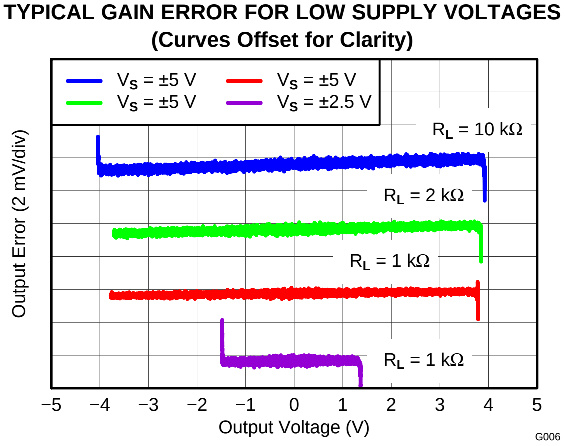


Figure 7.

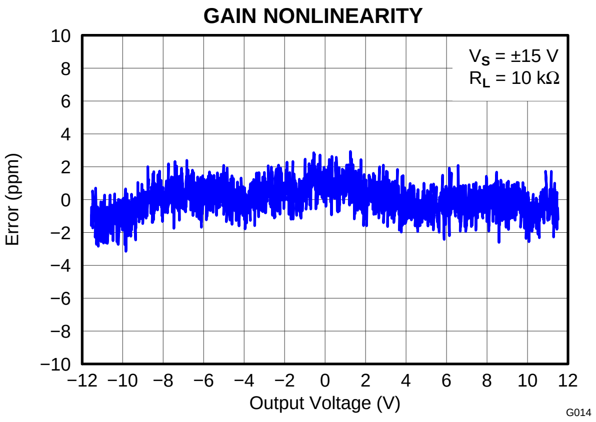


Figure 8.

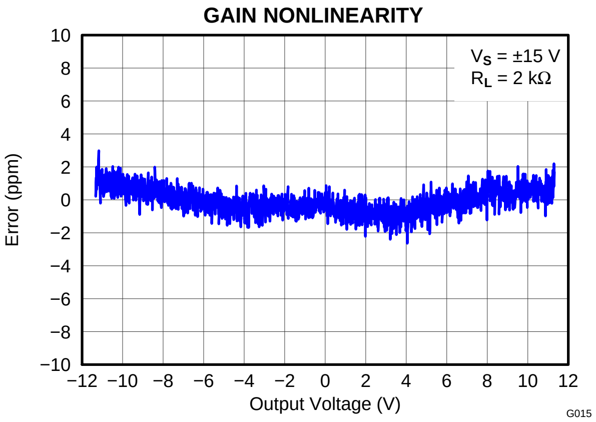


Figure 9.

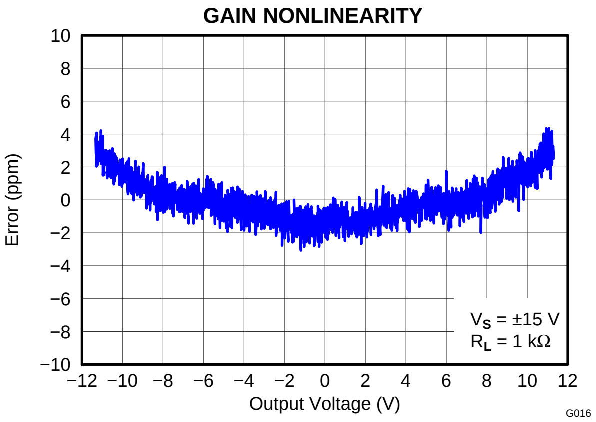


Figure 10.

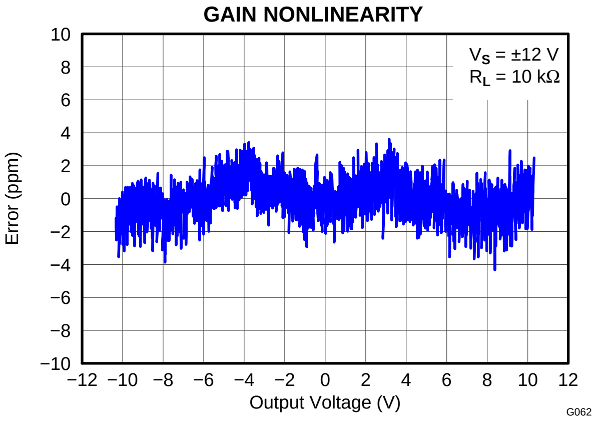


Figure 11.

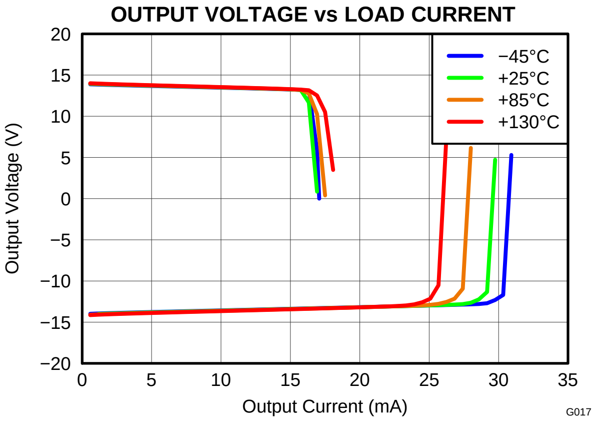


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

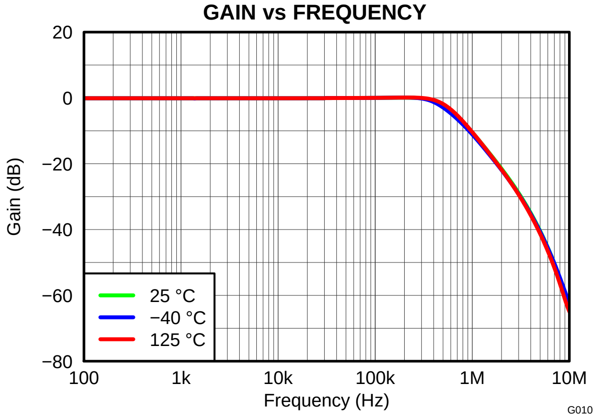

GAIN vs FREQUENCY

Figure 13.

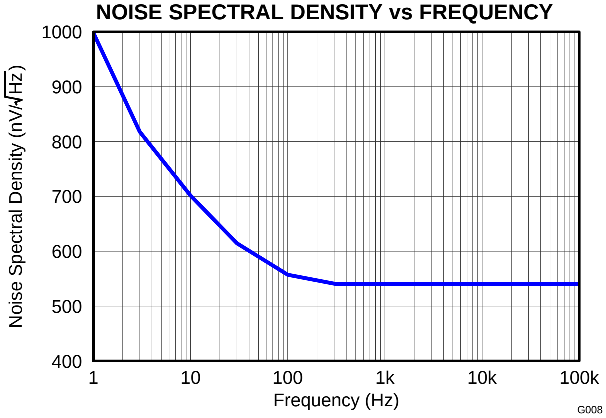

NOISE SPECTRAL DENSITY vs FREQUENCY

Figure 14.

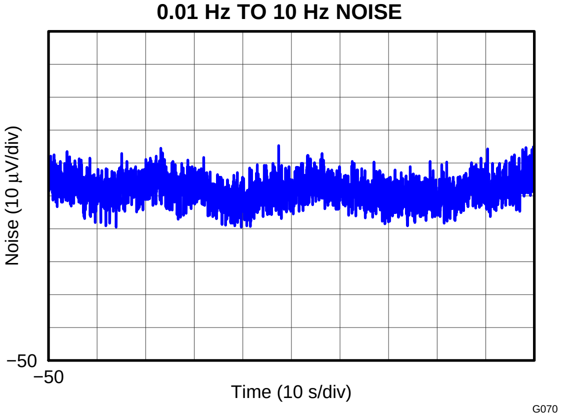

0.01 Hz TO 10 Hz NOISE

Figure 15.

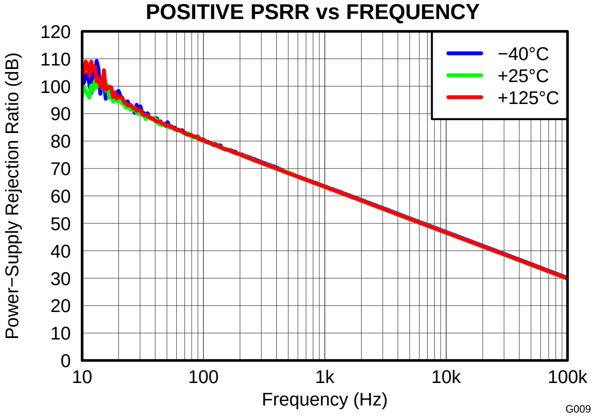

POSITIVE PSRR vs FREQUENCY

Figure 16.

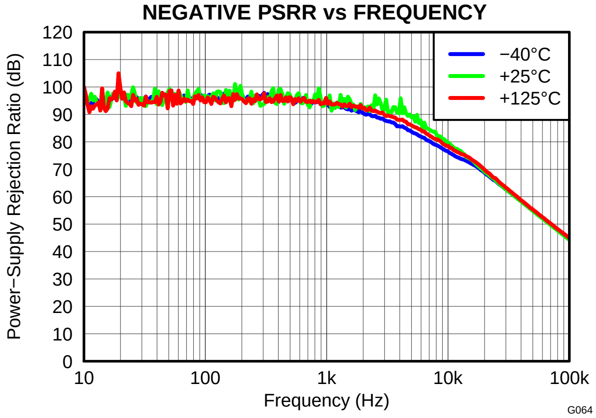

NEGATIVE PSRR vs FREQUENCY

Figure 17.

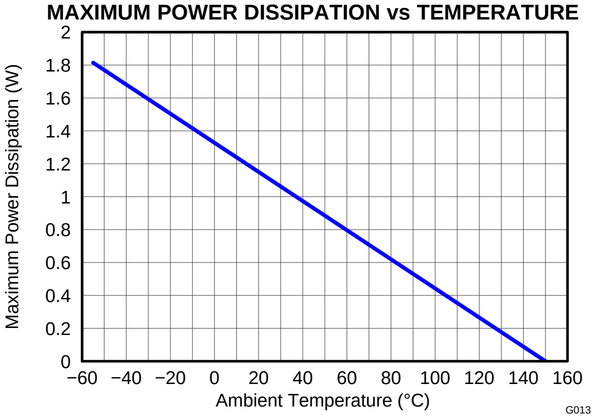

MAXIMUM POWER DISSIPATION vs TEMPERATURE

Figure 18.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25°C$, $R_L = 2\ k\Omega$ connected to ground, and $V_S = \pm15\ V$, unless otherwise noted.

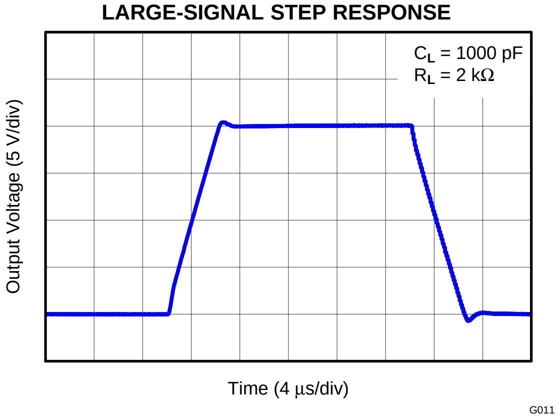

LARGE-SIGNAL STEP RESPONSE

Figure 19.

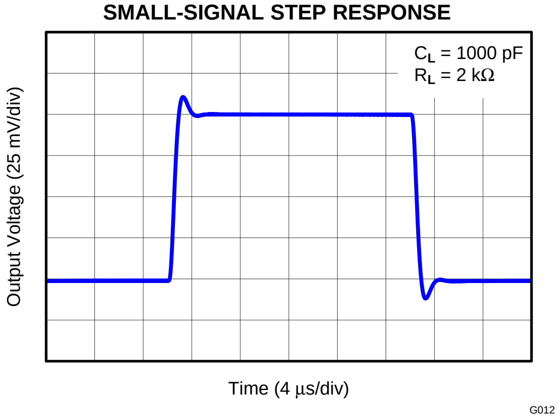

SMALL-SIGNAL STEP RESPONSE

Figure 20.

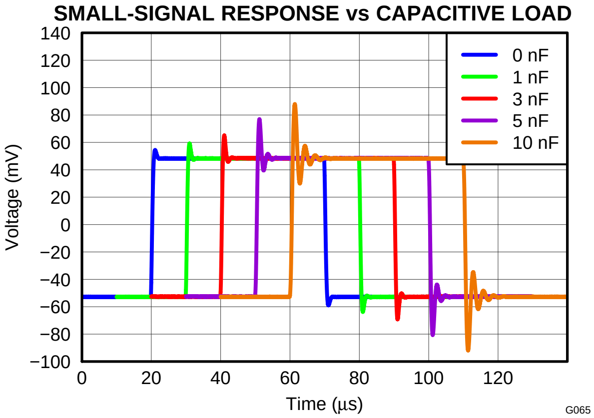

SMALL-SIGNAL RESPONSE vs CAPACITIVE LOAD

Figure 21.

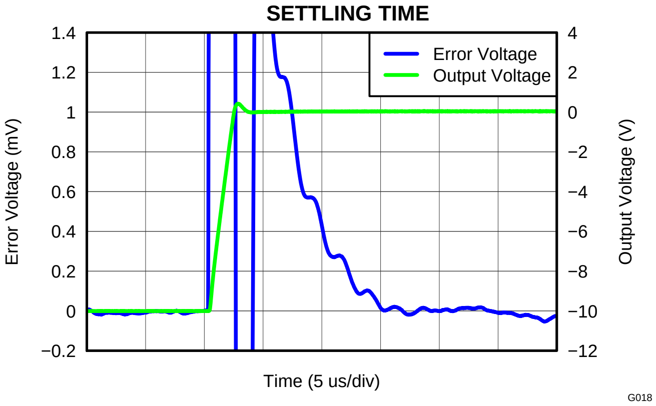

SETTLING TIME

Figure 22.

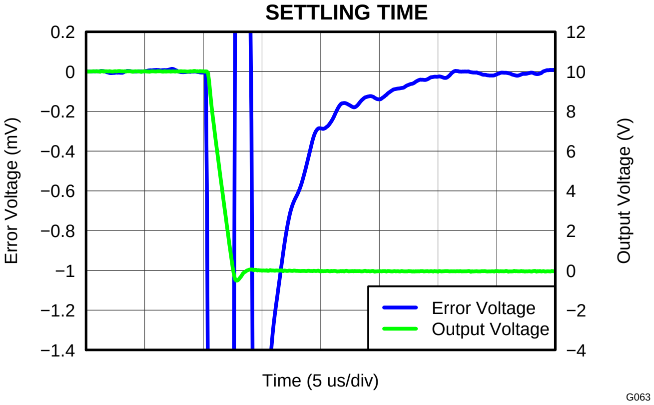

SETTLING TIME

Figure 23.

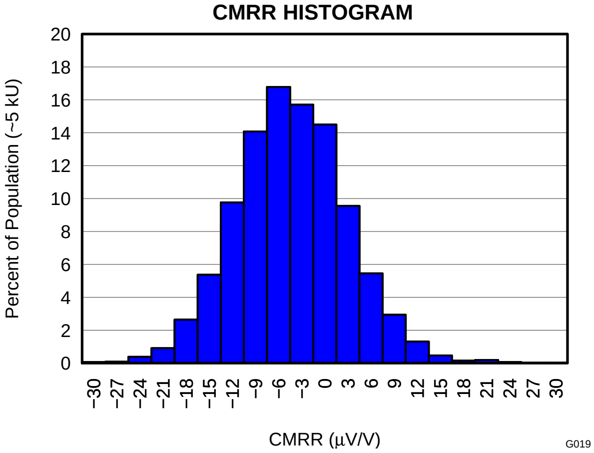

CMRR HISTOGRAM

Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

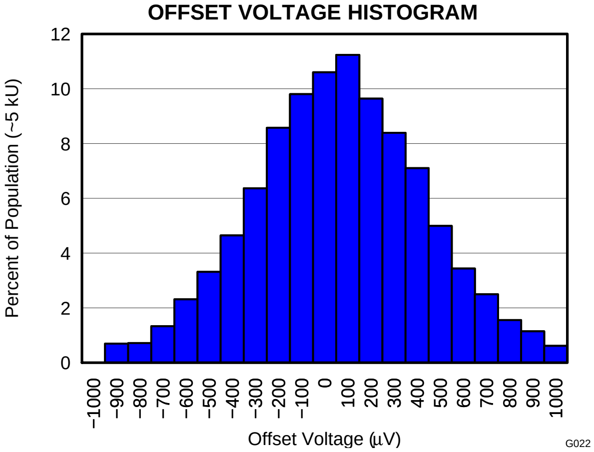
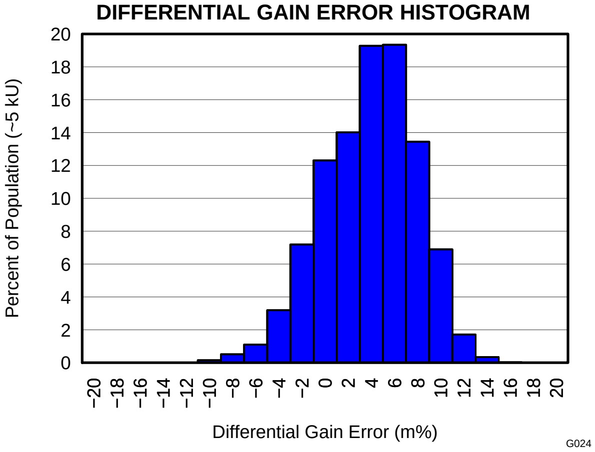


Figure 25.



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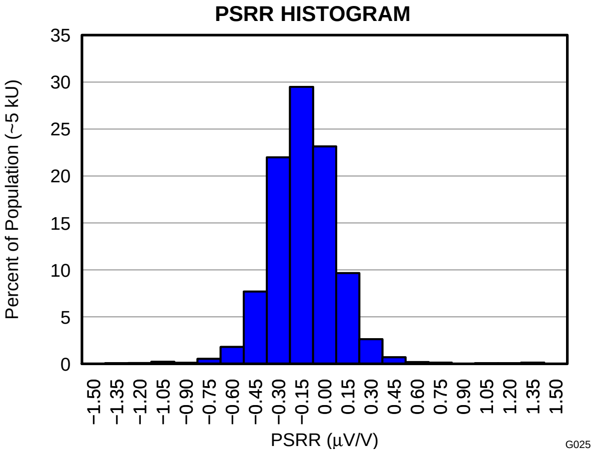


Figure 27.

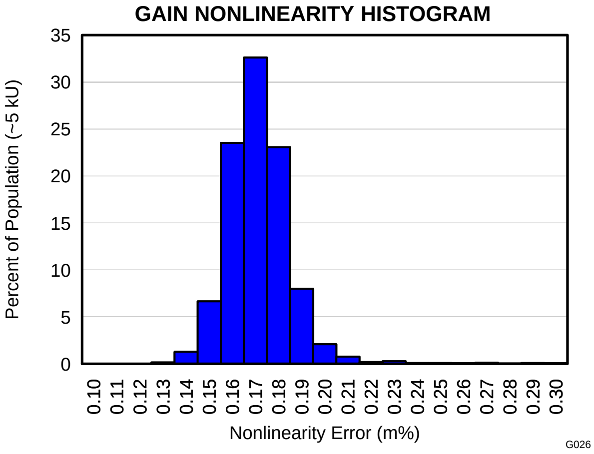


Figure 28.

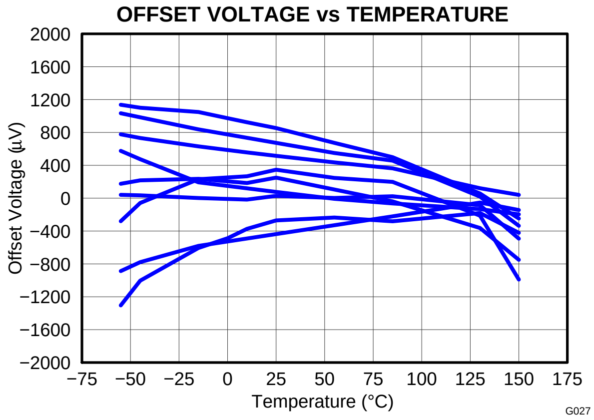


Figure 29.

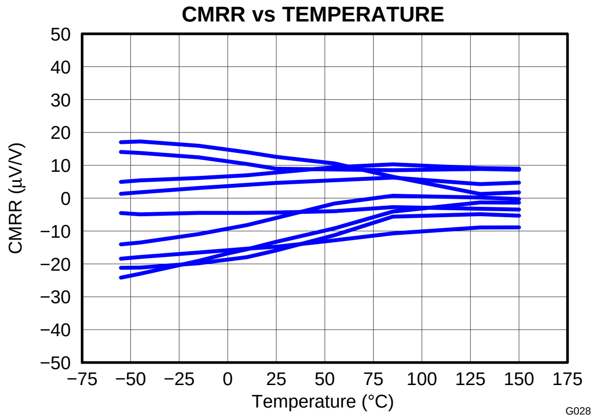


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

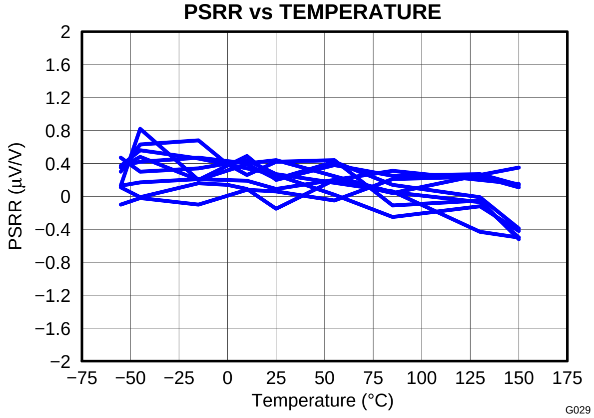


Figure 31.

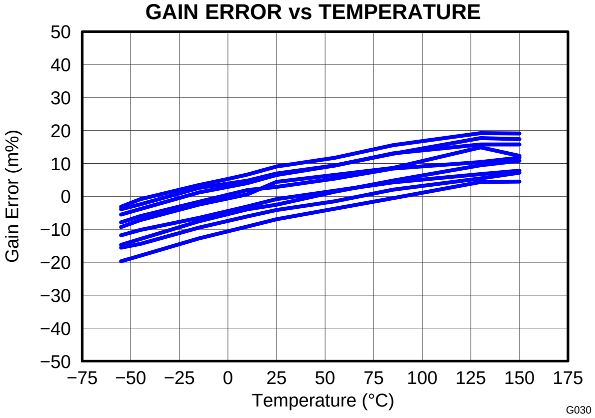


Figure 32.

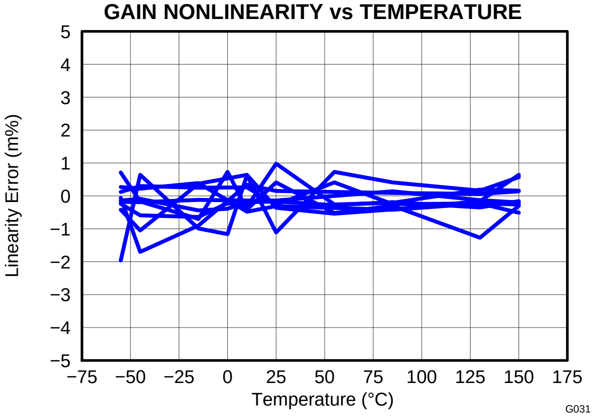


Figure 33.

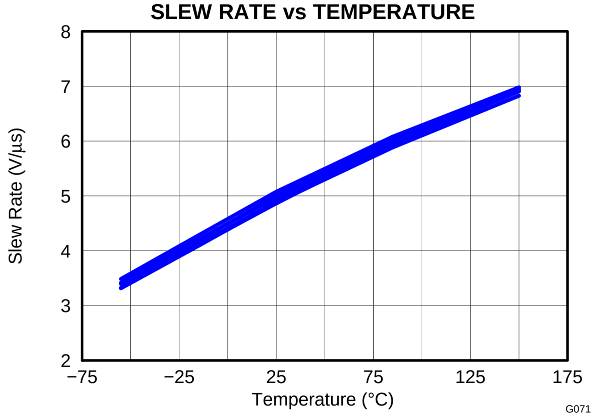


Figure 34.

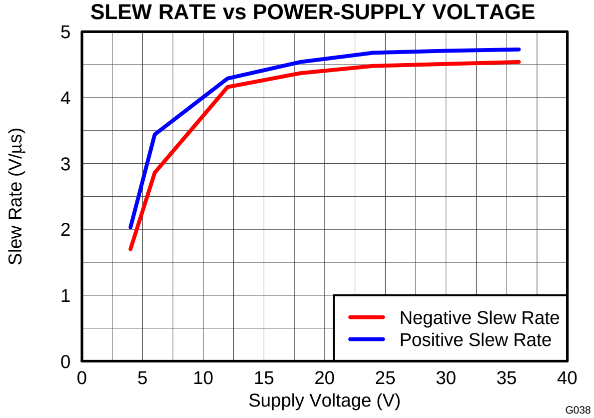


Figure 35.

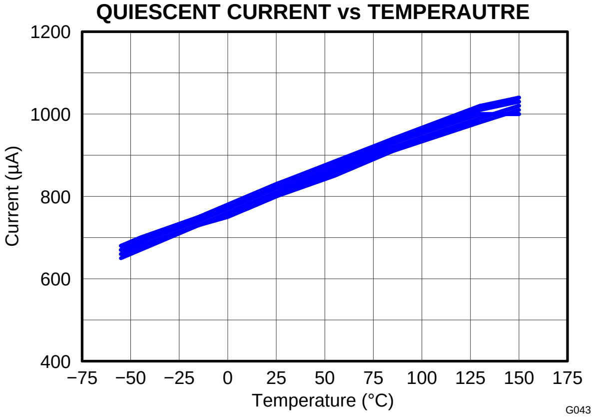


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

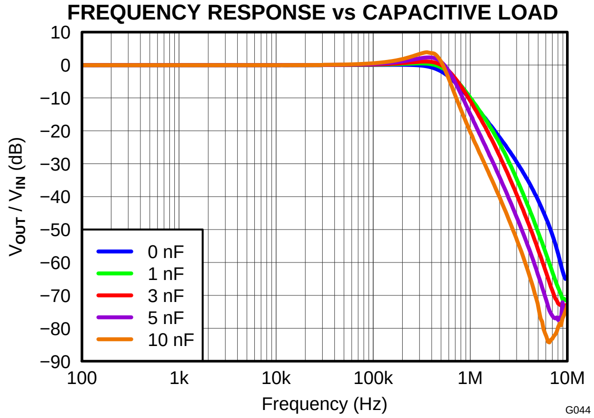

FREQUENCY RESPONSE vs CAPACITIVE LOAD

Figure 37.

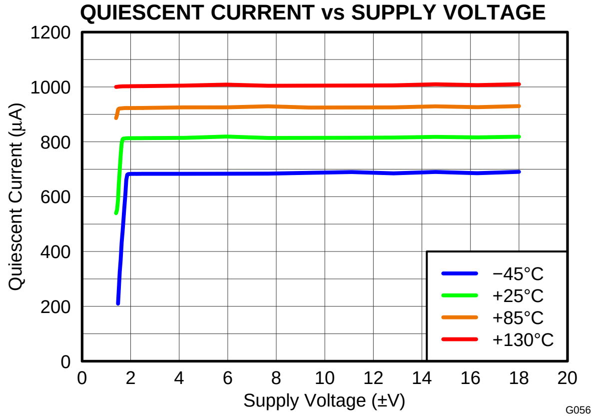

QUIESCENT CURRENT vs SUPPLY VOLTAGE

Figure 38.

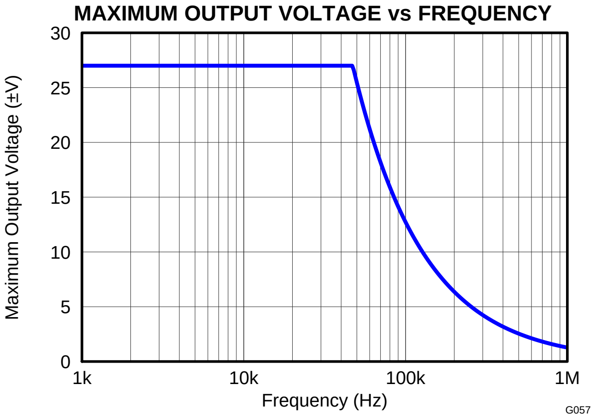

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

Figure 39.

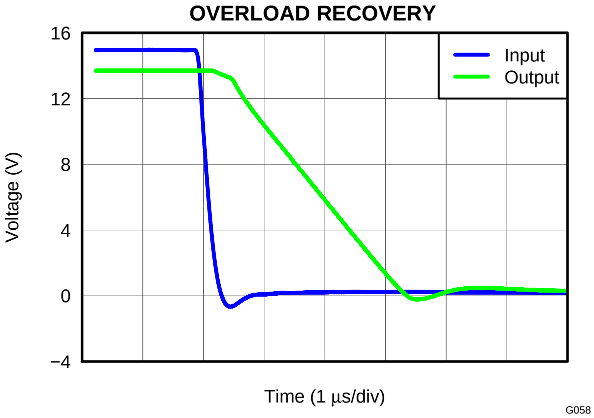

OVERLOAD RECOVERY

Figure 40.

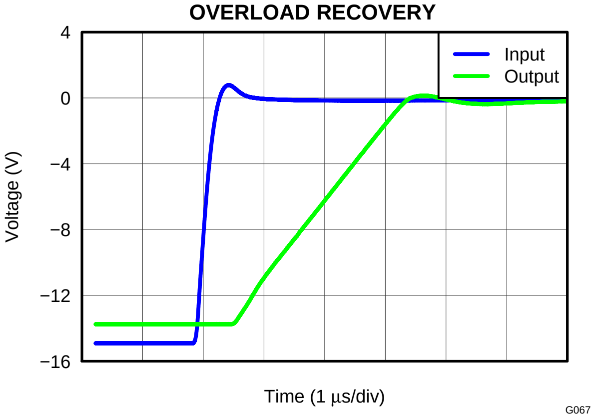

OVERLOAD RECOVERY

Figure 41.

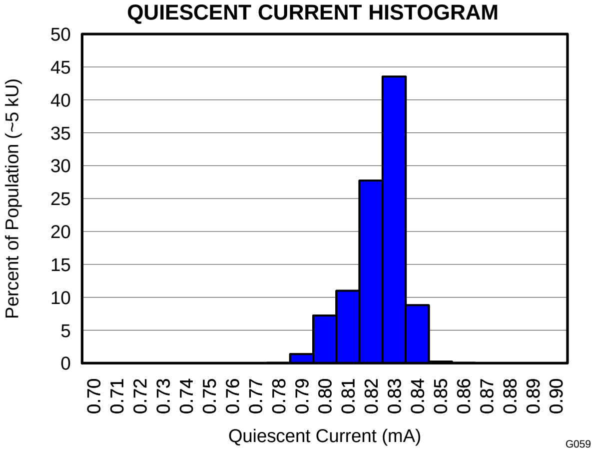

QUIESCENT CURRENT HISTOGRAM

Figure 42.

APPLICATION INFORMATION

BASIC INFORMATION

Figure 43 shows the basic connections required for dual-supply operation. Applications with noisy or high-impedance power-supply lines may require decoupling capacitors placed close to the device pins. The output voltage is equal to the differential input voltage between pins 2 and 3. The common-mode input voltage is rejected. Figure 44 shows the basic connections required for single-supply operation.

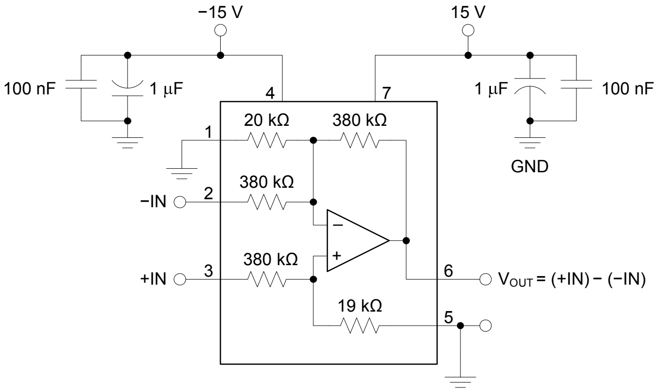


Figure 43. Basic Power and Signal Connections for Dual-Supply Operation

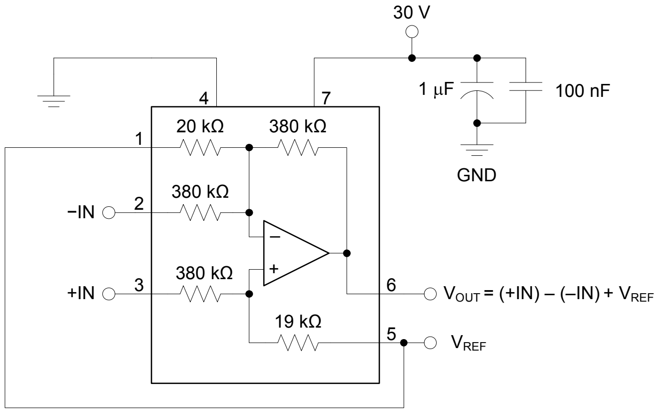


Figure 44. Basic Power and Signal Connections for Single-Supply Operation

TRANSFER FUNCTION

Most applications use the INA149 as a simple unity-gain difference amplifier. The transfer function is given in Equation 1:

$$V_{OUT} = (+IN) - (-IN) \quad (1)$$

Some applications, however, apply voltages to the reference terminals (REF_A and REF_B). The complete transfer function is given in Equation 2:

$$V_{OUT} = (+IN) - (-IN) + 20 \times REF_A - 19 \times REF_B \quad (2)$$

COMMON-MODE RANGE

The high common-mode range of the INA149 is achieved by dividing down the input signal with a high precision resistor divider. This resistor divider brings both the positive input and the negative input within the input range of the internal operational amplifier. This input range depends on the supply voltage of the INA149.

Both Figure 2 and Figure 3 can be used to determine the maximum common-mode range for a specific supply voltage. The maximum common-mode range can also be calculated by ensuring that both the positive and the negative input of the internal amplifier are within 1.5 V of the supply voltage.

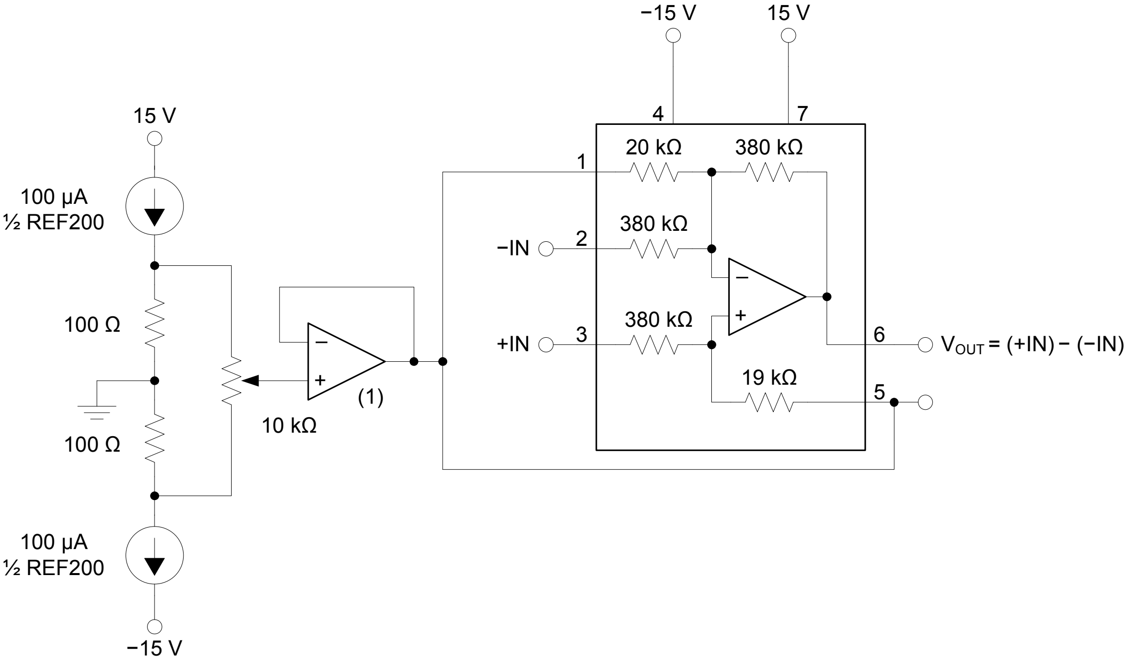
In case the voltage at the inputs of the internal amplifier exceeds the supply voltage, the internal ESD diodes start conducting current. This current must be limited to 10 mA to make sure not to exceed the absolute maximum ratings for the device.

COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA149 depends on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedance driving the two inputs. A 75-Ω resistance in series with pins 2 or 3 decreases the common-mode rejection ratio (CMRR) from 100 dB (typical) to 74 dB.

Resistance in series with the reference pins also degrades CMR. A 4-Ω resistance in series with pins 1 or 5 decreases CMRR from 100 dB to 74 dB.

Most applications do not require trimming. Figure 45 shows an optional circuit that may be used for trimming offset voltage and common-mode rejection.



(1) The OPA171 (a 36-V, low-power, RRO, general-purpose operational amplifier) can be used for this application.

Figure 45. Offset Voltage Trim Circuit

MEASURING CURRENT

The INA149 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. Figure 46 shows the INA149 used to measure the supply currents of a device under test.

The sense resistor imbalances the input resistor matching of the INA149, thus degrading its CMR. Also, the input impedance of the INA149 loads R_S, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor (R_C), equal to the value of R_S, as shown in Figure 46. If R_S is less than 5 Ω, degradation in the CMR is negligible and R_C can be omitted. If R_S is larger than approximately 1 kΩ, trimming R_C may be required to achive greater than 90-dB CMR. This error is caused by the INA149 input impedance mismatch.

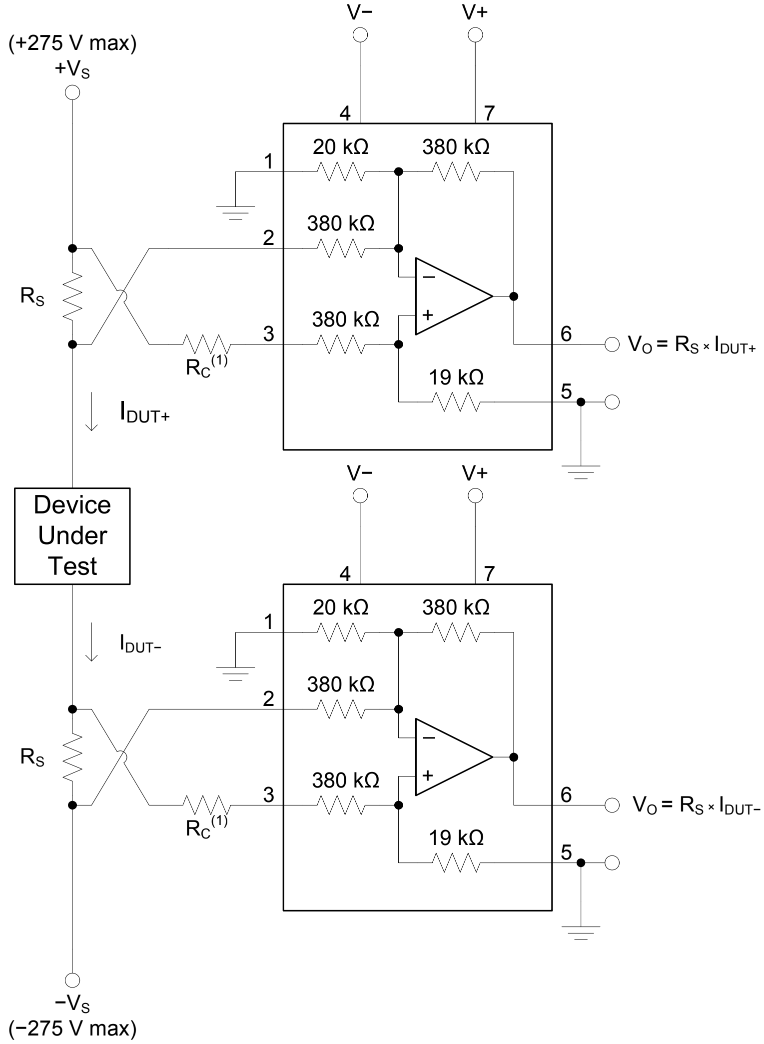


Figure 46. Measuring Supply Currents of a Device Under Test

If R_S is more than approximately 50 Ω, the gain error is greater than the 0.02% specification of the INA149. This gain error can be corrected by slightly increasing the value of R_S. The corrected value (R_S') can be calculated by

$$R_S' = R_S \times 380\text{ k}\Omega/(380\text{ k}\Omega - R_S) \quad (3)$$

Example: For a 1-V/mA transfer function, the nominal, uncorrected value for R_S would be 1 kΩ. A slightly larger value (R_S' = 1002.6 Ω), compensates for the gain error as a result of loading.

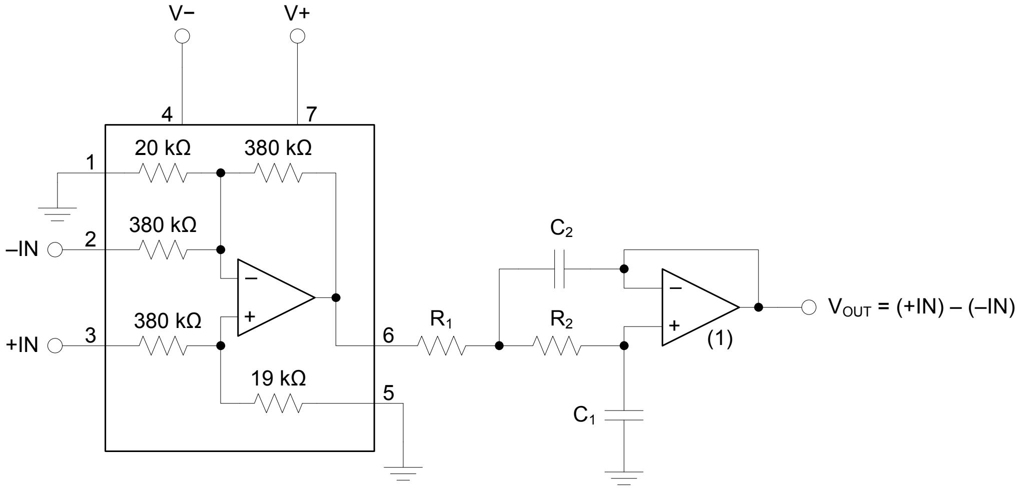
The 380-kΩ term in the equation for R_S' has a tolerance of 25%, thus sense resistors above approximately 400 Ω may require trimming to achive gain accuracy better than 0.02%.

NOISE PERFORMANCE

The wideband noise performane of the INA149 is dominated by the internal resistor network. The thermal or *Johnson noise* of these resistors measures approximately 550 nV/√Hz. The internal op amp contributes virtually no excess noise at frequencies above 100 Hz.

Many applications may be satisfied with less than the full 500-kHz bandwidth of the INA149. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in Figure 47 limits bandwidth and reduces noise. Because the INA149 has a 1/f noise corner frequency of approximately 100 Hz, a cutoff frequency below 100 Hz does not further reduce noise.

Component values for different filter frequencies are shown in Table 1.



(1) For most applications, the OPA171 can be used as an operational amplifier. For directly driving successive-approximation register (SAR) data converters, the OPA140 is a good choice.

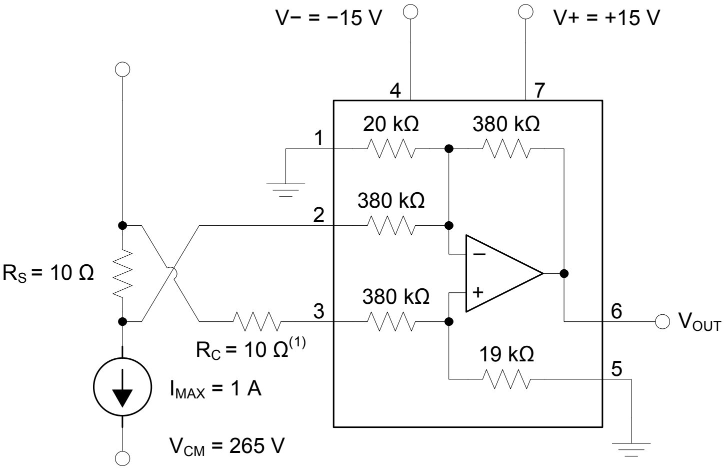
Figure 47. Output Filter for Noise Reduction

Table 1. Components Values for Different Filter Bandwidths

BUTTERWORTH LOW-PASS ($f_{-3\ dB}$)	OUTPUT NOISE (mV_{PP})	R_1	R_2	C_1	C_2
200 kHz	1.8	No filter			
100 kHz	1.1	11 kΩ	11.3 kΩ	100 pF	200 pF
10 kHz	0.35	11 kΩ	11.3 kΩ	1 nF	2 nF
1 kHz	0.11	11 kΩ	11.3 kΩ	10 nF	20 nF
100 Hz	0.05	11 kΩ	11.3 kΩ	0.1 µF	0.2 µF

ERROR BUDGET ANALYSIS

The following error budget analysis demonstrates the importance of a high common-mode rejection ratio when measuring small differential signals in the presence of high common-mode voltages. Figure 48 shows a typical current measurement application.



(1) See the *Measuring Current* section for details about R_C.

Figure 48. Typical Current Measurement Application

The maximum current through the shunt resistor (R_S) is 1 A and generates a full-scale voltage drop of 10 V. All error sources in this calculation are shown in relation to this full-scale voltage. The common-mode voltage in this scenario is 265 V and the temperature range is from room temperature (+25°C) to +85°C. Table 2 shows the dominant error sources for the INA149 and a competitor device.

Table 2. Error Budget Analysis

ERROR SOURCE	INA149	COMPETIOR A	ERROR (ppm of FS)	
			INA149	**COMPETITOR A**
Accuracy, T_A = +25°C				
Initial gain error	0.02% FS	0.05% FS	200	500
Offset voltage	1100 µV	1000 µV	110	100
Common mode	265 V/90 dB = 8380 µV	265 V/77 dB = 37432 µV	838	3743
		Total acuracy error	1148	4343
Temperature drift				
Gain	10 ppm/°C × 60°C	10 ppm/°C × 60°C	600	600
Offset voltage	10 µV/°C × 60°C	20 µV/°C × 60°C	60	120
		Total drift error	660	720
		Total error	**1808**	**5063**

If a smaller shunt resistor is used, the full-scale voltage drop is also smaller. A shunt resistor of 1 Ω causes a 1-V voltage drop with a current of 1 A flowing through it. The error of 1808 ppm for a full-scale voltage of 10 V becomes 18080 ppm (1.6%) for a full-scale voltage of only 1 V.

This example demonstrates that the dominate source of error, even over temperature, comes from the CMRR specification of the devices. The common-mode error is 46% of the total error for the INA149 and 74% of the total error for the competitor device.

BATTERY CELL VOLTAGE MONITOR

The INA149 can be used to measure the voltages of single cells in a stacked battery pack. Figure 49 shows an examples for such an application.

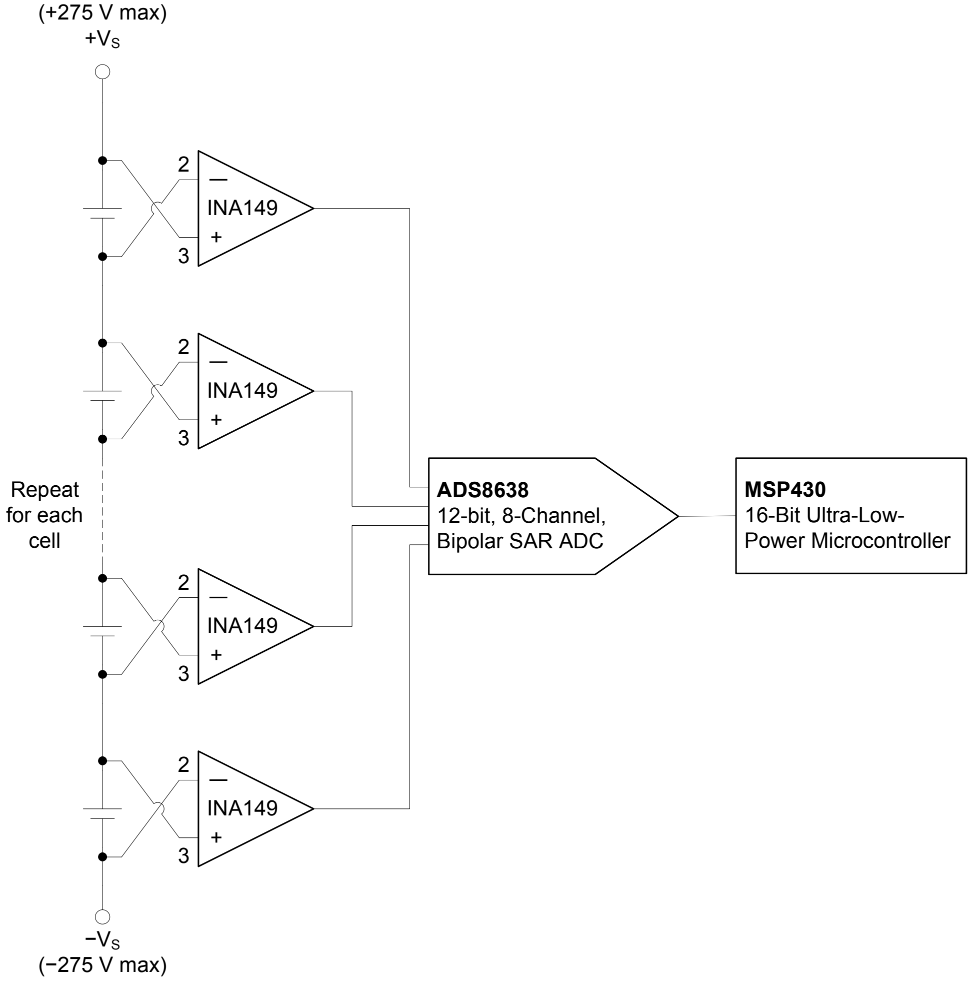


Figure 49. Battery Cell Voltage Monitor

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2011) to Revision B	Page
• Changed package marking data in Package/Ordering Information table	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA149AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 149A	Samples
INA149AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 149A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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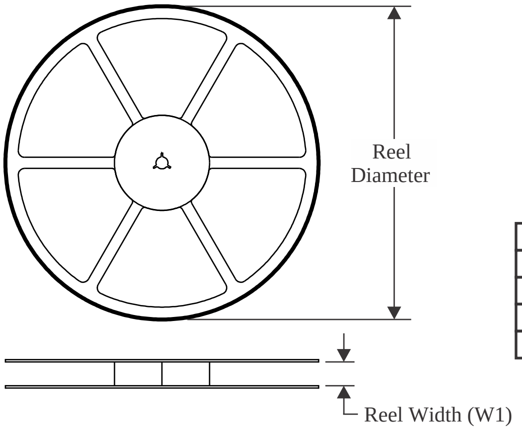
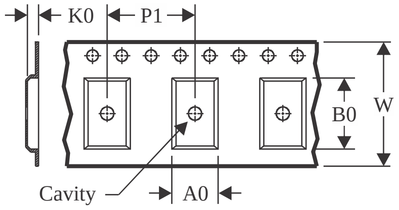
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

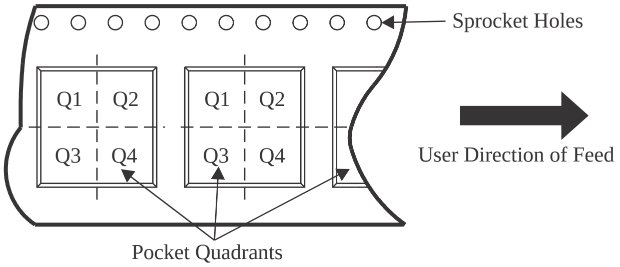


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

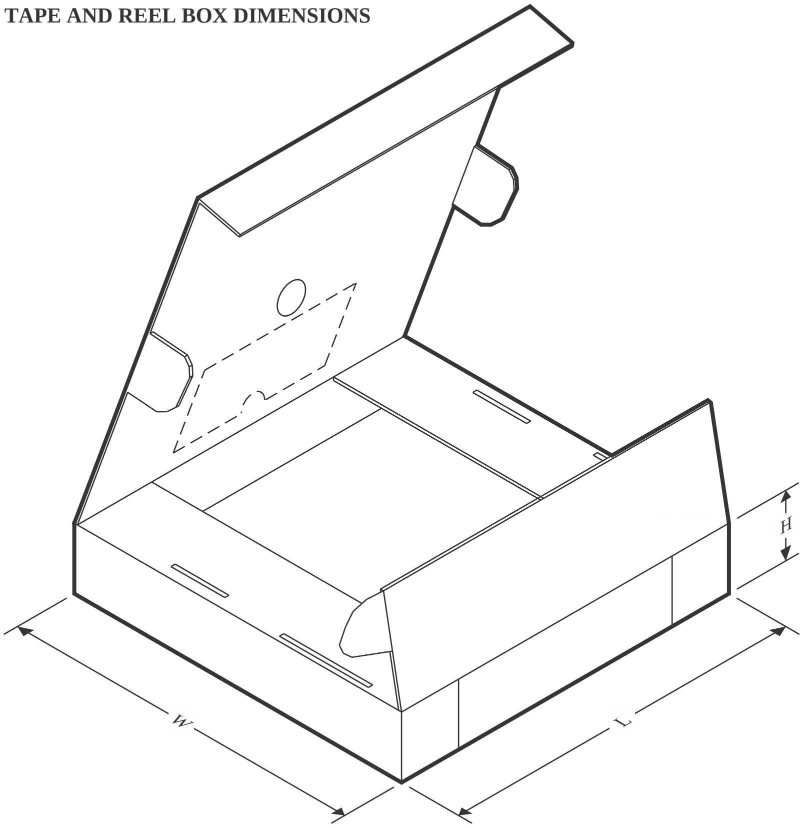
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA149AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

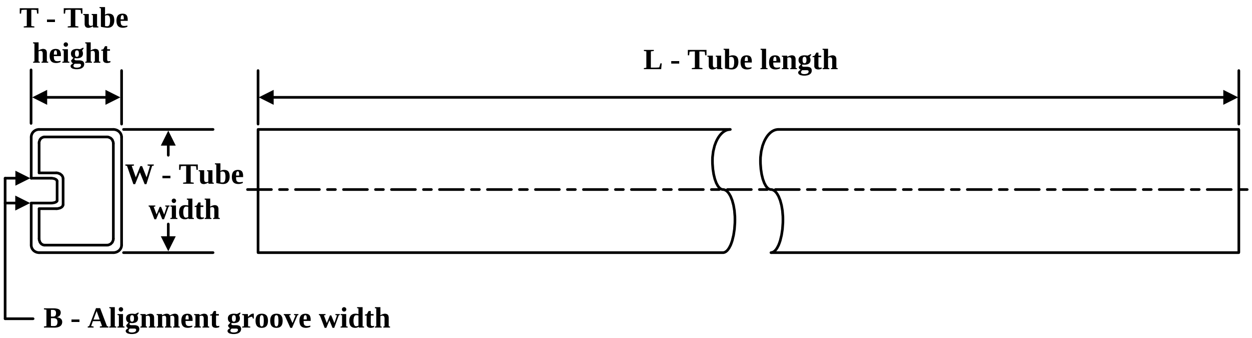
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

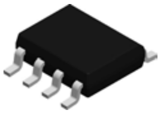
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA149AIDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA149AID	D	SOIC	8	75	506.6	8	3940	4.32

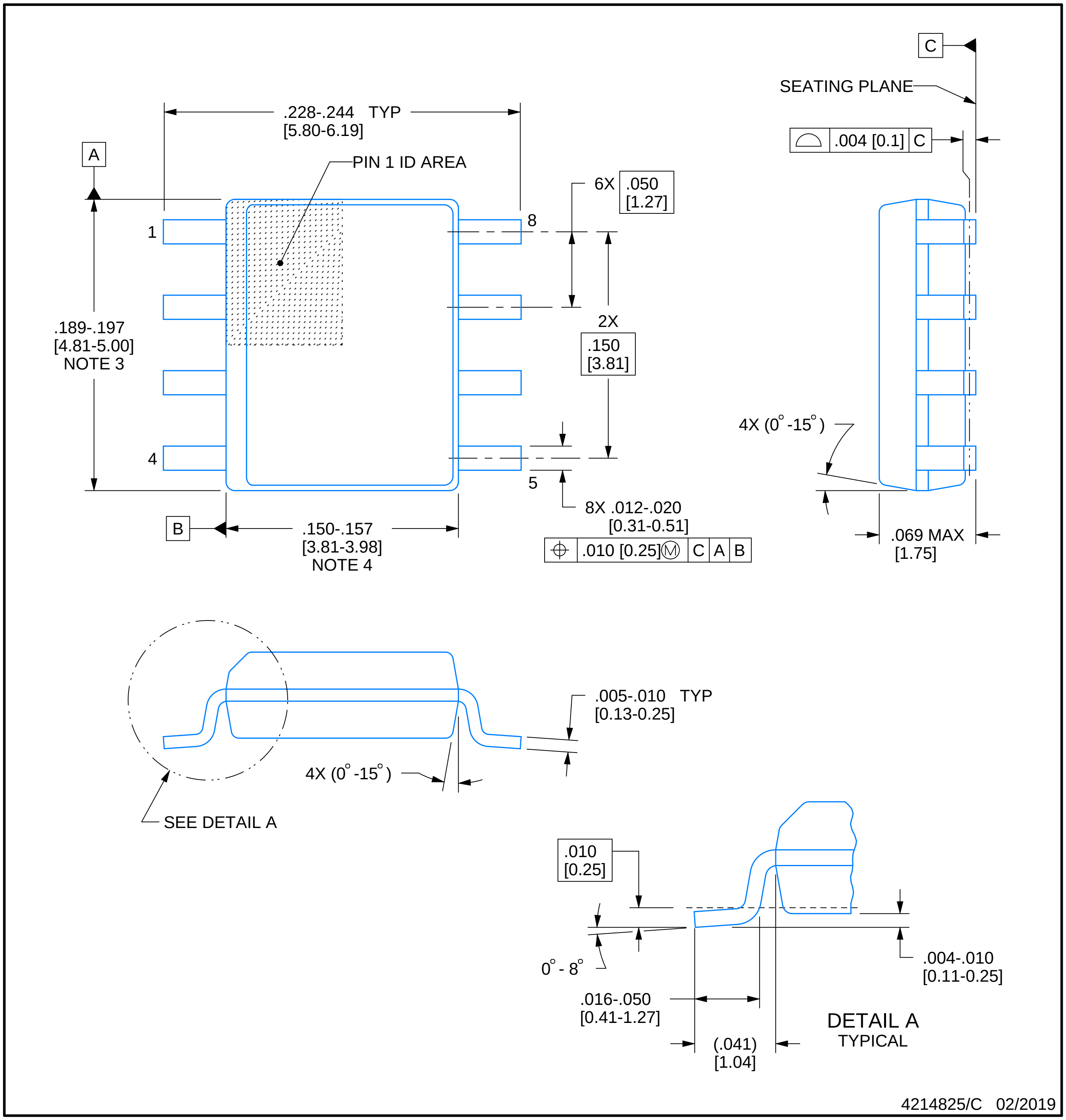


PACKAGE OUTLINE

D0008A

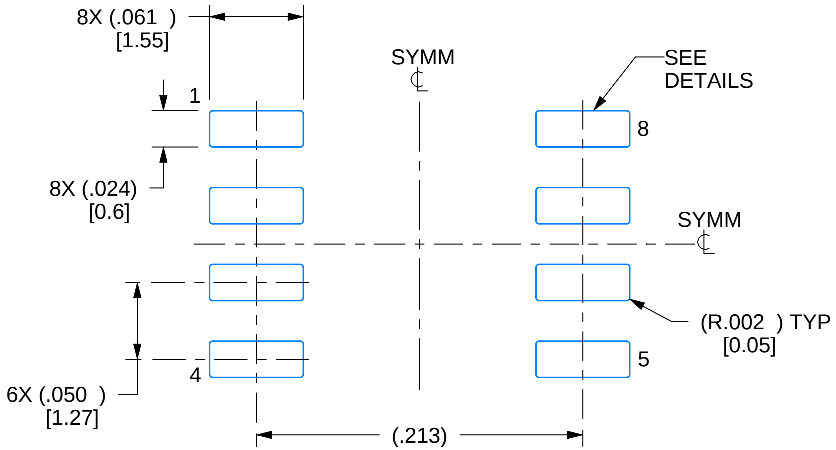
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

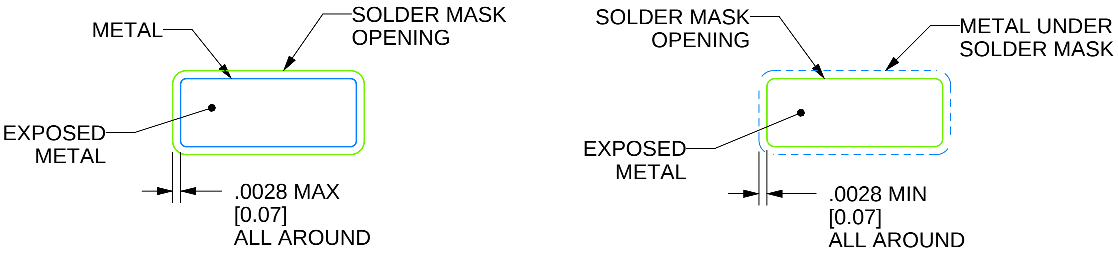


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

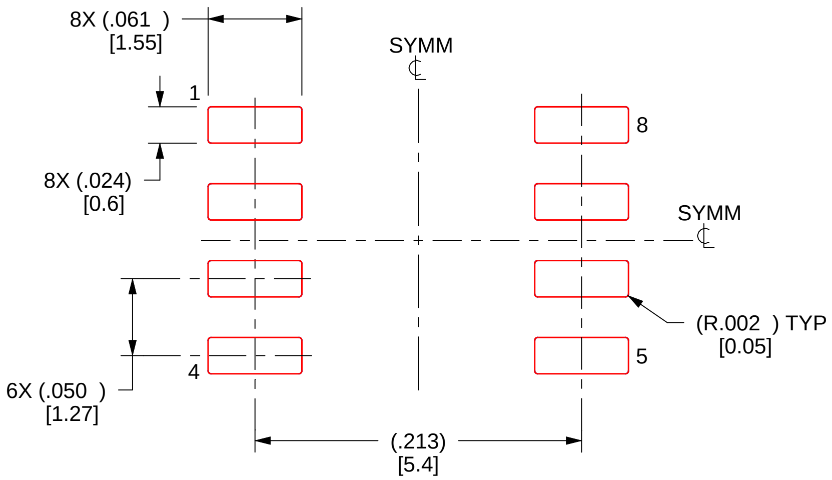
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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