AVS System Controller

Check for Samples: LM10000

FEATURES

- **Flexible Enable Inputs to Allow Independent Enable Control of External Controller and LM10000**
- **Fault Input Restores Output Voltage Setting to Default Value**
- **CNTL_EN Output That Enables/Disables External Controller**
- **7-Bit Current DAC That Can Directly Connect to the Feedback Node of an External Controller and Provide Smooth Voltage Control**
- **Programmable Slew Rate Control**

APPLICATIONS

- **AVS-Enabled ASICs and FPGAs**

KEY SPECIFICATIONS

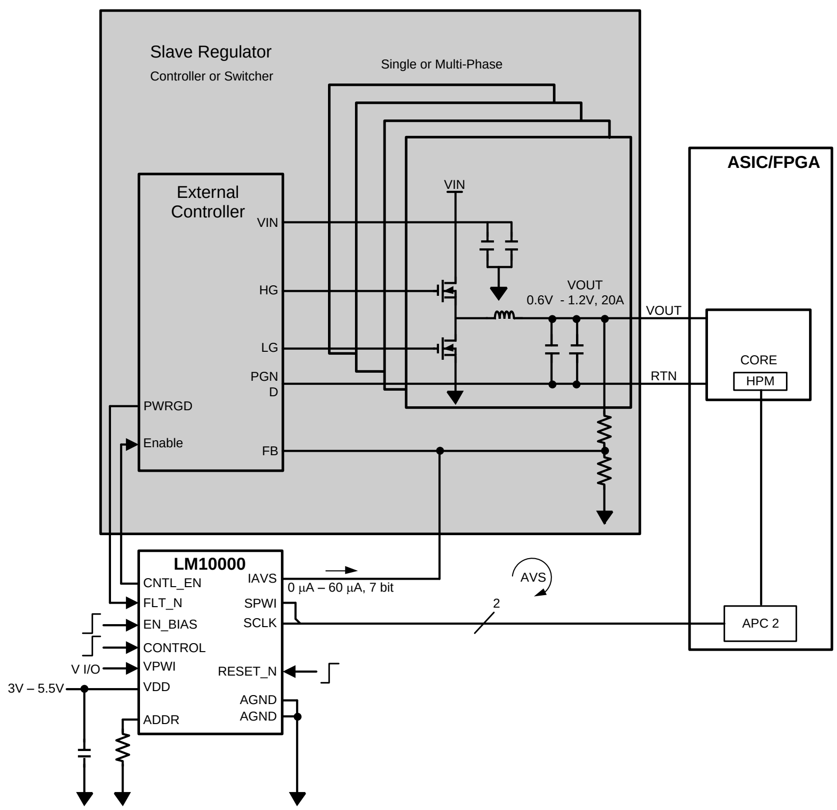
- **PWI 2.0 Interface**
- **AVS Control for One Output**
- **Precision Enable**

DESCRIPTION

The LM10000 is used to enable Adaptive Voltage Scaling (AVS) to non-AVS regulators. It includes a complete Slave Power Controller (SPC 2.0) to communicate to the PowerWise™ Interface (PWI 2.0), and a programmable current output DAC that allows voltage control to any regulator utilizing a feedback node/resistors to set the output voltage.

In addition to enabling AVS the LM10000 allows the system to control power states such as sleep and shutdown, and to configure the voltage step slew rate from the PWI.

TYPICAL APPLICATION CIRCUIT



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CONNECTION DIAGRAM

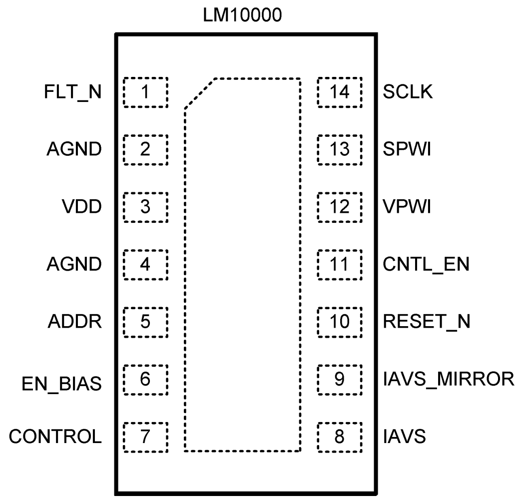


Figure 1. 14-Lead Plastic WSON

PIN DESCRIPTIONS

Pin No.	Pad Name	Type	Pad Description
1	FLT_N	Input	External fault input. Usually connected to PWGD output of integrated regulator.
2	AGND	GND	
3	VDD	Power	Analog Bias power input.
4	AGND	GND	
5	ADDR	Input	PWI address selection
6	EN_BIAS	Input	Enable input.
7	CONTROL	Input	V_{OUT} control input from system. Logic level.
8	IAVS	Output	Current DAC output that connects to feedback node of integrated regulator
9	IAVS_MIRROR	Output	Current DAC output that mirrors IAVS output current
10	RESET_N	Input	Reset, active low.
11	CNTL_EN	Output	Enable signal that connects to integrated regulator
12	VPWI	Power	PWI IO bias power
13	SPWI	I/O	PWI Data
14	SCLK	Input	PWI Clock

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1) (2)(3)

VPWI to GND		−0.2V to VDD
FLT_N, VDD, ADR, EN_BIAS, CONTROL, IAVS, IAVS_MIRROR, RESET_N, CNTL_EN, VPWI, SPWI, SCLK to GND		−0.2V to 6V
Junction Temperature		−45°C to +125°C
Storage Temperature		−45°C to +150°C
Soldering Information: See http://www.ti.com/lit/SNOA549		
ESD Ratings (4)	Human Body Model	2kV
	Machine Model	200V

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. **Operating ratings** indicate conditions for which the device operates correctly. **Operating Ratings** do not imply ensured performance limits.
(2) The power MOSFETs can run on a separate 1V to 14V rail (Input voltage, V_{IN}). Practical lower limit of V_{IN} depends on selection of the external MOSFET. See the MOSFET GATE DRIVERS section under Application Information for further details.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) ESD using the human body model which is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

OPERATING RATINGS (1) (2)

VDD	3.0V to 5.5V
VPWI (3)	1.6V to 3.6V

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. **Operating ratings** indicate conditions for which the device operates correctly. **Operating Ratings** do not imply ensured performance limits.
(2) The power MOSFETs can run on a separate 1V to 14V rail (Input voltage, V_{IN}). Practical lower limit of V_{IN} depends on selection of the external MOSFET. See the MOSFET GATE DRIVERS section under Application Information for further details.
(3) VPWI cannot be higher than VDD.

THERMAL PROPERTIES

Junction-to-Ambient thermal resistance	54.7°C

ELECTRICAL CHARACTERISTICS

Limits appearing in standard type apply for T_J = 25°C. Limits appearing in **boldface** type apply over full operating junction temperature range (−40°C ≤ T_J ≤ +125°C. Unless otherwise noted, specifications apply to the LM10000 Typical Application Circuit (pg. 2) with: V_{DD} = 5.0V, C_{IN} = 1µF.

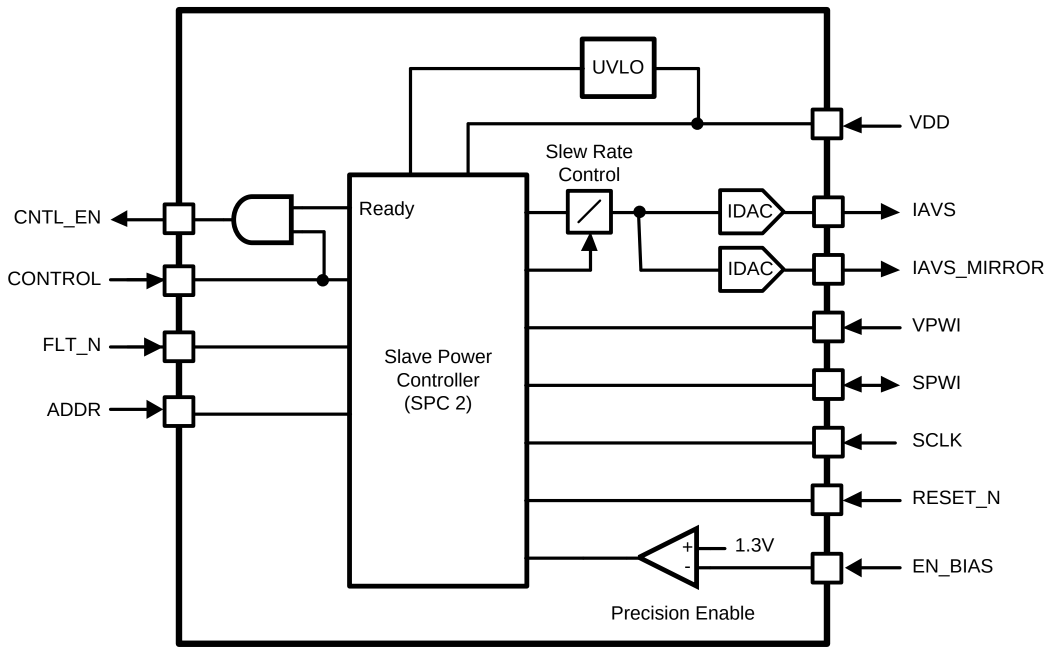
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_q	Quiescent Current	EN_BIAS = 0V, CONTROL = 0V		1.5	**10**	µA
		EN_BIAS = VDD, CONTROL = VDD R0 = 0x7F		315	**410**	
		EN_BIAS = VDD, PWI Sleep Command		196	**300**	
		EN_BIAS = VDD, PWI Shutdown Command		23	**75**	
UVLO	Rising Threshold			2.65	**2.75**	V
	Falling Threshold		**2.27**	2.40		
	Hysteresis			257		mV
I_{ADDR}	Address pin source current			7.5		µA
IDAC						
ACC	Accuracy	Measured at full scale	**−3**		**3**	%
LSB	DAC Step Size	$I_{DAC-MAX} / 2^n$ (1≤ n ≤ 7)		470		nA
	Resolution		7			Bits
FS	Full Scale			59.69		µA
INL	Integral Non-Linearity		−2		2	LSB
DNL	Differential Non-Linearity		−0.5		0.5	LSB

ELECTRICAL CHARACTERISTICS (continued)

Limits appearing in standard type apply for T_J = 25°C. Limits appearing in **boldface** type apply over full operating junction temperature range (−40°C ≤ T_J ≤ +125°C. Unless otherwise noted, specifications apply to the LM10000 Typical Application Circuit (pg. 2) with: V_{DD} = 5.0V, C_{IN} = 1µF.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ZE	Zero Code Error/Offset Error			57		nA
LOGIC AND CONTROL INPUTS						
EN_BIAS_{TH}	Precision enable threshold	Rising		1.32	**1.4**	V
		Falling	**1.09**	1.19		
I_{IL}	Input Current Low	FLT_N, RESET_N	**−10**			µA
		ENBIAS, CONTROL	**−1**			
		SPWI, SCLK	**−1**			
I_{IH}	Input Current High	FLT_N, RESET_N			**1**	µA
		ENBIAS, CONTROL			**10**	
		SPWI, SCLK			**5**	
V_{IL}	Input Low Voltage	CONTROL, FLT_N, RESET_N			**0.5**	V
V_{IH}	Input High Voltage	CONTROL, FLT_N, RESET_N	**1.1**			V
V_{IL_PWI}	Input Low Voltage, PWI	SPWI, SCLK, 1.6 < VPWI < 3.6			**30**	% of VPWI
V_{IH_PWI}	Input High Voltage, PWI	SPWI, SCLK, 1.6 < VPWI < 3.6	**70**			
f_{SCLK}	PWI2 SCLK	**DC useful for testing/debug	0		15M	Hz
LOGIC AND CONTROL OUTPUTS						
V_{OL}	Output Low Level	CNTL_EN, I_{SINK} ≤ 100 µA			0.4	V
V_{OH}	Output High Level	CNTL_EN, I_{SOURCE} ≤ 100 µA	VDD - 0.4			
V_{OH_PWI}	Output High Level, PWI	SPWI, I_{SOURCE} ≤ 1mA	VPWI - 0.4			

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

EN_BIAS to CNTL_EN Delay (CONTROL held HIGH)

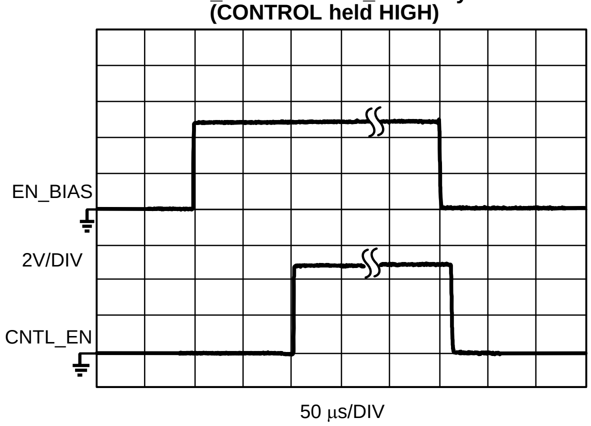


Figure 2.

CONTROL to CNTL_EN Delay (EN_BIAS held HIGH)

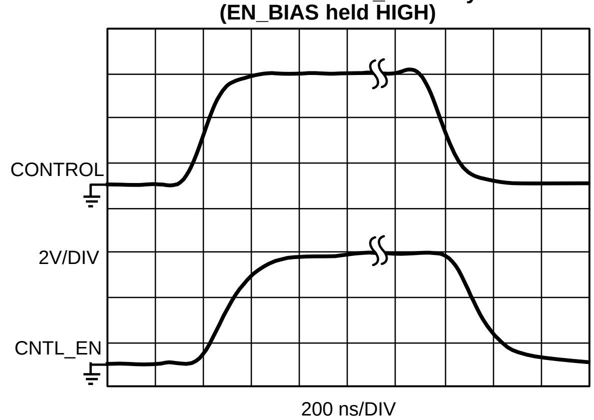


Figure 3.

V_{OUT} Reset by FLT_N Trigger

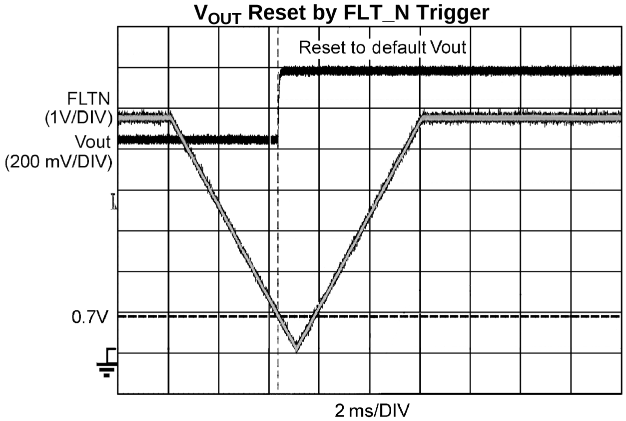


Figure 4.

IAVS Slew Rate Programmability

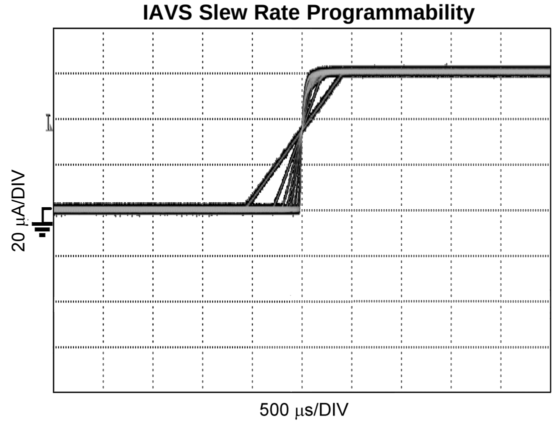


Figure 5.

LM10000 PWI REGISTER MAP

The PWI 2.0 standard defines 32 8-bit base registers, and up to 256 8-bit extended registers, on each PWI slave. The table below summarizes these registers and shows default register bit values after reset, as programmed by the factory. The following sub-sections provide additional details on the use of each individual register.

Table 1. SUMMARY(1)

Base Registers											
Register Address	Register Name	Register Usage	Type	Reset Default Value							
				7	6	5	4	3	2	1	0
0x00	R0	IAVS	R/W	0*	Configured by R9						
0x03	R3		R/O	0	0	0	0	1	1	1	FLT_N
0x04	R4	Device Capability	R/O	0	0	0	0	0	0	1	0
0x09	R9	IAVS Default	R/W	IAVS Default Code							
0x0A	R10	Ramp Control	R/W	1	0	0	1	1	1	0	0
0x0F	R15	Revision ID	N/A	0	0	0	0	0	0	0	0
0x1F	R31	Reserved **Do not write to**	R/W	-	-	-	-	-	-	-	-

(1) A bit with an asterisk (*) denotes a register bit that is always read as a fixed value. Writes to these bits will be ignored. A bit with a hyphen (-) denotes a bit in an unimplemented register location. A write into unimplemented register(s) will be ignored. A read of an unimplemented register(s) will produce a “No response frame”. Please refer to PWI specification version 2.0 for further information.

R0 - IAVS AVS FEEDBACK CURRENT INJECTION	
Address	0x00
Type	R/W
Reset Default	8h'7F

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:0	IAVS Sourcing Current	Programmed voltage value. Default value is in **bold.**	
		Current Data Code [6:0]	Current (µA)
		7h'00	60
		7h'xx	Linear Scaling
		7h'7F	**0 (default)**

R3 - STATUS LM10520 ADDRESS	
Address	0x03
Type	R/O
Reset Default	–

Bit	Field Name	Description or Comment
7:4	Not Used	Always read back 0
3:1	Not Used	Always read back 1
0	FLT_N	1: FLT_N is high (no fault) 0: FLT_N is low (fault)

R4 - DEVICE CAPABILITY REGISTER	
Address	0x04
Type	R/O
Reset Default	8h'02

Bit	Field Name	Description or Comment
7:3		Always read back 0
2:0		Always read back 010, specifying PWI 2.0

R9 - IAVS DEFAULT REGISTER	
Address	0x09
Type	R/W
Reset Default	8h'7F

Bit	Field Name	Description or Comment	
7	Sign	Always read back 0.	
6:0	IAVS Default	Current Data Code [6:0]	Current (µA)
		7h'00	60
		7h'xx	Linear Scaling
		7h'7F	**0 (Default)**

R10 - RAMP CONTROL	
Address	0x0A
Type	R/W
Reset Default	8h'9C

Bit	Field Name	Description or Comment				
7	Ramp Control Enable	1: Enabled 0: Disabled				
6	Not Used	Always read 0				
5:3	Ramp Time Step Control	Ramp Time Step Control			Ramp Time Step (µs)	
		0	0	0	1	
		0	0	1	2	
		0	1	0	3	
		0	1	1	4	
		1	0	0	6	
		1	0	1	8	
		1	1	0	12	
		1	1	1	16	
2:0	Ramp Code Step Control	Ramp Code Step			Rising Step (LSB)	Falling Step (LSB)
		0	0	0	1	1
		0	0	1	2	1
		0	1	0	3	2
		0	1	1	4	3
		1	0	0	6	4
		1	0	1	8	5
		1	1	0	12	6
		1	1	1	16	8

R15 - REVISION ID REGISTER	
Address	0x0F
Type	R/O
Reset Default	8h'00

Bit	Field Name	Description or Comment
7:0		Always read back 0

OPERATION DESCRIPTION

GENERAL DESCRIPTION

The LM10000 provides all the circuitry needed to enable most DC/DC regulators to work in a PowerWise® Adaptive Voltage Scaling (AVS) system. It communicates via the PowerWise Interface (PWI), and has analog outputs to control the output voltage of a slave power regulator. The slave power regulator can be any device that sets its output voltage with a feedback resistor divider.

THEORY OF OPERATION

The LM10000 can be thought of as a D/A converter, converting PWI communication to analog outputs. One of the outputs is a current DAC (IAVS), which is connected to the feedback node of a slave regulator. Therefore, all PWI Change Voltage Commands (CVC) are decoded into a 7-bit current DAC output. The impedance of the feedback node at DC appears as the top feedback resistor. This is because the control loop of the slave regulator effectively maintains a constant current/voltage across the bottom feedback resistor, and creates low impedance at the V_{OUT} node. Therefore, as more current is sourced into the feedback node, the more the output voltage is reduced. See Figure 6.

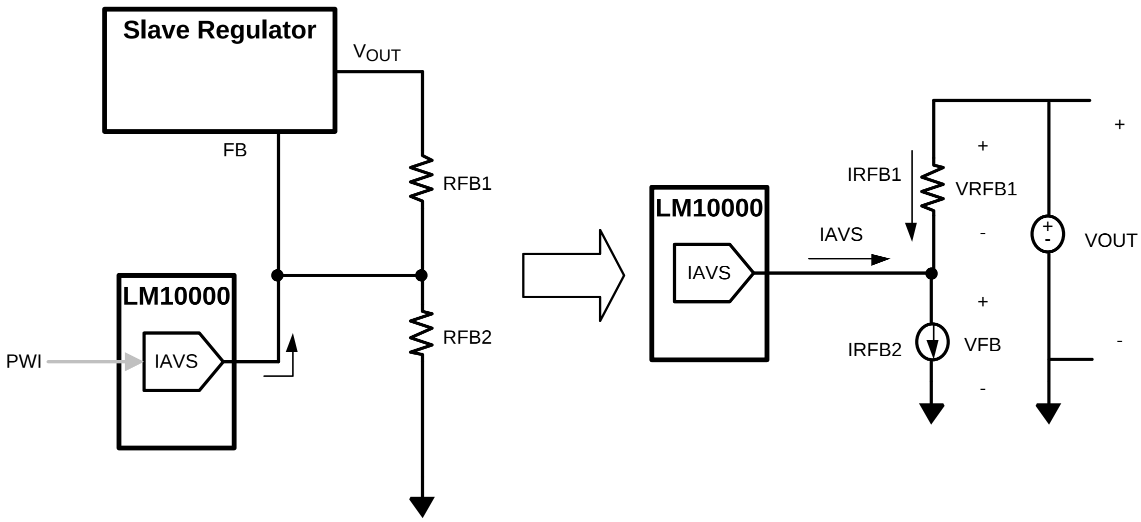


Figure 6. Output Voltage Is Controlled Via current Injection Into Feedback Node

DIGITAL POWER MANAGEMENT

In addition to adaptive voltage scaling, the PWI and LM10000 enhance the slave regulator with basic digital power management control. This includes control of power states such as SHUTDOWN, SLEEP, and ACTIVE, ON/OFF sequencing, and voltage scaling slew rate. Figure 7 shows the LM10000 with available system connectivity options. The LM10000 has a flexible set of logic enable pins to allow the system easy interface to power states and sequencing. A logic CNTL_EN output is provided to drive the slave regulator enable according the power state of the LM10000. For example, if a PWI SHUTDOWN command is issued to LM10000, the CNTL_EN output is immediately driven to 0V, which if connected to the slave regulator enable input, will turn off the output voltage and enter a low I_q state. A summary of the logic inputs and outputs is given is LOGIC INPUTS AND OUTPUTS table.

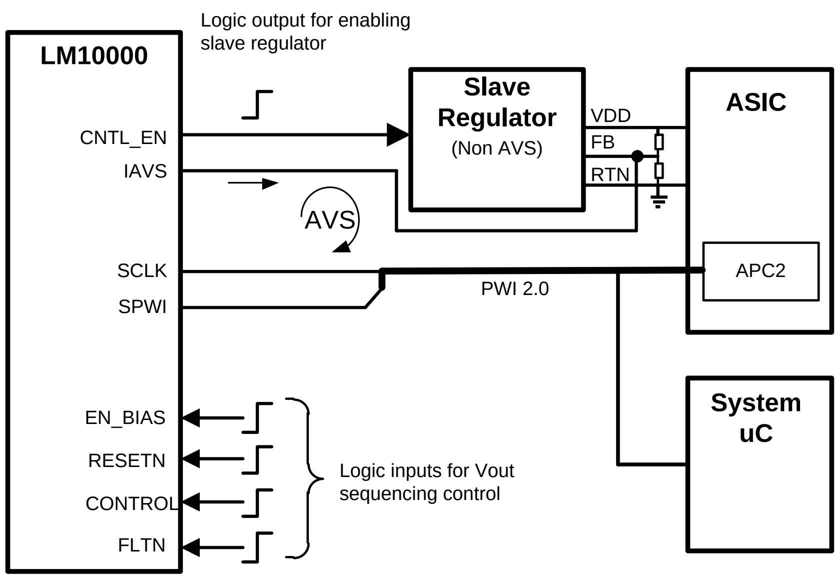


Figure 7. LM10000 provides flexible digital power management via multi-master PWI 2.0, and flexible V_{OUT} sequencing control

IAVS OUTPUT CURRENT: CONTROLLING THE OUTPUT VOLTAGE

The LM10000 uses a 7-bit current DAC to control the output voltage of a slave power regulator. Since it is a current output, IAVS can be connected directly to the feedback node of the slave power regulator. IAVS has a range of 0 – 60 µA with 7 bits of resolution, or a 0.469 µA LSB.

A typical connection of the IAVS injection current into a slave regulator is shown in Figure 8. The output voltage VOUT is expressed as:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) - I_{AVS} \times R_{FB1} \quad (1)$$

Where VFB = the regulated feedback voltage of the slave regulator. This equation is valid for V_{OUT} > VFB.

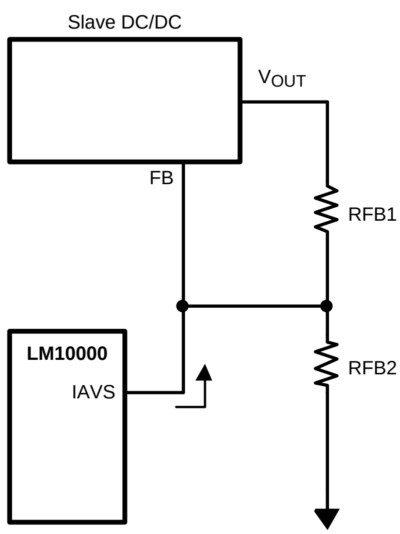


Figure 8. IAVS Injection Current Into A Slave Regulator

USING REGISTER R9 TO CHANGE THE DEFAULT OUTPUT VOLTAGE

The LM10000 default IAVS current is set by R9. R9 is trimmed to 0x7F, so that IAVS = 0µA when power is applied to LM10000. Between power cycling, R9 can be changed so that IAVS defaults to values between 0 - 60 µA. This can be useful for software trim of the default output voltage of the LM10000 controlled regulator. In order to do this, the system must take care to write to R9 before enabling the output (the output can be enabled/disabled while keeping the LM10000 logic on via the CONTROL input). Therefore, R9 must be written to by some system controller that is on a different power domain than that provided by LM10000. In addition, the “INITIAL_VDD” register in the Advanced Power Controller (APC) must have the same value as R9 so that the APC and LM10000 default to the same voltage code.

IAVS MIRROR OUTPUT CURRENT

IAVS Mirror sources a current equal to IAVS.

DIGITAL SLEW RATE CONTROL

The IAVS and IAVS Mirror outputs have an adjustable, digital slew rate control. The slew rate control is programmed in register R10. The slew rate of the output voltage will effect both the output and input inrush current needed to scale the output voltage up or down. The amount of output current source or sink needed to scale the output voltage is governed by the equation describing current in a capacitor:

$$iC = C \times dV/dt \quad (2)$$

Therefore, more current is needed for larger voltage steps (dV) and for smaller settling times (dt). This current is in addition to the load current that the slave regulator is providing. It is recommended that the total current (load current + voltage slew current) not exceed the slave regulator current limit.

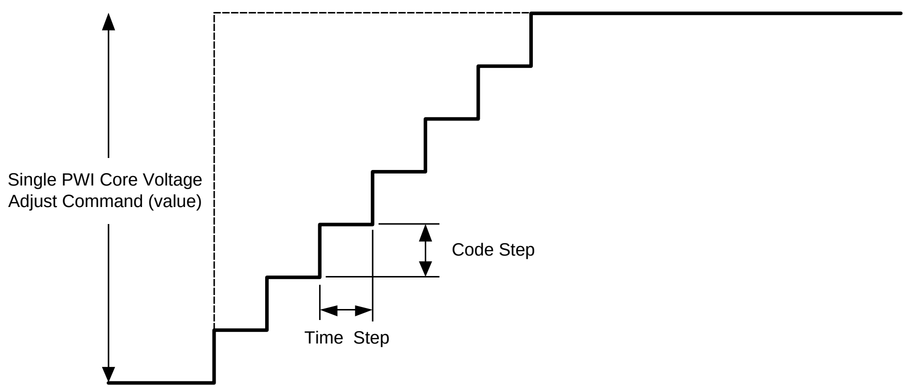


Figure 9. Digital Slew Rate Control

PWI ADDRESS

A resistor from the ADDR pin to ground sets the device's PWI address. The device senses the resistance as it is initializing from the shutdown state. The device will not update the address until it cycles through shutdown again. Use the table below to choose the appropriate resistor to place form ADDR pin to ground.

PWI Address	Resistance (± 1% tolerance)
0	≤ 40.2 kΩ
1	60.4 kΩ
2	80.6 kΩ
3	100 kΩ
4	120 kΩ
5	140 kΩ
6	160 kΩ
7	180 kΩ

INPUTS: ENBIAS, CONTROL, FLT_N, RESET_N, SCLK, SPWI

ENBIAS

The ENBIAS logic input enables the internal circuitry of the LM10000. The LM10000 goes through an initialization procedure upon the rising edge of ENBIAS. Initialization is complete within 100 µsec, after which the device is ready to be used.

If at any point ENBIAS goes low, the device enters a low I_q shutdown state.

CONTROL

The CONTROL logic input allows control of the CNTL_EN output without incurring delays associated with initialization. This signal is effectively ANDed with the internal 'ready' signal, which is high once initialization is complete.

The CONTROL pin level toggles the device between Active and Sleep states, and will reset the R0 register

FLT_N

The FLT_N logic input resets and holds the R0 register when its input signal is low. It has no effect on CNTL_EN. This provides a convenient way to support automatic fault recovery modes in the slave power regulator. When connected to a standard PWGD pin of a DC/DC regulator, FLT_N will reset and hold R0 as long as PWGD is low, allowing the slave regulator to recover from the fault by returning to the default voltage. Once FLT_N returns high, R0 can be written to.

RESET_N

The RESET_N provides a separate, level controlled logic reset.

SCLK and SPWI

SCLK and SPWI provide serial PWI communication

OUTPUTS: CNTL_EN, IAVS

CNTL_EN

The CNTL_EN output connects to the slave regulator enable pin. CNTL_EN allows power state control via the PWI interface or ENBIAS/CONTROL logic inputs. For a direct connection from CNTL_EN to the enable pin of the slave regulator, the enable pin on the slave regulator needs to be level based and active high (a logic high voltage enables the slave regulator). LM10000 will drive CNTL_EN to the VDD voltage to enable the slave regulator, and to 0V to disable the slave regulator. In the case that the enable/disable on the slave regulator is a different function (impedance based or active low), extra circuitry is required.

UVLO

The LM10000 includes a UVLO circuit with hysteresis that triggers off of VDD. The system designer should be aware of the different UVLO thresholds of LM10000 and the slave regulator it is controlling. Since LM10000 is controlling the output of the slave regulator, the UVLO circuits in both the LM10000, and the slave regulator can react to severe input voltage transients. This is normally not a problem unless the application is operating very close to the UVLO thresholds of the two devices.

STATES

STARTUP

During the startup state, the LM10000 initializes all its registers and enables its bandgap. This process typically takes 100 µsec. CNTL_EN is low during startup.

ACTIVE

During the active state, CNTL_EN is high, the IAVS DACs are enabled, and PWI registers can be accessed.

SLEEP

During the sleep state, CNTL_EN is low, the IAVS DACs are disabled, and PWI registers can be accessed.

FAULT

During the fault state, the IAVS current register (R0) is reset, after which the LM10000 automatically returns to its previous state.

SHUTDOWN

During the shutdown state, CNTL_EN is low, the IAVS DACs are disabled, and most internal circuitry is disabled. Only the PWI state machine is biased to allow register access.

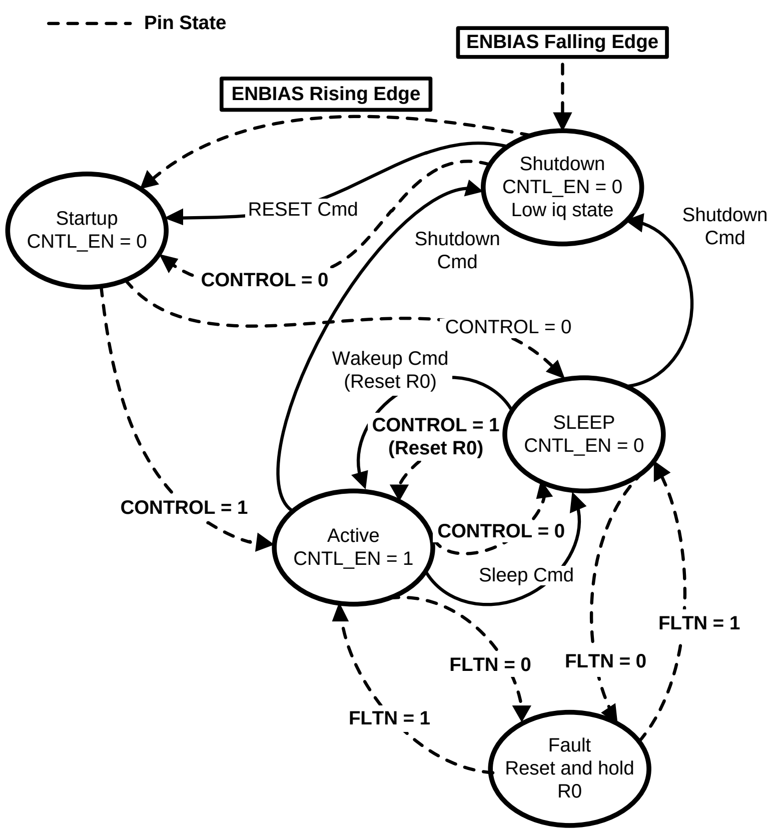


Figure 10. LM10000 State Diagram

APPLICATION CIRCUITS

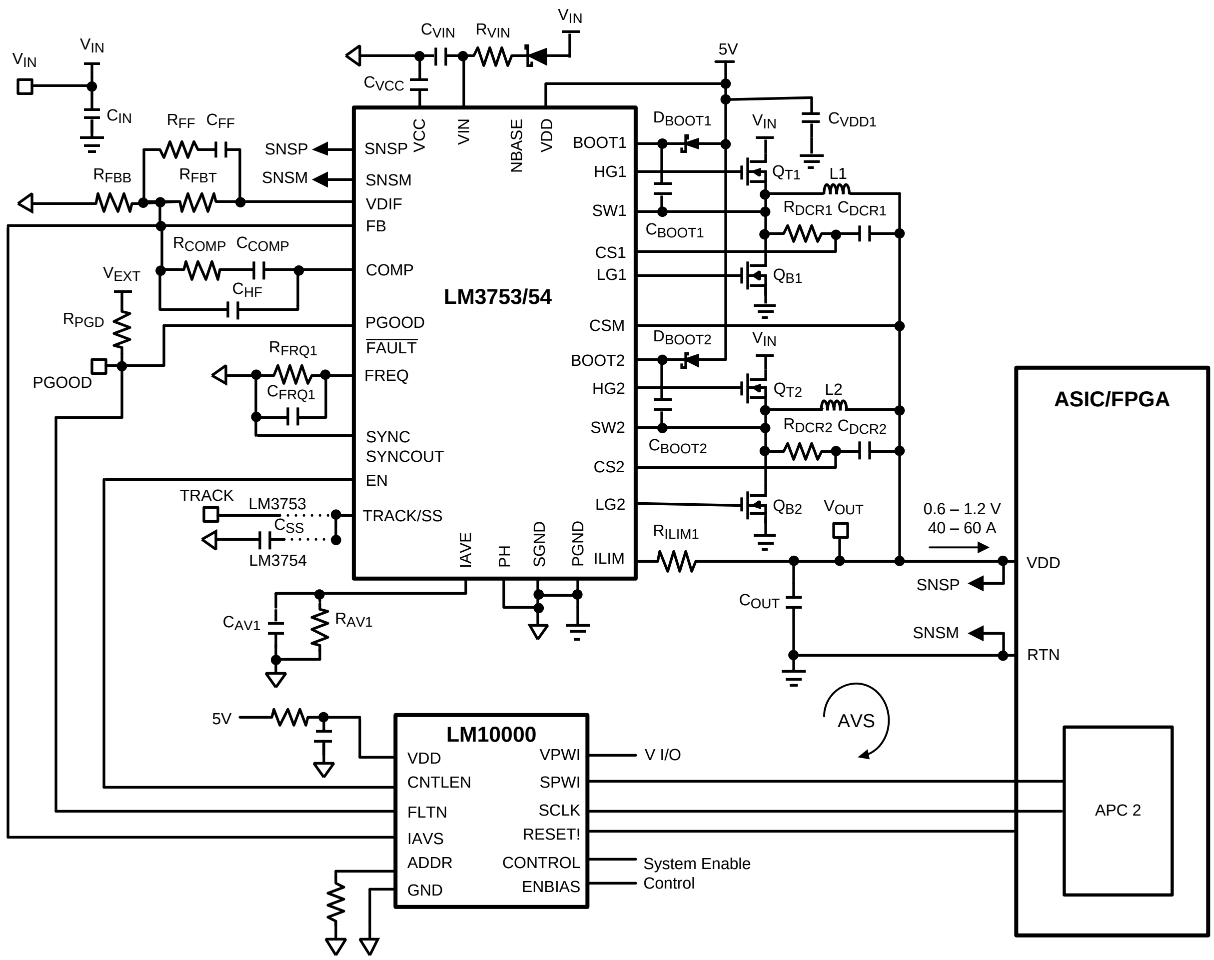


Figure 11. 60A AVS solution using LM10000 paired with LM3573/4 2-Phase Controller

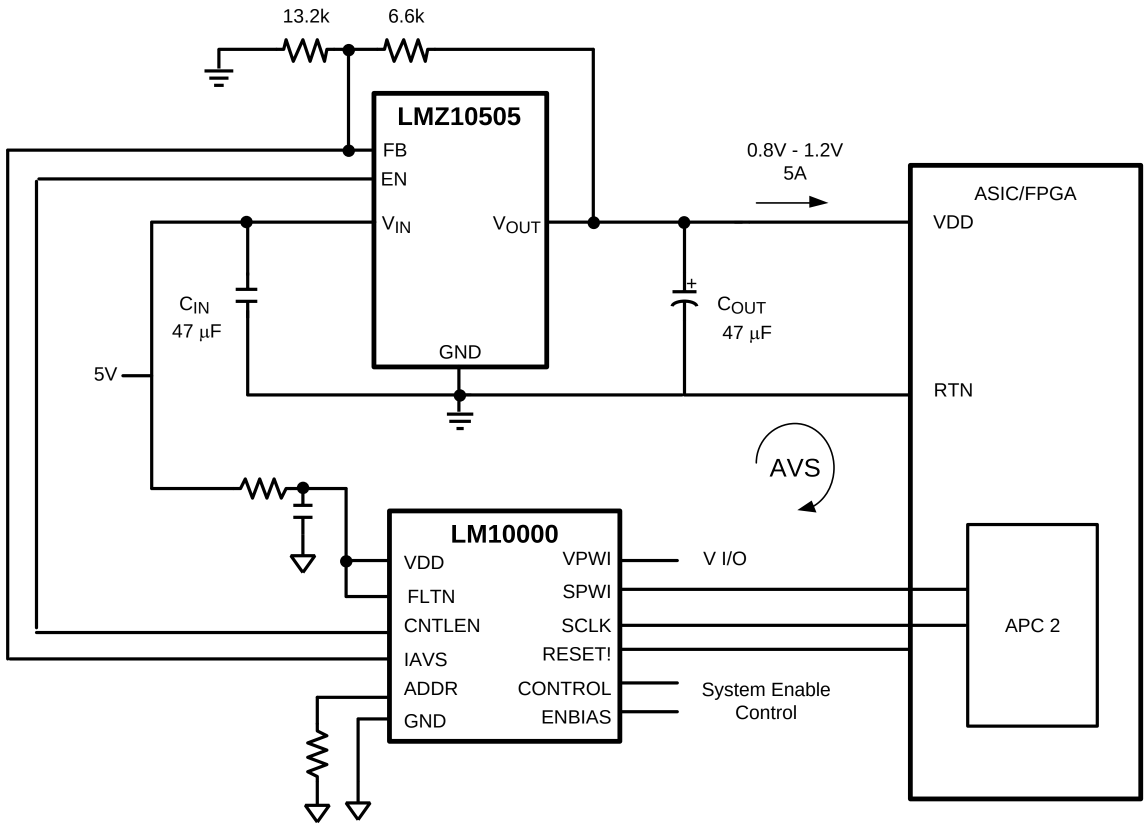


Figure 12. 5A AVS solution LM10000 paired with LMZ10505 Simple Switcher Module

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10000SD/NOPB	ACTIVE	WSON	NHK	14	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	10000SD	Samples
LM10000SDE/NOPB	ACTIVE	WSON	NHK	14	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	10000SD	Samples
LM10000SDX/NOPB	ACTIVE	WSON	NHK	14	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	10000SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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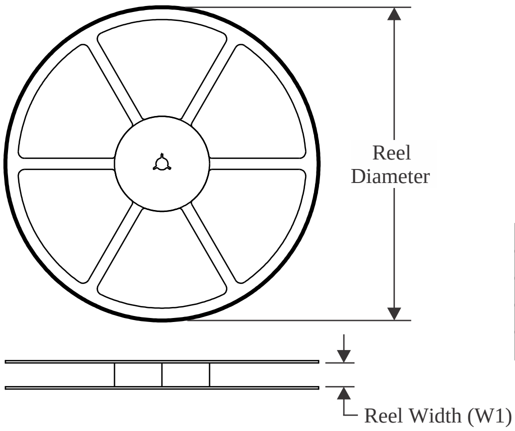
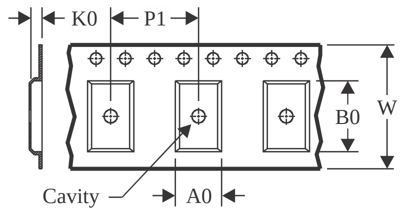
TAPE AND REEL INFORMATION

REEL DIMENSIONS

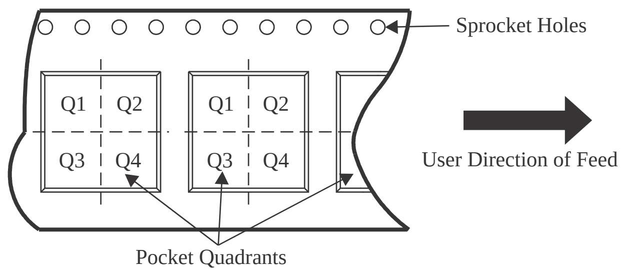


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

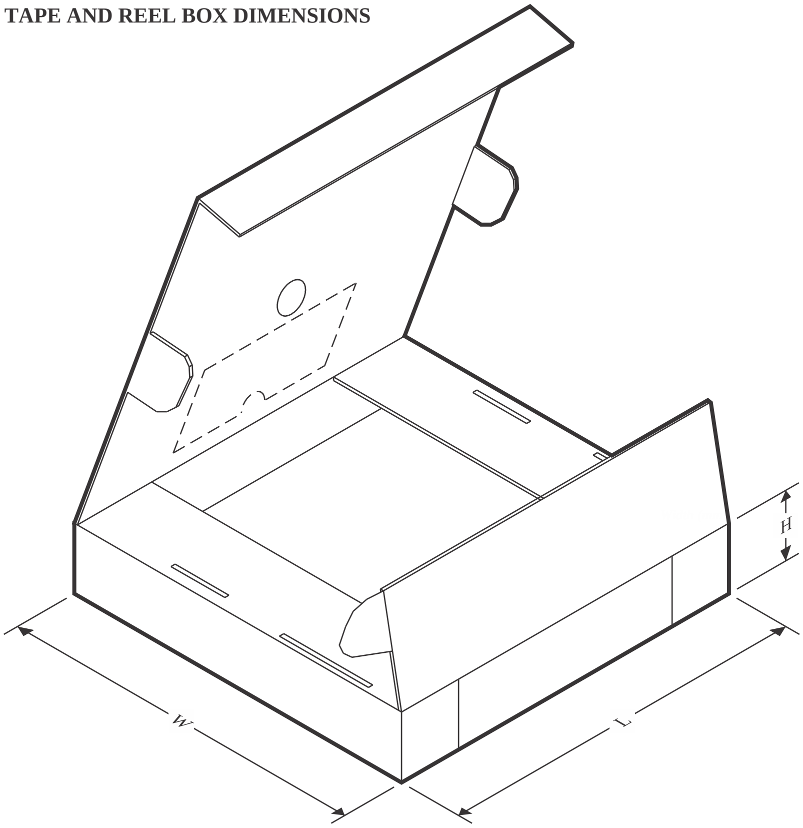
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10000SD/NOPB	WSON	NHK	14	1000	178.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1
LM10000SDE/NOPB	WSON	NHK	14	250	178.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1
LM10000SDX/NOPB	WSON	NHK	14	4500	330.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1

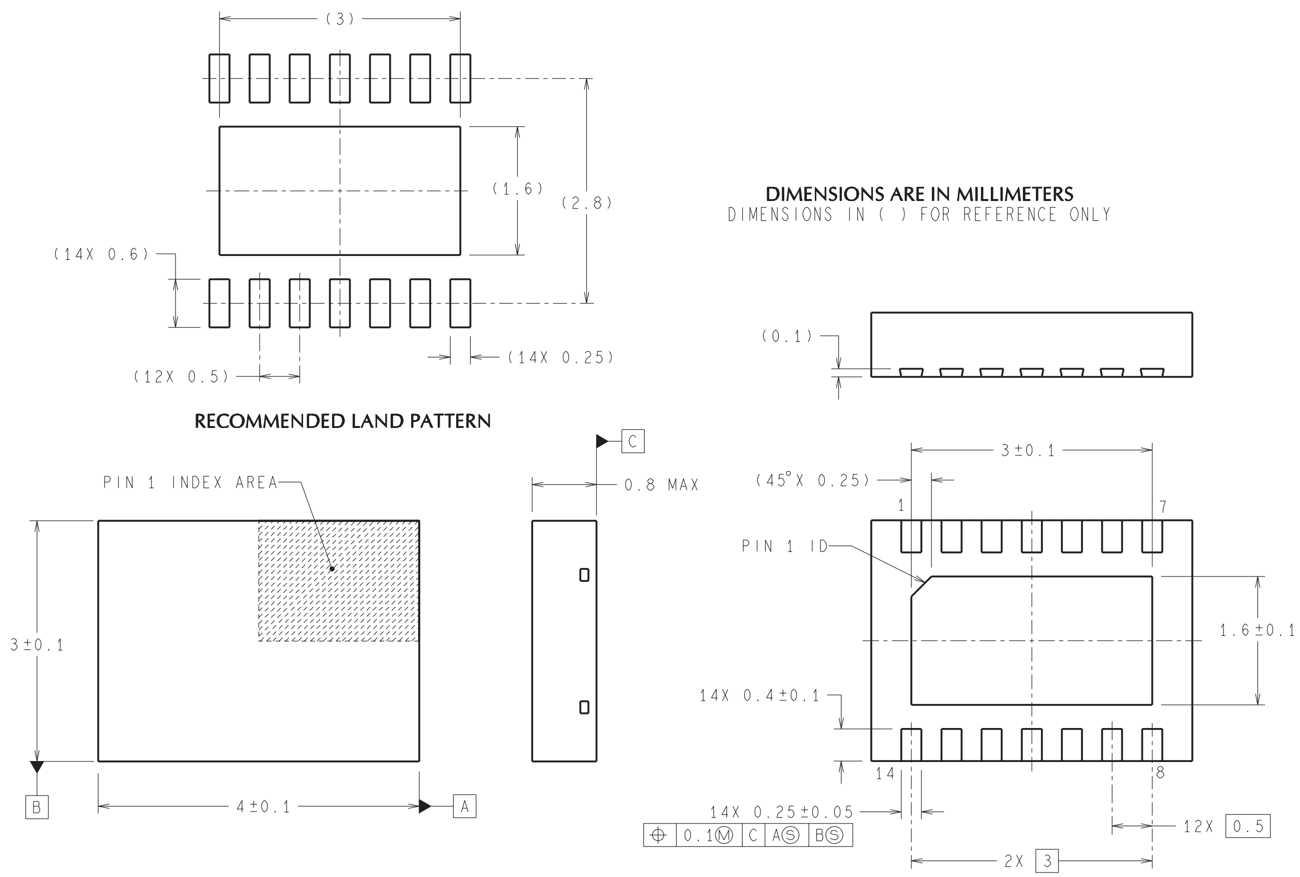
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10000SD/NOPB	WSON	NHK	14	1000	210.0	185.0	35.0
LM10000SDE/NOPB	WSON	NHK	14	250	210.0	185.0	35.0
LM10000SDX/NOPB	WSON	NHK	14	4500	367.0	367.0	35.0

NHK0014A



SDA14A (Rev A)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265