LM48557 Boomer™ Mono, Bridge-Tied Load, Ceramic Speaker Driver with I²C Volume Control and Reset

Check for Samples: LM48557

FEATURES

- **Integrated Charge Pump**
- **Bridge-Tied Load Output**
- **Differential Input**
- **High PSRR**
- **I²C Volume and Mode Control**
- **Reset Input**
- **Advanced Click-and-Pop Suppression**
- **Low Supply Current**
- **Minimum External Components**
- **Micro-Power Shutdown**
- **Available in Space-Saving 16-Bump DSBGA Package**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Notebook Electronic Devices**
- **MP3 Players**

KEY APPLICATIONS

- **Output Voltage at V_{DD} = 4.2V**
  - **R_L = 1µF +22Ω, THD+N ≤ 1%: 5.8 V_{RMS} (Typ)**

DESCRIPTION

The LM48557 is a single supply, mono, ceramic speaker driver with an integrated charge-pump, designed for portable devices, such as cell phones and portable media players, where board space is at a premium. The LM48557 charge pump allows the device to deliver 5.8V_{RMS} from a single 4.2V supply.

The LM48557 features high power supply rejection ratio (PSRR), 80dB at 217Hz, allowing the device to operate in noisy environments without additional power supply conditioning. Flexible power supply requirements allow operation from 2.7V to 4.5V. The LM48557 features an active low reset input that reverts the device to its default state. Additionally, the LM48557 features a 36-step I²C volume control and mute function. The low power Shutdown mode reduces supply current consumption to 0.01µA.

The LM48557's superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48557 is available in an ultra-small 16-bump DSBGA package (1.965mm x 1.965mm).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Boomer is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Application

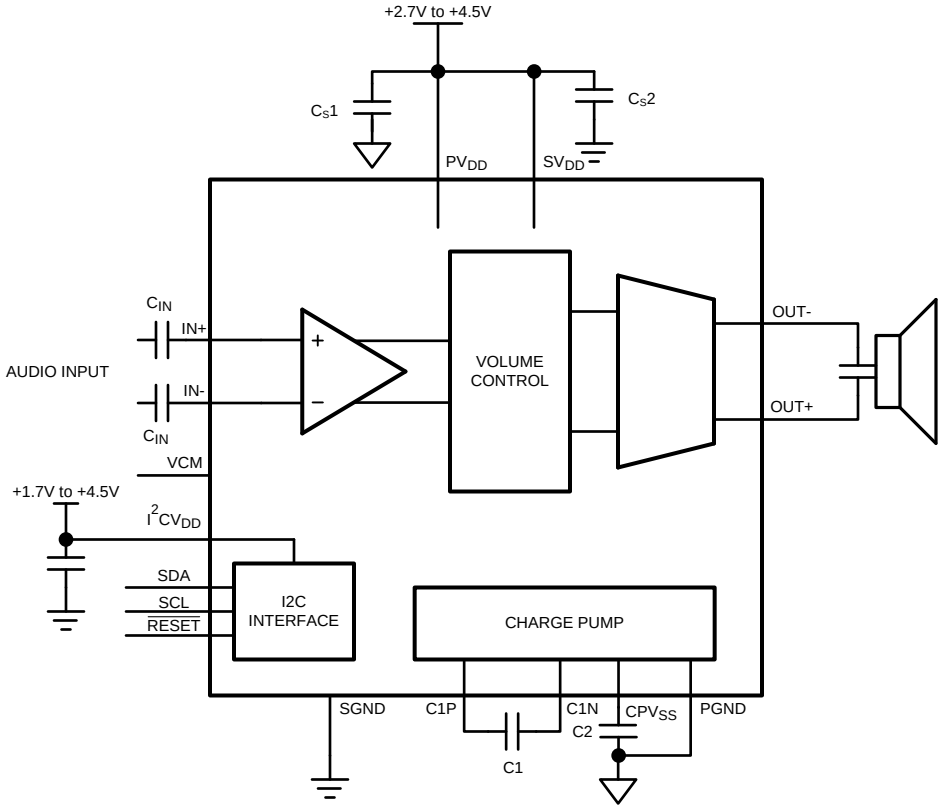


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

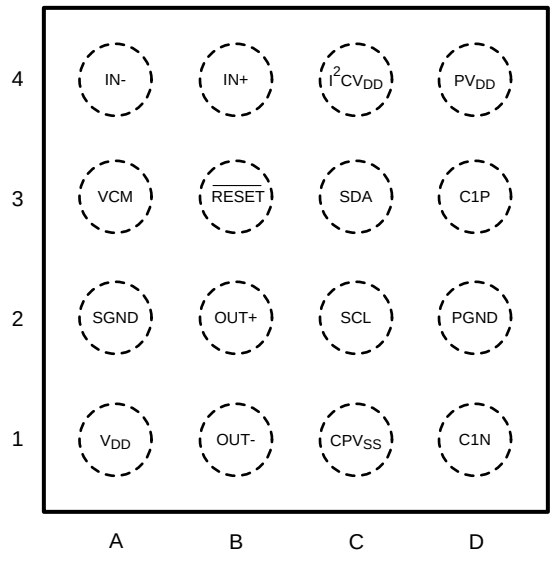


Figure 2. YZR Package - Top View
See Package Number YZR001611A

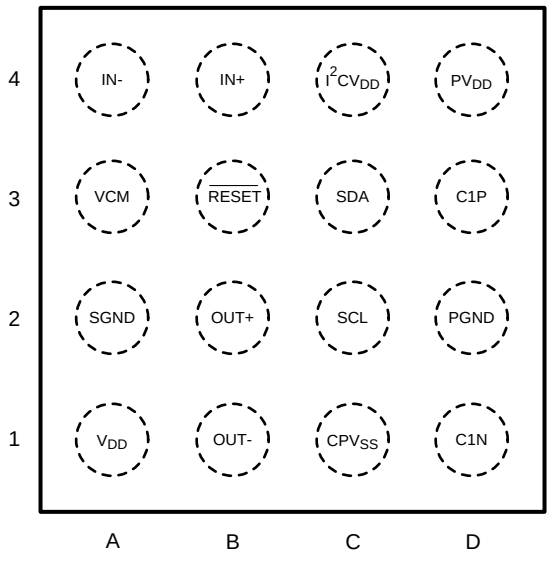


Figure 3. YPD Package - Top View
See Package Number YPD001611A

Copyright © 2009–2013, Texas Instruments Incorporated

Table 1. Bump Descriptions

Bump	Name	Description
A1	SV_{DD}	Signal Power Supply
A2	SGND	Signal Ground
A3	VCM	Common Mode Sense Input
A4	IN-	Amplifier Inverting input
B1	OUT-	Amplifier Inverting output
B2	OUT+	Amplifier Non-Inverting Output
B3	$\overline{\text{RESET}}$	Active Low Reset Input. Connect to V_{DD} for normal operation. Toggle between V_{DD} and GND to reset the device.
B4	IN+	Amplifier Non-Inverting Input
C1	CPV_{SS}	Charge Pump Output
C2	SCL	I^2C Serial Clock Input
C3	SDA	I^2C Serial Data Input
C4	I^2CV_{DD}	I^2C Supply Voltage
D1	C1N	Charge Pump Flying Capacitor Negative Terminal
D2	PGND	Power Ground
D3	C1P	Charge Pump Flying Capacitor Positive Terminal
D4	PV_{DD}	Power Supply

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage(1)		5.25V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation(4)		Internally Limited
ESD Rating-Human Body Model(5)		2kV
ESD Rating-Machine Model(6)		150V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (typ) - (YZR001611A)	63°C/W
Soldering Information: See AN-1112 "Micro SMD Wafer Level Chip Scale Package."		

(1) "Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The Electrical Characteristics tables list specified specifications under the listed Operating Ratings except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.
(5) Human body model, applicable std. JESD22-A114C.
(6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)		$-40°C \le T_A \le +85°C$
Supply Voltage	PV_{DD} and SV_{DD}	$2.7V \le V_{DD} \le 4.5V$
	I^2CV_{DD}	$1.7V \le I^2CV_{DD} \le 4.5V$

Copyright © 2009–2013, Texas Instruments Incorporated

Electrical Characteristics V_{DD} = 4.2V(1)(2)

The following specifications apply for A_V = 6dB, R_L = 1µF + 22Ω, C1 = 2.2µF, C2 = 2.2µF, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48557			Units
			Min(3)	Typ(4)	Max(3)	
V_{DD}	Supply Voltage Range		2.7		4.5	V
I^2CV_{DD}	I^2C Supply Voltage Range		1.7		4.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, R_L = ∞		5	8	mA
I_{SD}	Shutdown Current	Shutdown Enabled		0.01	1	µA
$\|V_{OS}\|$	Differential Output Offset Voltage	V_{IN} = 0V, A_V = 0dB		3	12	mV
		V_{IN} = 0V, A_V = 48dB		40	160	mV
V_{IH}	Logic High Input Threshold	$\overline{RESET}$, V_{DD} = 2.7V to 4.5V	1.4			V
V_{IL}	Logic Low Input Threshold	$\overline{RESET}$, V_{DD} = 2.7V to 4.5V			0.4	V
A_V	Gain	Minimum Gain Setting Volume Control = 000001	-25.5	-25	-24.5	dB
		Maximum Gain Setting Volume Control = 111111	47	48	49	dB
$A_{V(MUTE)}$	Mute Attenuation	Volume Control = 000000		–90		dB
R_{IN}	Input Resistance		1	3		MΩ
V_{IN}	Common Mode Input Voltage Range		-1		1	V_{P-P}
V_O	Output Voltage	R_L = 1µF + 22Ω, THD+N = 1%				
		f = 1kHz	5.5	5.8		V_{RMS}
			15.6	16.4		V_{P-P}
		f = 5kHz		4.0		V_{RMS}
		R_L = 2.2µF + 10Ω, THD+N = 1%				
		f = 1kHz		5.6		V_{RMS}
		f = 5kHz		2.9		V_{RMS}
THD+N	Total Harmonic Distortion + Noise	V_O = 4V_{RMS}, f = 1kHz, A_V = 48dB		0.05		%
PSRR	Power Supply Rejection Ratio (Figure 4)	V_{DD} = 4.2V + 200mV_{P-P} (sine), Inputs AC GND, C_{IN} = 0.1µF, A_V = 0dB				
		f_{RIPPLE} = 217Hz		80		dB
		f_{RIPPLE} = 1kHz		80		dB
		V_{DD} = 4.2V + 200mV_{P-P} (sine), Inputs AC GND, C_{IN} = 0.1µF, A_V = 48dB				
		f = 1kHz	15	40		dB
		f = 5kHZ		40		dB
CMRR	Common Mode Rejection Ratio (Figure 5)	V_{CM} = 200mV_{P-P} (sine), C_{IN} = 0.1µF, A_V = 48dB				
		f_{RIPPLE} = 500Hz	16	36		dB
		f_{RIPPLE} = 1kHz		37		dB
f_{SW}	Charge Pump Switching Frequency		230	300	370	kHz
SNR	Signal To Noise Ratio	V_{OUT} = 5V_{RMS}, f = 1kHz, A_V = 48dB		74		dB
$\in_{OS}$	Output Noise	A_V = 0dB, A-Weighted Filter		20	30	µV
		A_V = 48dB, A-weighted Filter		1		mV

(1) "Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The Electrical Characteristics tables list specified specifications under the listed Operating Ratings except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Datasheet min/max specification limits are specified by test or statistical analysis.

(4) Typical values represent most likely parametric norms at T_A = +25ºC, and at theOperation Rating at the time of product characterization and are not ensured.

Copyright © 2009–2013, Texas Instruments Incorporated

Electrical Characteristics V_{DD} = 4.2V[1][2] (continued)

The following specifications apply for A_V = 6dB, R_L = 1µF + 22Ω, C1 = 2.2µF, C2 = 2.2µF, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48557			Units
			Min[3]	Typ[4]	Max[3]	
T_{WU}	Wake Up Time	From shutdown		5		ms

Copyright © 2009–2013, Texas Instruments Incorporated

I^2C Interface Characteristics 1.7V ≤ I^2CV_{DD} ≤ 4.5V(1)(2)

The following specifications apply for R_{PU} = 1kΩ to I^2CV_{DD}, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48557			Units
			Min(3)	Typ(4)	Max(3)	
V_{IH}	Logic Input High Threshold	SDA, SCL	0.7 x I^2CV_{DD}			V
V_{IL}	Logic Input Low Threshold	SDA, SCL			0.3 x I^2CV_{DD}	V
V_{OL}	Logic Output Low Threshold	SDA, I_{SDA} = 3.6mA			0.35	V
I_{OH}	Logic Output High Current	SDA, SCL, I^2CV_{DD} = 4.5V			2	µA
	SCL Frequency				400	kHz
6	SDA Setup Time		100			ns
5	SDA Stable Time		0	250	900	ns
1	Start Condition Time		100			ns
7	Stop Condition Time		100			ns

(1) "Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The Electrical Characteristics tables list specified specifications under the listed Operating Ratings except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(3) Datasheet min/max specification limits are specified by test or statistical analysis.
(4) Typical values represent most likely parametric norms at T_A = +25ºC, and at theOperation Rating at the time of product characterization and are not ensured.

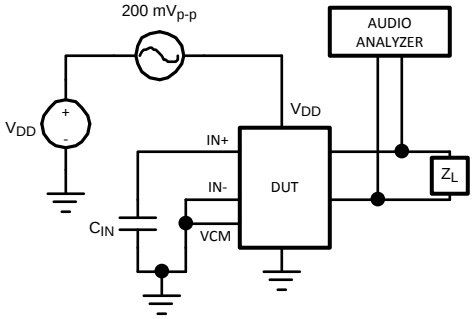


Figure 4. PSRR Test Circuit

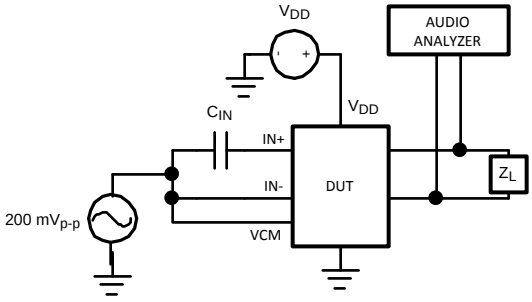


Figure 5. CMRR Test Circuit

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 3.6V, Z_L = 1µF + 22Ω
A_V = 48dB, V_O = 2.5V

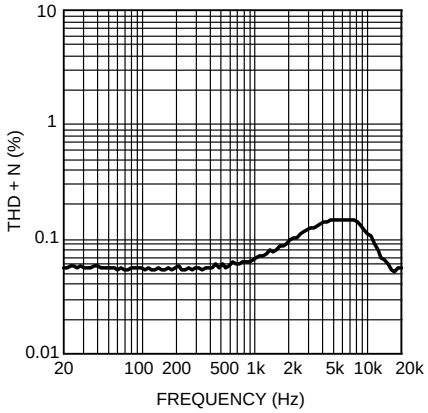


Figure 6.

THD+N vs Frequency
V_{DD} = 4.2V, Z_L = 1µF + 22Ω
A_V = 48dB

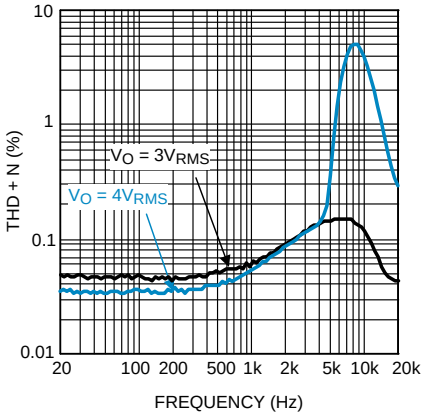


Figure 7.

THD+N vs Output Voltage
Z_L = 1µF + 22Ω, A_V = 0dB

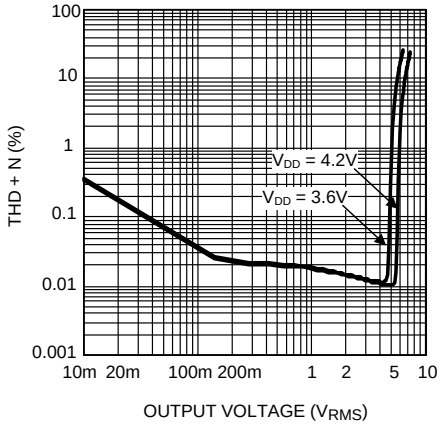


Figure 8.

Output Voltage vs Frequency
V_{DD} = 4.2V, Z_L = 1µF + 22Ω
THD+N = 1%

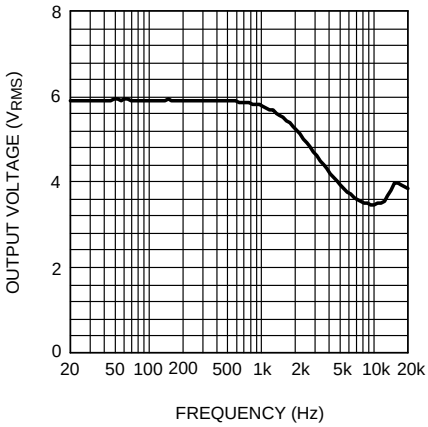


Figure 9.

Power Consumption vs Output Voltage
V_{DD} = 3.6V, Z_L = 1µF + 22Ω

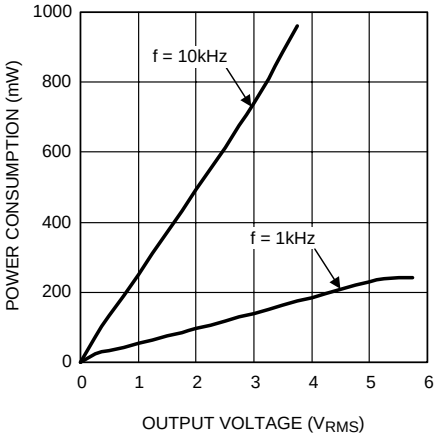


Figure 10.

Power Consumption vs Output Voltage
V_{DD} = 4.2V, Z_L = 1µF + 22Ω

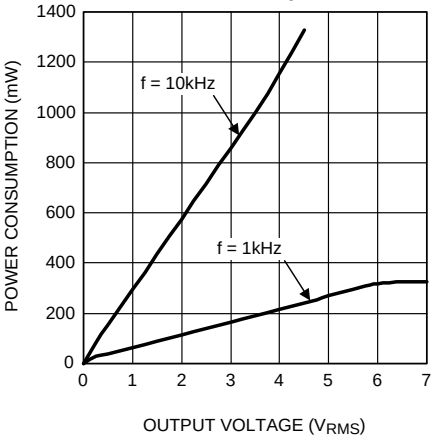


Figure 11.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

CMRR vs Frequency
V_{DD} = 4.2V, V_{RIPPLE} = 200mV_{P-P}, A_V = 48dB

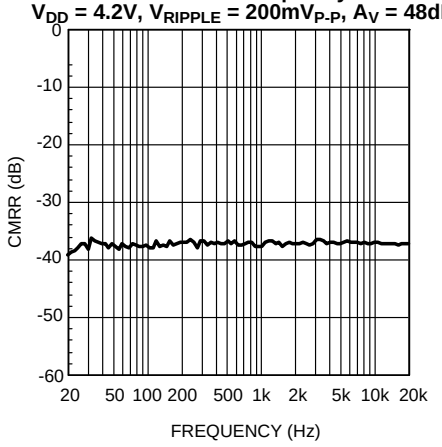


Figure 12.

PSRR vs Frequency
V_{DD} = 4.2V, V_{RIPPLE} = 200mV_{P-P}

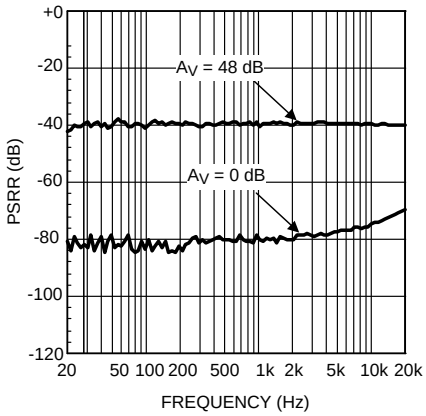


Figure 13.

Output Voltage vs Supply Voltage
Z_L = 1µF + 22Ω, THD+N = 1%

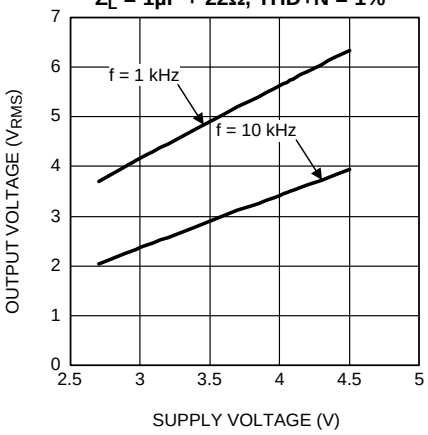


Figure 14.

Supply Current vs Supply Voltage
No Load

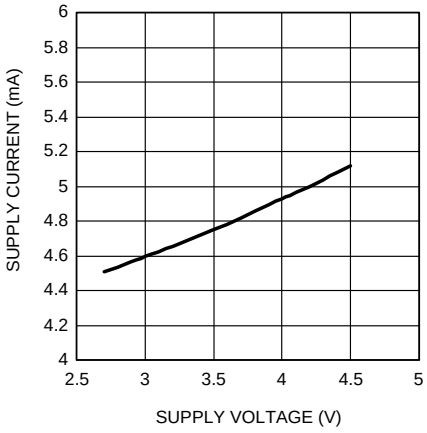


Figure 15.

Charge Pump Output Voltage vs Load Current
V_{DD} = 4.2V

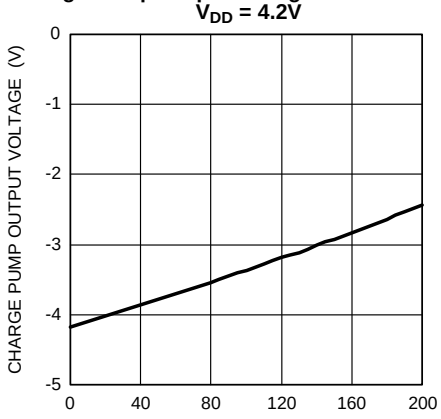


Figure 16.

Copyright © 2009–2013, Texas Instruments Incorporated

APPLICATION INFORMATION

I²C COMPATIBLE INTERFACE

The LM48557 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48557 and the master can communicate at clock rates up to 400kHz. Figure 17 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48557 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 18). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 19). The LM48557 device address is 11011110.

I²C BUS FORMAT

The I²C bus format is shown in Figure 19. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/W bit. Set R/$\overline{W}$ = 0; the LM48557 is a WRITE-ONLY device and will not respond to R/$\overline{W}$ = 1. In other words, the LM48557 will not issue an ACK when R/$\overline{W}$ = 1. Each address bit is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the LM48557. If the LM48557 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. The LM48557 has two registers, Mode Control and Volume Control. The register address and register data are combined into a single byte, the most significant bit (MSB) indicates which register is being addressed. To address the Mode Control register, set the MSB of the data byte to 0, followed by seven bits of register data. To address the Volume Control register, set the MSB of the data byte to 1, followed by seven bits of register data. After the 8-bit register data word is sent, the LM48557 sends another ACK bit. The LM48557 supports single and multi-byte write operations, any number of data bytes can be transmitted to the device between START and STOP conditions. Following the acknowledgement of the last register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

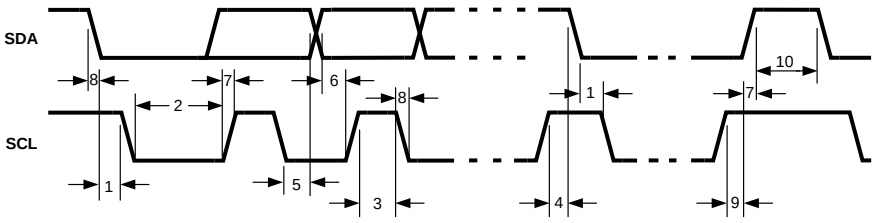


Figure 17. I²C Timing Diagram

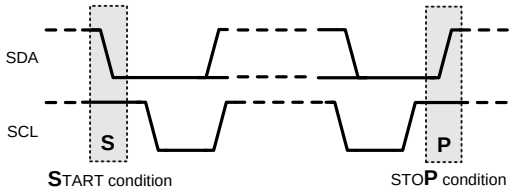


Figure 18. Start and Stop Diagram

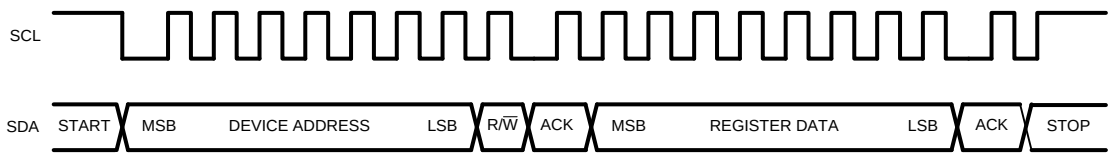


Figure 19. Example Write Sequence

Table 2. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 R/$\overline{W}$
Device Address	1	1	0	1	1	1	1	0

Table 3. Control Registers

Register Name	B7	B6	B5	B4	B3	B2	B1	B0
Mode Control	0	0	0	0	0	0	MUTE	$\overline{SHDN}$
Volume Control	1	0	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

Table 4. Mode Control Registers

BIT	NAME	VALUE	DESCRIPTION	DEFAULT SETTING
B0	$\overline{SHDN}$	0	Shutdown mode	0
		1	Normal operation	
B1	MUTE	0	Normal operation	0
		1	Device mute, A_V = -90dB.	
B2	RESERVED(1)	X	Unused, Set to 0	0
B3	RESERVED(1)	X	Unused, Set to 0	0
B4	TESTMODE	0	Set B4 to 0. B4 = 1 enables TESTMODE. See TEST MODE.	0
B5	RESERVED(1)	X	Unused, Set to 0	0
B6	RESERVED(1)	X	Unused, Set to 0	0
B7	REGISTER ADDRESS	0	Set to 0 to access Mode Control register	0

(1) RESERVED bits are Don't Cares and are ignored by the device. The state of the RESERVED bits does not affect device operation.

Table 5. Volume Control Registers

BIT	NAME	VALUE	DESCRIPTION	DEFAULT SETTING
B0:B5	VOL0:VOL5	See Table 6	Controls amplifier gain/attenuation	0
B6	RESERVED(1)	X	Unused, Set to 0	0
B7	REGISTER ADDRESS	1	Set to 1 to access Volume Control register	1

(1) RESERVED bits are Don't Cares and are ignored by the device. The state of the RESERVED bits does not affect device operation.

SINGLE AND MULTI-BYTE WRITE OPERATION

The LM48557 supports both single-byte and multi-byte write operations. A single-byte write operation begins with the master device transmitting a START condition followed by the device address (Figure 20). After receiving the correct device address, the LM48557 generates an ACK bit. The master device transmits the register data byte, after which the LM48557 generates and ACK bit. Following the ACK, the master issues a STOP condition, completing the singly-byte data transfer.

Copyright © 2009–2013, Texas Instruments Incorporated

A multi-byte write operation is similar to a single-byte operation, the master device issues a START condition and device address, and the LM48557 responds with an ACK (Figure 21). The master device then transmits the first data byte. Following the LM48557's ACK, the master device does not issue a STOP condition, transmitting a second data byte instead. The LM48557 responds with an ACK bit. The master device can continue to issue data bytes, and the LM48557 will respond with an ACK, until a STOP condition is issued. Once a STOP condition is issued, the LM48557 ignores the I^2C bus until the master issues the LM48557's device address.

Figure 20. Single-Byte Write Example

Figure 21. Multi-Byte Write Example

GENERAL AMPLIFIER FUNCTION

The LM48557 is a fully differential ceramic speaker driver that utilizes Ti's inverting charge pump technology to deliver over $5.8V_{RMS}$ to a 1µF ceramic speaker while operating from a single 4.2V supply. The low noise, inverting charge pump generates a negative supply voltage (CPV_{SS}) from the positive supply voltage (PV_{DD}). The LM48557 takes advantage of the increased head room created by the charge pump and the bridge-tied load (BTL) architecture, delivering significantly more voltage than a single-ended, single-supply amplifier to the speaker.

Table 6. Volume Control Table

VOLUME STEP	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	GAIN (dB)
1 (MUTE)	0	0	0	0	0	0	-90
2	0	0	0	0	0	1	-25
3	0	0	0	0	1	0	-22
4	0	0	0	0	1	1	-19
5	0	0	0	1	0	0	-16
6	0	0	0	1	0	1	-13
7	0	0	0	1	1	0	-10
8	0	0	0	1	1	1	-8
9	0	0	1	0	0	0	-6
10	0	0	1	0	0	1	-4
11	0	0	1	0	1	0	-2
12	0	0	1	0	1	1	0
13	0	0	1	1	0	0	2
14	0	0	1	1	0	1	4
15	0	0	1	1	1	0	6
16	0	0	1	1	1	1	8
17	0	1	0	0	0	0	10
18	0	1	0	0	0	1	12
19	0	1	0	0	1	0	14
20	0	1	0	0	1	1	16
21	0	1	0	1	0	0	18
22	0	1	0	1	0	1	20
23	0	1	0	1	1	0	22
24	0	1	0	1	1	1	24

Copyright © 2009–2013, Texas Instruments Incorporated

Table 6. Volume Control Table (continued)

VOLUME STEP	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	GAIN (dB)
25	0	1	1	0	0	0	26
26	0	1	1	0	0	1	28
27	0	1	1	0	1	0	30
28	0	1	1	0	1	1	32
29	0	1	1	1	0	0	34
30	0	1	1	1	0	1	36
31	0	1	1	1	1	0	38
32	0	1	1	1	1	1	40
Do Not Use Volume Steps 33-60 See Table 7							
61	1	1	1	1	0	0	42
62	1	1	1	1	0	1	44
63	1	1	1	1	1	0	46
64	1	1	1	1	1	1	48

Table 7. Unused Volume Steps

VOLUME STEP	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	GAIN (dB)
33	1	0	0	0	0	0	-90
34	1	0	0	0	0	1	-25
35	1	0	0	0	1	0	-22
36	1	0	0	0	1	1	-19
37	1	0	0	1	0	0	-16
38	1	0	0	1	0	1	-13
39	1	0	0	1	1	0	-10
40	1	0	0	1	1	1	-8
41	1	0	1	0	0	0	-6
42	1	0	1	0	0	1	-4
43	1	0	1	0	1	0	0
44	1	0	1	0	1	1	4
45	1	0	1	1	0	0	8
46	1	0	1	1	0	1	12
47	1	0	1	1	1	0	14
48	1	0	1	1	1	1	16
49	1	1	0	0	0	0	18
50	1	1	0	0	0	1	20
51	1	1	0	0	1	0	22
52	1	1	0	0	1	1	24
53	1	1	0	1	0	0	26
54	1	1	0	1	0	1	28
55	1	1	0	1	1	0	30
56	1	1	0	1	1	1	32
57	1	1	1	0	0	0	34
58	1	1	1	0	0	1	36
59	1	1	1	0	1	0	38
60	1	1	1	0	1	1	40

Copyright © 2009–2013, Texas Instruments Incorporated

VOLUME CONTROL

The LM48557 has a 64 step volume control, but only 36 steps are recommended for use. Use steps 1 through 32 and steps 61 through 64 to set the gain of the device. Accessing steps 33 through 60 results in the repeated gain conditions shown in Table 7. Steps 33 through 60 are not tested and should not be used.

SHUTDOWN FUNCTION

The LM48557 features a low-power shutdown mode that disables the device lowers the quiescent current to 0.01µA. Set bit B0 ($\overline{SHDN}$) of the Mode Control register to 0 to disable the amplifier and charge pump. Set $\overline{SHDN}$ to 1 for normal operation. Shutdown mode does not clear the I^2C register. When re-enabled, the device returns to its previous volume setting. To clear the I^2C register, either remove power from the device, or toggle $\overline{RESET}$ (see $\overline{RESET}$ section).

$\overline{RESET}$

The LM48557 features an active low reset input. Driving $\overline{RESET}$ low clears the I^2C register. Volume control is set to 000000 (-90dB) and $\overline{SHDN}$ is set to 0, disabling the device. While $\overline{RESET}$ is low, the LM48557 ignores any I^2C data. After the device is reset, and $\overline{RESET}$ is driven high, the LM48557 remains in shutdown mode with the volume set to -90dB. Re-enable the device by writing to the I^2C register.

MUTE

The LM48557 features a mute mode. Set bit B1 (MUTE) of the Mode Control register to 1 to mute the device. In mute mode, the gain is set to -90dB, equivalent to the volume step 1. Set MUTE = 0 to unmute the device. Once unmuted, the device returns to its previous volume step.

TEST MODE

If enabled, TESTMODE does not affect device performance under normal operating conditions. Operating above the recommended supply voltage range with TESTMODE enabled can result in damage to the device.

PROPER SELECTION OF EXTERNAL COMPONENTS

Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1µF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and C2 dominate the output impedance. A lower value capacitor can be used in systems where low maximum output power requirements.

Charge Pump Hold Capacitor (C2)

The value and ESR of the hold capacitor (C2) directly affects the ripple on CPV_{SS}. Increasing the value of C2 reduces output ripple. Decreasing the ESR of C2 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems where low maximum output power requirements.

Copyright © 2009–2013, Texas Instruments Incorporated

Input Capacitor Selection

Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48557. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using the equation below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (Hz) \tag{1}$$

Where the value of R_{IN} is given in the Electrical Characteristics Table.

High pass filtering the audio signal helps protect the speakers. When the LM48557 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

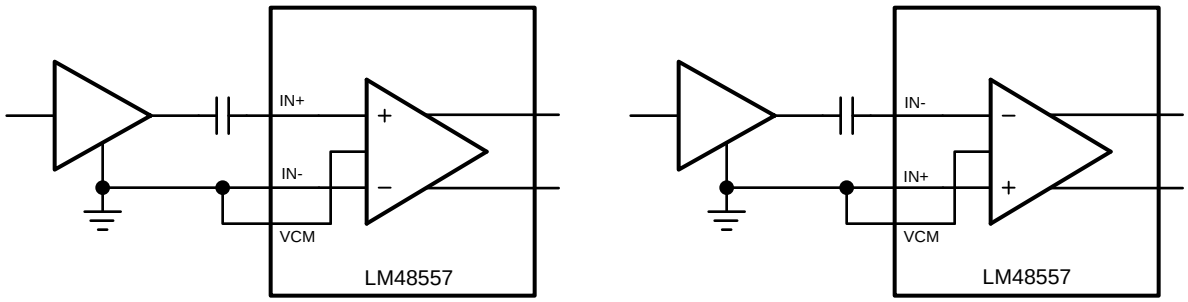
COMMON MODE SENSE

The LM48557 features a common mode sense pin (VCM, pin A3) that includes additional common mode cancelling circuitry that improves the CMRR. When the volume control is set at a high gain step such as 48dB, any mismatch in the input capacitors would degrade CMRR performance significantly. With the VCM pin connected to the ground of the input source, it takes the input capacitor mismatches out of the equation and therefore improves the CMRR. Another advantage with this feature is that only one input capacitor is needed in the single-ended configuration as opposed to two well matched capacitors. See next section for details of different configurations of the LM48857.

SINGLE-ENDED INPUT CONFIGURATION

Ground-Referenced Audio Source

The LM48557 input stage is compatible with ground-referenced input sources, such as CODECs with an integrated headphone amplifier. Connect either input, IN+ or IN- to the CODEC output, and connect the unused input and VCM to the CODEC output ground (Figure 22). An input coupling capacitor in series with the source and device input is recommended to block the CODEC output offset voltage, minimizing click and pop and zipper noise during volume transitions.



Non-Inverting Configuration Inverting Configuration

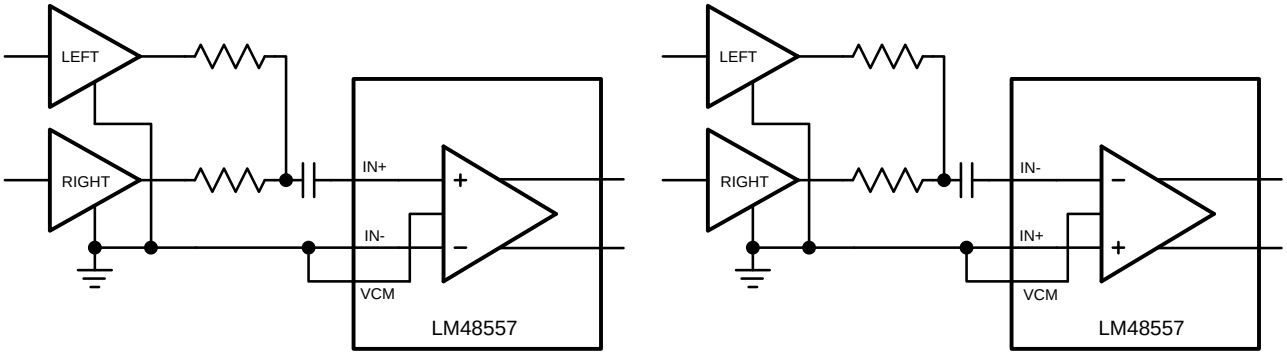
Figure 22. Single-Ended Input Configuration with a Ground-Referenced Source

NON-GROUND REFERENCED AUDIO SOURCE

Stereo-to-Mono Conversion

The LM48557 can convert a single-ended stereo signal to a mono BTL signal (Figure 23). Connect the left and right CODEC outputs in parallel through two equal value resistors to either IN+ or IN-, and connect the unused input and VCM to the CODEC ground. Select the value of the resistors based on the desired frequency response created by the combination of the input resistor and the input coupling capacitor.

Copyright © 2009–2013, Texas Instruments Incorporated



Non-Inverting Configuration Inverting Configuration

Figure 23. Single-Ended Stereo-to-Mono BTL Conversion

PCB Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48557 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

Table 8. LM48557TL Demoboard Bill of Materials

Designator	Quantity	Description
U1	1	LM48557TL Differential, Mono, Ceramic Speaker Driver with I^2C Volume Control, and Reset
C1, C2, C5, C6, C7	5	CAP CERAMIC 2.2µF 10V X5R 10% 0603
C3, C4	2	CAP .1µF 16V CERAMIC X7R 10% 1206
C8	1	CAP TANT LOESR 10µF 16V 10% SMD
J2	1	CONN SOCKET PCB VERT 16POS .1"
JU1, JU2, JU3, JU4, VCM, VDD, GND, I^2CV_{DD}, IN+, IN-, OUT+, OUT-	12	CONN HEADER VERT .100 2POS 30Au
JU5	1	CONN HEADER VERT .100 3POS 30Au
R1, R2	2	RES 5.1K OHM 1/10W 5% 0603 SMD
R3	1	RES 20K OHM 1/10W 5% 0603 SMD
JU1_SH, JU2_SH, JU3_SH, JU5_SH	4	Jumper Shunt w/handle, 30uin gold plated, 0.100" pitch

Copyright © 2009–2013, Texas Instruments Incorporated

PC Board Layout

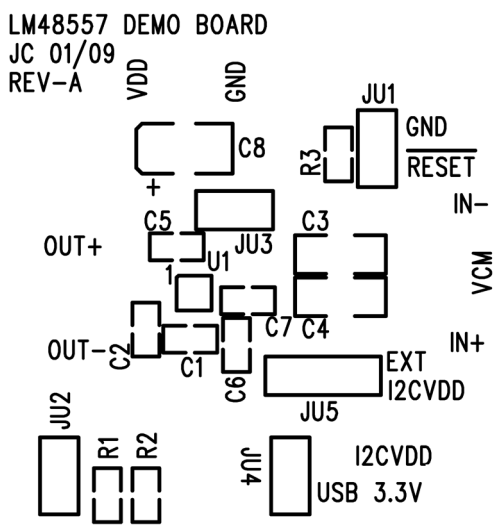


Figure 24. Silk Screen

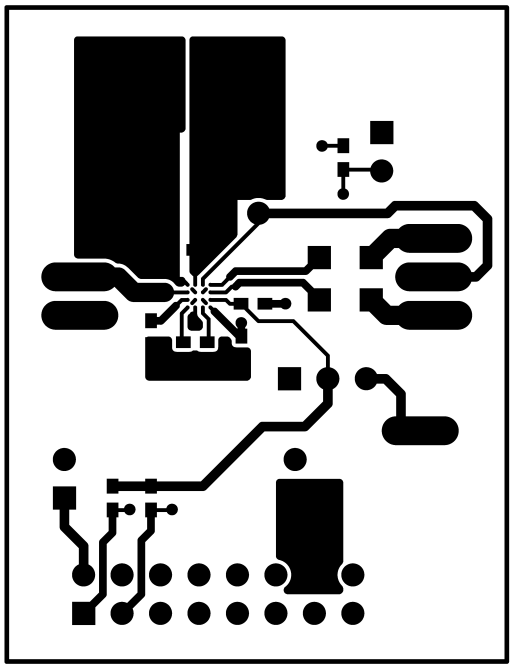


Figure 25. Top Layer

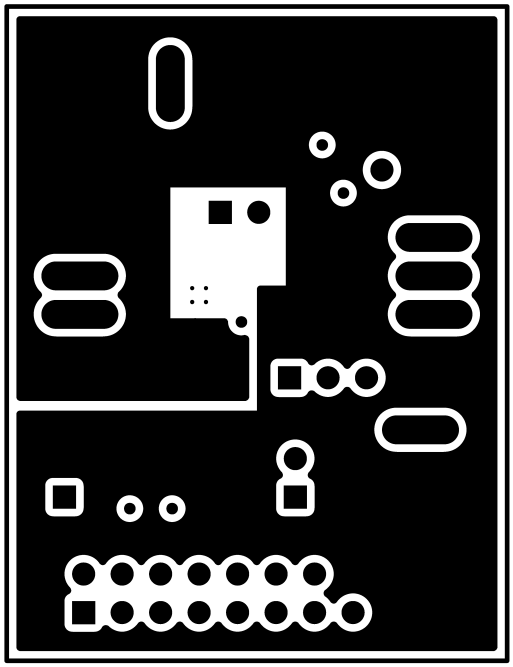


Figure 26. Layer 2

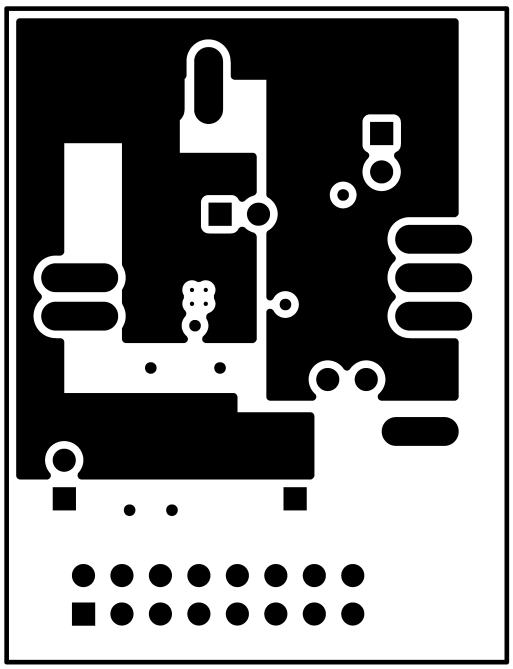


Figure 27. Layer 3

Copyright © 2009–2013, Texas Instruments Incorporated

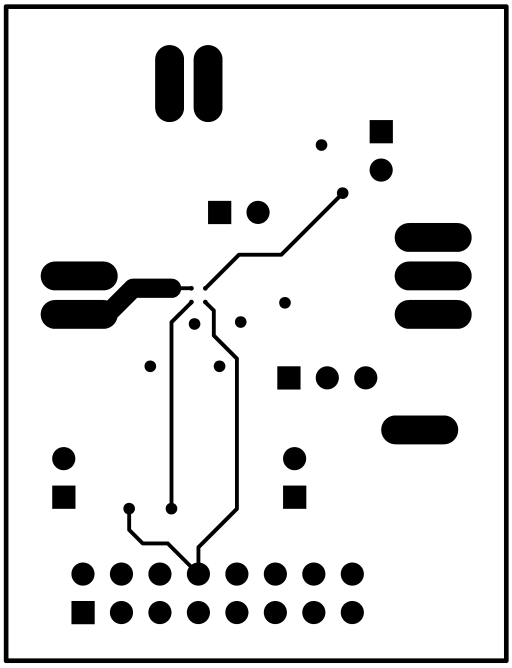


Figure 28. Bottom Layer

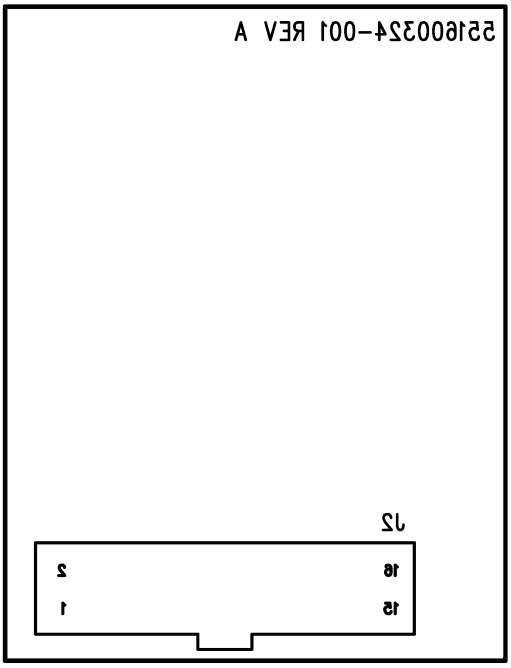


Figure 29. Bottom Silkscreen

Demo Board Schematic

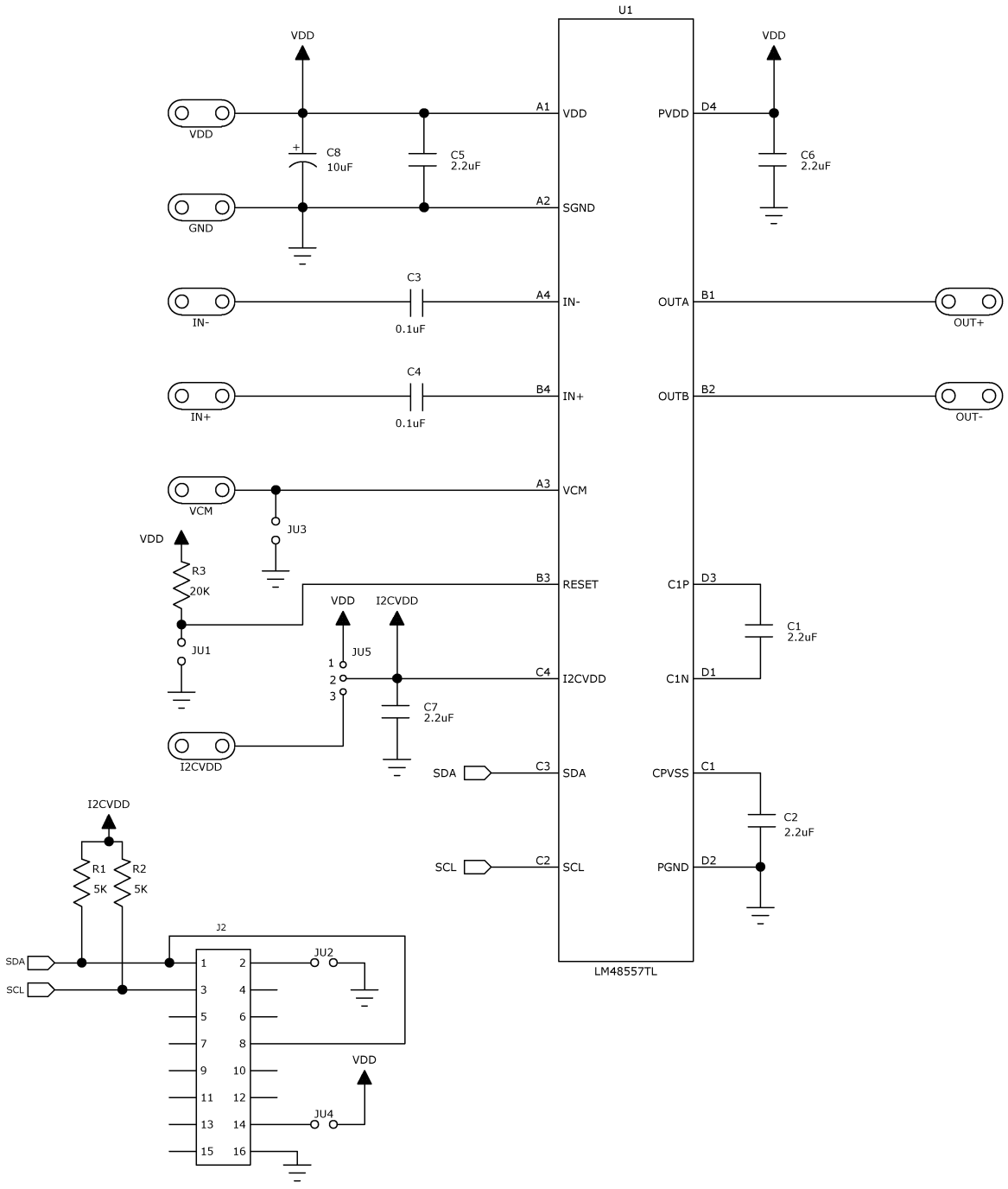


Figure 30. LM48557 Demo Board Schematic

Copyright © 2009–2013, Texas Instruments Incorporated

Revision History

Rev	Date	Description
1.0	07/08/09	Initial released.
1.01	07/15/09	Deleted the “Tru-GND...” trademark on the cover page.
1.02	08/05/09	Text edits.
1.03	08/06/09	Fixed a typo error.
1.04	01/11/10	Added the LM48557UR package drawing, top markings, and the marketing outline.
D	02/05/2013	Changed layout of National Data Sheet to TI format.

Copyright © 2009–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM48557TL/NOPB	ACTIVE	DSBGA	YZR	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		GM2	Samples
LM48557TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		GM2	Samples
LM48557UR/NOPB	ACTIVE	DSBGA	YPD	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		GN5	Samples
LM48557URX/NOPB	ACTIVE	DSBGA	YPD	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		GN5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

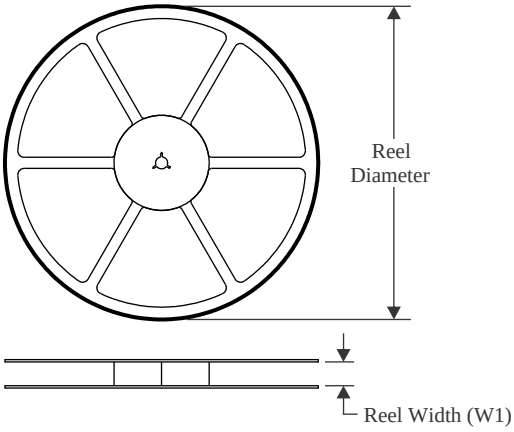
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

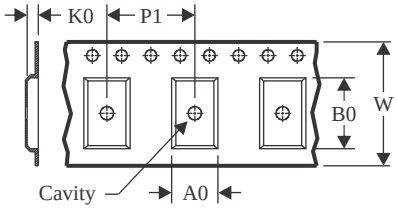
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

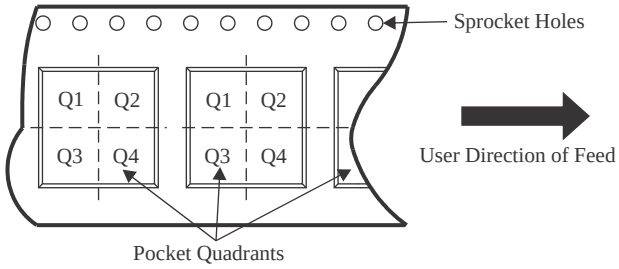


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

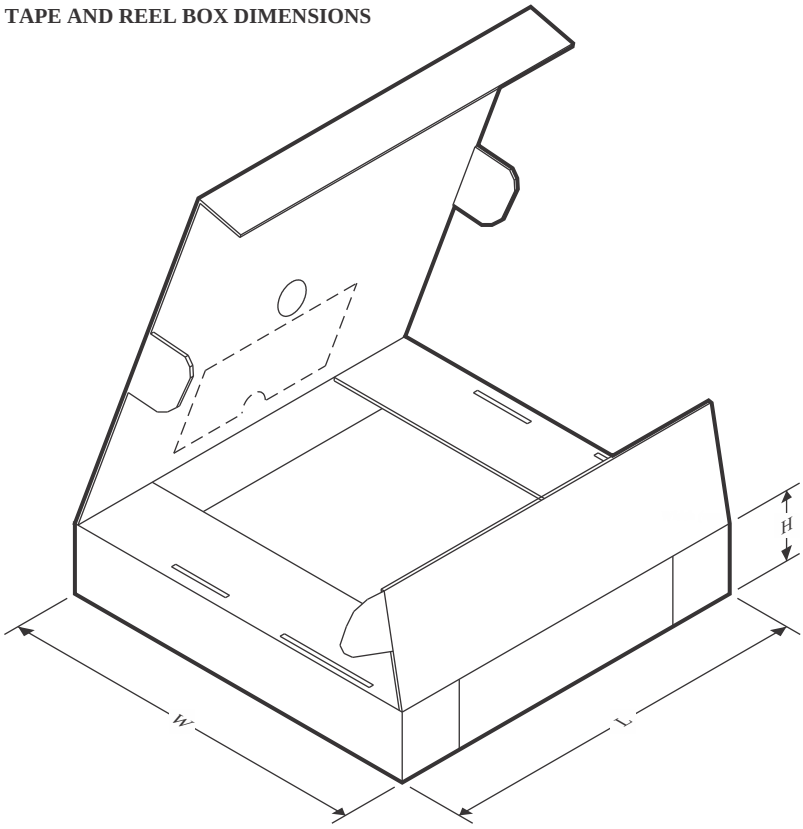
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48557TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM48557TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM48557UR/NOPB	DSBGA	YPD	16	250	178.0	8.4	2.11	2.11	0.56	4.0	8.0	Q1
LM48557URX/NOPB	DSBGA	YPD	16	3000	178.0	8.4	2.11	2.11	0.56	4.0	8.0	Q1

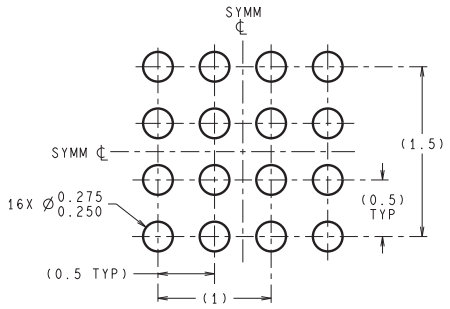
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

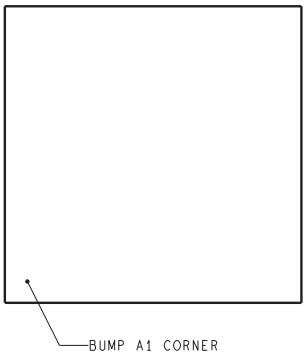
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48557TL/NOPB	DSBGA	YZR	16	250	208.0	191.0	35.0
LM48557TLX/NOPB	DSBGA	YZR	16	3000	208.0	191.0	35.0
LM48557UR/NOPB	DSBGA	YPD	16	250	208.0	191.0	35.0
LM48557URX/NOPB	DSBGA	YPD	16	3000	208.0	191.0	35.0

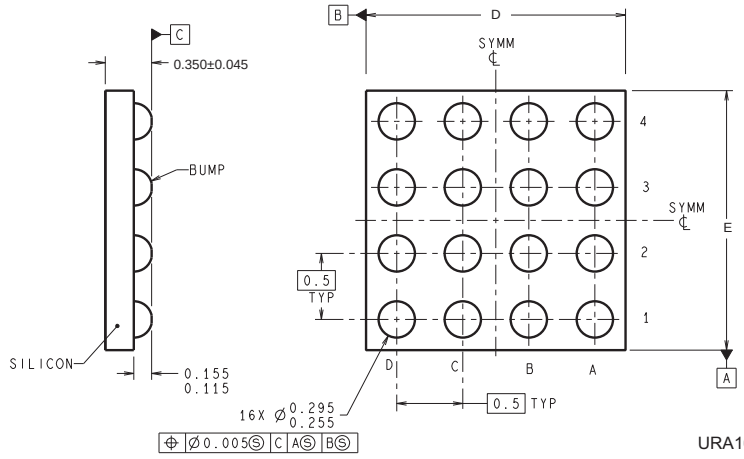
YPD0016



LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





URA16XXX (Rev A)

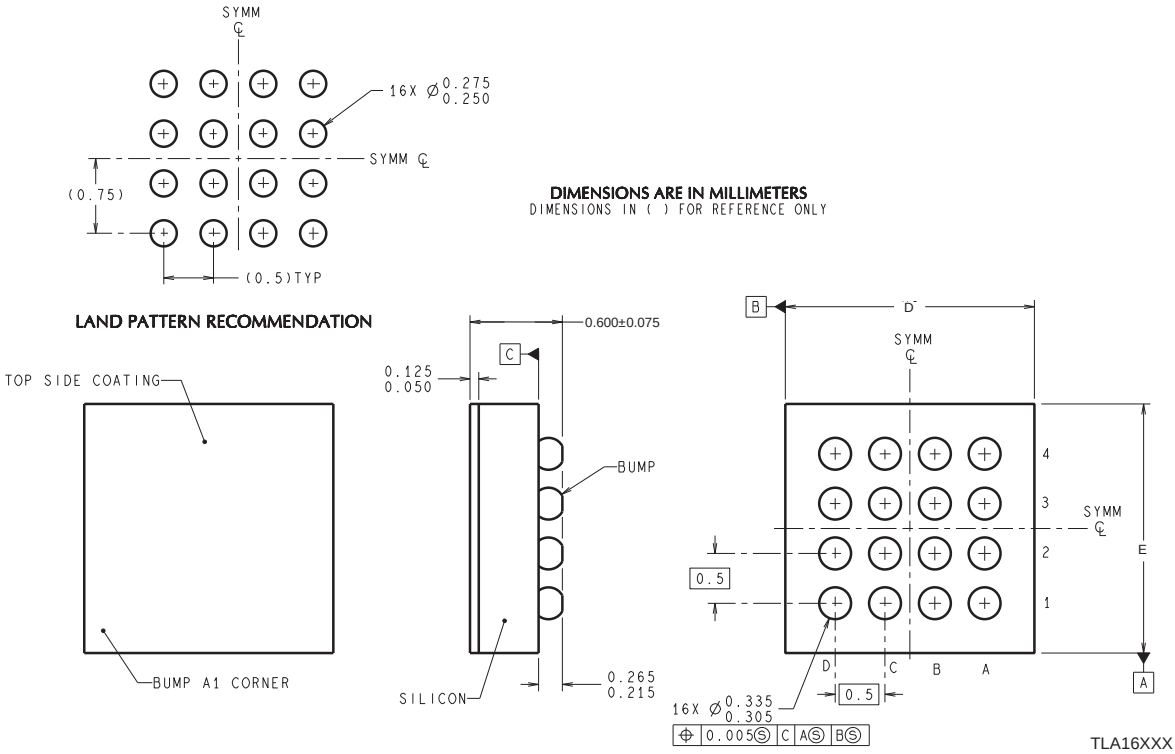
D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.99 mm, Min = 1.93 mm

4215146/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

YZR0016



D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.99 mm, Min = 1.93 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated