

## LM66200 1.6V 至 5V、2.5A 双理想二极管，具有自动切换功能

### 1 特性

- 输入电压范围：1.6V 至 5.5V
- 最大持续电流：2.5A
- 导通电阻：40mΩ (典型值)
- 待机电流：50nA (典型值)
- 静态电流：1.32 μA (典型值)
- 自动二极管切换
- 受控输出压摆率：
  - 电压为 3.3V 时为 1.3ms (典型值)
- VOUT 大于 VINx 时实现反向电流阻断
- 热关断

### 2 应用

- 电表
- 电机驱动器
- 楼宇自动化
- 电子销售终端
- 资产跟踪器

### 3 说明

LM66200 是一款双输入理想二极管器件，具有 1.6V 至 5.5V 的额定电压和每通道 2.5A 的最大额定电流。该器件使用 N 沟道 MOSFET 在电源之间切换，同时在第一次施加电压时提供受控的压摆率。

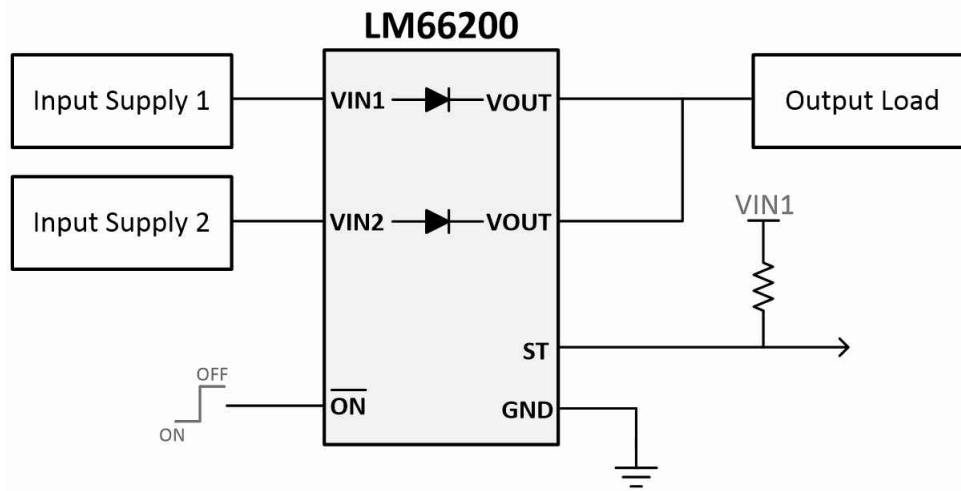
凭借 1.32 μA (典型值) 的低静态电流和 50nA (典型值) 的低待机电流，LM66200 适用于其中一个输入由电池供电的系统。这些低电流延长了电池的使用寿命和续航时间。

LM66200 采用自动二极管模式，可为电压最高的电源分配优先级，并将其输送至输出端。低电平有效使能引脚 ( $\overline{\text{ON}}$ ) 可禁用两个通道，允许用户在无需任一电源的情况下将器件设为关断模式。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
LM66200	SOT (8)	2.1mm × 1.6mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用



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## 4 Revision History

DATE	REVISION	NOTES
November 2021	*	Initial release.

## 5 Pin Configuration and Functions

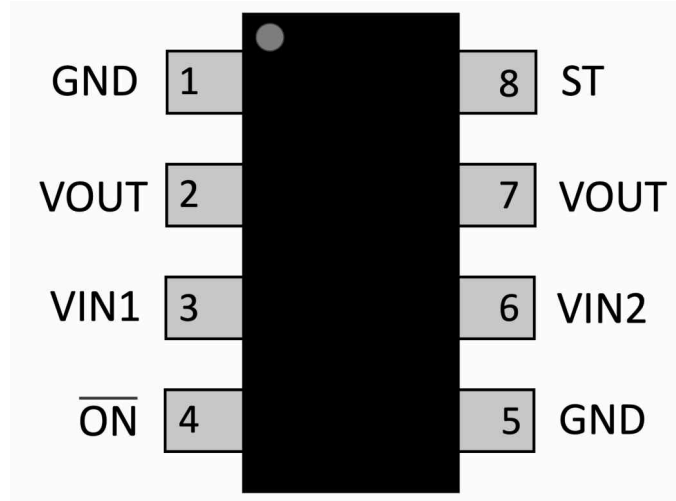


图 5-1. DRL Package 8-Pin SOT Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1, 5	—	Device ground
VOUT	2, 7	O	Output power
VIN1	3	I	Channel 1 input power
$\overline{\text{ON}}$	4	I	Active low enable pin. Device is enabled when $\overline{\text{ON}}$ is pulled low and the device turns off both channels when $\overline{\text{ON}}$ is pulled high.
VIN2	6	I	Channel 2 input power
ST	8	O	Status pin. Pulled high when VIN1 is being used and pulled low when VIN2 is being used. Can be pulled up to VIN1 to reduce quiescent current when VIN2 is powering the output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{IN1}, V_{IN2}$	Input Voltage	- 0.3	6	V
$V_{OUT}$	Output Voltage	- 0.3	6	V
$V_{ST}, V_{ON}$	Control Pin Voltage	- 0.3	6	V
$I_{MAX}$	Maximum Current		2.5	A
$I_{MAX,PLS}$	Maximum Pulsed Current Max duration 1ms, Duty cycle of 2%		4	A
$T_J$	Junction temperature		Internally Limited	°C
$T_{stg}$	Storage temperature	- 65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), ANSI/ESDA/ JEDEC JS-002, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN1}, V_{IN2}$	Input Voltage	1.6		5.5	V
$V_{OUT}$	Output Voltage	0		5.5	V
$V_{ST}, V_{ON}$	Control Pin Voltage	0		5.5	V
$T_A$	Ambient Temperature	- 40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM66200	UNIT
		DRL (SOT)	
		8-PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
<b>Power Consumption</b>							
I <sub>STBY, VIN1</sub>	VIN1 Standby Current	VIN2 powers VOUT VIN2 > VIN1 + 0.2 V	25°C	0.22			µA
			-40°C to 85°C			0.31	µA
			-40°C to 105°C			0.32	µA
I <sub>STBY, VIN2</sub>	VIN2 Standby Current	VIN1 powers VOUT VIN1 > VIN2 + 0.1 V	25°C	0.05			µA
			-40°C to 85°C			0.07	µA
			-40°C to 105°C			0.09	µA
I <sub>Q, VIN1</sub>	VIN1 Quiescent Current	VIN1 powers VOUT VIN1 > VIN2 + 0.1 V	25°C	1.32			µA
			-40°C to 85°C			3.6	µA
			-40°C to 105°C			4.4	µA
I <sub>Q, VIN2</sub>	VIN2 Quiescent Current	VIN2 powers VOUT VIN2 > VIN1 + 0.2 V	25°C	1.35			µA
			-40°C to 85°C			3.7	µA
			-40°C to 105°C			4.5	µA
I <sub>SD, VIN1</sub>	VIN1 Shutdown Current	ON = 5 V VIN1 > VIN2 VOUT = 0 V	25°C	0.1			µA
			-40°C to 85°C			1.3	µA
			-40°C to 105°C			2.9	µA
		ON = 5 V VIN1 < VIN2 VOUT = 0 V	25°C	0.05			µA
			-40°C to 85°C			1	µA
			-40°C to 105°C			2.4	µA
I <sub>SD, VIN2</sub>	VIN2 Shutdown Current	ON = 5 V VIN2 > VIN1 VOUT = 0 V	25°C	0.05			µA
			-40°C to 85°C			1.3	µA
			-40°C to 105°C			2.9	µA
		ON = 5 V VIN2 < VIN1 VOUT = 0 V	25°C	0.05			µA
			-40°C to 85°C			0.7	µA
			-40°C to 105°C			2.1	µA
I <sub>ON</sub>	ON pin leakage	VIN1 = VIN2 = PR1 = 5.5 V	-40°C to 105°C			0.1	µA
I <sub>ST</sub>	ST pin leakage	VIN1 = VIN2 = ST = 5.5 V	-40°C to 105°C			0.03	µA
<b>Performance</b>							
R <sub>ON</sub>	On-Resistance	VIN <sub>x</sub> = 5 V I <sub>OUT</sub> = 200 mA	25°C	37	46		mΩ
			-40°C to 85°C			55	mΩ
			-40°C to 105°C			60	mΩ
		VIN <sub>x</sub> = 3.3 V I <sub>OUT</sub> = 200 mA	25°C	40	48		mΩ
			-40°C to 85°C			55	mΩ
			-40°C to 105°C			59	mΩ
		VIN <sub>x</sub> = 1.8 V I <sub>OUT</sub> = 200 mA	25°C	41	51		mΩ
			-40°C to 85°C			61	mΩ
			-40°C to 105°C			66	mΩ
		VIN <sub>x</sub> = 1.6 V I <sub>OUT</sub> = 200 mA	25°C	42	52		mΩ
			-40°C to 85°C			68	mΩ
			-40°C to 105°C			74	mΩ
V <sub>OL, ST</sub>	Status pin V <sub>OL</sub>	I <sub>ST</sub> = 1 mA	-40°C to 105°C			0.1	V
t <sub>ST</sub>	Status pin response time		-40°C to 105°C			5	µs

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

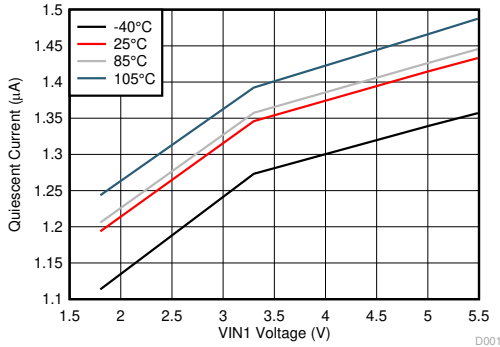
PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
V <sub>ON</sub>	$\overline{\text{ON}}$ reference voltage	1.6 V ≤ VINx ≤ 5.5 V	- 40°C to 105°C	0.8	1	1.2	V
<b>Protection</b>							
t <sub>RCB</sub>	Reverse current blocking response time	V <sub>OUT</sub> > VINx + 1 V	- 40°C to 105°C		2		us
V <sub>RCB,R</sub>	Reverse current blocking rising threshold	1.6 V ≤ VINx ≤ 5.5 V	- 40°C to 105°C		42	70	mV
V <sub>RCB,F</sub>	Reverse current blocking falling threshold	1.6 V ≤ VINx ≤ 5.5 V	- 40°C to 105°C		17	40	mV
I <sub>RCB</sub>	Reverse current blocking activation current	1.6 V ≤ VINx ≤ 5.5 V	- 40°C to 105°C		1.4	4	A
TSD	Thermal shutdown		-		170		°C
TSD <sub>HYS</sub>	Thermal shutdown hysteresis		-		20		°C

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

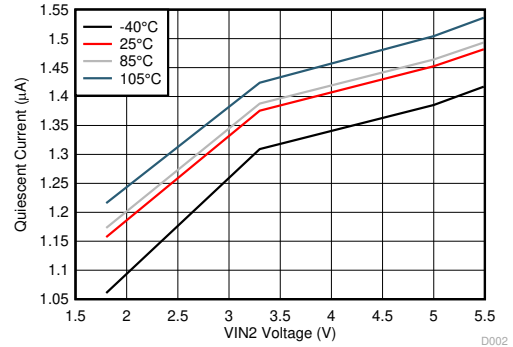
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Switchover</b>						
t <sub>SW</sub>	Switchover time, VINx = 5 V	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10uF		8		us
t <sub>SW</sub>	Switchover time, VINx = 3.3 V	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10uF		6.2		us
t <sub>SW</sub>	Switchover time, VINx = 1.8 V	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10uF		17.7		us
t <sub>D</sub>	Delay time, VINx = 5 V	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 10uF		1		ms
t <sub>D</sub>	Delay time, VINx = 3.3 V	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 10uF		1.2		ms
t <sub>D</sub>	Delay time, VINx = 1.8 V	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 10uF		1.4		ms
t <sub>SS</sub>	Soft-start time, VINx = 5 V	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 10uF		1.7		ms
t <sub>SS</sub>	Soft-start time, VINx = 3.3 V	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 10uF		1.3		ms
t <sub>SS</sub>	Soft-start time, VINx = 1.8 V	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 10uF		0.9		ms

## 6.7 Typical Characteristics



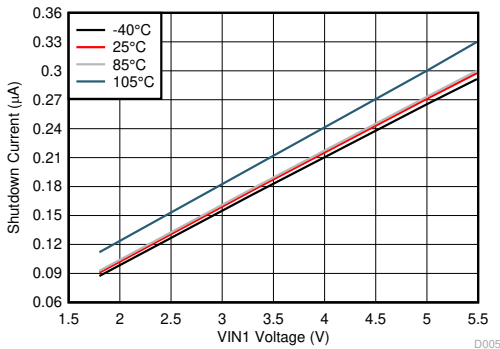
VIN2 = 1.6 V VOUT = Open

图 6-1. VIN1 Quiescent Current vs Input Voltage



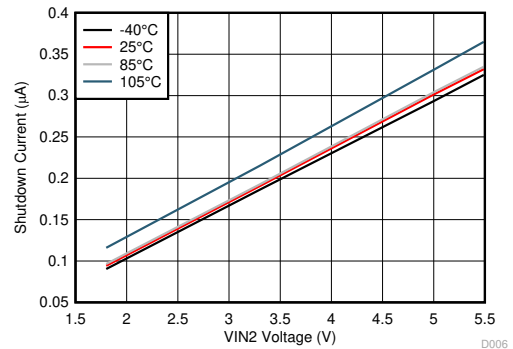
VIN1 = 1.6 V VOUT = Open

图 6-2. VIN2 Quiescent Current vs Input Voltage



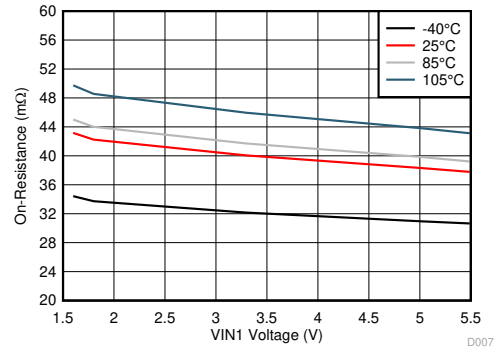
VIN2 = 1.6 V VOUT = 0 V

图 6-3. VIN1 Shutdown Current vs Input Voltage



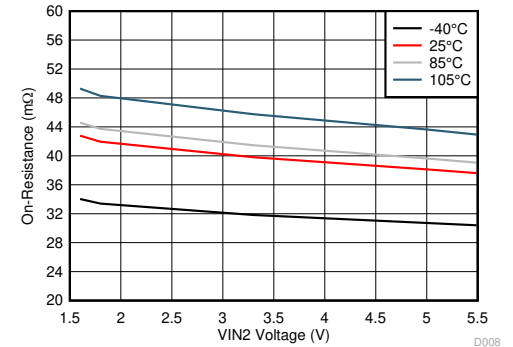
VIN1 = 1.6 V VOUT = 0 V

图 6-4. VIN2 Shutdown Current vs Input Voltage



I<sub>OUT</sub> = 200 mA

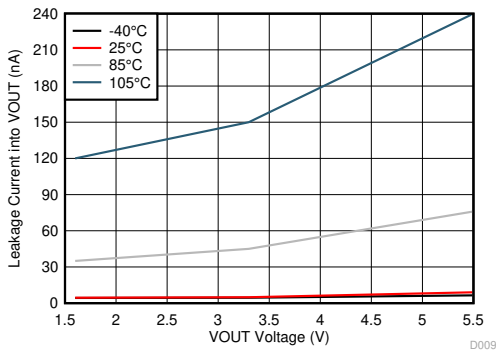
图 6-5. Channel 1 On-Resistance vs Input Voltage



I<sub>OUT</sub> = 200 mA

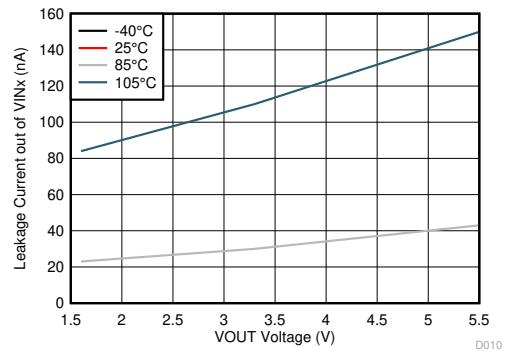
图 6-6. Channel 2 On-Resistance vs Input Voltage

### 6.7 Typical Characteristics (continued)



$V_{INx} = 0\text{ V}$        $V_{INy} = \text{Open}$

图 6-7. Reverse Leakage Current into VOUT



$V_{INx} = 0\text{ V}$        $V_{INy} = \text{Open}$

图 6-8. Reverse Leakage Current out of VINx

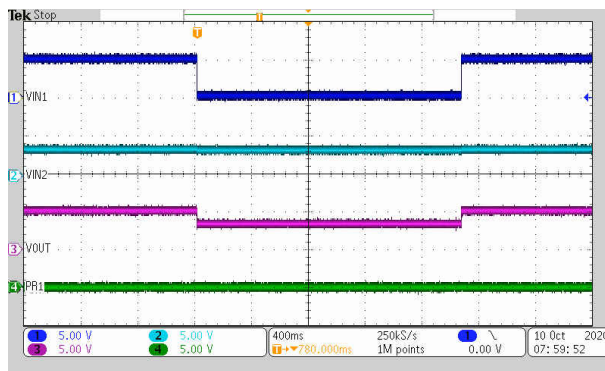


图 6-9. Diode Mode Switchover Behavior ( $R_L = 10\ \Omega$ ,  $C_L = 10\ \mu\text{F}$ )



## 7 Detailed Description

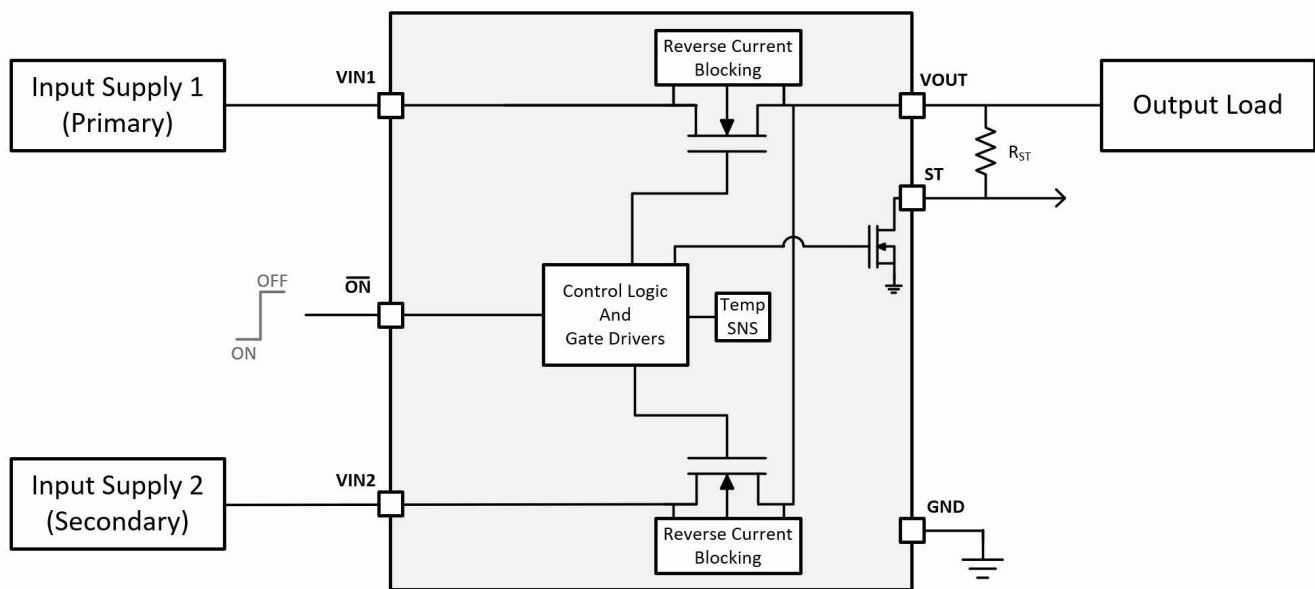
### 7.1 Overview

The LM66200 is a dual ideal diode device with a voltage rating of 1.6 V to 5.5 V and a maximum current rating of 2.5 A per channel. The device uses N-channel MOSFETs to switch between supplies, while providing a controlled slew rate when voltage is first applied.

When in operation, the device has a quiescent of 1.32  $\mu$ A (typical), which is drawn from the highest VINx supply. The lower voltage VINx supply only sees a standby current of 50 nA (typical).

The LM66200 uses automatic diode mode to prioritize the highest voltage supply and pass it through to the output. The active low enable pin ( $\overline{\text{ON}}$ ) allows the user to disable both channels, putting the device into shutdown mode when neither supply is needed.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The below sections detail the features of the LM66200.

#### 7.3.1 Truth Table

The below table shows the expected behavior of the LM66200.

VIN1	VIN2	$\overline{\text{ON}}$	ST	VOUT
VIN1 > VIN2		Low	High	VIN1
VIN1 < VIN2		Low	Low	VIN2
X	X	High	Low	Hi-Z

X = do not care

#### 7.3.2 Soft Start

When an input voltage is applied to the LM66200 and the output voltage is lower than 1 V, the output is brought up with soft start to minimize the inrush current due to output capacitance. During switchover, soft start is not used to minimize output voltage drop. For linear soft start behavior, iTI recommends to have an output capacitance of at least 0.1  $\mu$ F.

### 7.3.3 Status Indication

The ST pin is an open drain output that must be pulled up to an external voltage for proper operation. When the LM66200 is powering the output using VIN1, the ST pin is pulled high. When the LM66200 is powering the output using VIN2, the ST pin is pulled low. During a fault condition the ST pin is pulled low, regardless of the channel being used.

### 7.4 VINx Collapse Rate

The LM66200 uses the highest voltage supply to power the device. When one supply drops below the other, the device changes the supply used to power the device. If the supply powering the device drops at a rate faster than  $1\text{ V}/10\ \mu\text{s}$ , the other supply must be at 2.5 V or higher to prevent the device from resetting. If the other supply is lower than 2.5 V, then the device is not be able to switch to the supply quickly enough, and the device resets and turns on with soft start timing. To slow down the decay of the input, capacitance can be added to the input or output.

### 7.5 Output Voltage Drop

The output voltage drop is based on the load capacitance and load resistance. The stronger the resistive load, the faster the output discharges during switchover. The higher the capacitance on the output, the less the voltage drops during switchover.

### 7.6 Device Functional Modes

The below sections detail the operation of the LM66200 device.

#### 7.6.1 Automatic Switchover

When both inputs are applied to the device, the highest voltage is used to power the output. IThe  $\overline{\text{ON}}$  pin is used as an active low device enable, turning off the device when it is pulled high. When the device is turned back on, soft start is used to power the output. The expected behavior for the device is shown in the waveform below.

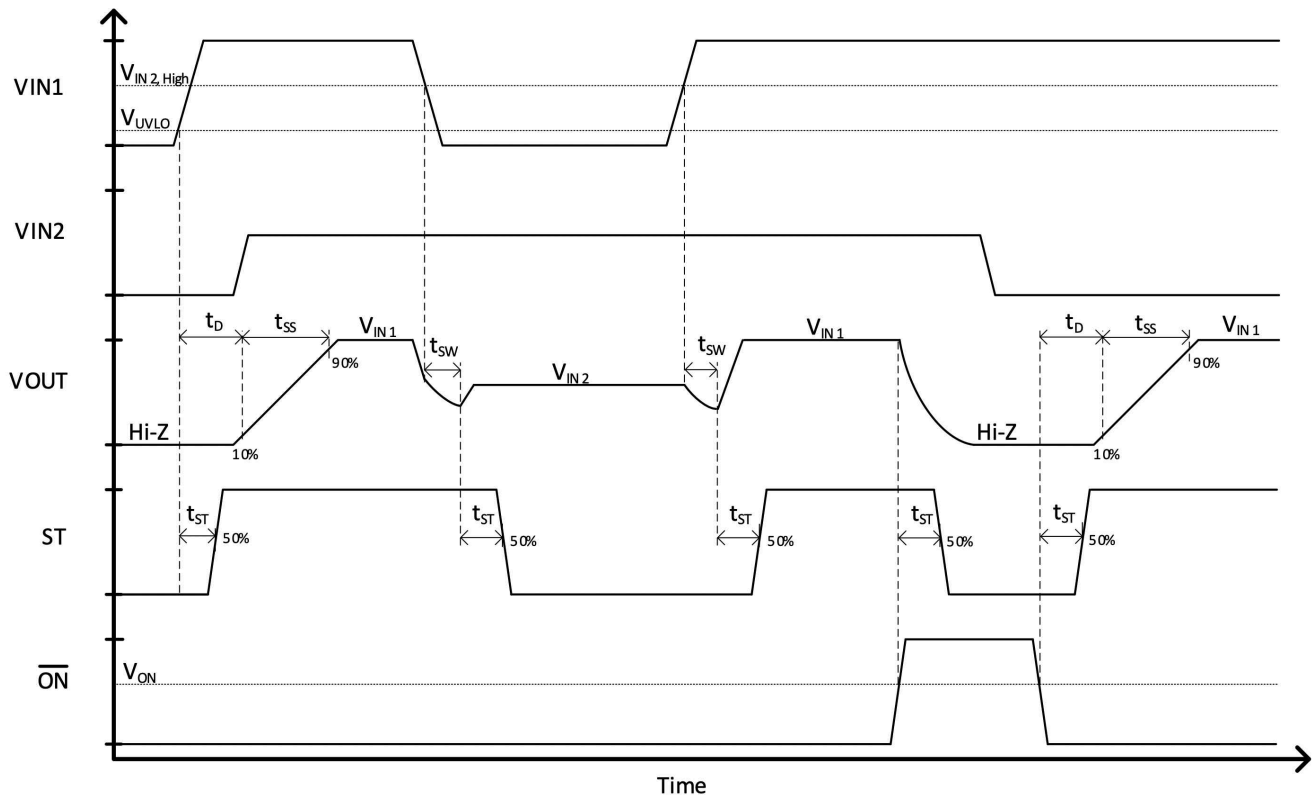


图 7-1. Automatic Switchover Waveform

## 8 Application and Implementation

### Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

### 8.2 Typical Application

This typical application demonstrates how the LM66200 device can be used to control inrush current for high output capacitances.

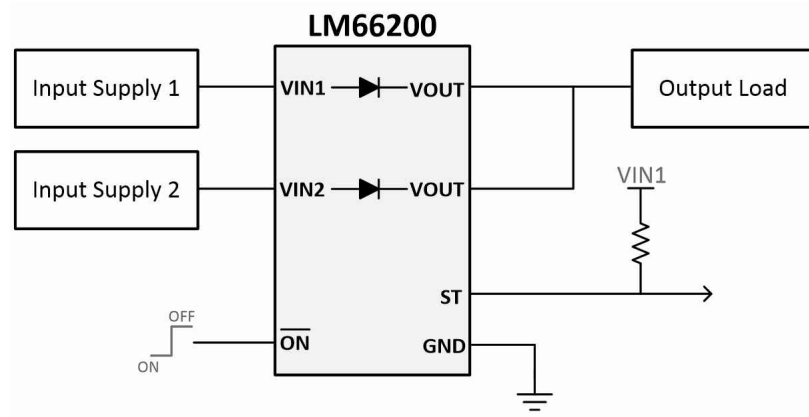


图 8-1. LM66200 Typical Application Diagram

#### 8.2.1 Design Requirements

For this example, the values below are used as the design parameters.

表 8-1. Design Parameters

PARAMETER	VALUE
VIN1 input voltage	5 V
Output capacitance	100 $\mu$ F
Maximum inrush current	500 mA

## 8.2.2 Detailed Design Procedure

Use 方程式 1 to determine how much inrush current is caused by the output capacitor.

$$I_{\text{INRUSH}} = C_{\text{OUT}} \times V_{\text{OUT}} / t_{\text{SS}} \quad (1)$$

where

- $I_{\text{INRUSH}}$  = amount of inrush current caused by  $C_{\text{OUT}}$
- $C_{\text{OUT}}$  = capacitance on  $V_{\text{OUT}}$
- $t_{\text{SS}}$  = output voltage soft start time
- $V_{\text{OUT}}$  = final value of the output voltage

With a final output voltage of 5 V, the expected rise time is 1.7 ms. Using the inrush current equation, the inrush current caused by a 100- $\mu\text{F}$  capacitance is 294 mA, well below the 500-mA target.

## 8.2.3 Application Performance Plots

The below oscilloscope capture shows 5 V being applied to  $V_{\text{IN1}}$ . The output comes up with slew rate control and limits the inrush current to below 500 mA.

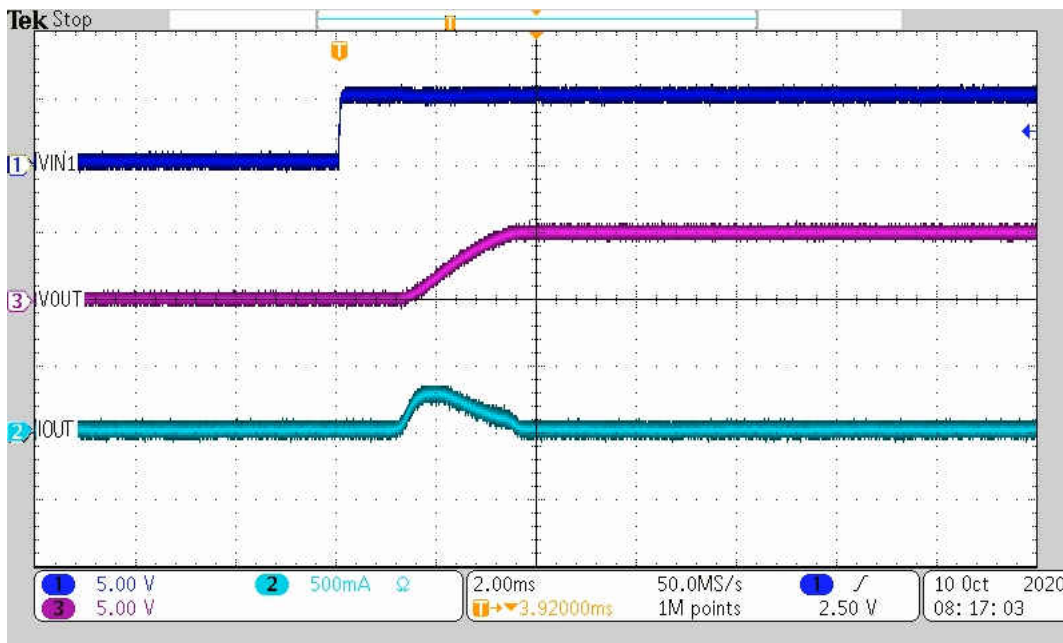


图 8-2. LM66200 Inrush Current Control

## 9 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supplies must be well regulated and placed as close to the device terminals as possible. The power supplies must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1  $\mu$ F is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

## 10 Layout

### 10.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN1, VIN2, VOUT, and GND helps minimize the parasitic electrical effects.

### 10.2 Layout Example

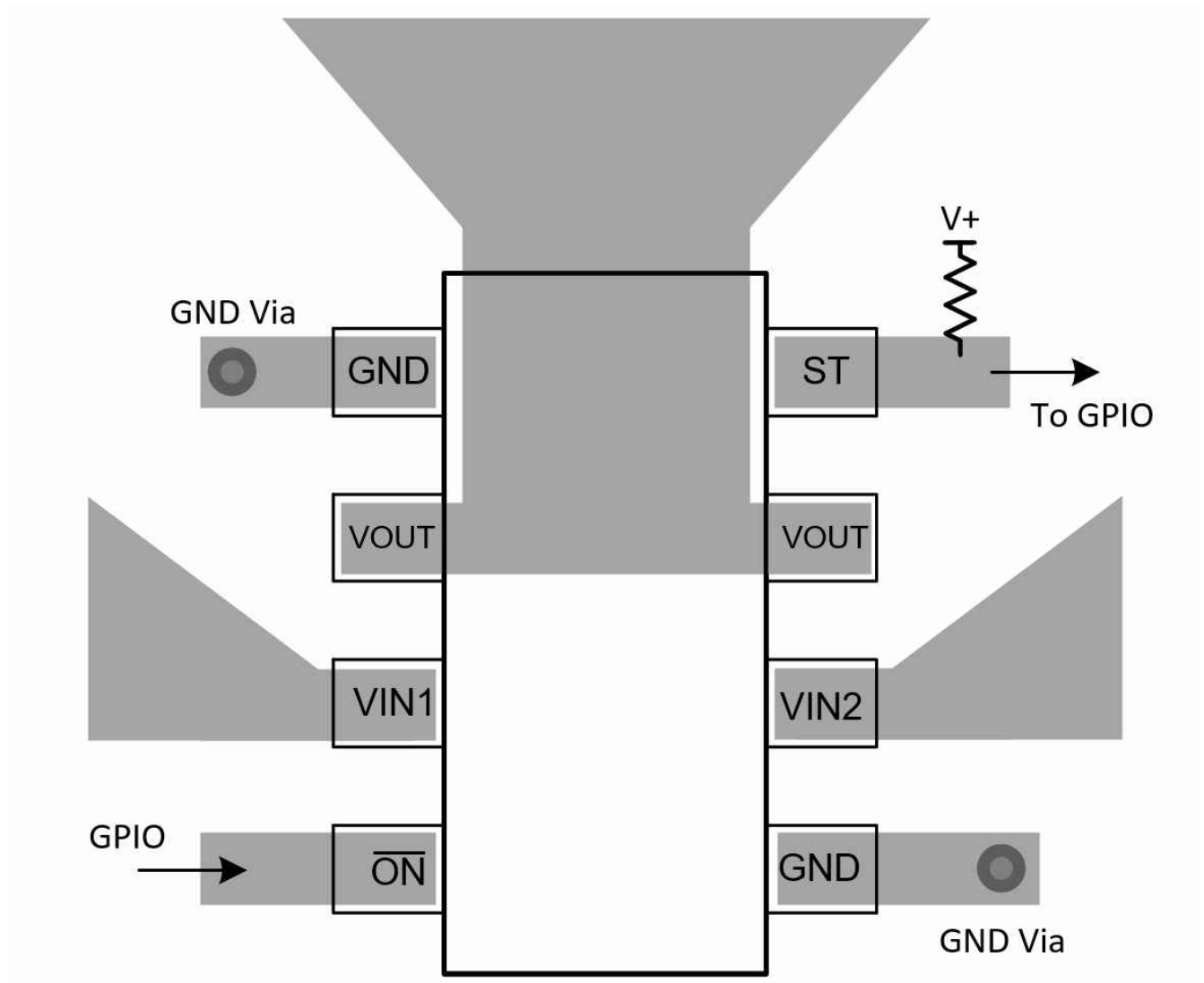


图 10-1. LM66200 Layout Example

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Basics of Power MUX application note](#)
- Texas Instruments, [11 Ways to Protect Your Power Path e-book](#)

#### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 11.3 Trademarks

所有商标均为其各自所有者的财产。

#### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM66200DRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI   SN	Level-1-260C-UNLIM	-40 to 125	LM66	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

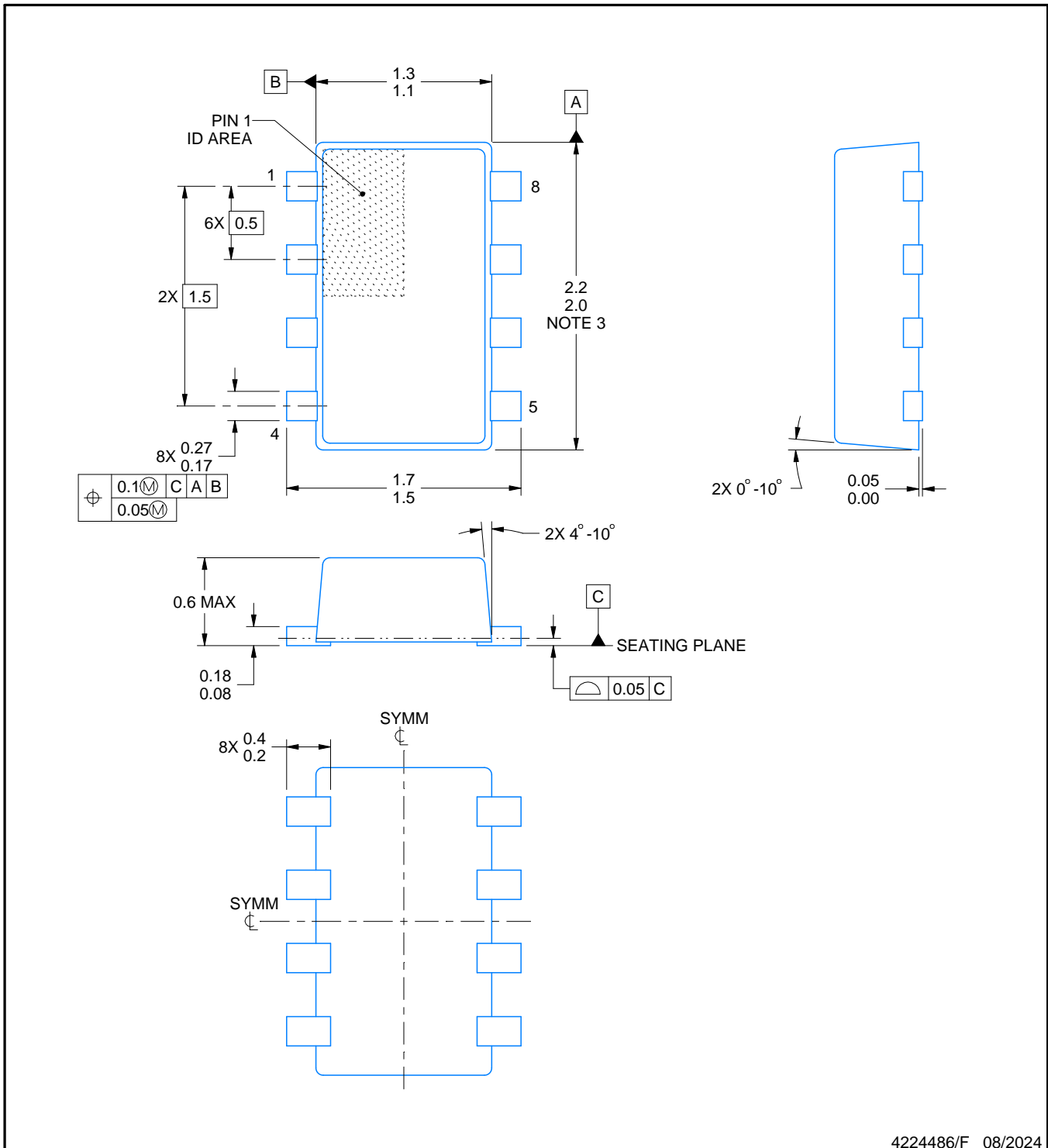
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

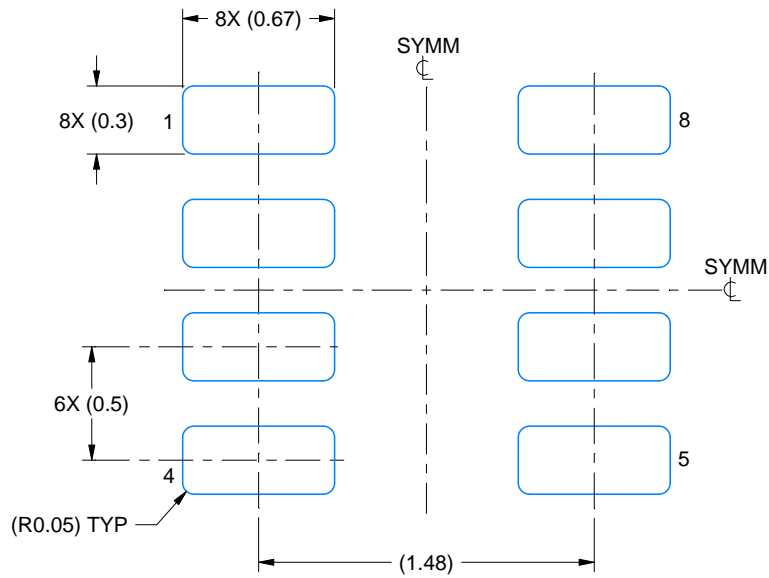


# EXAMPLE BOARD LAYOUT

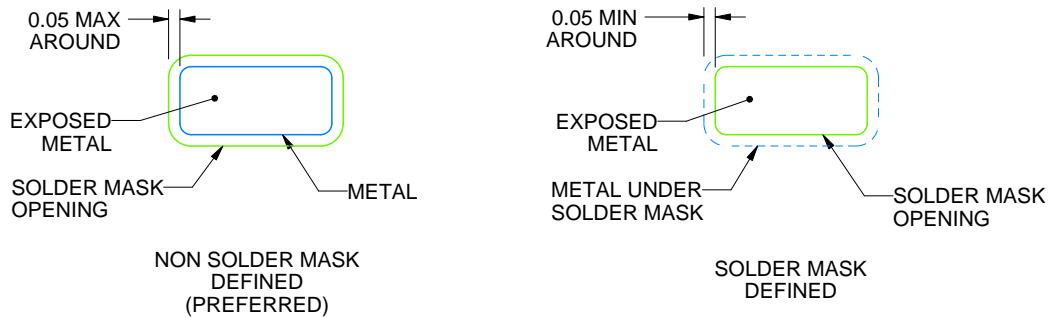
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

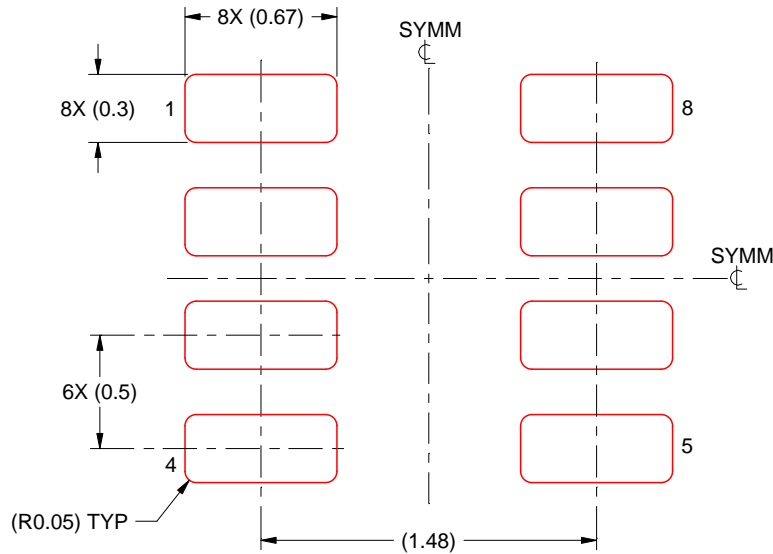
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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