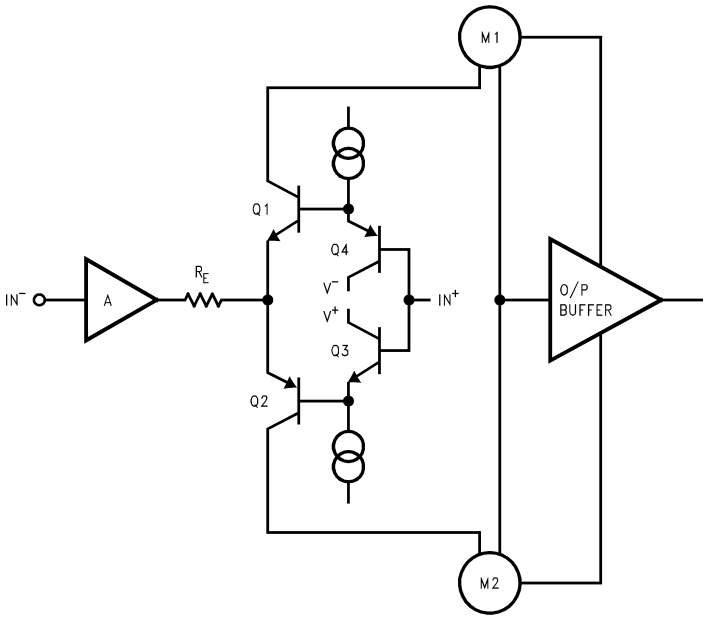
LM7171 超高速、高输出电流、电压反馈放大器

1 特性

- 典型值（除非另有说明）
- 易于使用的电压反馈拓扑
- 极高压摆率：4100V/μs
- 宽单位增益带宽：200MHz
- −3dB 频率（A_V = +2 时）：220MHz
- 低电源电流：6.5mA
- 高开环增益：85dB
- 高输出电流：100mA
- 差分电压增益和相位：0.01%，0.02º
- 额定工作电压为 ±15V 和 ±5V

2 应用

- HDSL 和 ADSL 驱动器
- 多媒体广播系统
- 专业摄像机
- 视频放大器
- 复印机、扫描仪、传真
- HDTV 放大器
- 脉冲放大器和峰值检测器
- CATV 和光纤信号处理



注意：M1 和 M2 是电流镜。

简化版原理图

3 说明

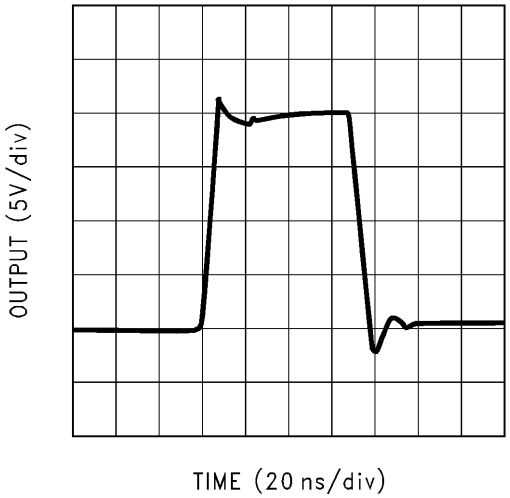
LM7171 是一款高速电压反馈放大器，具有电流反馈放大器的转换特性，但可用于所有传统电压反馈放大器配置。LM7171 在增益低至 +2 或 −1 时保持稳定。该器件提供 4100V/μs 的超高压摆率和 200MHz 的宽单位增益带宽，同时仅消耗 6.5mA 的电源电流。LM7171 是视频和高速信号处理应用的理想选择，例如 HDSL 和脉冲放大器。LM7171 具有 100mA 的输出电流，可作为变压器驱动器或激光二极管驱动器，用于视频分配。

该器件由 ±15V 电源供电，允许较大的信号摆幅，并提供更大的动态范围和信噪比。LM7171 具有低 SFDR 和 THD，非常适合 ADC/DAC 系统。此外，LM7171 的额定工作电压为 ±5V，适用于便携式应用。

封装信息

器件型号	封装(1)	封装尺寸(2)
LM7171	D（SOIC，8）	4.90mm × 6mm
	P（PDIP，8）	9.81mm × 9.43mm

(1) 如需更多信息，请参阅节 9。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



大信号脉冲响应 A_V = +2，V_S = ±15V

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4 Pin Configuration and Functions

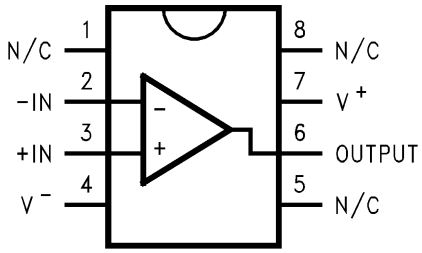


图 4-1. D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	No connection
2	– IN	Input	Inverting power supply
3	+IN	Input	Noninverting power supply
4	V –	Input	Supply voltage
5	NC	—	No connection
6	OUTPUT	Output	Output
7	V+	Input	Supply voltage
8	NC	—	No connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage ($V^+ - V^-$)		36	V
VI	Differential input voltage(2)		±10	V
I_{SC}	Output current short to ground(3)		Continuous	A
T_J	Junction temperature(4)		150	℃

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input differential voltage is applied at V_S = ±15V.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 2500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_S	Supply voltage	5.5		36	V
T_A	Ambient temperature	−40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		LM7171			UNIT
		D (SOIC) A Version	D (SOIC) B Version	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.5	172	108	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.7	62.4	52.4	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.9	55.7	51.9	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	17.6	16.5	6.8	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	65.1	55.1	51.1	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics: ±15V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	LM7171A			0.2	1	mV
			T_A = –40°C to +85°C			4	
		LM7171B			0.2	3	
			T_A = –40°C to +85°C			7	
TCV_{OS}	Input offset voltage average drift				35		µV/°C
I_B	Input bias current				2.7	10	µA
		T_A = –40°C to +85°C				12	
I_{OS}	Input offset current				0.1	4	µA
		T_A = –40°C to +85°C				6	
R_{IN}	Input resistance	Common mode			320		MΩ
		Differential mode			18		
R_O	Open-loop output resistance				19		Ω
CMRR	Common-mode rejection ratio	LM7171A	V_{CM} = ±10V	85	105		dB
			V_{CM} = ±10V, T_A = –40°C to +85°C	80			
		LM7171B	V_{CM} = ±10V	75	105		
			V_{CM} = ±10V, T_A = –40°C to +85°C	70			
PSRR	Power supply rejection ratio	LM7171A	V_S = ±15V	85	90		dB
			V_S = ±15V, T_A = –40°C to +85°C	80			
		LM7171B	V_S = ±15V				
			V_S = ±15V, T_A = –40°C to +85°C				
V_{CM}	Input common-mode voltage	CMRR > 60dB			±13.35		V
A_V	Large-signal voltage gain	LM7171A	R_L = 1kΩ, V_{OUT} = ±5V	80	85		dB
			R_L = 1kΩ, V_{OUT} = ±5V, T_A = –40°C to +85°C	75			
			R_L = 100Ω, V_{OUT} = ±5V	75	81		
			R_L = 100Ω, V_{OUT} = ±5V, T_A = –40°C to +85°C	70			
		LM7171B	R_L = 1kΩ, V_{OUT} = ±5V	75	85		
			R_L = 1kΩ, V_{OUT} = ±5V, T_A = –40°C to +85°C	70			
			R_L = 100Ω, V_{OUT} = ±5V	70	81		
			R_L = 100Ω, V_{OUT} = ±5V, T_A = –40°C to +85°C	66			

5.5 Electrical Characteristics: ±15V（续）

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output swing	R_L = 1kΩ		13	13.3		V
			T_A = –40°C to +85°C	12.7			
		R_L = 1kΩ		–13	–13.2		
			T_A = –40°C to +85°C	–12.7			
		R_L = 100Ω		10.5	11.8		
			T_A = –40°C to +85°C	9.5			
		R_L = 100Ω		–9.5	–10.5		
			T_A = –40°C to +85°C	–9			
	Output current (open loop)	Sourcing, R_L = 100Ω		105	118		mA
			T_A = –40°C to +85°C	95			
		Sinking, R_L = 100Ω		95	105		
			T_A = –40°C to +85°C	90			
	Output current (in linear region)	Sourcing, R_L = 100Ω			100		
		Sinking, R_L = 100Ω			100		
I_{SC}	Output short-circuit current	Sourcing			140		
		Sinking			135		
I_S	Supply current				6.5	8.5	
						9.5	
SR	Slew rate	A_V = +2, V_{IN} = 13V_{PP}			4100		V/μs
		A_V = +2, V_{IN} = 10V_{PP}			3100		
	Unity-gain bandwidth	LM7171A			160		MHz
		LM7171B			200		
	−3dB frequency	A_V = +2			220		MHz
Φ_m	Phase margin				50		Deg
t_s	Settling time (0.1%)	A_V = −1, V_{OUT} = ±5V, R_L = 500Ω	LM7171A		16		ns
			LM7171B		42		ns
t_p	Propagation delay	A_V = −2, V_{IN} = ±1V, R_L = 500Ω			5		ns
HD2	Second harmonic distortion	LM7171A	f_{IN} = 10kHz		–123		dBc
			f_{IN} = 5MHz		–75		
		LM7171B	f_{IN} = 10kHz		–110		
			f_{IN} = 5MHz		–75		
HD3	Third harmonic distortion	LM7171A	f_{IN} = 10kHz		–133		dBc
			f_{IN} = 5MHz		–88		
		LM7171B	f_{IN} = 10kHz		–115		
			f_{IN} = 5MHz		–55		
e_n	Input-referred voltage noise	f = 10kHz	LM7171A		8.5		nV/√Hz
			LM7171B		14		
i_n	Input-referred current noise	f = 10kHz	LM7171A		1		pA/√Hz
			LM7171B		1.5		

5.6 Electrical Characteristics: ±5V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	LM7171A			0.3	1.5	mV
			T_A = –40°C to +85°C			4	
		LM7171B			0.3	3.5	
			T_A = –40°C to +85°C			7	
TCV_{OS}	Input offset voltage average drift				35		µV/°C
I_B	Input bias current				3.3	10	µA
		T_A = –40°C to +85°C				12	
I_{OS}	Input offset current				0.1	4	µA
		T_A = –40°C to +85°C				6	
R_{IN}	Input resistance	Common mode			250		MΩ
		Differential mode			18		
R_O	Open-loop output resistance				18		Ω
CMRR	Common-mode rejection ratio	LM7171A	V_{CM} = ±2.5V	80	104		dB
			V_{CM} = ±2.5V, T_A = –40°C to +85°C	75			
		LM7171B	V_{CM} = ±2.5V	70	104		
			V_{CM} = ±2.5V, T_A = –40°C to +85°C	65			
PSRR	Power supply rejection ratio	LM7171A	V_S = ±5V	85	90		dB
			V_S = ±5V, T_A = –40°C to +85°C	80			
		LM7171B	V_S = ±5V	75	90		
			V_S = ±5V, T_A = –40°C to +85°C	70			
V_{CM}	Input common-mode voltage range	CMRR > 60dB			±3.2		V
A_V	Large-signal voltage gain	LM7171A	R_L = 1kΩ, V_{OUT} = ±1V	75	78		dB
			R_L = 1kΩ, V_{OUT} = ±1V, T_A = –40°C to +85°C	70			
			R_L = 100Ω, V_{OUT} = ±1V	72	76		
			R_L = 100Ω, V_{OUT} = ±1V, T_A = –40°C to +85°C	67			
		LM7171B	R_L = 1kΩ, V_{OUT} = ±1V	70	78		
			R_L = 1kΩ, V_{OUT} = ±1V, T_A = –40°C to +85°C	65			
			R_L = 100Ω, V_{OUT} = ±1V	68	76		
			R_L = 100Ω, V_{OUT} = ±1V, T_A = –40°C to +85°C	63			

5.6 Electrical Characteristics: ±5V（续）

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output swing	R_L = 1kΩ		3.2	3.4		V
				–3.2	–3.4		
			T_A = –40°C to +85°C	3			
				–3			
		R_L = 100Ω		2.9	3.1		
				–2.9	–3		
			T_A = –40°C to +85°C	2.8			
				–2.8			
	Output current (open loop)	Sourcing, R_L = 100Ω		29	31		mA
			T_A = –40°C to +85°C	28			
		Sinking, R_L = 100Ω		29	30		
			T_A = –40°C to +85°C	28			
	Output current (in linear region)	Sourcing, R_L = 100Ω			30		mA
		Sinking, R_L = 100Ω			31		
I_{SC}	Output short-circuit current	Sourcing			135		mA
		Sinking			100		
I_S	Supply current				6.2	8	mA
		T_A = –40°C to +85°C				9	
SR	Slew rate	A_V = +2, V_{IN} = 3.2V_{PP}	LM7171A		1200		V/μs
			LM7171B		950		
	Unity-gain bandwidth	LM7171A			125		MHz
		LM7171B			125		
	−3dB frequency	A_V = +2	LM7171A		140		MHz
			LM7171B		140		
Φ_m	Phase margin	LM7171A			68		Deg
		LM7171B			57		
t_s	Settling time (0.1%)	A_V = −1, V_{OUT} = ±1V, R_L = 500Ω	LM7171A		15		ns
			LM7171B		56		
t_p	Propagation delay	A_V = −2, V_{IN} = ±1V, R_L = 500Ω	LM7171A		2.5		ns
			LM7171B		6		
HD2	Second harmonic distortion	LM7171A	f_{IN} = 10kHz		–125		dBc
			f_{IN} = 5MHz		–72		
		LM7171B	f_{IN} = 10kHz		–102		
			f_{IN} = 5MHz		–70		
HD3	Third harmonic distortion	LM7171A	f_{IN} = 10kHz		–129		dBc
			f_{IN} = 5MHz		–81		
		LM7171B	f_{IN} = 10kHz		–110		
			f_{IN} = 5MHz		–51		
e_n	Input-referred voltage noise	f = 10kHz	LM7171A		8.5		nV/√Hz
			LM7171B		14		

5.6 Electrical Characteristics: ±5V（续）

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
i_n	Input-referred current noise	f = 10kHz	LM7171A		1		pA/ √ Hz
			LM7171B		1.8		

5.7 Typical Characteristics: LM7171A

at T_A= 25°C (unless otherwise noted)

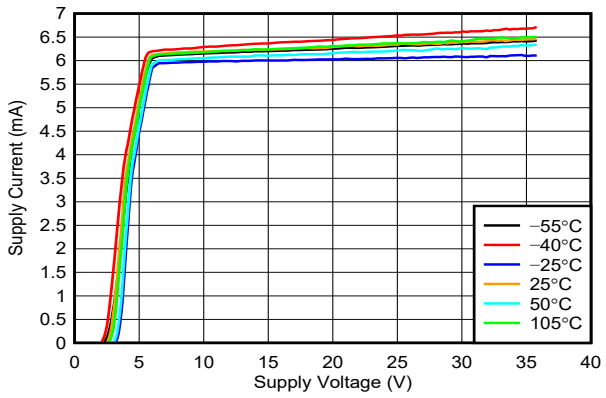


图 5-1. Supply Current vs Supply Voltage

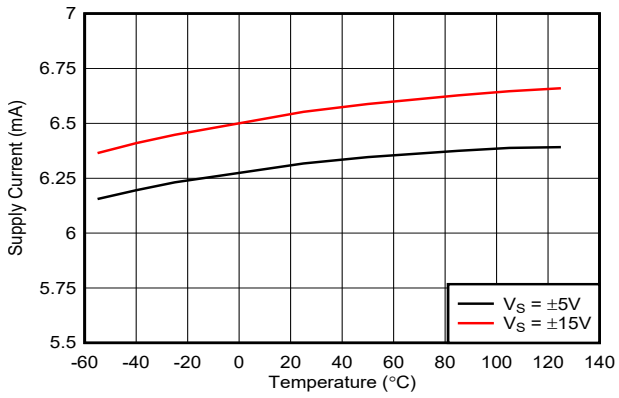


图 5-2. Supply Current vs Temperature

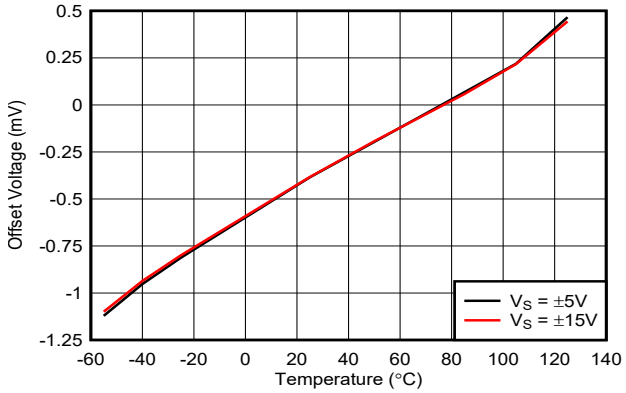


图 5-3. Input Offset Voltage vs Temperature

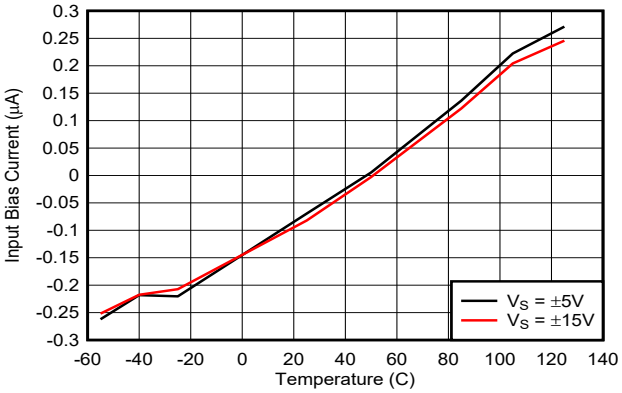


图 5-4. Input Bias Current vs Temperature

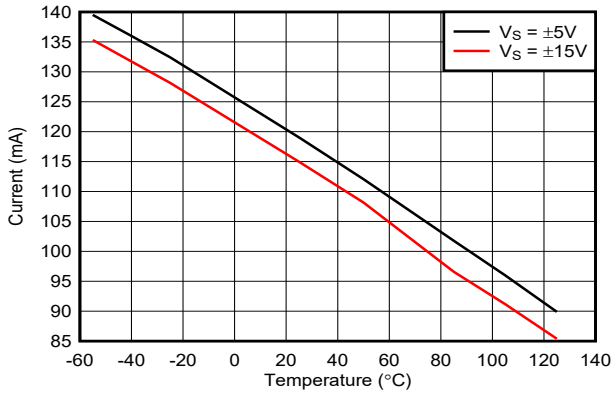


图 5-5. Short Circuit Current vs Temperature (Sourcing)

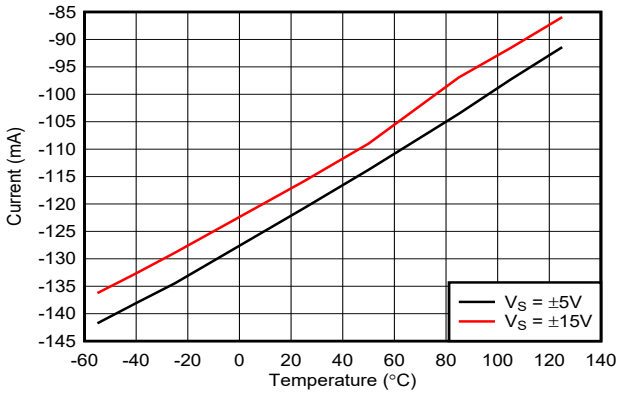
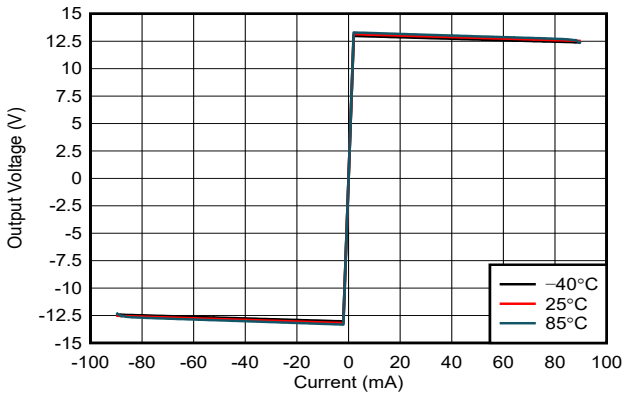


图 5-6. Short Circuit Current vs Temperature (Sinking)

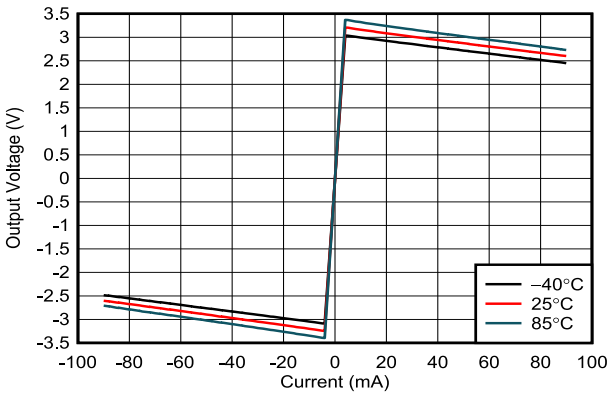
5.7 Typical Characteristics: LM7171A (continued)

at T_A= 25°C (unless otherwise noted)



V_S = ±15V

图 5-7. Output Voltage vs Output Current



V_S = ±5V

图 5-8. Output Voltage vs Output Current

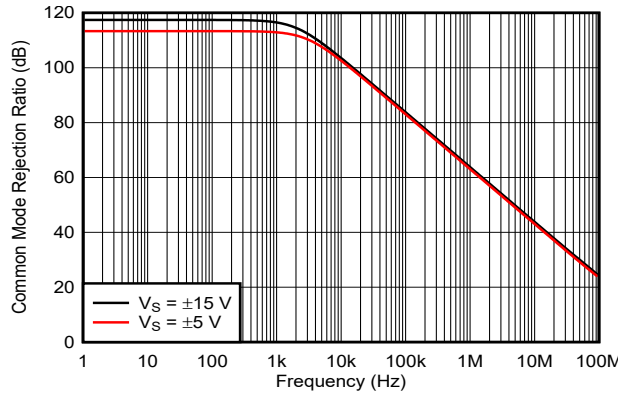
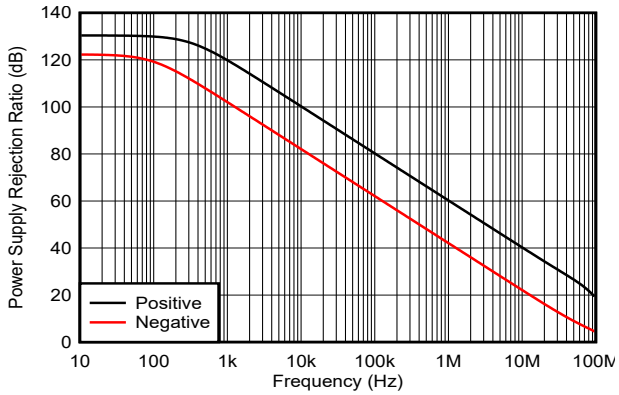
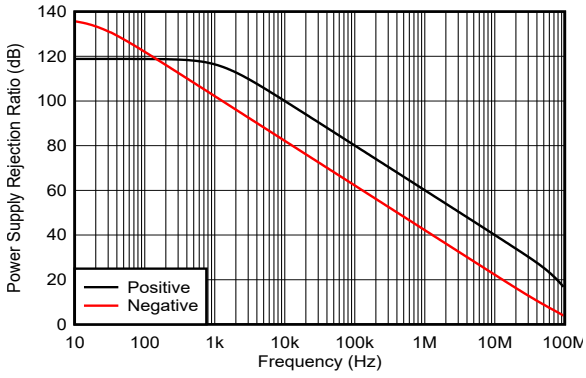


图 5-9. CMRR vs Frequency



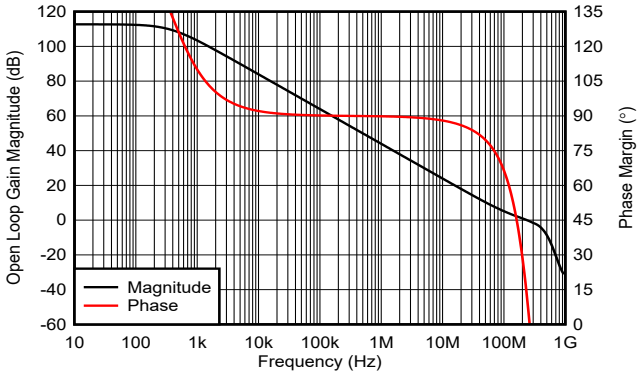
V_S = 30V

图 5-10. PSRR vs Frequency



V_S = 10V

图 5-11. PSRR vs Frequency

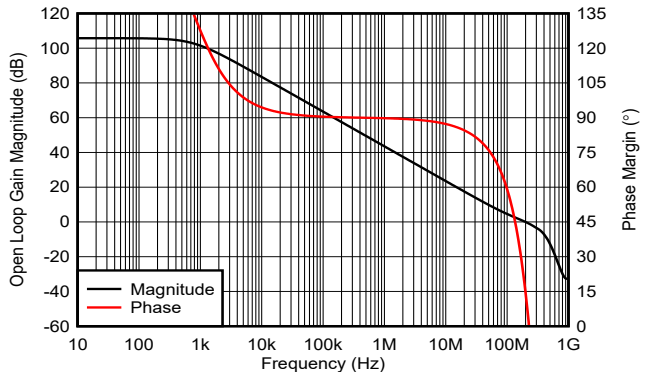


V_S = ±15V

图 5-12. Open Loop Frequency Response

5.7 Typical Characteristics: LM7171A (continued)

at T_A= 25°C (unless otherwise noted)



V_S = ±5V

图 5-13. Open Loop Frequency Response

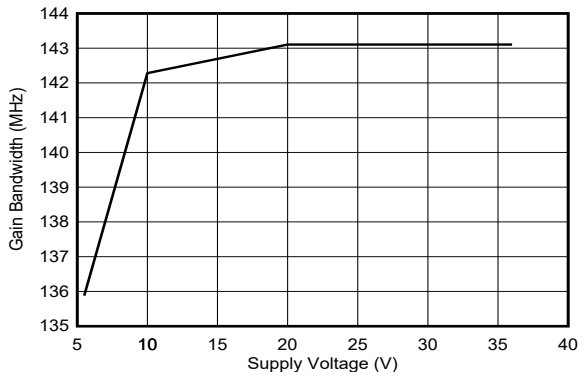


图 5-14. Gain-Bandwidth Product vs Supply Voltage

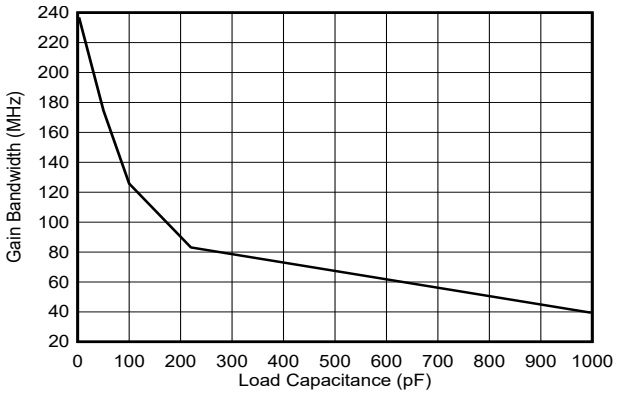


图 5-15. Gain-Bandwidth Product vs Load Capacitance

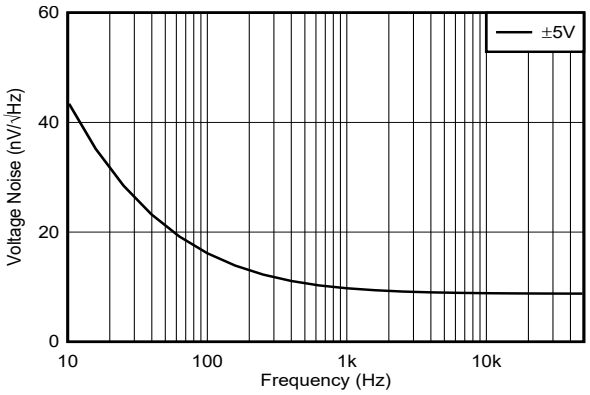


图 5-16. Input Voltage Noise vs Frequency

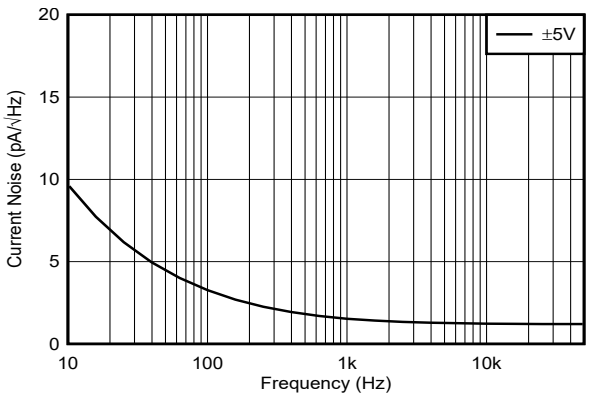


图 5-17. Input Current Noise vs Frequency

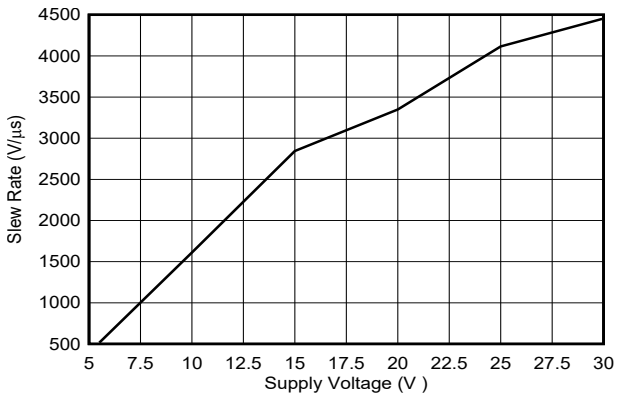


图 5-18. Slew Rate vs Supply Voltage

5.7 Typical Characteristics: LM7171A (continued)

at T_A= 25°C (unless otherwise noted)

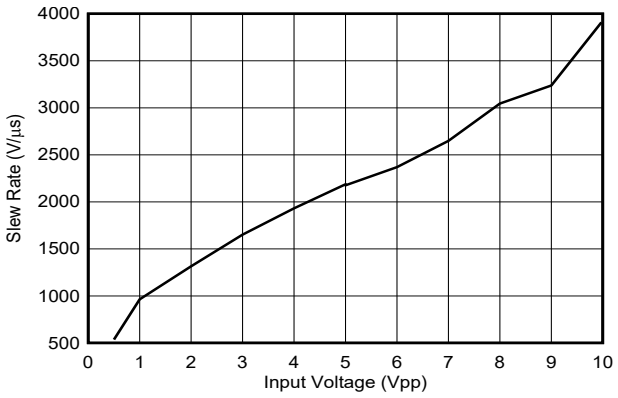


图 5-19. Slew Rate vs Input Voltage

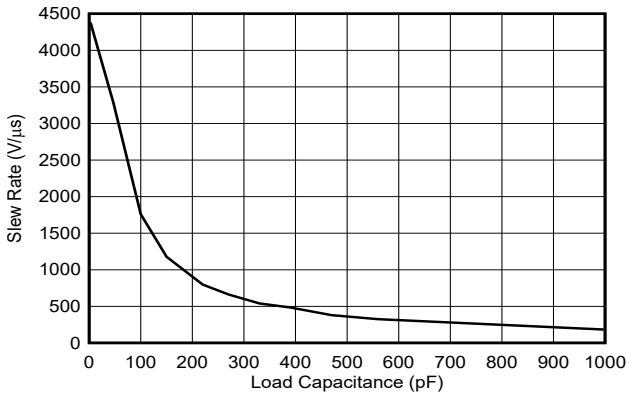
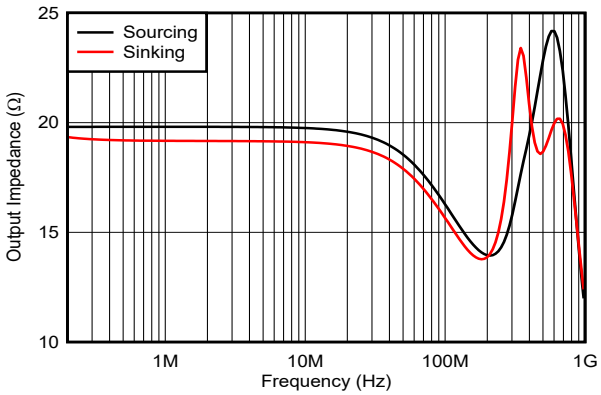
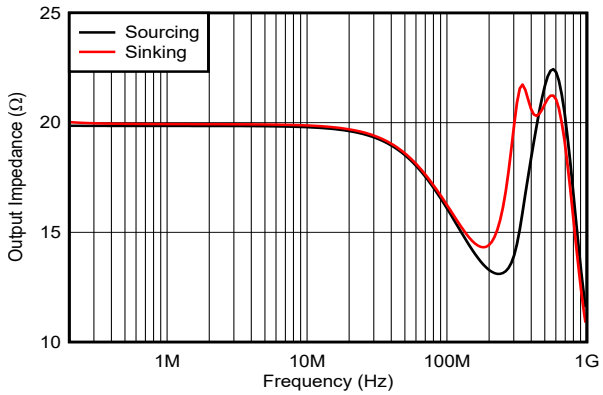


图 5-20. Slew Rate vs Load Capacitance



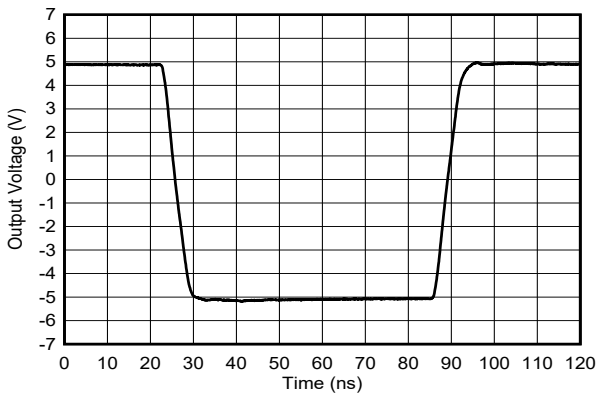
V_S = ±15V

图 5-21. Open Loop Output Impedance vs Frequency



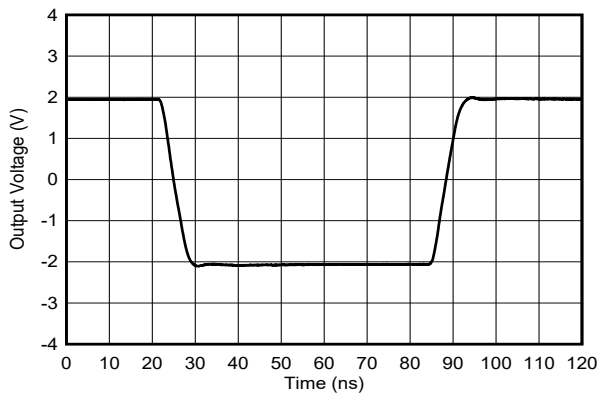
V_S = ±5V

图 5-22. Open Loop Output Impedance vs Frequency



A_V = −1 V_S = ±15V

图 5-23. Large-Signal Pulse Response

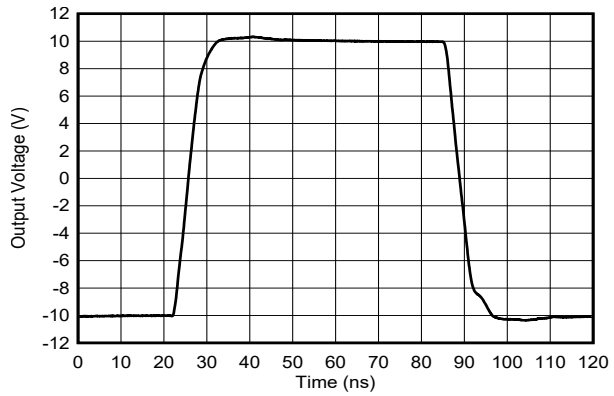


A_V = −1 V_S = ±5V

图 5-24. Large-Signal Pulse Response

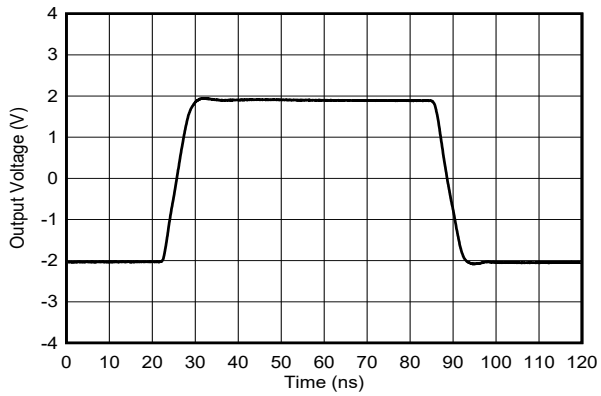
5.7 Typical Characteristics: LM7171A (continued)

at T_A= 25°C (unless otherwise noted)



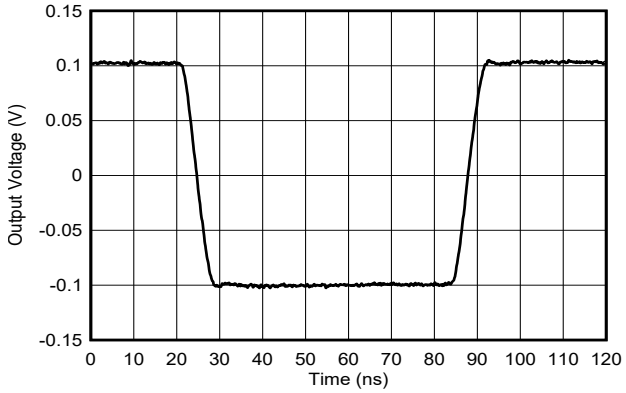
A_V = +2 V_S = ±15V

图 5-25. Large-Signal Pulse Response



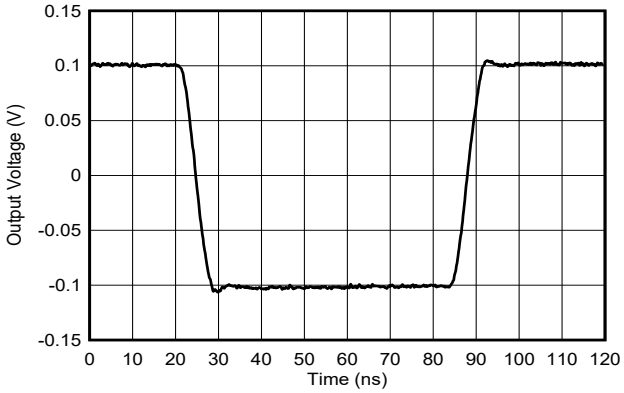
A_V = +2 V_S = ±5V

图 5-26. Large-Signal Pulse Response



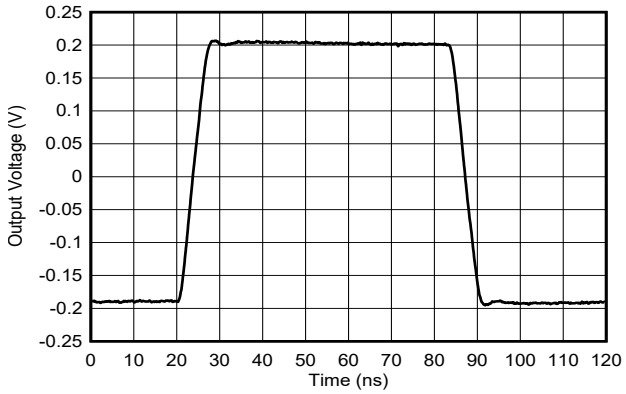
A_V = −1 V_S = ±15V

图 5-27. Small-Signal Pulse Response



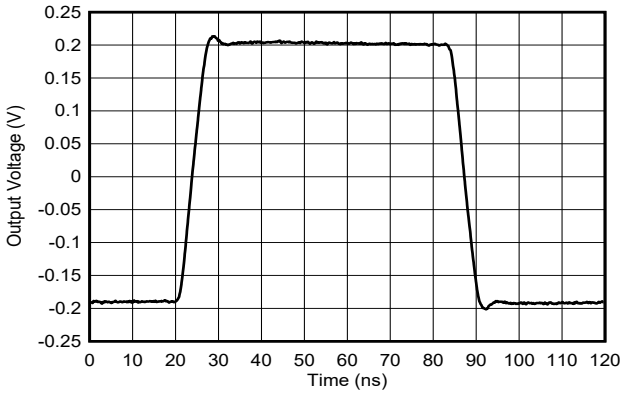
A_V = −1 V_S = ±5V

图 5-28. Small-Signal Pulse Response



A_V = +2 V_S = ±15V

图 5-29. Small-Signal Pulse Response

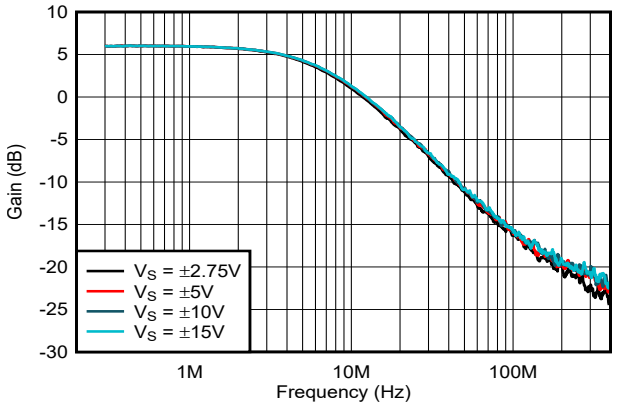


A_V = +2 V_S = ±5V

图 5-30. Small-Signal Pulse Response

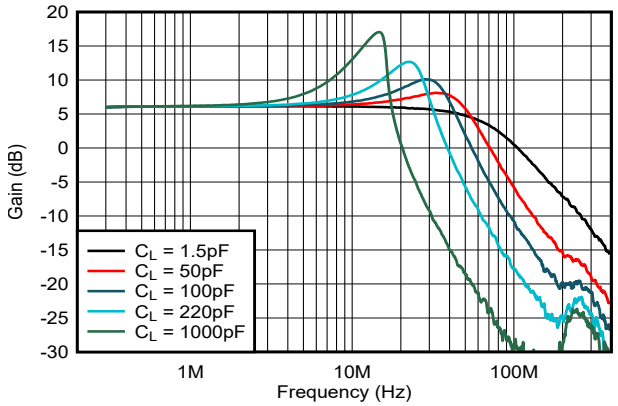
5.7 Typical Characteristics: LM7171A (continued)

at T_A= 25°C (unless otherwise noted)



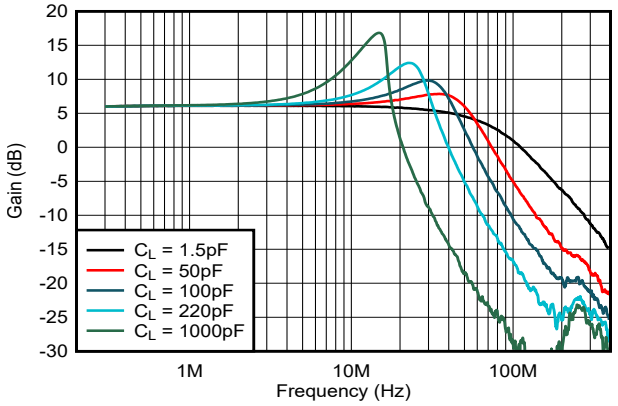
A_V = +2

图 5-31. Closed-Loop Frequency Response vs Supply Voltage



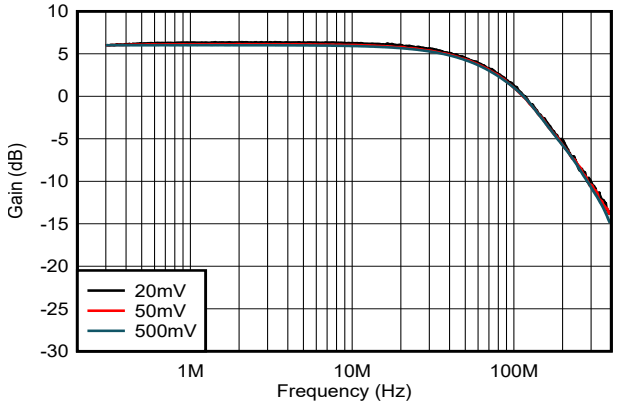
A_V = +2 V_S = ±5V

图 5-32. Closed-Loop Frequency Response vs Capacitive Load



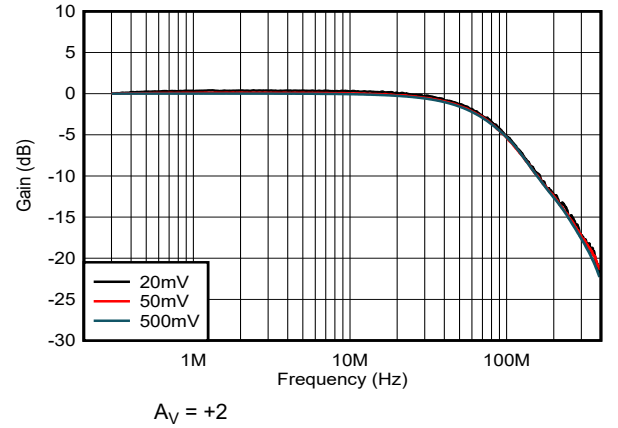
A_V = +2 V_S = ±15V

图 5-33. Closed-Loop Frequency Response vs Capacitive Load



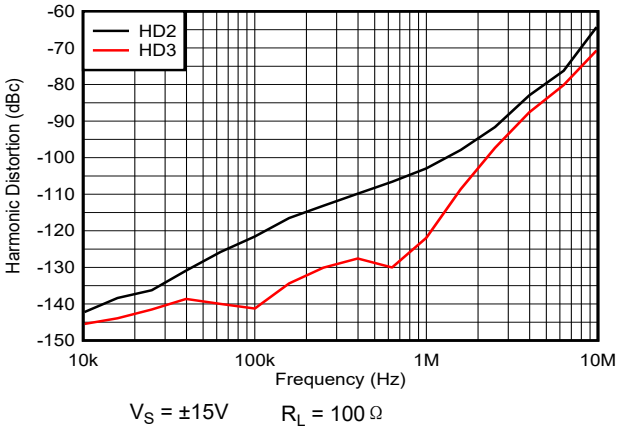
A_V = +2

图 5-34. Closed-Loop Frequency Response vs Input Signal Level



A_V = +2

图 5-35. Closed-Loop Frequency Response vs Input Signal Level

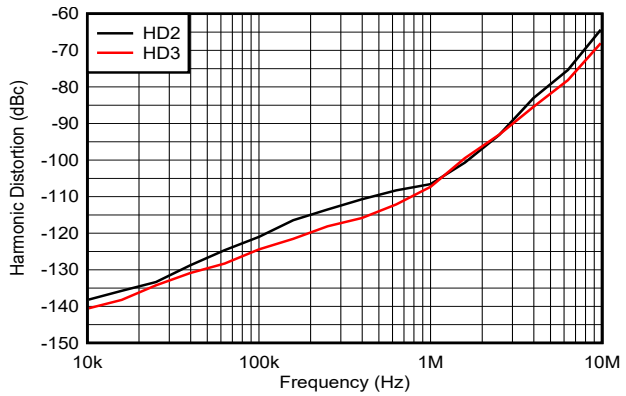


V_S = ±15V R_L = 100 Ω

图 5-36. Total Harmonic Distortion vs Frequency

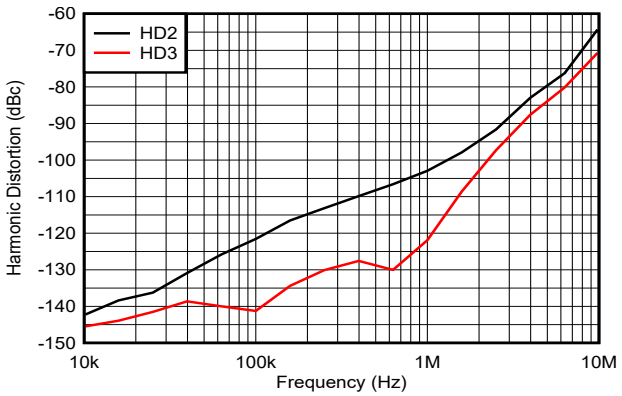
5.7 Typical Characteristics: LM7171A (continued)

at T_A= 25°C (unless otherwise noted)



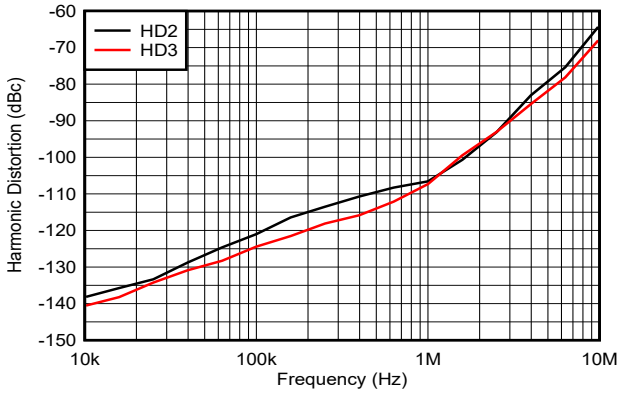
V_S = ±5V R_L = 100 Ω

图 5-37. Total Harmonic Distortion vs Frequency



V_S = ±15V R_L = 2.5k Ω

图 5-38. Harmonic Distortion vs Frequency



V_S = ±5V R_L = 2.5k Ω

图 5-39. Harmonic Distortion vs Frequency

5.8 Typical Characteristics: LM7171B

at T_A= 25°C (unless otherwise noted)

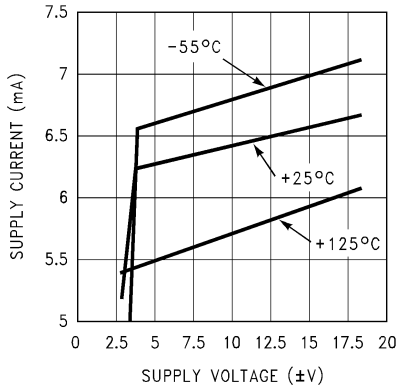


图 5-40. Supply Current vs Supply Voltage

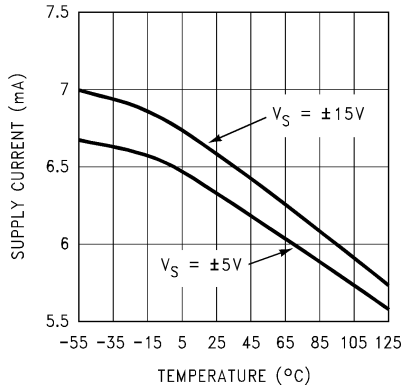


图 5-41. Supply Current vs Temperature

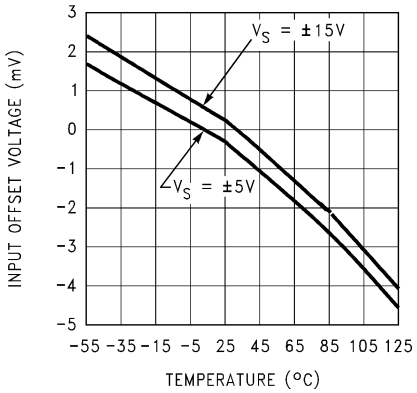


图 5-42. Input Offset Voltage vs Temperature

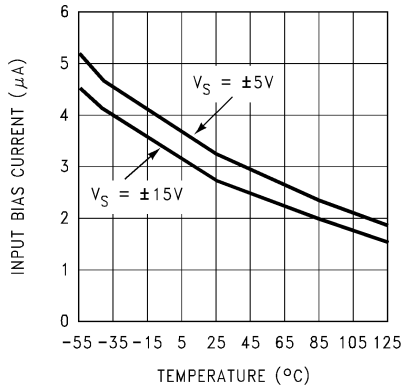


图 5-43. Input Bias Current vs Temperature

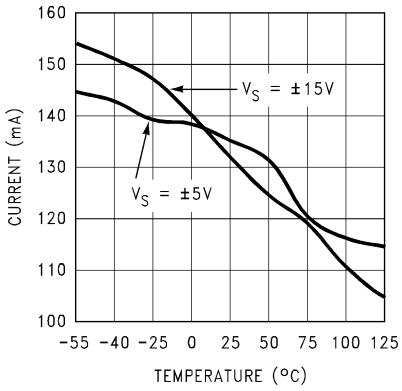


图 5-44. Short Circuit Current vs Temperature (Sourcing)

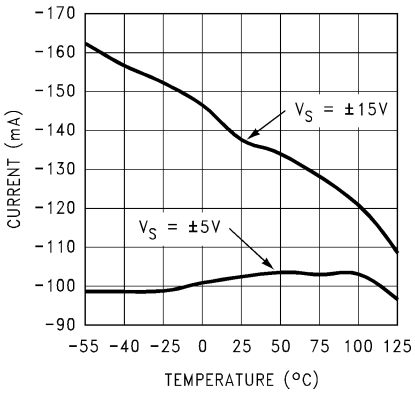


图 5-45. Short Circuit Current vs Temperature (Sinking)

5.8 Typical Characteristics: LM7171B (continued)

at T_A= 25°C (unless otherwise noted)

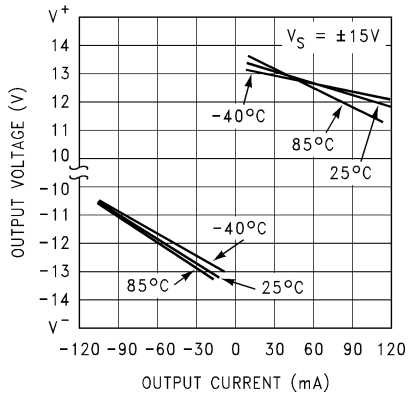


图 5-46. Output Voltage vs Output Current

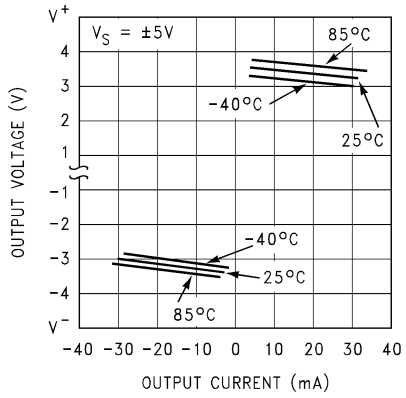


图 5-47. Output Voltage vs Output Current

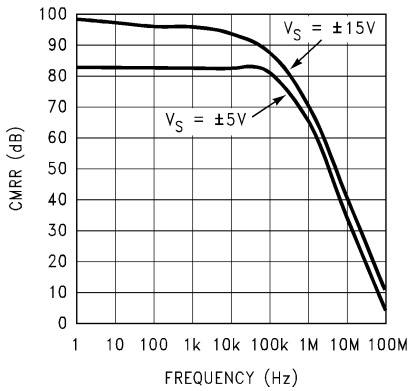


图 5-48. CMRR vs Frequency

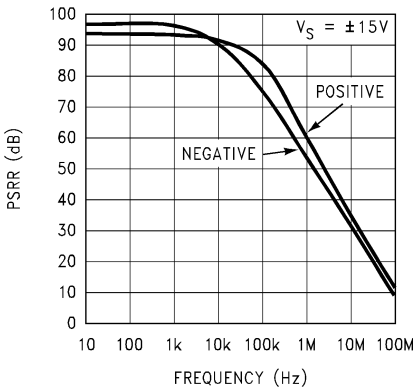


图 5-49. PSRR vs Frequency

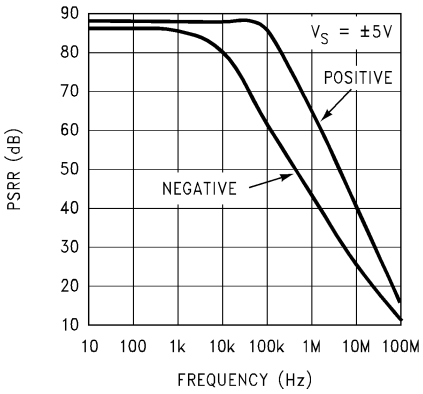


图 5-50. PSRR vs Frequency

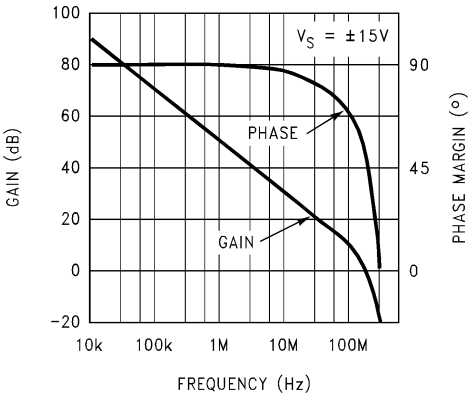


图 5-51. Open Loop Frequency Response

5.8 Typical Characteristics: LM7171B (continued)

at T_A= 25°C (unless otherwise noted)

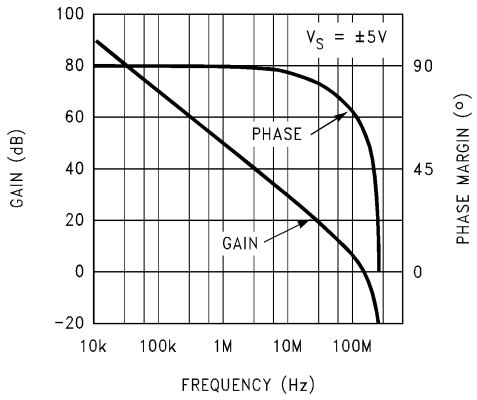


图 5-52. Open Loop Frequency Response

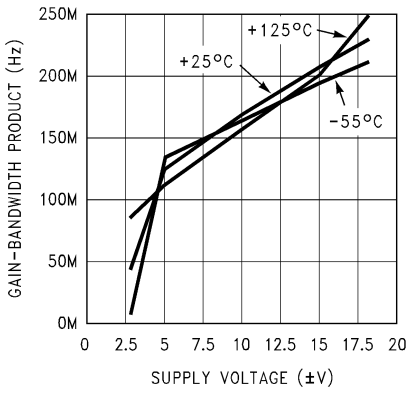


图 5-53. Gain-Bandwidth Product vs Supply Voltage

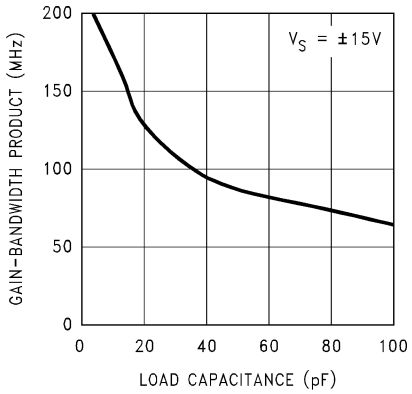


图 5-54. Gain-Bandwidth Product vs Load Capacitance

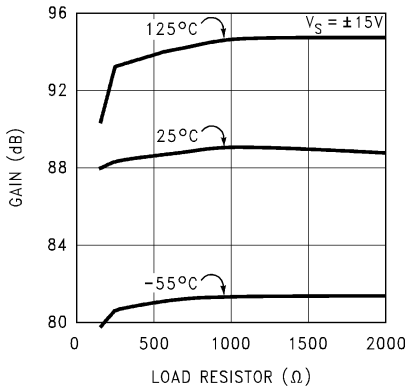


图 5-55. Large Signal Voltage Gain vs Load

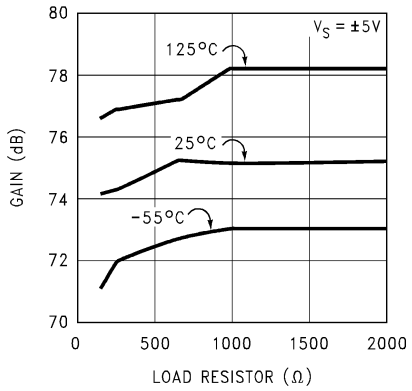


图 5-56. Large Signal Voltage Gain vs Load

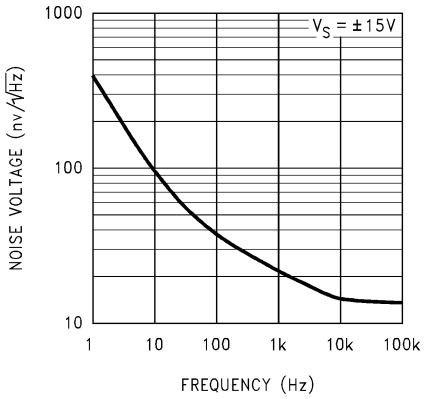


图 5-57. Input Voltage Noise vs Frequency

5.8 Typical Characteristics: LM7171B (continued)

at T_A= 25°C (unless otherwise noted)

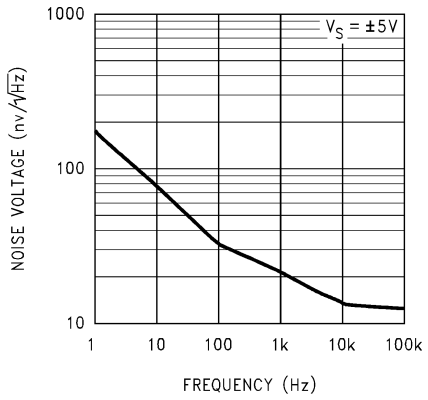


图 5-58. Input Voltage Noise vs Frequency

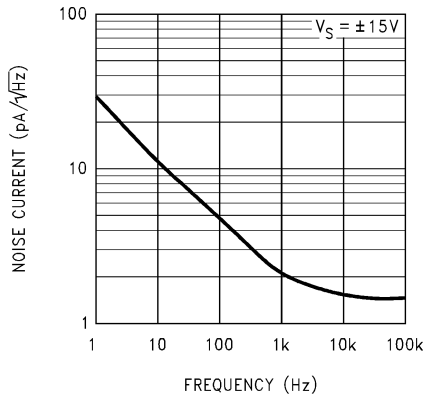


图 5-59. Input Current Noise vs Frequency

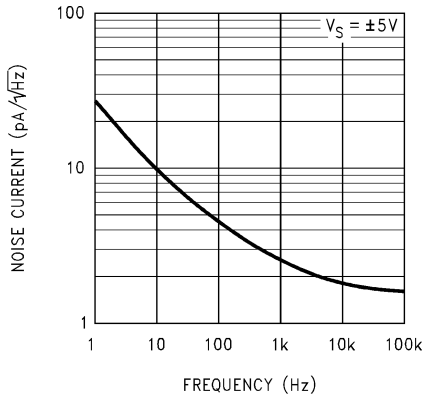


图 5-60. Input Current Noise vs Frequency

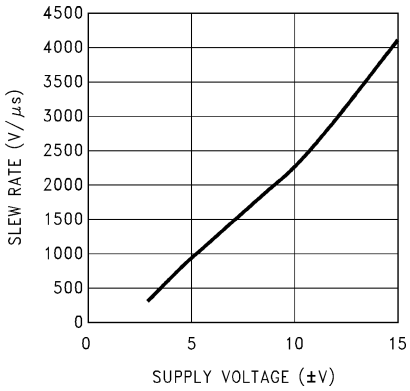


图 5-61. Slew Rate vs Supply Voltage

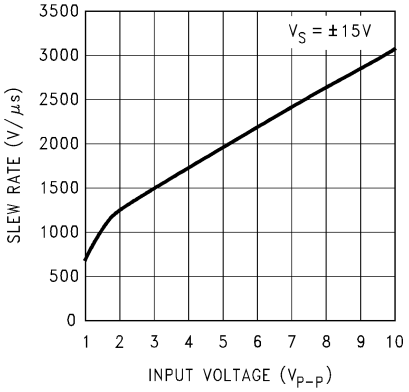


图 5-62. Slew Rate vs Input Voltage

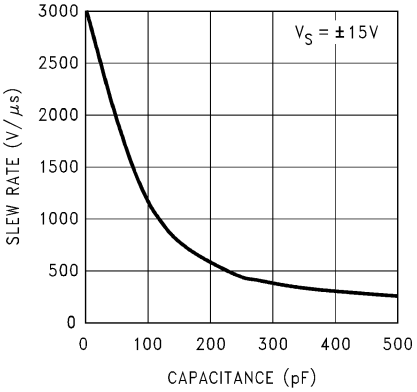


图 5-63. Slew Rate vs Load Capacitance

5.8 Typical Characteristics: LM7171B (continued)

at T_A= 25°C (unless otherwise noted)

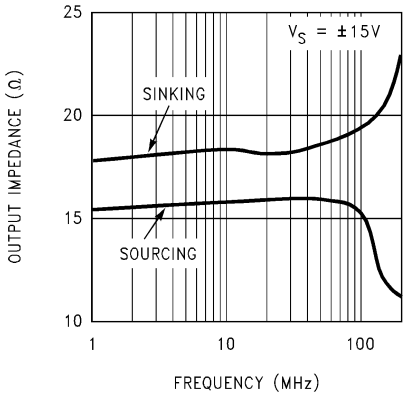


图 5-64. Open Loop Output Impedance vs Frequency

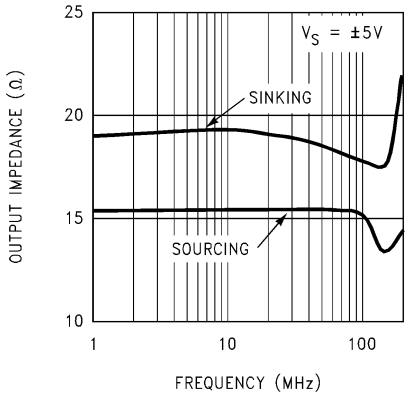
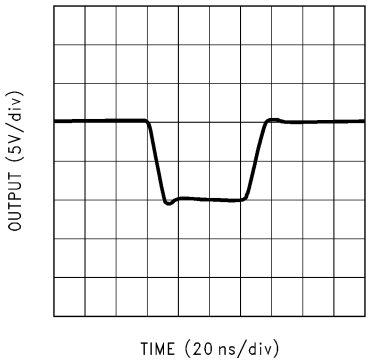
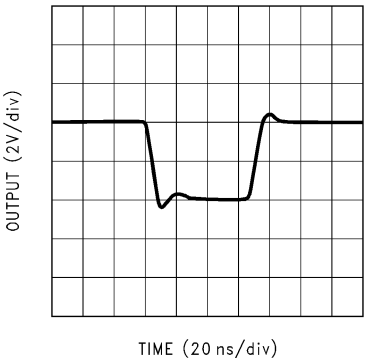


图 5-65. Open Loop Output Impedance vs Frequency



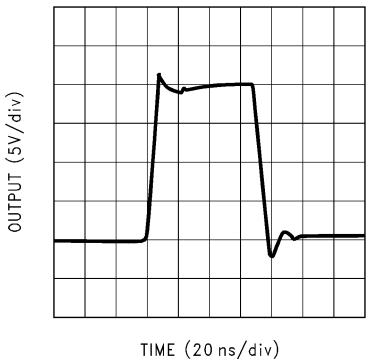
A_V = –1 V_S = ±15V

图 5-66. Large-Signal Pulse Response



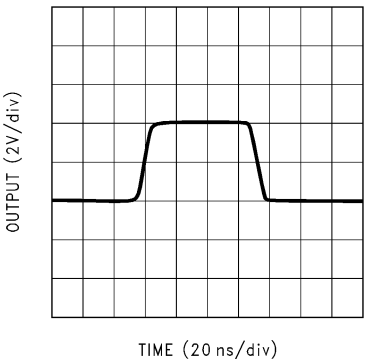
A_V = –1 V_S = ±5V

图 5-67. Large-Signal Pulse Response



A_V = +2 V_S = ±15V

图 5-68. Large-Signal Pulse Response

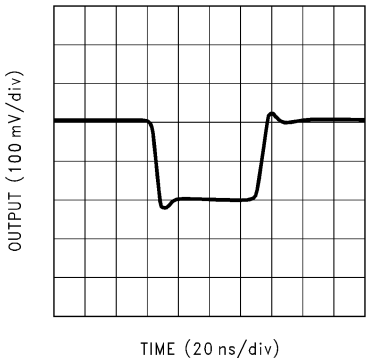


A_V = +2 V_S = ±5V

图 5-69. Large-Signal Pulse Response

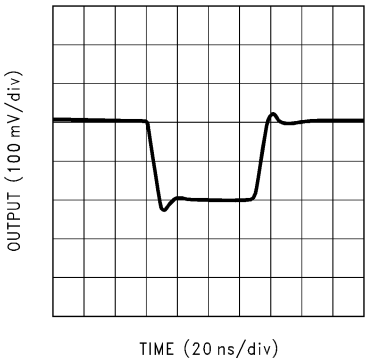
5.8 Typical Characteristics: LM7171B (continued)

at T_A= 25°C (unless otherwise noted)



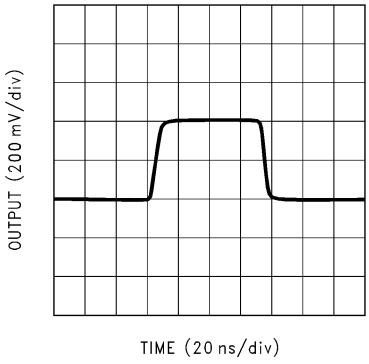
A_V = – 1 V_S = ±15V

图 5-70. Small-Signal Pulse Response



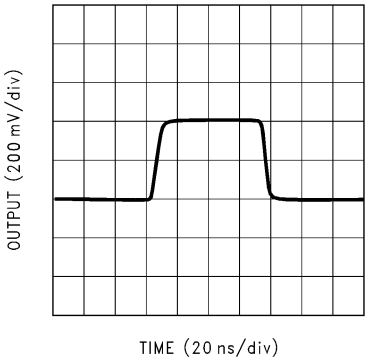
A_V = – 1 V_S = ±5V

图 5-71. Small-Signal Pulse Response



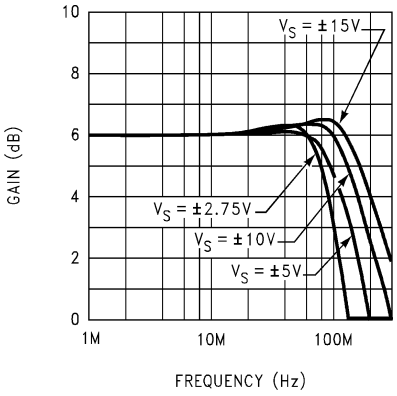
A_V = +2 V_S = ±15V

图 5-72. Small-Signal Pulse Response



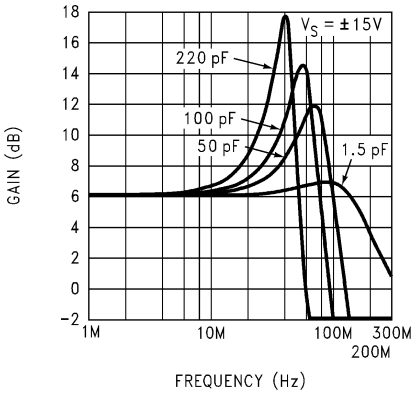
A_V = +2 V_S = ±5V

图 5-73. Small-Signal Pulse Response



A_V = +2

图 5-74. Closed-Loop Frequency Response vs Supply Voltage

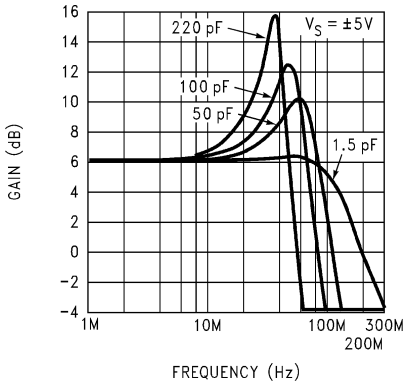


A_V = +2

图 5-75. Closed-Loop Frequency Response vs Capacitive Load

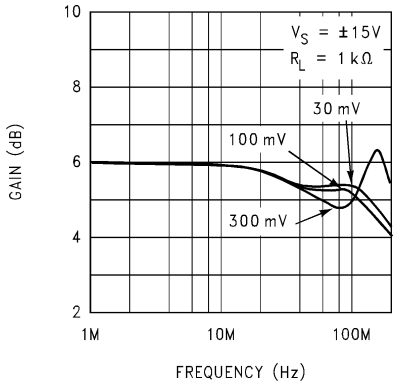
5.8 Typical Characteristics: LM7171B (continued)

at T_A= 25°C (unless otherwise noted)



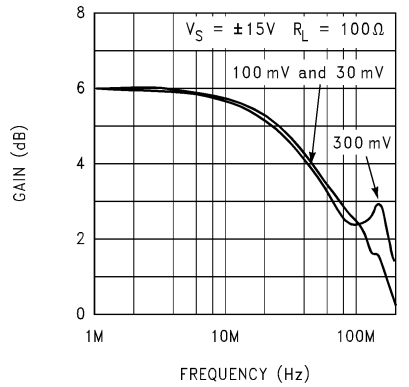
A_V = +2

图 5-76. Closed-Loop Frequency Response vs Capacitive Load



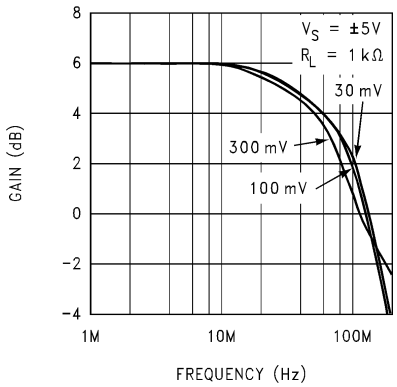
A_V = +2

图 5-77. Closed-Loop Frequency Response vs Input Signal Level



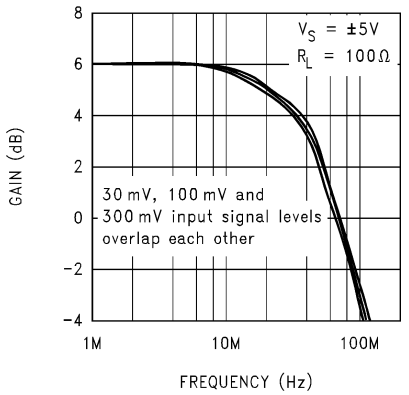
A_V = +2

图 5-78. Closed-Loop Frequency Response vs Input Signal Level



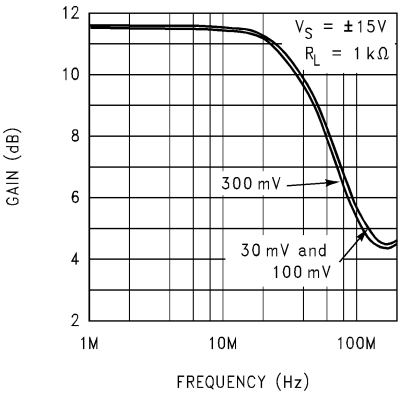
A_V = +2

图 5-79. Closed-Loop Frequency Response vs Input Signal Level



A_V = +2

图 5-80. Closed-Loop Frequency Response vs Input Signal Level

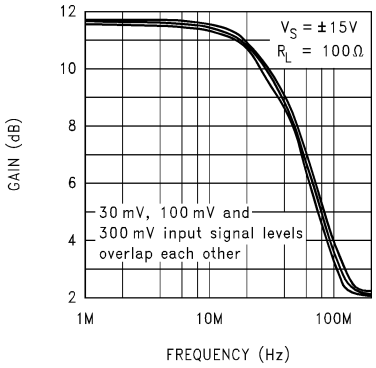


A_V = +4

图 5-81. Closed-Loop Frequency Response vs Input Signal Level

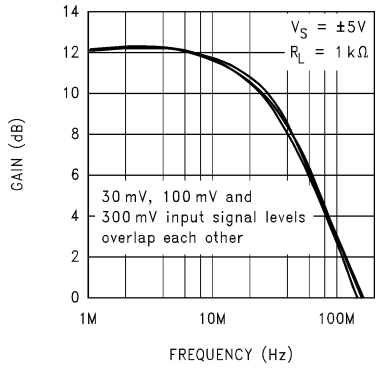
5.8 Typical Characteristics: LM7171B (continued)

at T_A= 25°C (unless otherwise noted)



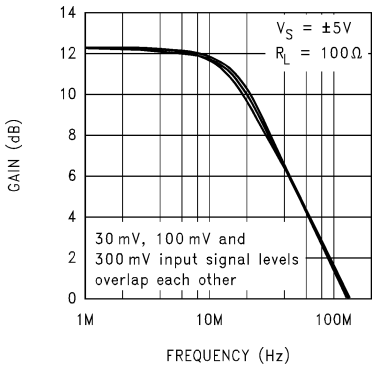
A_V = +4

图 5-82. Closed-Loop Frequency Response vs Input Signal Level



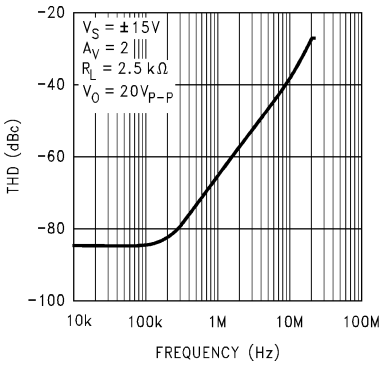
A_V = +4

图 5-83. Closed-Loop Frequency Response vs Input Signal Level



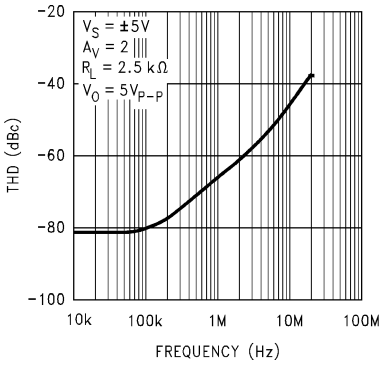
A_V = +4

图 5-84. Closed-Loop Frequency Response vs Input Signal Level



THD measurement at low frequency limited by test instrument

图 5-85. Total Harmonic Distortion vs Frequency



THD measurement at low frequency limited by test instrument

图 5-86. Total Harmonic Distortion vs Frequency

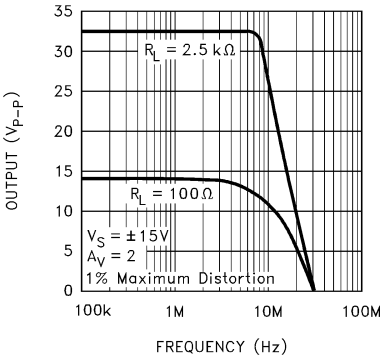


图 5-87. Undistorted Output Swing vs Frequency

5.8 Typical Characteristics: LM7171B (continued)

at T_A= 25°C (unless otherwise noted)

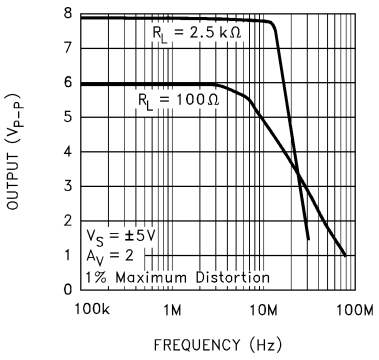


图 5-88. Undistorted Output Swing vs Frequency

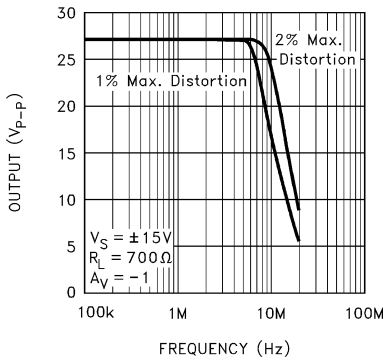
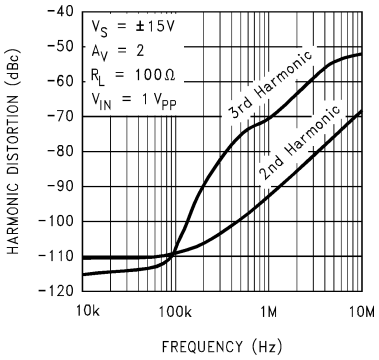
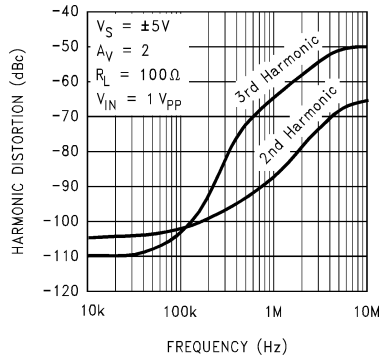


图 5-89. Undistorted Output Swing vs Frequency



THD measurement at low frequency limited by test instrument

图 5-90. Harmonic Distortion vs Frequency



THD measurement at low frequency limited by test instrument

图 5-91. Harmonic Distortion vs Frequency

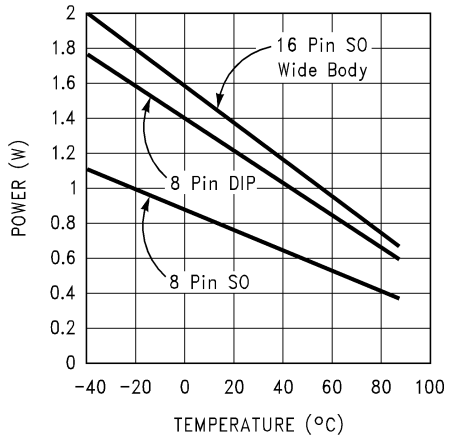


图 5-92. Maximum Power Dissipation vs Ambient Temperature

6 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

6.1 Application Information

The LM7171 is a very high-speed, voltage-feedback amplifier (VFA). This device consumes only 6.5mA of supply current while providing a unity-gain bandwidth of 200MHz and a slew rate of 4100V/μs. The LM7171 also has other great features such as low differential gain and phase and high output current.

The LM7171 is a true VFA. Unlike a current-feedback amplifier (CFA) with a low inverting input impedance and a high noninverting input impedance, both inputs of a VFA have high-impedance nodes. The low-impedance inverting input of a CFA and a feedback capacitor create an additional pole that leads to instability. As a result, CFAs cannot be used in traditional op-amp circuits such as photodiode amplifiers, I-to-V converters, and integrators, where a feedback capacitor is required.

6.1.1 Circuit Operation

The class AB input stage in LM7171 is fully symmetrical and has a similar slewing characteristic to a CFA. In the LM7171 simplified schematic, Q1 through Q4 form the equivalent of the current-feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

6.1.2 Slew Rate Characteristic

The slew rate of LM7171 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations. A curve of slew rate versus input voltage level is provided in 节 *5.8*.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external resistor such as 1kΩ in series with the input of LM7171, the bandwidth is reduced to help lower the overshoot.

6.1.2.1 Slew-Rate Limitation

If the amplifier input signal amplitude is too large and the frequency too high, the amplifier is slew-rate limited. This limiting can cause ringing in the time domain and peaking in the frequency domain at the output of the amplifier.

For the A_V = +2 curves, slight peaking occurs. This peaking at high frequency (> 100MHz) is due to a large input signal at a high enough frequency that exceeds the amplifier slew rate. The peaking in the frequency response does not limit the pulse response in the time domain, and the LM7171 is stable with a noise gain of ≥ +2.

6.1.3 Compensation for Input Capacitance

The combination of an amplifier input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value of

$$C_F > (R_G \times C_{IN}) / R_F \quad (1)$$

can be used to cancel that pole. For LM7171, a feedback capacitor of 2pF is recommended. 图 6-1 illustrates the compensation circuit.

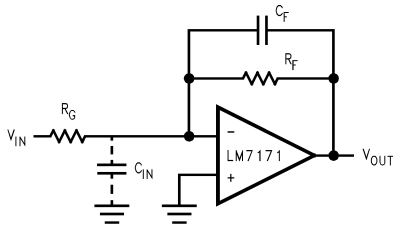


图 6-1. Compensating for Input Capacitance

6.2 Typical Applications

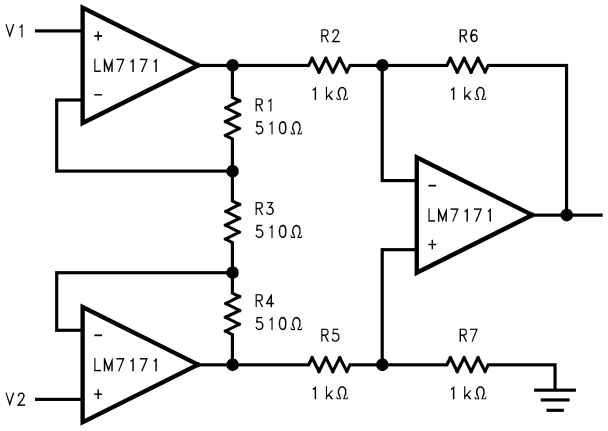


图 6-2. Fast Instrumentation Amplifier

$$V_{IN} = V_2 - V_1$$
$$\text{if R6} = \text{R2, R7} = \text{R5, and R1} = \text{R4}$$
$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

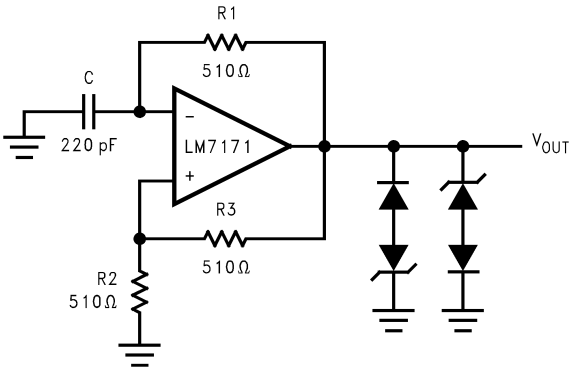


图 6-3. Multivibrator

$$f = \frac{1}{2\left(R1\,C\ln\left(1 + 2\frac{R2}{R3}\right)\right)}$$

$f = 4\ MHz$

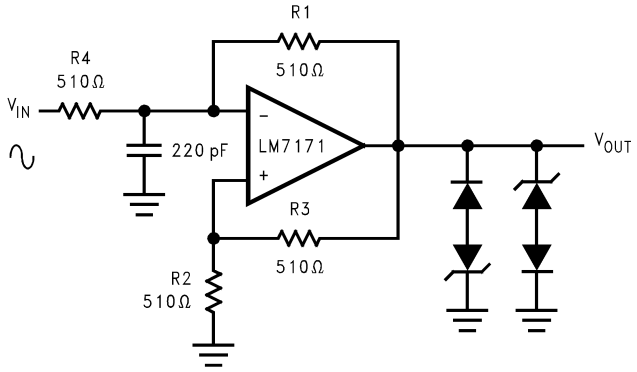


图 6-4. Pulse Width Modulator

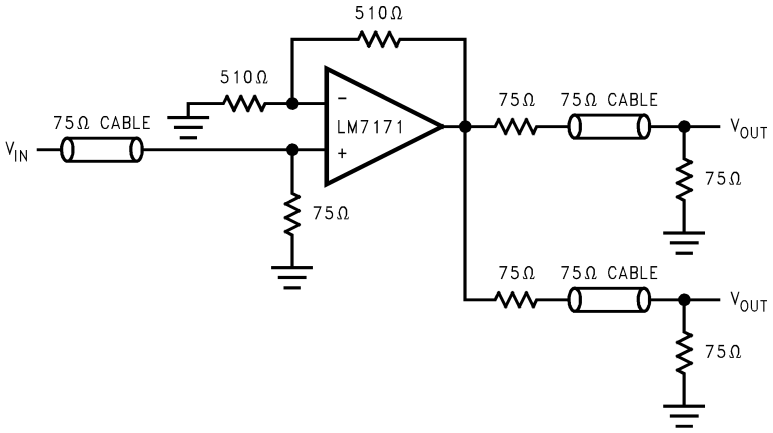


图 6-5. Video Line Driver

6.3 Power Supply Recommendations

6.3.1 Power-Supply Bypassing

Bypassing the power supply is necessary to maintain low power-supply impedance across frequency. To bypass both positive and negative power supplies individually, place 0.01 µF ceramic capacitors directly to the power-supply pins, and 2.2 µF tantalum capacitors close to the power-supply pins.

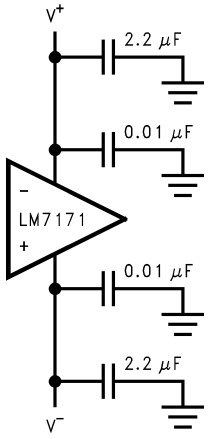


图 6-6. Power-Supply Bypassing

6.3.2 Termination

In high-frequency applications, reflections occur if signals are not properly terminated. 图 6-7 shows a properly terminated signal while 图 6-8 shows an improperly terminated signal.

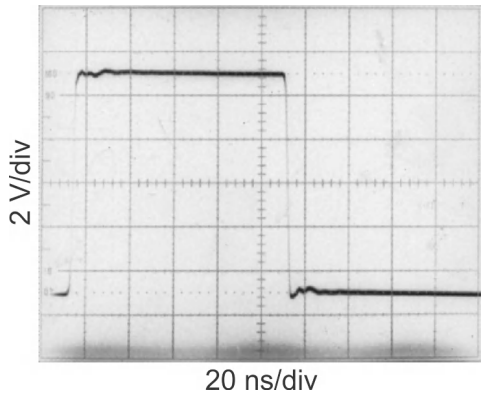


图 6-7. Properly Terminated Signal

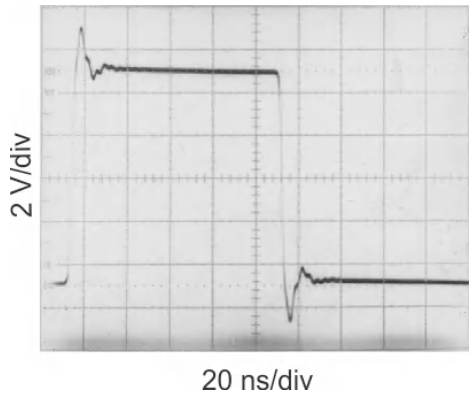


图 6-8. Improperly Terminated Signal

To minimize reflection, use coaxial cable with matching characteristic impedance to the signal source. Terminate the other end of the cable with the same-value terminator or resistor. For commonly used cables, RG59 has a 75Ω characteristic impedance, and RG58 has a 50Ω characteristic impedance.

6.3.3 Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, place an isolation resistor as shown in 图 6-9. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM7171, a 50Ω isolation resistor is recommended for initial evaluation. 图 6-10 shows the LM7171 driving a 150pF load with the 50Ω isolation resistor.

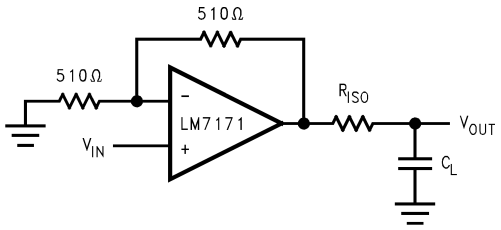


图 6-9. Isolation Resistor Used to Drive Capacitive Load

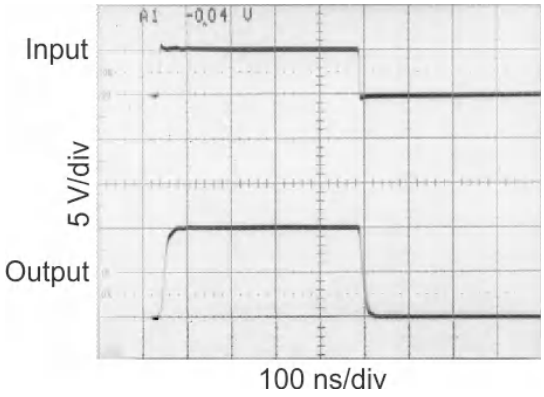


图 6-10. The LM7171 Driving a 150pF Load With a 50Ω Isolation Resistor

6.3.4 Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (2)$$

where

- P_D is the power dissipation in a device
- $T_{J(max)}$ is the maximum junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the thermal resistance of a particular package

For example, for the LM7171 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 730mW.

Thermal resistance, $R_{\theta JA}$, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher $R_{\theta JA}$ becomes. The 8-pin DIP package has a lower thermal resistance (108°C/W) than that of 8-pin SOIC (172°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

where

- P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; P_L is not the power dissipated by the load.

  Furthermore,
- P_Q is the supply current × total supply voltage with no load
- P_L is the output current × (voltage difference between supply voltage and output voltage of the same side of supply voltage)

For example, the total power dissipated by the LM7171 with V_S = ±15V and output voltage of 10V into 1kΩ is

$$P_D = P_Q + P_L \quad (4)$$

$$= (6.5mA) \times (30V) + (10mA) \times (15V - 10V) \quad (5)$$

$$= 195mW + 50mW \quad (6)$$

$$= 245mW \quad (7)$$

6.4 Layout

6.4.1 Layout Guidelines

6.4.1.1 Printed Circuit Board and High-Speed Op Amps

There are many things to consider when designing printed circuit boards (PCBs) for high-speed op amps. Without proper caution, excessive ringing, oscillation, and other degraded ac performance can easily occur in high-speed circuits. As a rule, keep signal traces short and wide to provide low inductance and low impedance paths. Ground any unused board space to reduce stray signal pickup. Ground critical components at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect high-frequency performance. Soldering the amplifier directly into the PCB without using any socket is better.

6.4.1.2 Using Probes

Active (FET) probes are an excellent choice for taking high-frequency measurements because of the wide bandwidth, high input impedance, and low input capacitance. However, the probe ground leads provide a long ground loop that produces errors in measurement. Instead, ground the probes directly by removing the ground leads and probe jackets and using scope probe jacks.

6.4.1.3 Component Selection and Feedback Resistor

In high-speed applications, keep all component leads short. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface-mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects. such as ringing or oscillation in high-speed amplifiers. For LM7171, a feedback resistor of 510Ω gives optimized performance.

7 Device and Documentation Support

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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7.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (September 2014) to Revision D (February 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 更新了*封装信息*	1
• Deleted footnote from *Recommended Operating Conditions*	3
• Changed DC and AC specifications tables to *Electrical Characteristics: ±15V*	4
• Changed LM7171A unity-gain bandwidth from 200MHz to 160MHz	4
• Changed LM7171A settling time from 42ns to 16ns	4
• Changed LM7171 A Input-referred voltage noise from 14nV/ √Hz to 8.5nV/ √Hz	4
• Changed LM7171 A Input-referred current noise from 1.5pA/ √Hz to 1pA/ √Hz	4
• Changed DC and AC specifications tables to *Electrical Characteristics: ±5V*	6
• Changed LM7171A slew rate from 950V/µs to 1200V/µs	6
• Changed LM7171A phase margin from 57° to 68°	6
• Changed LM7171A settling time from 56ns to 15ns	6
• Changed LM7171A propagation delay from 6ns to 2.5ns	6
• Changed LM7171A input-referred voltage noise from 14nV/ √Hz to 8.5nV/ √Hz	6
• Changed LM7171A input-referred current noise from 1.8pA/ √Hz to 1pA/ √Hz	6
• Added new *Typical Characteristics* section for LM7171A	9
• Deleted second paragraph in *Slew-Rate Limitation*	25

Changes from Revision B (March 2013) to Revision C (September 2014)	Page
• 更改了数据表流程和布局，以符合新的 TI 新标准。添加了以下部分：器件信息表、应用和实施；布局；器件和文档支持；机械、封装和可订购信息	1

Changes from Revision A (March 2013) to Revision B (March 2013)	Page
• Changed layout of National Data Sheet to TI format	26

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM7171AIM/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LM71 71AIM	
LM7171AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L71AIM, LM71) 71AIM	Samples
LM7171BIM/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LM71 71BIM	
LM7171BIMX/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LM71 71BIM	
LM7171BIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM7171 BIN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

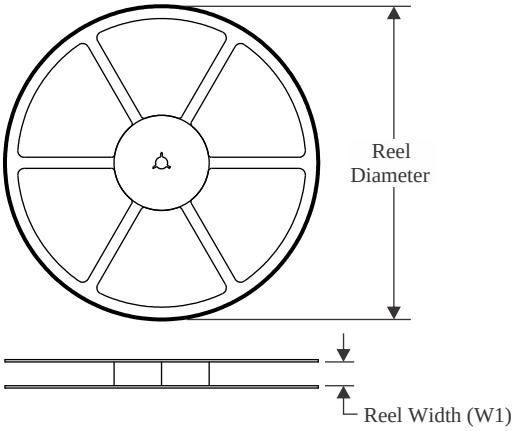
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

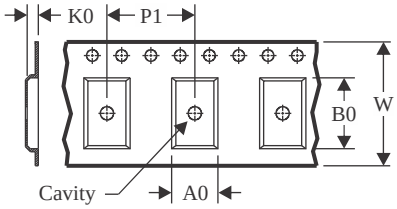
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

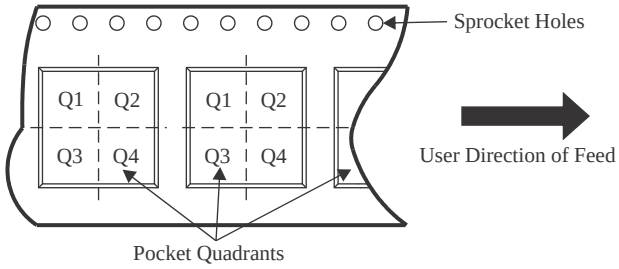


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

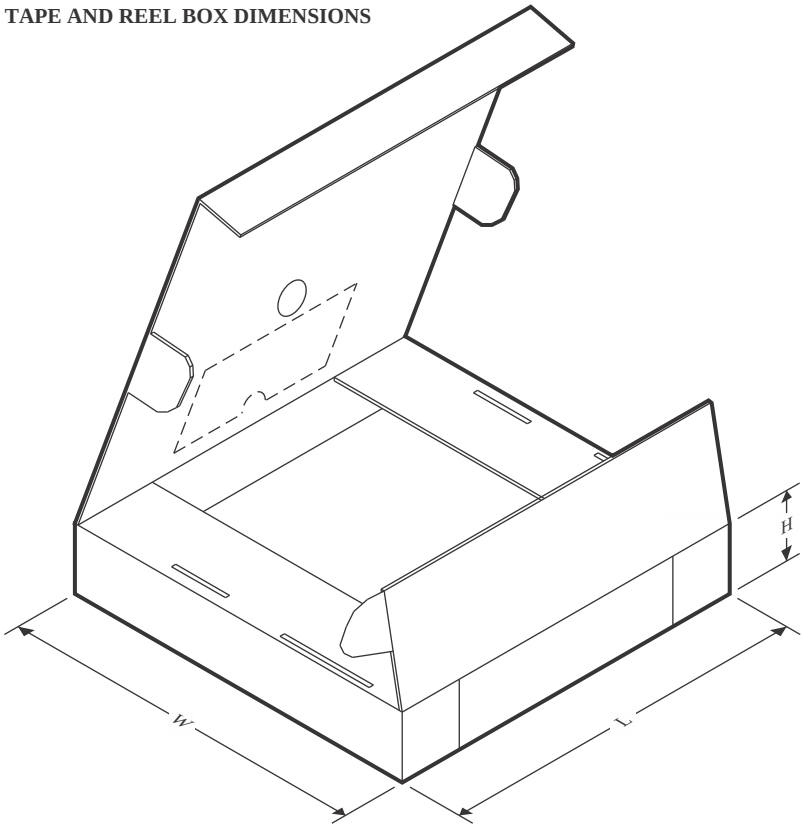
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7171AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

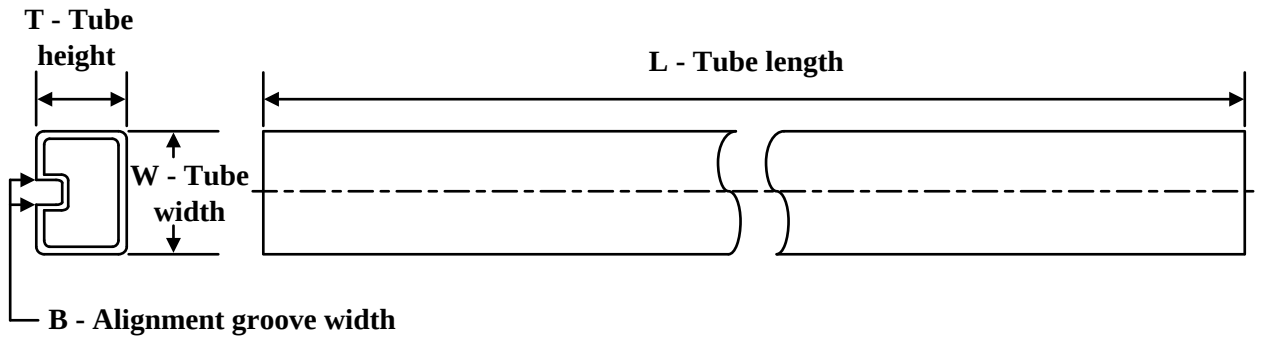
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

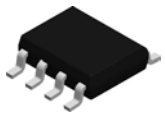
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7171AIMX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM7171BIN/NOPB	P	PDIP	8	40	502	14	11938	4.32

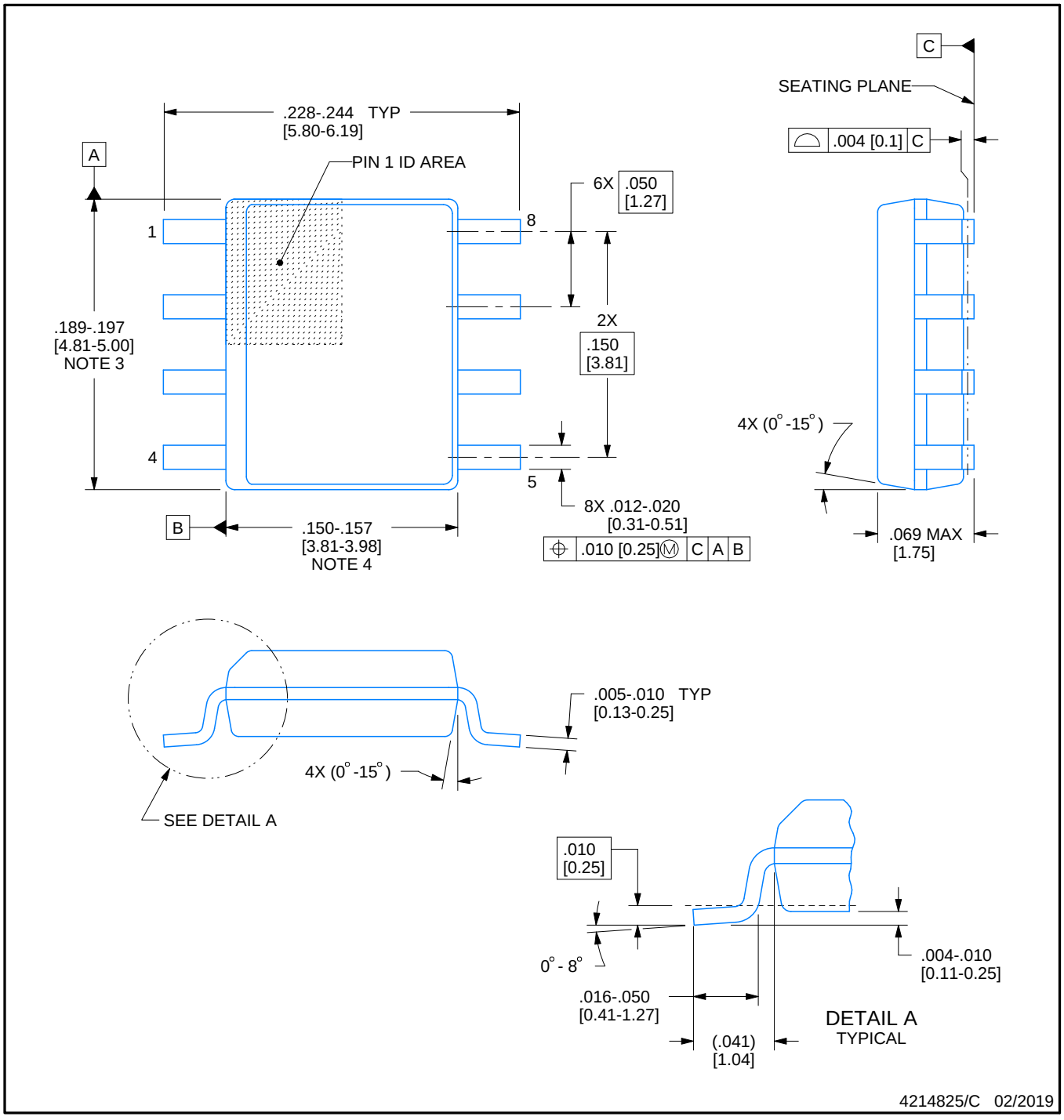


PACKAGE OUTLINE

D0008A

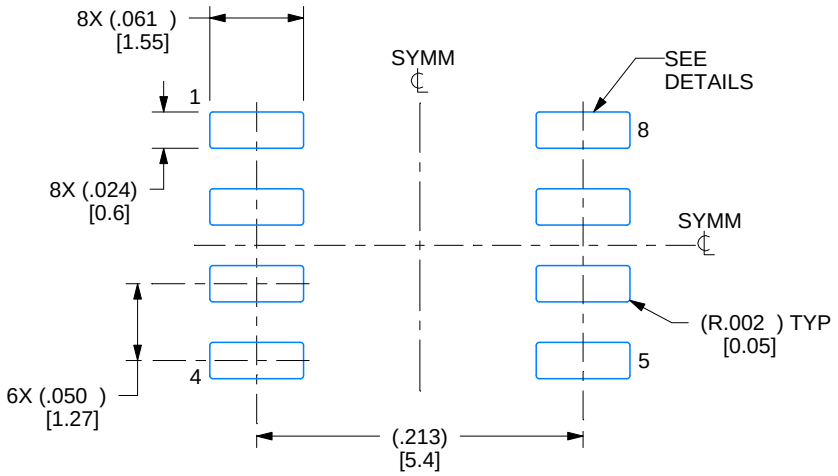
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

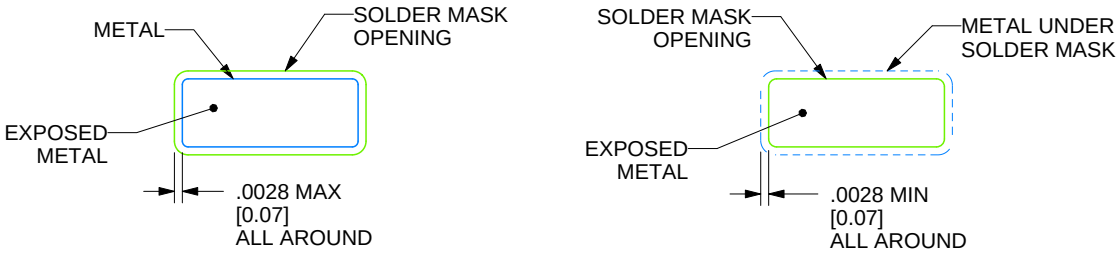


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

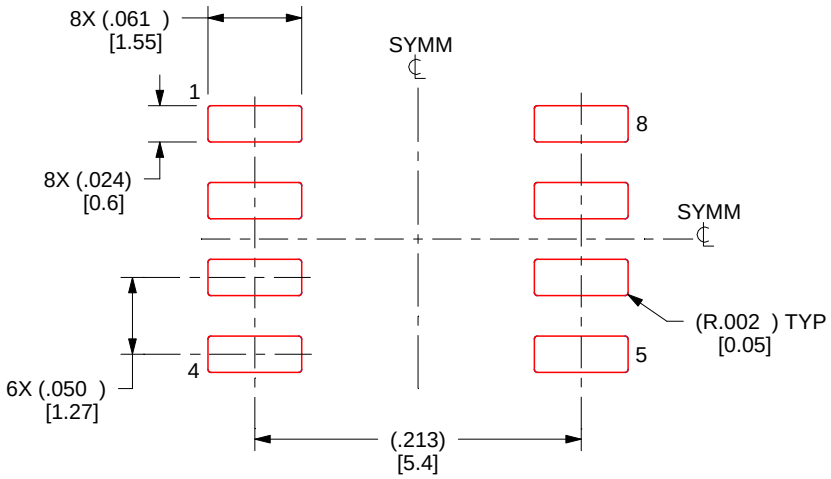
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



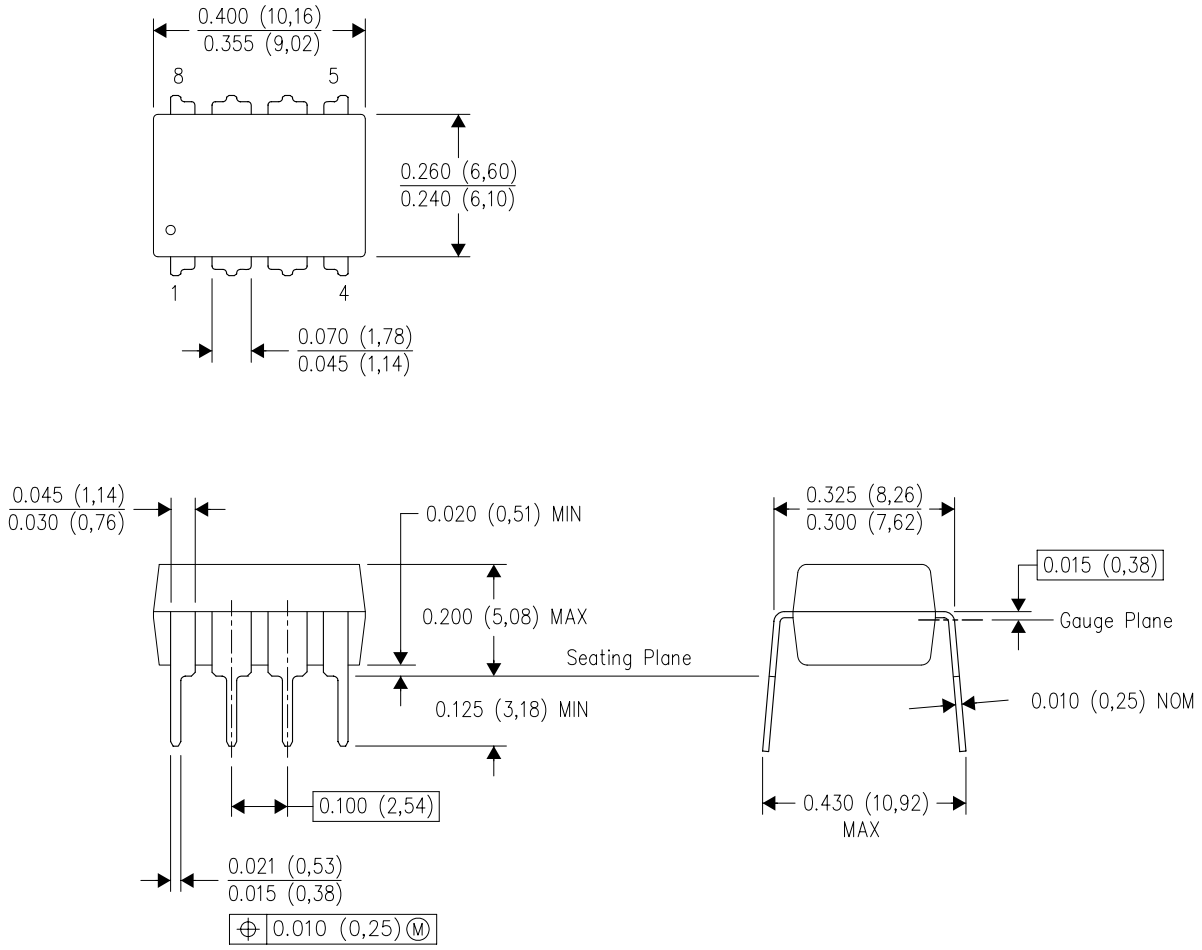
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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