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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
September 2021	*	Initial Release

5 Pin Configuration and Functions

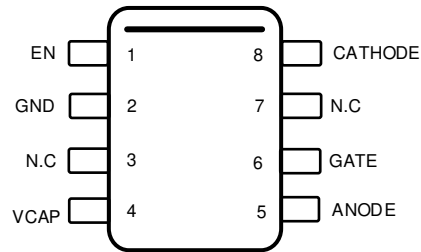


图 5-1. DDF Package 8-Pin SOT-23 Top View

表 5-1. Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	EN	I	Enable pin. Can be connected to ANODE for always ON operation.
2	GND	G	Ground pin
3	N.C		No connection. Keep this pin floating.
4	VCAP	O	Charge pump output. Connect to external charge pump capacitor.
5	ANODE	I	Anode of the diode and input power. Connect to the source of the external N-channel MOSFET.
6	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
7	N.C		No connection. Keep this pin floating.
8	CATHODE	I	Cathode of the diode. Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input Pins	ANODE to GND	- 65	65	V
	EN to GND, $V_{(ANODE)} > 0$ V	- 0.3	65	V
	EN to GND, $V_{(ANODE)} \leq 0$ V	$V_{(ANODE)}$	$(65 + V_{(ANODE)})$	V
Output Pins	GATE to ANODE	- 0.3	15	V
	VCAP to ANODE	- 0.3	15	V
Output to Input Pins	CATHODE to ANODE	- 5	75	V
Operating junction temperature ⁽²⁾		- 55	150	°C
Storage temperature, T_{stg}		- 55	150	°C

- (1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device can not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per JEDEC JS-001 ⁽¹⁾	±2000	V	
		Charged device model (CDM), per JEDEC JS-002 ⁽²⁾	Corner pins (VCAP, EN, ANODE, CATHODE)		±750
			Other pins		±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP155 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
Input Pins	ANODE to GND	- 60		60	V
	CATHODE to GND			60	
	EN to GND	- 60		60	
Input to Output pins	ANODE to CATHODE	- 70			V
External capacitance	ANODE	22			nF
	CATHODE, VCAP to ANODE	0.1			µF
External MOSFET max V_{GS} rating	GATE to ANODE	15			V
T_J	Operating junction temperature range ⁽²⁾	- 55		125	°C

- (1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see [Electrical Characteristics](#).
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM74700-EP	
		DDF (SOT)	
		8 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

$T_J = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $V_{(ANODE)} = 12\text{ V}$, $C_{(VCAP)} = 0.1\ \mu\text{F}$, $V_{(EN)} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ANODE} SUPPLY VOLTAGE						
$V_{(ANODE)}$	Operating input voltage		4		60	V
$V_{(ANODE\ POR)}$	VANODE POR Rising threshold				3.9	V
	VANODE POR Falling threshold		2.2	2.8	3.1	V
$V_{(ANODE\ POR(Hys))}$	VANODE POR Hysteresis		0.39		0.7	V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)} = 0\text{ V}$		0.9	1.5	μA
$I_{(Q)}$	Operating Quiescent Current			80	140	μA
		$V_{ANODE} = 28\text{ V}$		80	150	μA
ENABLE INPUT						
$V_{(EN_IL)}$	Enable input low threshold		0.5	0.9	1.22	V
$V_{(EN_IH)}$	Enable input high threshold		1.06	2	2.6	
$V_{(EN_Hys)}$	Enable Hysteresis		0.52		1.42	V
$I_{(EN)}$	Enable sink current	$V_{(EN)} = 12\text{ V}$		3	5	μA
V_{ANODE} to V_{CATHODE}						
$V_{(AK\ REG)}$	Regulated Forward $V_{(AK)}$ Threshold		13	20	30	mV
		$V_{ANODE} = 28\text{ V}$	13	20	30	mV
$V_{(AK)}$	$V_{(AK)}$ threshold for full conduction mode		34	55	70	mV
$V_{(AK\ REV)}$	$V_{(AK)}$ threshold for reverse current blocking		-17	-11	-5	mV
		$V_{ANODE} = 28\text{ V}$	-17	-11	-5	mV
Gm	Regulation Error AMP Transconductance ⁽¹⁾		440	1800	4900	$\mu\text{A/V}$
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(ANODE)} - V_{(CATHODE)} = 100\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$	3	11		mA
	Peak sink current	$V_{(ANODE)} - V_{(CATHODE)} = -20\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$		2370		mA
	Regulation max sink current	$V_{(ANODE)} - V_{(CATHODE)} = 0\text{ V}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$	2	26		μA
RDS_{ON}	discharge switch RDS_{ON}	$V_{(ANODE)} - V_{(CATHODE)} = -20\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 100\text{ mV}$	0.4		2	Ω
CHARGE PUMP						

6.5 Electrical Characteristics (continued)

$T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$; typical values at $T_J = 25^\circ\text{C}$, $V_{(ANODE)} = 12\text{ V}$, $C_{(VCAP)} = 0.1\ \mu\text{F}$, $V_{(EN)} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(VCAP)}$	Charge Pump source current (Charge pump on)	$V_{(VCAP)} - V_{(ANODE)} = 7\text{ V}$	162	300	600	μA
	Charge Pump sink current (Charge pump off)	$V_{(VCAP)} - V_{(ANODE)} = 14\text{ V}$		5	10	μA
$V_{(VCAP)} - V_{(ANODE)}$	Charge pump voltage at $V_{(ANODE)} = 3.2\text{ V}$	$I_{(VCAP)} \leq 30\ \mu\text{A}$	8			V
	Charge pump turn on voltage		10.4	11.6	12.9	V
	Charge pump turn off voltage		11	12.4	13.9	V
	Charge Pump Enable comparator Hysteresis		0.54	0.8	1.36	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} - V_{(ANODE)}$ UV release at rising edge	$V_{(ANODE)} - V_{(CATHODE)} = 100\text{ mV}$	5.6	6.6	8.7	V
	$V_{(VCAP)} - V_{(ANODE)}$ UV threshold at falling edge	$V_{(ANODE)} - V_{(CATHODE)} = 100\text{ mV}$	5.05	5.4	6	V
CATHODE						
$I_{(CATHODE)}$	CATHODE sink current	$V_{(ANODE)} = 12\text{ V}$, $V_{(ANODE)} - V_{(CATHODE)} = -100\text{ mV}$		1.2	2	μA
		$V_{(ANODE)} - V_{(CATHODE)} = -100\text{ mV}$		1.6	2.2	μA
		$V_{(ANODE)} = -12\text{ V}$, $V_{(CATHODE)} = 12\text{ V}$		1.25	2.06	μA

(1) Parameter guaranteed by design and characterization

6.6 Switching Characteristics

$T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$; typical values at $T_J = 25^\circ\text{C}$, $V_{(ANODE)} = 12\text{ V}$, $C_{(VCAP)} = 0.1\ \mu\text{F}$, $V_{(EN)} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to Gate Turn On delay	$V_{(VCAP)} > V_{(VCAP\ UVLOR)}$		75	110	μs
$t_{\text{Reverse delay}}$	Reverse voltage detection to Gate Turn Off delay	$V_{(ANODE)} - V_{(CATHODE)} = 100\text{ mV}$ to -100 mV		0.45	0.75	μs
		$V_{(ANODE)} = 28\text{ V}$, $V_{(ANODE)} - V_{(CATHODE)} = 100\text{ mV}$ to -100 mV		0.45	0.75	μs
$t_{\text{Forward recovery}}$	Forward voltage detection to Gate Turn On delay	$V_{(ANODE)} - V_{(CATHODE)} = -100\text{ mV}$ to 700 mV		1.4	3.1	μs
		$V_{(ANODE)} = 28\text{ V}$, $V_{(ANODE)} - V_{(CATHODE)} = -100\text{ mV}$ to 700 mV		1.4	2.6	μs

6.7 Typical Characteristics

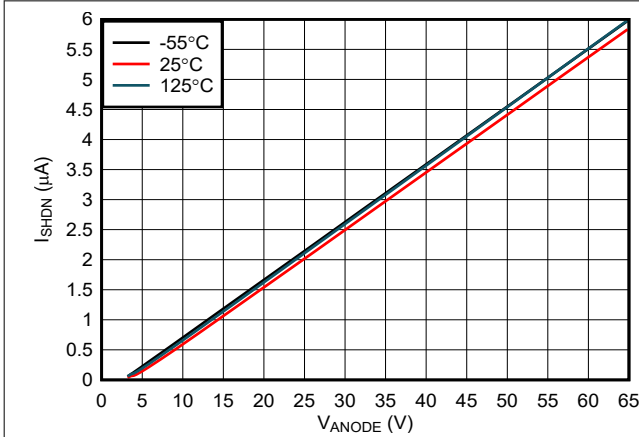


图 6-1. Shutdown Supply Current vs Supply Voltage

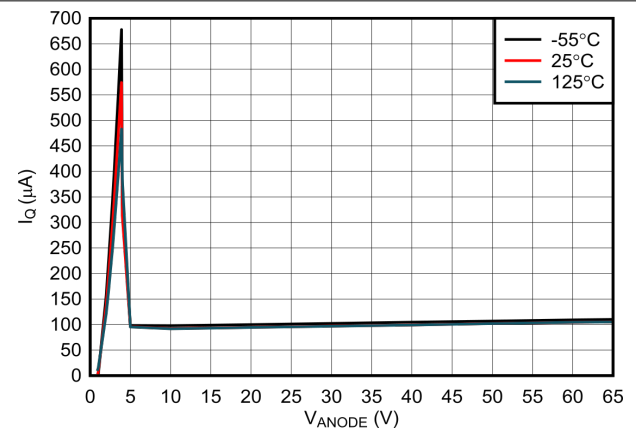


图 6-2. Operating Quiescent Current vs Supply Voltage

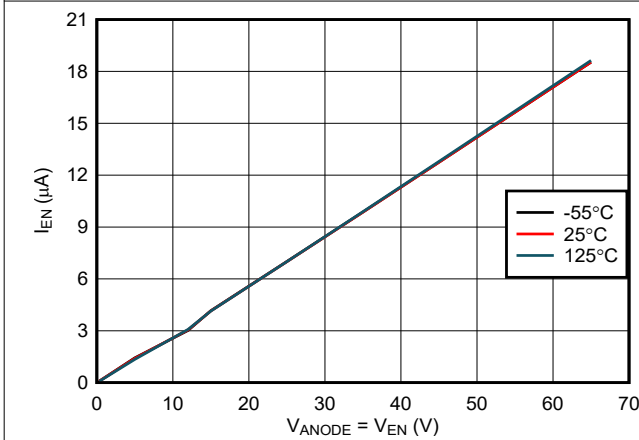


图 6-3. Enable Sink Current vs Supply Voltage

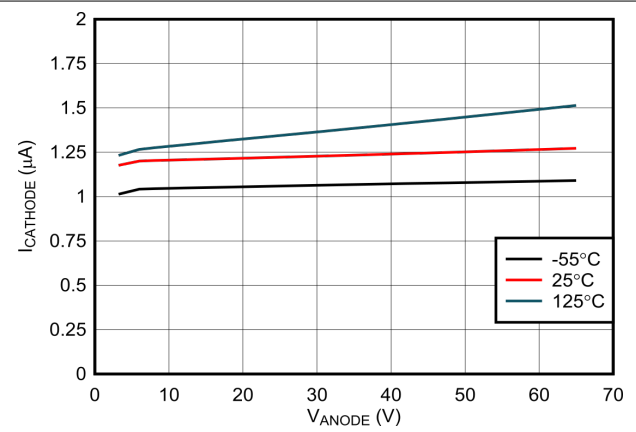


图 6-4. Cathode Sink Current vs Supply Voltage

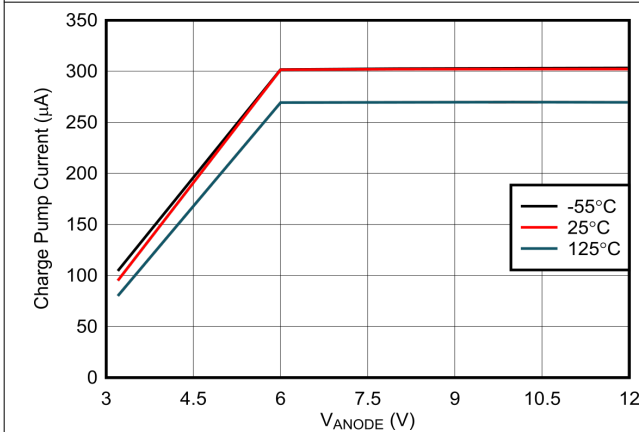


图 6-5. Charge Pump Current vs Supply Voltage at VCAP = 6 V

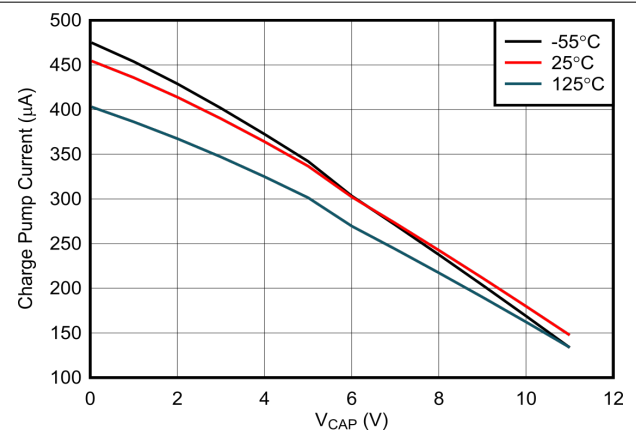


图 6-6. Charge Pump V-I Characteristics at VANODE >= 12 V

6.7 Typical Characteristics (continued)

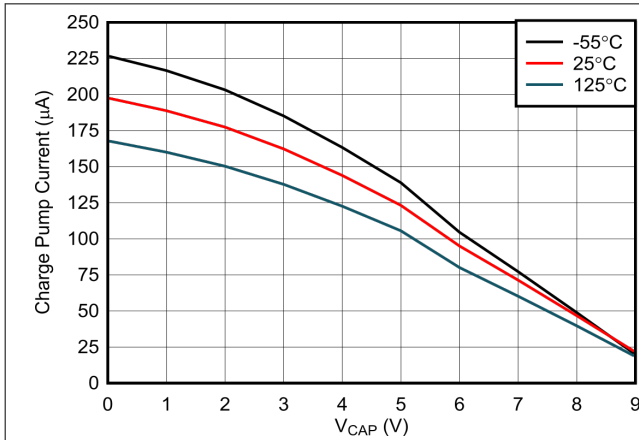


图 6-7. Charge Pump V-I Characteristics at VANODE = 3.2 V

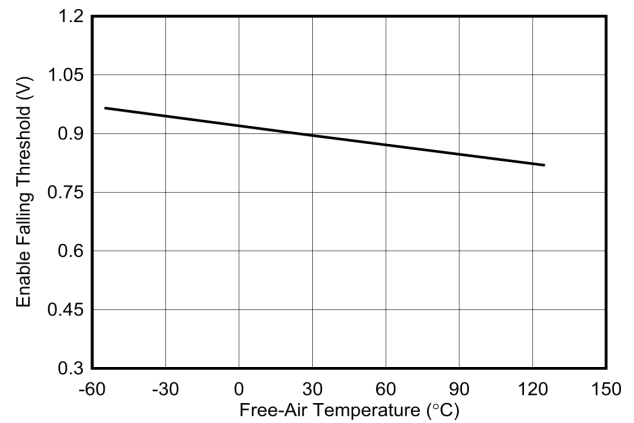


图 6-8. Enable Falling Threshold vs Temperature

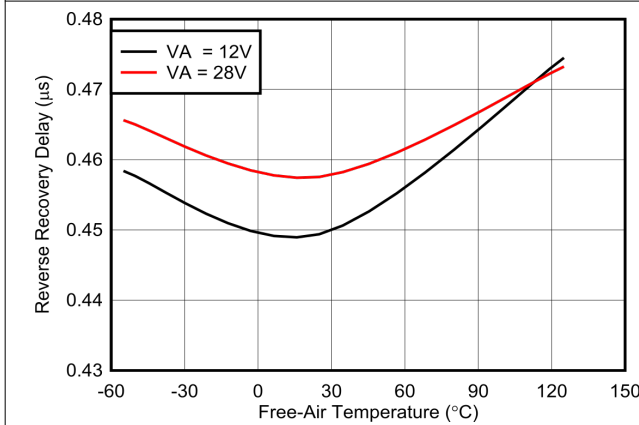


图 6-9. Reverse Current Blocking Delay vs Temperature

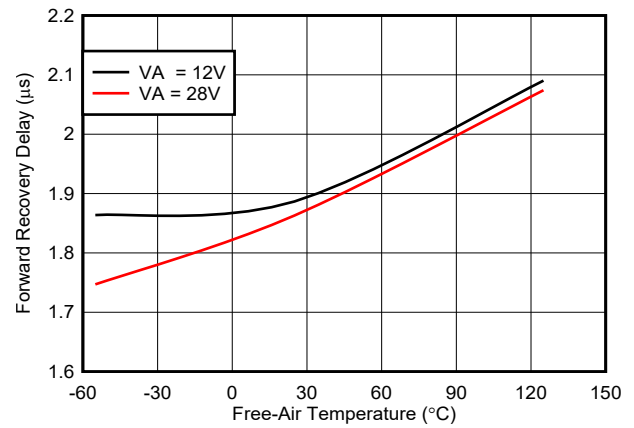


图 6-10. Forward Recovery Delay vs Temperature

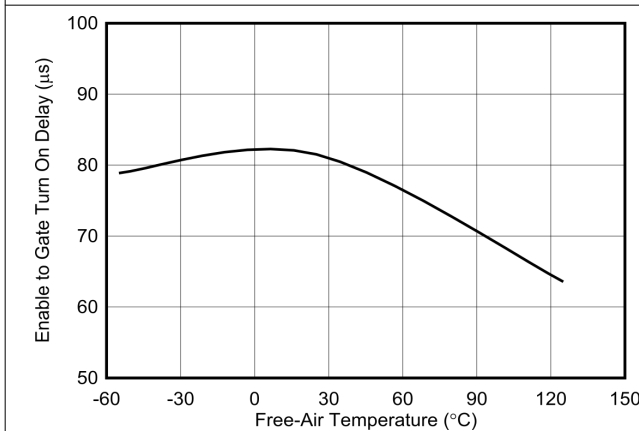


图 6-11. Enable to Gate Delay vs Temperature

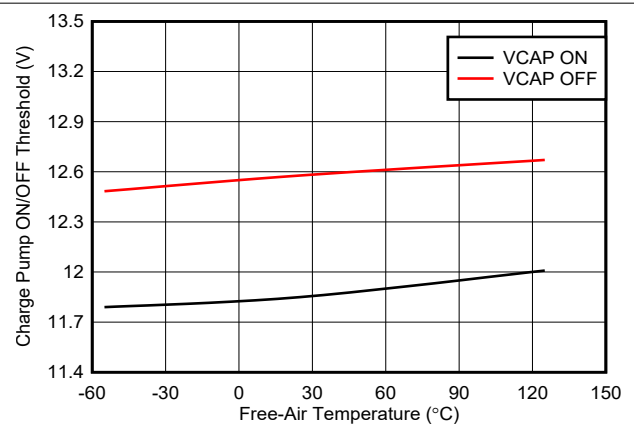


图 6-12. Charge Pump ON/OFF Threshold vs Temperature

6.7 Typical Characteristics (continued)

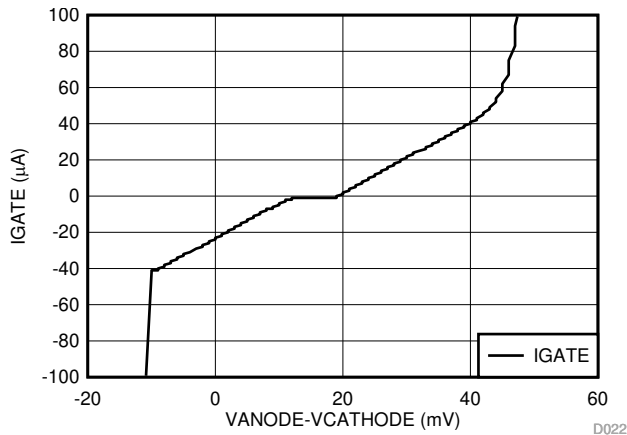


图 6-13. Gate Current vs Forward Voltage Drop

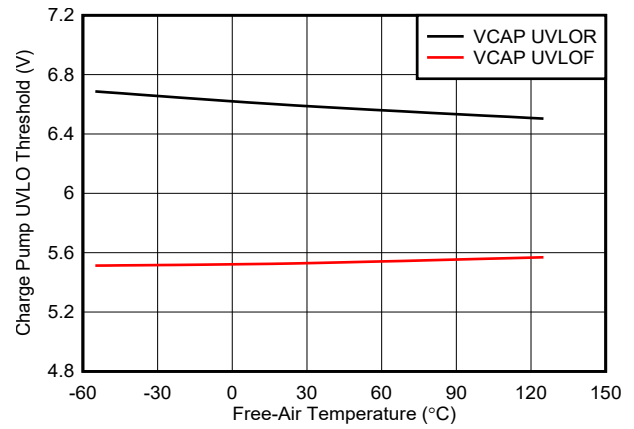


图 6-14. Charge Pump UVLO Threshold vs Temperature

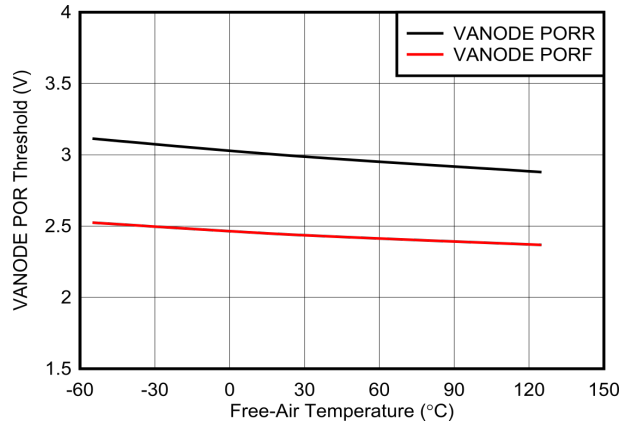


图 6-15. VANODE POR Threshold vs Temperature

7 Parameter Measurement Information

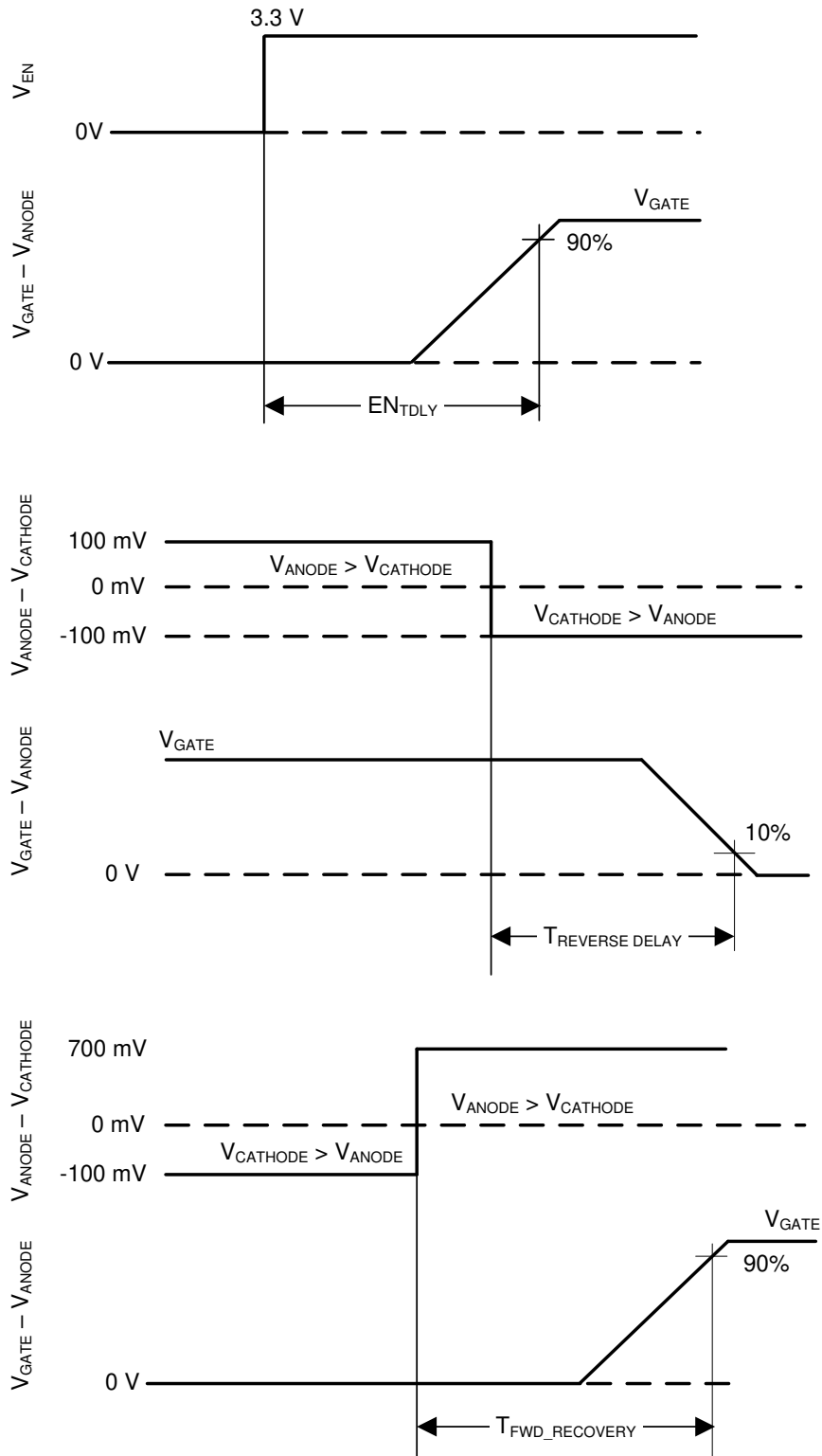


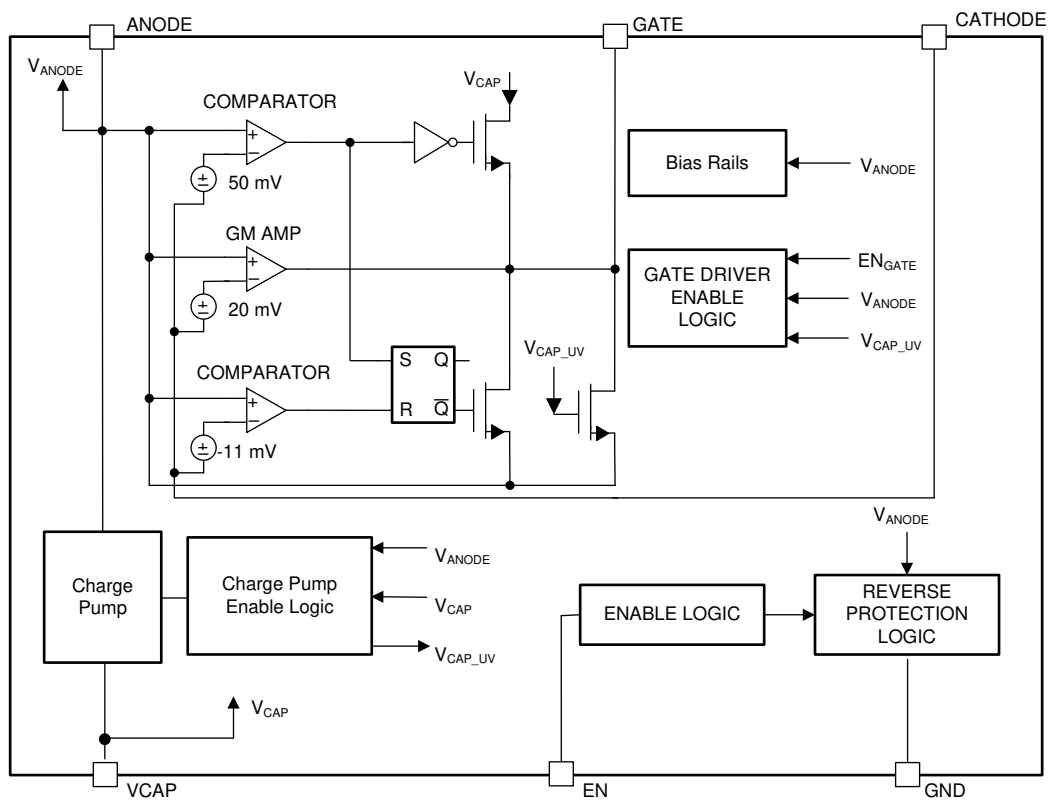
图 7-1. Timing Waveforms

8 Detailed Description

8.1 Overview

The LM74700-EP ideal diode controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit or be used in an ORing configuration while minimizing the number of external components. This easy to use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes, such as a P-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate drive voltage of approximately 15 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and GATE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20 mV. This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below -11 mV, resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN, is available to place the LM74700-EP in shutdown mode, disabling the N-Channel MOSFET and minimizing the quiescent current.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Voltage

The ANODE pin is used to power the LM74700-EP's internal circuitry, typically drawing 80 μA when enabled and 1 μA when disabled. If the ANODE pin voltage is greater than the POR Rising threshold, then LM74700-EP operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65 V to -65 V, allowing the LM74700-EP to withstand negative voltage transients.

8.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and ANODE pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor the EN pin voltage must be above the specified input high threshold, $V_{(EN_IH)}$. When enabled the charge pump sources a charging current of 300- μA typical. If EN pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to ANODE voltage must be above the undervoltage lockout threshold, typically 6.5 V, before the internal gate driver is enabled. Use [方程式 1](#) to calculate the initial gate driver enable delay.

$$T_{(DRV_EN)} = 75 \mu\text{s} + C_{(VCAP)} \times \frac{V_{(VCAP_UVLOR)}}{300 \mu\text{A}} \quad (1)$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across ANODE and VCAP pins
- $V_{(VCAP_UVLOR)} = 6.5 \text{ V}$ (typical)

To remove any chatter on the gate drive, approximately 800 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to ANODE voltage reaches 12.4 V, typically, at which point the charge pump is disabled decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCAP to ANODE voltage is below to 11.6-V typically, at which point the charge pump is enabled. The voltage between VCAP and ANODE continue to charge and discharge between 11.6 V and 12.4 V as shown in [图 8-1](#). By enabling and disabling the charge pump, the operating quiescent current of the LM74700-EP is reduced. When the charge pump is disabled it sinks to 5- μA typical.

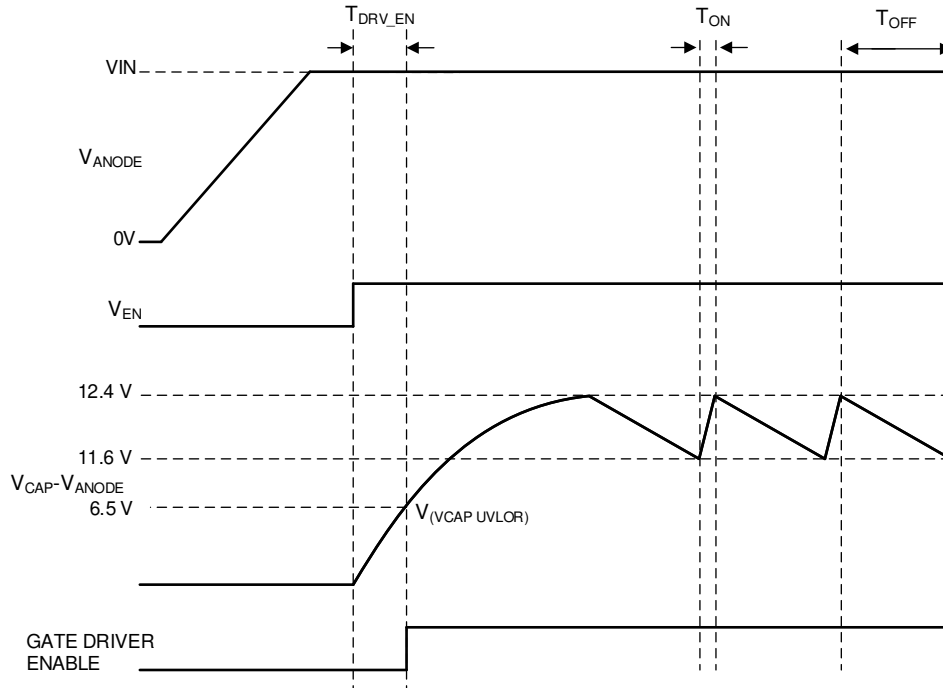


图 8-1. Charge Pump Operation

8.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are three defined modes of operation that the gate driver operates under forward regulation, full conduction mode and reverse current protection, according to the ANODE to CATHODE voltage. Forward regulation mode, full conduction mode and reverse current protection mode are described in more detail in the [Regulated Conduction Mode](#), [Full Conduction Mode](#) and [Reverse Current Production Mode](#) sections. 图 8-2 depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74700-EP. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is -11 mV.

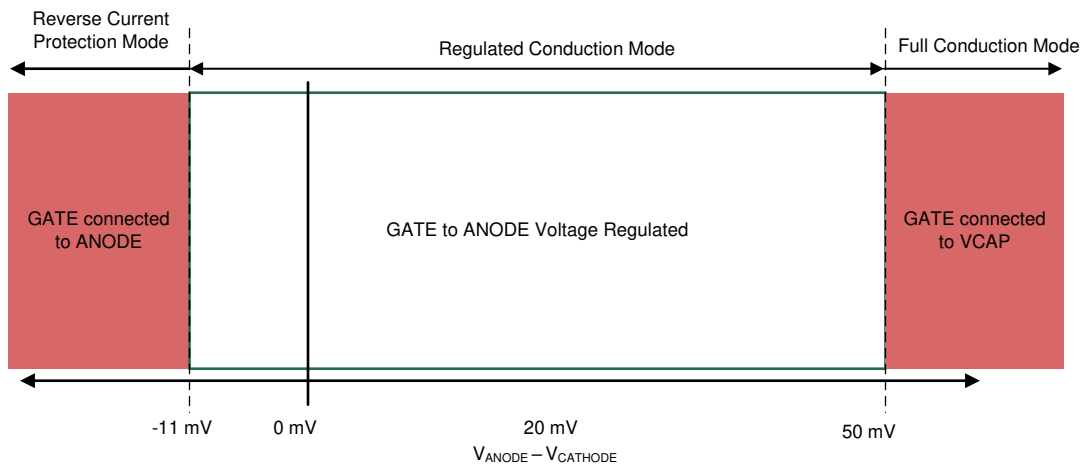


图 8-2. Gate Driver Mode Transitions

Before the gate driver is enabled, the following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to ANODE voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than VANODE POR Rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. Once these conditions are achieved, the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

8.3.4 Enable

The LM74700-EP has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in [Gate Driver](#) and [Charge Pump](#) sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74700-EP in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as -65 V. This ability allows for the EN pin to connect directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 3 μ A pulls EN pin low and disables the device.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The LM74700-EP enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74700-EP enters low I_Q operation with the ANODE pin only sinking 1 μ A. When the LM74700-EP is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET's body diode.

8.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE voltage of the LM74700-EP. Each of the three modes is described in the [Regulated Conduction Mode](#), [Full Conduction Mode](#) and [Reverse Current Protection Mode](#) sections.

8.4.2.1 Regulated Conduction Mode

For the LM74700-EP to operate in regulated conduction mode, the gate driver must be enabled as described in the [Gate Driver](#) section, and the current from source to drain of the external MOSFET must be within the range to result in an ANODE to CATHODE voltage drop of -11 mV to 50 mV. During forward regulation mode, the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. This closed loop regulation scheme enables graceful turn off of the MOSFET at very light loads and ensures zero DC reverse current flow.

8.4.2.2 Full Conduction Mode

For the LM74700-EP to operate in full conduction mode, the gate driver must be enabled as described in the [Gate Driver](#) section. The current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50-mV typical. If these conditions are achieved, the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFETs, $R_{DS(ON)}$ is minimized, reducing the power loss of the external MOSFET when forward currents are large.

8.4.2.3 Reverse Current Protection Mode

For the LM74700-EP to operate in reverse current protection mode, the gate driver must be enabled as described in the [Gate Driver](#) section, and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is typically less than -11 mV, reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LM74700-EP is used with N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in 图 9-1, where the LM74700-EP is used in series with a battery to drive the MOSFET Q1. The TVS is not required for the LM74700-EP to operate, but they are used to clamp the positive and negative voltage surges. The output capacitor, C_{OUT} , is recommended to protect the immediate output voltage collapse as a result of line disturbance.

9.2 Typical Application

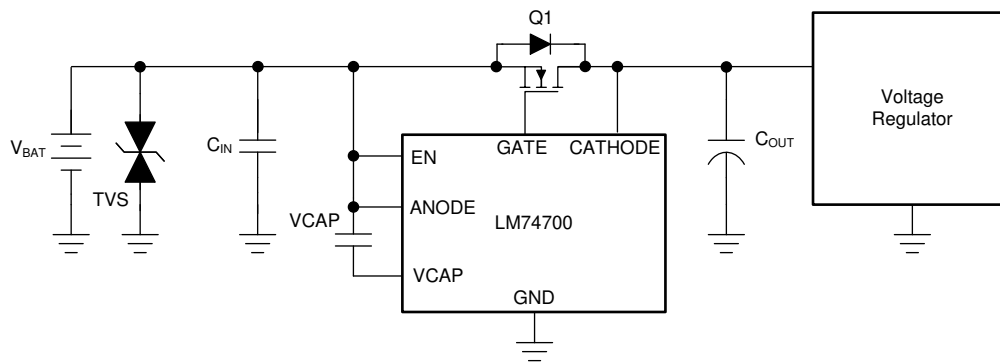


图 9-1. Typical Application Circuit

9.2.1 Design Requirements

A design example, with system design parameters, is listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V battery, 12-V nominal with 3.2-V cold crank and 35-V load dump
Output voltage	3.2 V during cold crank to 35-V load dump
Output current range	3-A nominal, 6-A maximum
Output capacitance	1- μ F minimum, 220- μ F typical hold up capacitance
Automotive EMC compliance	ISO 7637-2 and ISO 16750-2

9.2.2 Detailed Design Procedure

9.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current

9.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current, I_D , the maximum drain-to-source voltage, $V_{DS(MAX)}$, and the maximum source current through body diode and the drain-to-source On resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D , rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. TI recommends to use MOSFETs with voltage rating up to 60-V maximum with the LM74700-EP because anode-cathode maximum voltage is 65 V. The maximum V_{GS} LM74700-EP can drive is 13 V, so a MOSFET with 15-V minimum V_{GS} must be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a zener diode can be used to clamp V_{GS} to safe level. During startup, inrush current flows through the body diode to charge the bulk hold-up capacitors at the output. The maximum source current through the body diode must be higher than the inrush current that can be seen in the application.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ can not always be beneficial. Higher $R_{DS(ON)}$ will provide increased voltage information to LM74700-EP's reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. TI recommends to operate the MOSFET in regulated conduction mode during nominal load conditions and select $R_{DS(ON)}$, such that at nominal operating current, forward voltage drop V_{DS} is close to 20-mV regulation point and not more than 50 mV.

As a guideline, TI suggests to choose $(20 \text{ mV} / I_{Load(Nominal)}) \leq R_{DS(ON)} \leq (50 \text{ mV} / I_{Load(Nominal)})$.

MOSFET manufacturers usually specify $R_{DS(ON)}$ at 4.5-V V_{GS} and 10-V V_{GS} . $R_{DS(ON)}$ increases drastically below 4.5-V V_{GS} and $R_{DS(ON)}$ is highest when V_{GS} is close to MOSFET V_{th} . For stable regulation at light load conditions, TI recommends to operate the MOSFET close to 4.5-V V_{GS} , that is, much higher than MOSFET gate threshold voltage. TI recommends to choose MOSFET gate threshold voltage V_{th} of 2-V to 2.5-V maximum. Choosing a lower V_{th} MOSFET also reduces the turn ON time.

Based on the design requirements, preferred MOSFET ratings are:

- 60-V $V_{DS(MAX)}$ and ± 20 -V $V_{GS(MAX)}$
- $R_{DS(ON)}$ at 3-A nominal current: $(20 \text{ mV} / 3 \text{ A}) \leq R_{DS(ON)} \leq (50 \text{ mV} / 3 \text{ A}) = 6.67 \text{ m}\Omega \leq R_{DS(ON)} \leq 16.67 \text{ m}\Omega$.
- MOSFET gate threshold voltage V_{th} : 2-V maximum

DMT6007LFG MOSFET from Diodes Inc. is selected to meet this 12-V reverse battery protection design requirements and it is rated at:

- 60-V $V_{DS(MAX)}$ and ± 20 -V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 6.5-m Ω typical and 8.5-m Ω maximum rated at 4.5-V V_{GS}
- MOSFET V_{th} : 2-V maximum

Thermal resistance of the MOSFET must be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

9.2.2.3 Charge Pump VCAP, input and output capacitance

Minimum required capacitance for charge pump VCAP and input and output capacitance are:

- VCAP: Minimum 0.1 μF is required; recommended value of VCAP (μF) $\geq 10 \times C_{ISS(MOSFET)}(\mu\text{F})$
- C_{IN} : minimum 22 nF of input capacitance
- C_{OUT} : minimum 100 nF of output capacitance

9.2.3 Selection of TVS Diodes for 12-V Battery Protection Applications

TVS diodes are used in automotive systems for protection against transients. In the 12-V battery protection application circuit shown in [Figure 9-2](#), a bi-directional TVS diode is used to protect from positive and negative

9.2.5 Application Curves

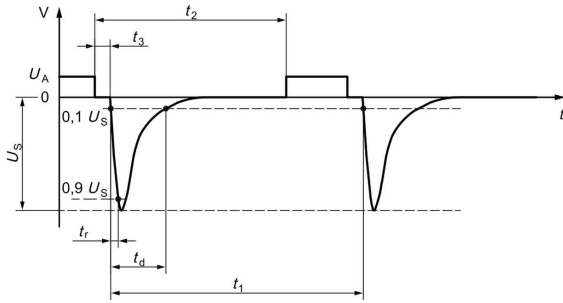
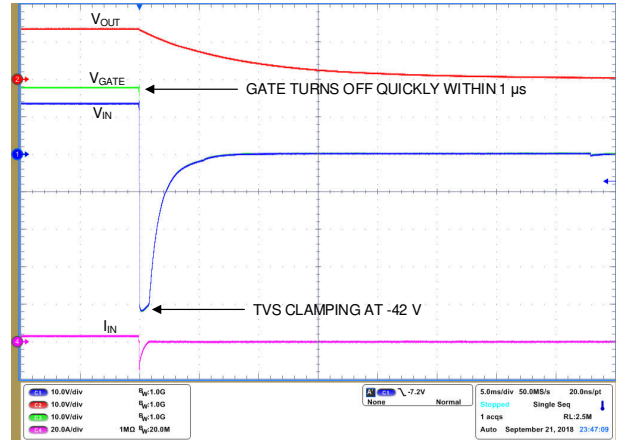
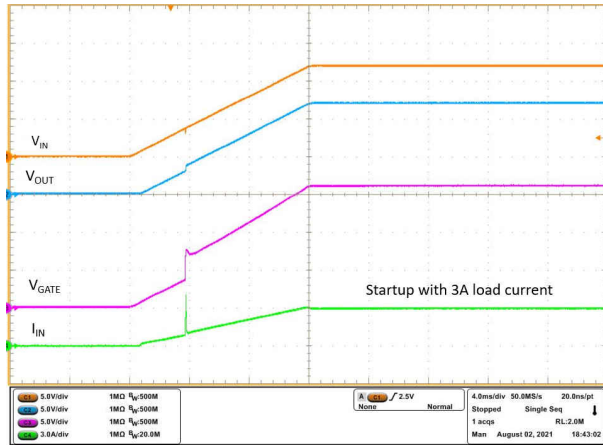


图 9-4. ISO 7637-2 Pulse 1



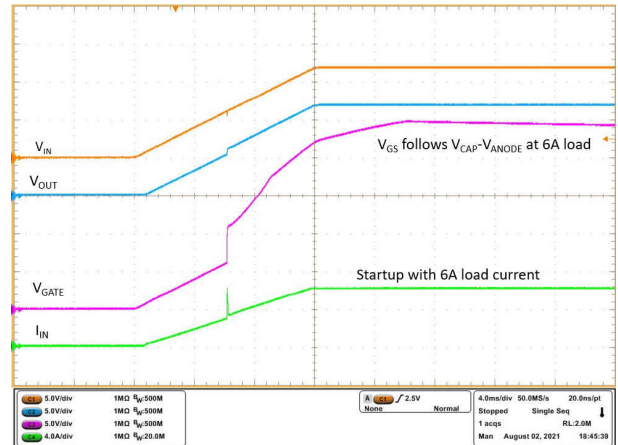
Time (5 ms/DIV)

图 9-5. Response to ISO 7637-2 Pulse 1



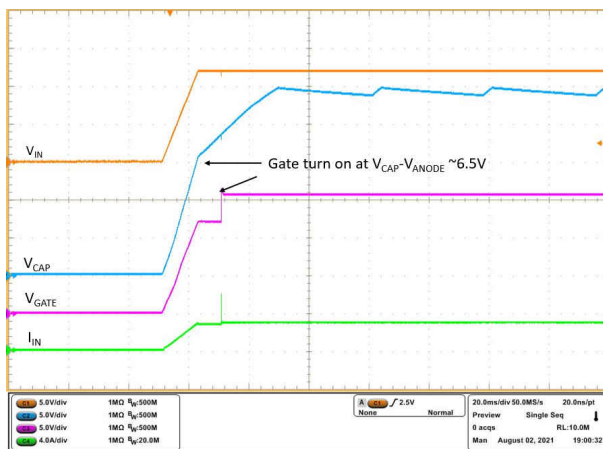
Time (4 ms/DIV)

图 9-6. Startup With 3-A Load



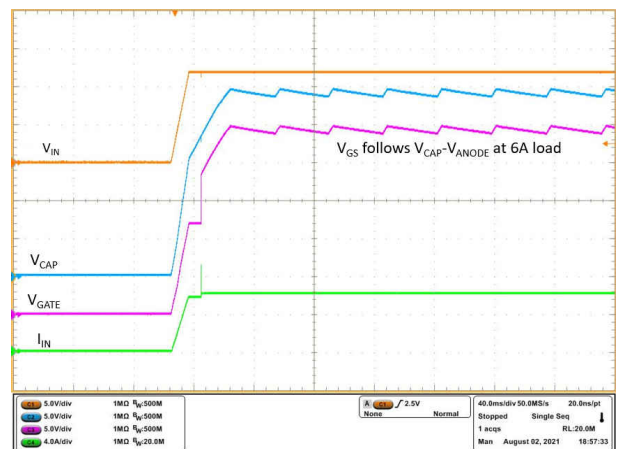
Time (4 ms/DIV)

图 9-7. Startup With 6-A Load



Time (20 ms/DIV)

图 9-8. VCAP During Startup at 3-A Load



Time (40 ms/DIV)

图 9-9. VCAP During Startup at 6-A Load

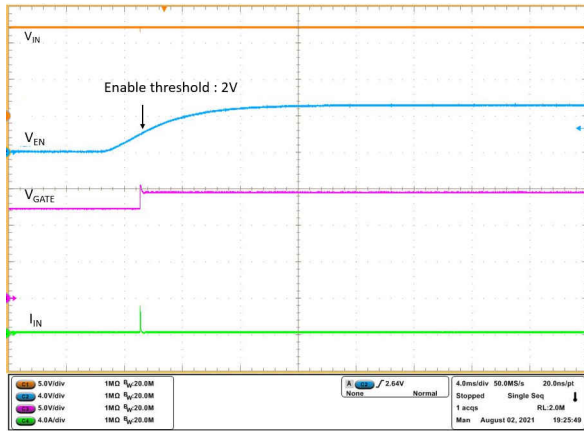


图 9-10. Enable Threshold

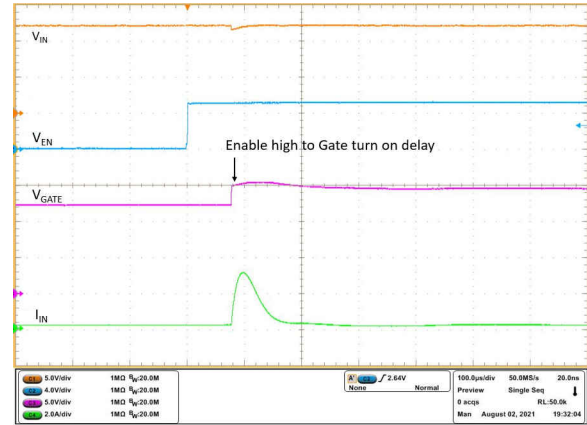


图 9-11. Enable Turn ON Delay

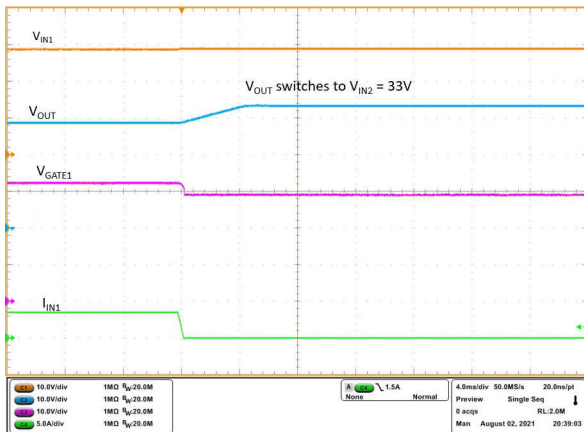


图 9-12. ORing V_{IN1} to V_{IN2} Switch Over

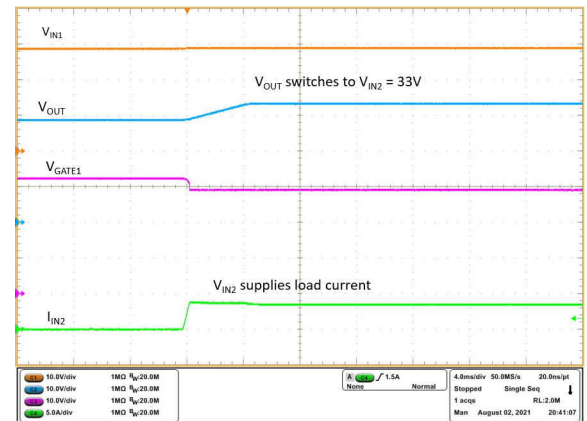


图 9-13. ORing V_{IN1} to V_{IN2} Switch Over

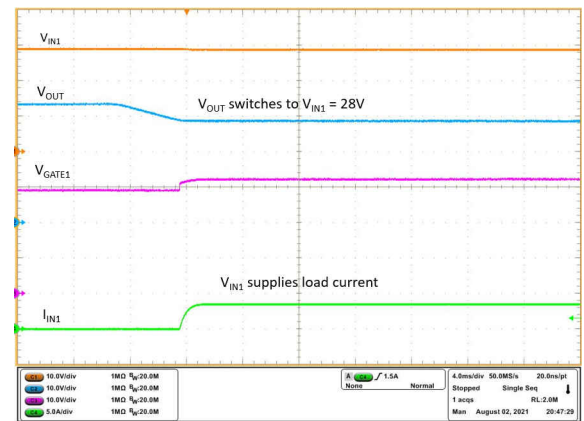


图 9-14. ORing V_{IN2} to V_{IN1} Switch Over

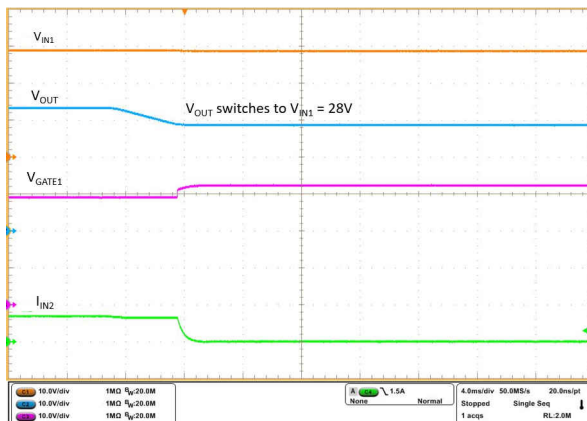
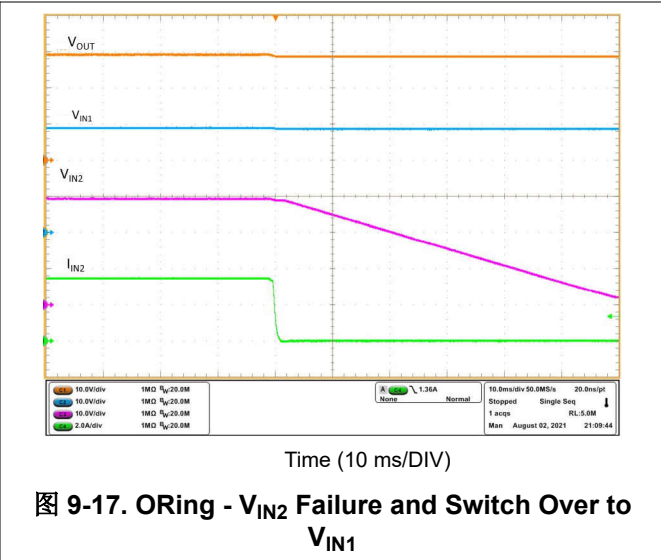
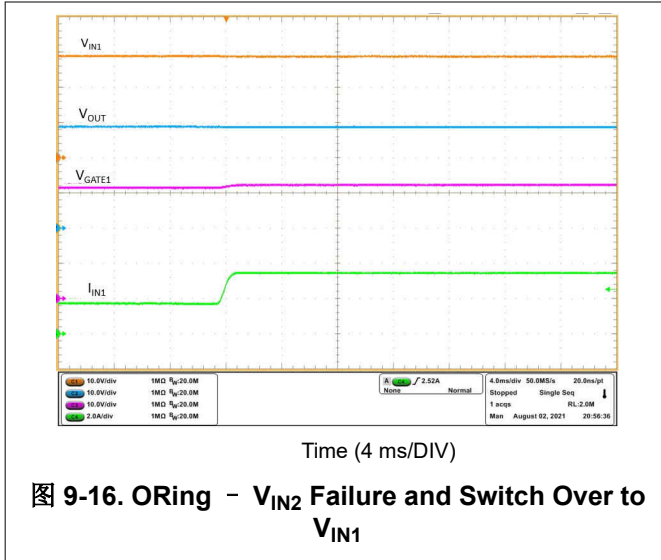


图 9-15. ORing V_{IN2} to V_{IN1} Switch Over



9.3 OR-ing Application Configuration

Basic redundant power architecture comprises of two or more voltage or power supply sources driving a single load. In its simplest form, the OR-ing solution for redundant power supplies consists of Schottky OR-ing diodes that protect the system against an input power supply fault condition. A diode OR-ing device provides effective and low cost solution with few components. However, the diodes forward voltage drops affects the efficiency of the system permanently, since each diode in an OR-ing application spends most of its time in forward conduction mode. These power losses increase the requirements for thermal management and allocated board space.

The LM74700-EP ICs combined with external N-Channel MOSFETs can be used in OR-ing Solution as shown in 图 9-18. The forward diode drop is reduced as the external N-Channel MOSFET is turned ON during normal operation. LM74700-EP quickly detects the reverse current, pulls down the MOSFET gate fast, leaving the body diode of the MOSFET to block the reverse current flow. An effective OR-ing solution needs to be extremely fast to limit the reverse current amount and duration. The LM74700-EP devices in OR-ing configuration constantly sense the voltage difference between Anode and Cathode pins, which are the voltage levels at the power sources (V_{IN1} , V_{IN2}) and the common load point respectively. The source to drain voltage V_{DS} for each MOSFET is monitored by the Anode and Cathode pins of the LM74700-EP. A fast comparator shuts down the Gate Drive through a fast pull-down within $0.45 \mu s$ (typical) as soon as $V_{(IN)} - V_{(OUT)}$ falls below $-11 mV$. The fast comparator turns on the Gate with 11-mA gate charge current once the differential forward voltage $V_{(IN)} - V_{(OUT)}$ exceeds 50 mV.

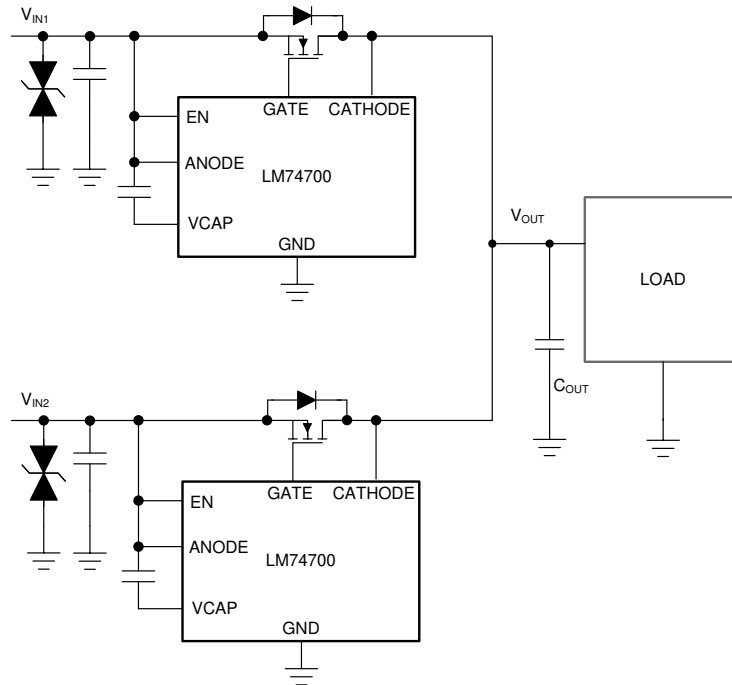


图 9-18. Typical OR-ing Application

图 9-12 到 图 9-15 显示在两个电源轨 V_{IN1} 为 28 V 和 V_{IN2} 为 33 V 之间的平滑切换。图 9-16 和 图 9-17 说明了当 V_{IN2} 发生故障时的性能。LM74700-EP 控制 V_{IN2} 电源轨的器件迅速关闭，因此输出保持不间断，并且 V_{IN1} 受到 V_{IN2} 故障的保护。

10 Power Supply Recommendations

LM74700-EP 理想二极管控制器是为 $3.2\text{ V} \leq V_{ANODE} \leq 65\text{ V}$ 的电源电压范围设计的。如果输入电源位于设备几英寸之外，建议输入陶瓷旁路电容器的值大于 22 nF。为防止 LM74700-EP 及其周围元件在直接输出短路条件下损坏，有必要使用具有过载和短路保护的电源。

11 Layout

11.1 Layout Guidelines

- Connect ANODE, GATE and CATHODE pins of LM74700-EP close to the MOSFET's SOURCE, GATE and DRAIN pins.
- The high current path for this solution is through the MOSFET. Therefore, it is important to use thick traces for source and drain of the MOSFET to minimize resistive losses.
- The charge pump capacitor across VCAP and ANODE pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate pin of the LM74700-EP must be connected to the MOSFET gate with short trace. Avoid excessively thin and long trace to the Gate Drive.
- Keep the GATE pin close to the MOSFET to avoid increase in MOSFET turn-off delay due to trace resistance.
- Obtaining acceptable performance with alternate layout schemes is possible. However, the layout shown in [图 11-1](#) is intended as a guideline.

11.2 Layout Example

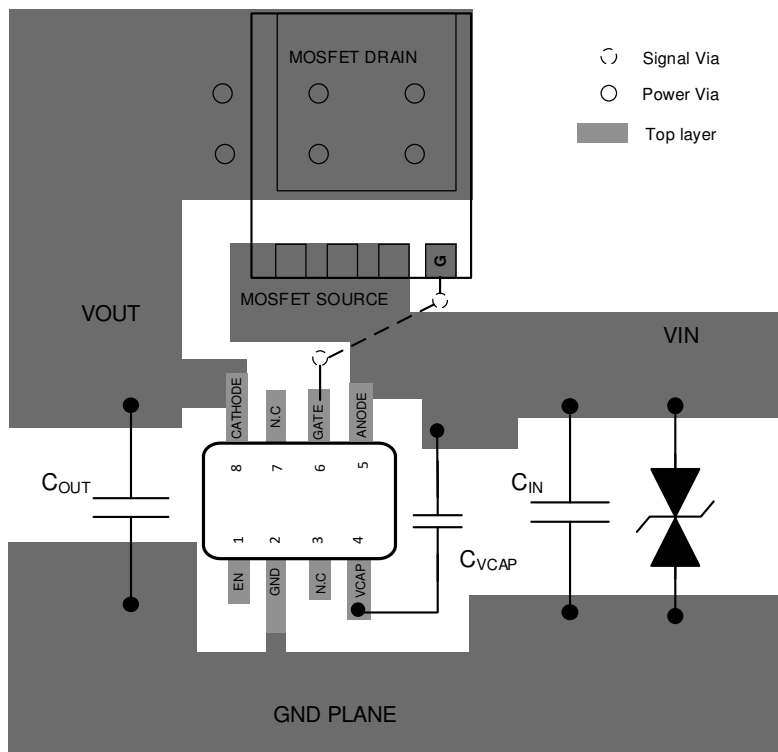


图 11-1. LM74700-EP DDF Package Layout Example

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74700MDDFREP	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-50 to 125	EP747	Samples
V62/21608	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-50 to 125	EP747	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM74700-EP :

- Automotive : [LM74700-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

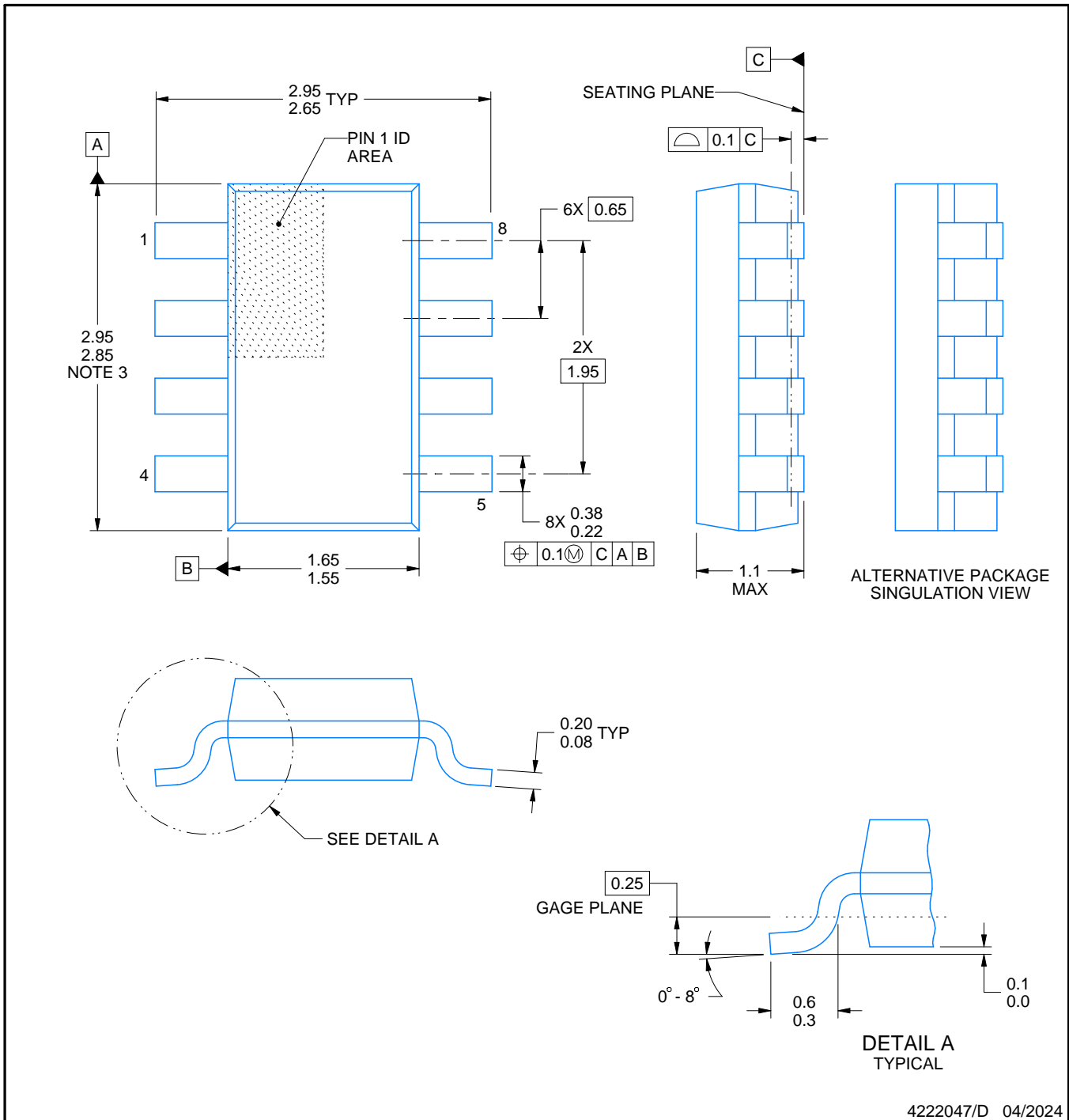
DDF0008A



PACKAGE OUTLINE

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/D 04/2024

NOTES:

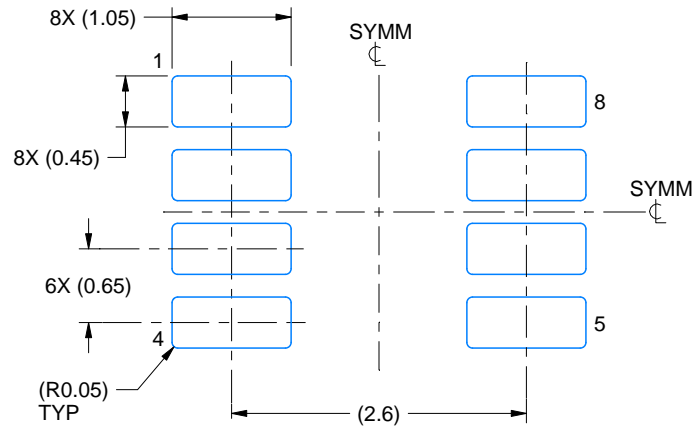
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

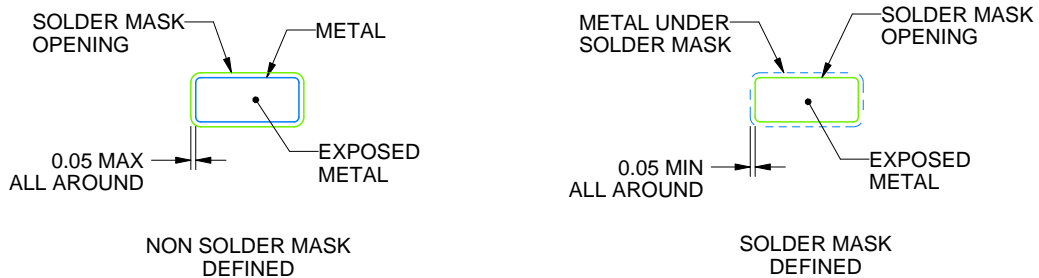
DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/D 04/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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