

## LMH6518 900MHz 数字控制可变增益放大器

### 1 特性

- 增益范围：40dB
- 增益步长大小：2dB
- 与 GSPS ADC 的组合增益分辨率：8.5m dB
- 最小增益：-1.16dB
- 最大增益：38.8dB
- -3dB 带宽 (BW)：900MHz
- 上升和下降时间：< 500ps
- 恢复时间：< 5ns
- 传播延迟变化：100ps
- HD2 (100MHz 时)：-50dBc
- HD3 (100MHz 时)：-53dBc
- 输入参考噪声 (最大增益)：0.98nV/√Hz
- 过压钳位可实现快速恢复
- 功耗：辅助关断 1.1W 至 0.75W

### 2 应用

- 示波器可编程增益放大器
- 差分 ADC 驱动器
- 高频单端输入至差分转换
- 精密增益控制应用
- 医疗应用
- RF/IF 应用

### 3 说明

LMH6518 是数字控制可变增益放大器，总增益范围为 40dB ( -1.16dB 至 38.8dB )，步长为 2dB。所有增益下的 -3dB 带宽均为 900MHz。每个设置的增益精度通常为 0.1dB。与具有可调节满量程范围的 TI 每秒千兆次采样 (GSPS) ADC 结合使用时，LMH6518 增益调整可适应从 6.8mV<sub>PP</sub> 到 920mV<sub>PP</sub> 的满量程输入信号，从而在 ADC 输入端获得 700mV<sub>PP</sub> 的标称值。辅助输出 (+OUT AUX 和 -OUT AUX) 跟随主输出，旨在用于示波器触发功能电路中，但也可在其他应用中用于别的用途。

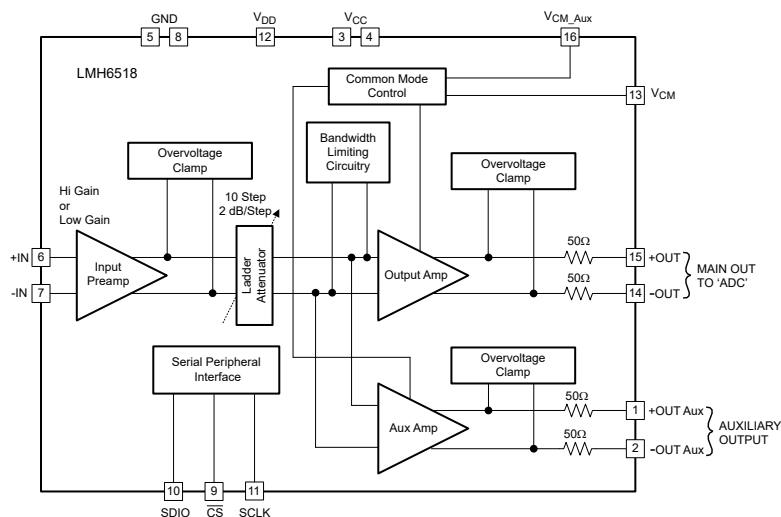
LMH6518 增益通过 SPI 兼容串行总线进行编程。在同时考虑器件增益和 GSPS ADC FS 输入时，可实现 8.5m dB 的信号路径组合增益分辨率。输入和输出为直流耦合。输出是差分的，并具有单独的共模电压控制 (针对主输出和辅助输出)，并且具有可选的带宽限制电路 (适用于主输出和辅助输出)，带宽限制选项包括 20MHz、100MHz、200MHz、350MHz、650MHz、750MHz 或全带宽。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
LMH6518	RGH ( WQFN , 16 )	4mm × 4mm

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



功能方框图



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## 4 Pin Configuration and Functions

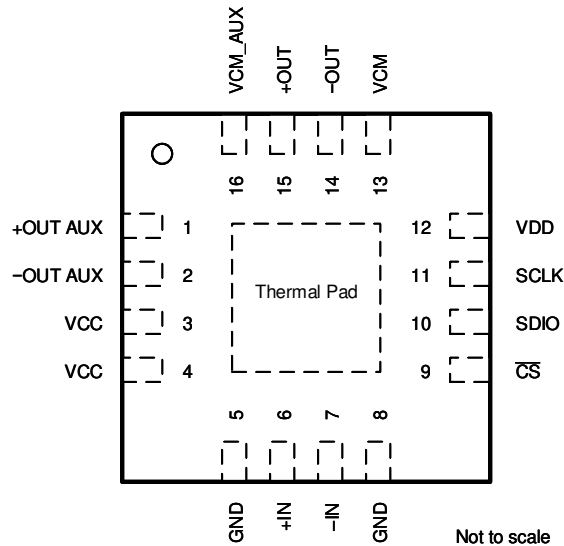


图 4-1. RGH Package, 16-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	+OUT AUX	O	Auxiliary positive output
2	-OUT AUX	O	Auxiliary negative output
3	VCC	P	Analog power supply
4	VCC	P	Analog power supply
5	GND	G	Ground, electrically connected to the WQFN heat sink
6	+IN	I	Positive input
7	-IN	I	Negative input
8	GND	G	Ground, electrically connected to the WQFN heat sink
9	$\overline{CS}$	I	Serial chip select (SPI, active low): While this signal is asserted, SCLK is used to accept serial data present on SDIO and to source serial data on SDIO. When this signal is deasserted, SDIO is ignored and SDIO is in a high-impedance state.
10	SDIO	I/O	Serial data-in or data-out (SPI). During a write operation, serial data are shifted into the device (8-bit command and 16-bit data) on this pin while $\overline{CS}$ signal is asserted. During a read operation, serial data are shifted out of the device on this pin while $\overline{CS}$ signal is asserted. At other times, and after one complete access cycle (24 bits; see 图 6-1 and 图 6-2), this input is ignored. This output is in a high-impedance state when $\overline{CS}$ is deasserted. This pin is bidirectional.
11	SCLK	I	Serial clock (SPI): Serial data are shifted into and out of the device synchronous with this clock signal. SCLK transitions with $\overline{CS}$ deasserted are ignored. To minimize digital crosstalk, stop SCLK when not used.
12	VDD	P	Digital power supply
13	VCM	I	Input from ADC to control main output common mode (CM) voltage
14	-OUT	O	Main negative output
15	+OUT	O	Main positive output
16	VCM_AUX	I	Input to control auxiliary output CM voltage
Pad	Thermal Pad	—	Thermal pad (WQFN heat sink), electrically connected to pins 5 and 8 (GND)

(1) G = ground, I = input, O = output, P = power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Analog supply voltage (5 V nominal)		5.5	V
V <sub>DD</sub>	Digital supply voltage (3.3 V nominal)		3.6	
	Differential input signal voltage		±1	V
	Maximum dc output value <sup>(2)</sup>		1700	mV <sub>PP</sub>
	Input common mode voltage	1	4	V
	V <sub>CM</sub> and V <sub>CM_Aux</sub>		2	V
	SPI inputs		3.6	V
	Soldering temperature	Infrared or convection (20 s)	235	°C
		Wave (10 s)	260	
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) When the LMH6518 output is held at saturation conditions for long time periods the part can develop a permanent output offset voltage. To manage this output offset condition the device attenuation must be set properly to avoid long periods of output saturation.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
		Machine model (MM)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Analog supply voltage		5 ±5%		V
V <sub>DD</sub>	Digital supply voltage		3.3 ±5%		V
T <sub>A</sub>	Ambient temperature	- 40		85	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMH6518	UNIT
		RGH (WQFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	40	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	31.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	11.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	11.5	°C/W

THERMAL METRIC <sup>(1)</sup>		LMH6518	UNIT
		RGH (WQFN)	
		16 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

Unless otherwise noted, all limits are specified at  $T_A = 25^\circ\text{C}$ , input  $\text{CM} = 2.5\text{ V}$ ,  $V_{\text{CM}} = 1.2\text{ V}$ ,  $V_{\text{CM\_Aux}} = 1.2\text{ V}$ , single-ended input drive,  $V_{\text{CC}} = 5\text{ V}$ ,  $V_{\text{DD}} = 3.3\text{ V}$ ,  $R_L = 100\text{-}\Omega$  differential (both main and auxiliary outputs),  $V_{\text{OUT}} = 0.7 V_{\text{PP}}$  differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see 表 8-1 for abbreviations used).<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
<b>DYNAMIC PERFORMANCE</b>						
LSBW	- 3-dB bandwidth	All gains		900		MHz
	Peaking	All gains		1		dB
GF_0.1 dB	$\pm 0.1$ -dB gain flatness	All gains		150		MHz
GF_1 dB	$\pm 1$ -dB gain flatness	All gains		400		MHz
TRS	Rise time			460		ps
TRL	Fall time			450		
OS	Overshoot	Main output		9%		
$t_{s\_1}$	Settling time	Main output, $\pm 0.5\%$		10		ns
$t_{s\_2}$	Settling time	Main output, $\pm 0.05\%$		14		
$t_{\text{recover}}$	Recovery time <sup>(4)</sup>	All gains		<5		ns
$P_D$	Propagation delay	$V_{\text{OUT}} = 0.7 V_{\text{PP}}$ , all gains		1.2		ns
$P_{D\_VAR}$	Propagation delay variation	Gain varied		100		ps
<b>NOISE, DISTORTION, AND RF SPECIFICATIONS</b>						
$e_{n\_1}$	Input noise spectral density	Max gain, 10 MHz		0.98		$\text{nV}/\sqrt{\text{Hz}}$
$e_{n\_2}$	Input noise spectral density	Preamp LG and 0-dB ladder, 10 MHz		4.1		$\text{nV}/\sqrt{\text{Hz}}$
$e_{no\_1}$	RMS output noise	Max gain, 100 Hz to 400 MHz		1.7		mV
$e_{no\_2}$	RMS output noise	Preamp LG, 0-dB ladder, 100 Hz to 400 MHz		940		$\mu\text{V}$
NF_1	Noise figure	Max gain, $R_S = 50\ \Omega$ each input, 10 MHz		3.8		dB
NF_2	Noise figure	Preamp LG, 0-dB ladder, $R_S = 50\ \Omega$ each input, 10 MHz		13.5		dB
HD2_1	2nd harmonic distortion <sup>(5)</sup>	Main output, 100 MHz, all gains		- 50		dBc
HD3_1	3rd harmonic distortion <sup>(5)</sup>	Main output, 100 MHz, all gains		- 53		dBc
HD2_2	2nd harmonic distortion <sup>(5)</sup>	Auxiliary output, 100 MHz, all gains		- 48		dBc
HD3_2	3rd harmonic distortion <sup>(5)</sup>	Auxiliary output, 100 MHz, all gains		- 50		dBc
HD2_3	2nd harmonic distortion <sup>(5)</sup>	Main output, 250 MHz, all gains		- 44		dBc
HD3_3	3rd harmonic distortion <sup>(5)</sup>	Main output, 250 MHz, all gains		- 50		dBc
HD2/HD3_4	2nd and 3rd harmonic distortion <sup>(5)</sup>	Auxiliary output, 250 MHz, all gains		- 42		dBc
IMD3	Intermodulation distortion <sup>(5)</sup>	$f = 250\text{ MHz}$ , main output		- 65		dBc
OIP3_1	Intermodulation intercept <sup>(5)</sup>	Main output, 250 MHz		26		dBm
P_1dB_main	- 1-dB compression	Main output, 250 MHz, 0-dB ladder		1.8		$V_{\text{PP}}$
		Main output, 250 MHz, 20-dB ladder		1		
P_1dB_aux	- 1-dB compression	Auxiliary output, 250 MHz, 0-dB ladder		1.65		$V_{\text{PP}}$
		Auxiliary output, 250 MHz, 20-dB ladder		1		

## 5.5 Electrical Characteristics (续)

Unless otherwise noted, all limits are specified at  $T_A = 25^\circ\text{C}$ , input  $\text{CM} = 2.5\text{ V}$ ,  $V_{\text{CM}} = 1.2\text{ V}$ ,  $V_{\text{CM\_Aux}} = 1.2\text{ V}$ , single-ended input drive,  $V_{\text{CC}} = 5\text{ V}$ ,  $V_{\text{DD}} = 3.3\text{ V}$ ,  $R_L = 100\text{-}\Omega$  differential (both main and auxiliary outputs),  $V_{\text{OUT}} = 0.7\text{ V}_{\text{PP}}$  differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see 表 8-1 for abbreviations used).<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
<b>GAIN PARAMETERS</b>						
$A_{V\_DIFF\_MAX}$	Maximum gain		38.1	38.8	39.5	dB
$A_{V\_DIFF\_MIN}$	Minimum gain		- 1.91	- 1.16	- 0.4	dB
Gain_Step	Gain step size	All gains including preamp step	1.8	2	2.2	dB
	Gain step size with ADC (see 节 7)	ADC FS adjusted		8.5		mdB
Gain_Range	Gain range		39	40	41	dB
$TC_{AV\_DIFF}$	Gain temp coefficient <sup>(6)</sup>	All gains		- 0.8		mdB/ $^\circ\text{C}$
Gain_Acc	Absolute gain accuracy	Compared to theoretical from max gain in 2-dB steps	0.75		0.75	dB
<b>MATCHING</b>						
Gain_match	Gain matching, main and auxiliary	All gains		$\pm 0.1$	$\pm 0.2$	dB
BW_match	- 3-dB bandwidth matching, main and auxiliary	All gains		5%		
RT_match	Rise time matching, main and auxiliary	All gains		5%		
PD_match	Propagation delay matching, main and auxiliary	All gains		100		ps
<b>ANALOG I/O</b>						
CMRR_1	CM rejection ratio (see 表 8-1)	Preamp HG, 0-dB ladder, $1.9\text{ V} < \text{CMVR} < 3.1\text{ V}$	45	86		dB
CMRR_2	CM rejection ratio (see 表 8-1)	Preamp LG, 0-dB ladder, $1.9\text{ V} < \text{CMVR} < 3.1\text{ V}$	40	55		dB
CMVR_1	Input common-mode voltage	Preamp HG, all ladder steps, $\text{CMRR} \geq 45\text{ dB}$	1.9		3.1	V
CMVR_2	Input common-mode voltage	Preamp LG, all ladder steps, $\text{CMRR} \geq 40\text{ dB}$	1.9		3.1	V
$\frac{ \Delta V_{O\_CM} }{\Delta I_{CM}}$		All gains, $2\text{ V} < \text{CMVR} < 3\text{ V}$	- 60	- 100		dB
CMRR_CM	CM rejection ratio relative to VCM (see 表 8-1)	Preamp LG, 0 dB		101		dB
$Z_{in\_diff}$	Differential input impedance	All gains		$150 \parallel 1.5$		$\text{k}\Omega \parallel \text{pF}$
$Z_{in\_CM}$	CM input impedance	Preamp HG		$420 \parallel 1.7$		$\text{k}\Omega \parallel \text{pF}$
		Preamp LG		$900 \parallel 1.7$		
FS <sub>OUT1</sub>	Full scale voltage swing	Main output, all gains, THD at 100 MHz $\leq - 40\text{ dBc}$	770 <sup>(7)</sup>	800		$\text{mV}_{\text{PP}}$
FS <sub>OUT2</sub>	Full scale voltage swing	Main output, clamped, 0-dB ladder		1800	1960	$\text{mV}_{\text{PP}}$
FS <sub>OUT3</sub>	Full scale voltage swing	Auxiliary output, all gains, THD at 100 MHz $\leq - 40\text{ dBc}$	770 <sup>(7)</sup>	800		$\text{mV}_{\text{PP}}$
FS <sub>OUT4</sub>	Full scale voltage swing	Auxiliary output, clamped, 0-dB ladder		1600	1760	$\text{mV}_{\text{PP}}$
$V_{\text{OUT\_MAX1}}$	Voltage at each output pin (clamped)	Main output, all gains, $V_{\text{CM}} = 1.2\text{ V}$	0.5		1.8	V
$V_{\text{OUT\_MAX2}}$	Voltage at each output pin (clamped)	Auxiliary output, all gains, $V_{\text{CM}} = 1.2\text{ V}$	0.8		2.2	V

## 5.5 Electrical Characteristics (续)

Unless otherwise noted, all limits are specified at  $T_A = 25^\circ\text{C}$ , input  $\text{CM} = 2.5\text{ V}$ ,  $V_{\text{CM}} = 1.2\text{ V}$ ,  $V_{\text{CM\_Aux}} = 1.2\text{ V}$ , single-ended input drive,  $V_{\text{CC}} = 5\text{ V}$ ,  $V_{\text{DD}} = 3.3\text{ V}$ ,  $R_L = 100\text{-}\Omega$  differential (both main and auxiliary outputs),  $V_{\text{OUT}} = 0.7\text{ V}_{\text{PP}}$  differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see 表 8-1 for abbreviations used).<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
$V_{\text{OUT\_MAX3}}$	Voltage at each output pin (clamped)	Main output, all gains, $V_{\text{CM}} = 1.45\text{ V}$				2.05	V
$V_{\text{OUT\_MAX4}}$	Voltage at each output pin (clamped)	Auxiliary output, all gains, $V_{\text{CM}} = 1.45\text{ V}$				2.45	V
$Z_{\text{OUT\_DIFF}}$	Differential output impedance	All gains		92	100	108	$\Omega$
$V_{\text{OOS}}$	Output offset voltage	All gains			$\pm 15$	$\pm 40$	mV
$V_{\text{OOS\_shift1}}$	Output offset voltage shift	Preamp LG to preamp HG			13.7		mV
$V_{\text{OOS\_shift2}}$	Output offset voltage shift	All gains, excluding preamp step			12.7		mV
$\text{TCV}_{\text{OOS}}$	Output offset voltage drift <sup>(6)</sup>	Preamp HG, 0-dB ladder			- 24		$\mu\text{V}/^\circ\text{C}$
		Preamp LG, 0-dB ladder			- 7		
$I_{\text{B}}$	Input bias current <sup>(8)</sup>	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			40	100	$\mu\text{A}$
		$T_A = -65^\circ\text{C}$ to $+150^\circ\text{C}$				140	
$V_{\text{OCM}}$	Output CM voltage	All gains	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1.2		V
			$T_A = -65^\circ\text{C}$ to $+150^\circ\text{C}$	0.95		1.45	
$V_{\text{OS\_CM}}$	Output CM offset	All gains			$\pm 15$	$\pm 30$	mV
$\text{TC}_{\text{VOS\_CM}}$	CM offset voltage temperature coefficient	All gains			+55		$\mu\text{V}/^\circ\text{C}$
$\text{BAL\_Error\_DC}$	Output gain balance error	DC, $\frac{\Delta V_{\text{O\_CM}}}{\Delta V_{\text{OUT}}}$			- 78		dB
$\text{BAL\_Error\_AC}$	Output gain balance error	250 MHz, $\frac{V_{\text{O\_CM}}}{V_{\text{OUT}}}$			- 45		dB
PB	Phase balance error (see 表 8-1)	250 MHz			$\pm 0.8$		deg
PSRR	Differential power-supply rejection (see 表 8-1)	Preamp HG, 0-dB ladder		- 60	- 87		dB
		Preamp LG, 0-dB ladder		- 50	- 70		
$\text{PSRR\_CM}$	CM power-supply rejection (see 表 8-1)	Preamp LG, 0-dB ladder		- 55	- 71		dB
$V_{\text{CM\_I}}$	$V_{\text{CM}}$ input bias current <sup>(8)</sup>	All gains	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$\pm 1$	$\pm 10$	nA
			$T_A = -65^\circ\text{C}$ to $+150^\circ\text{C}$			$\pm 20$	
$V_{\text{CM\_AUX\_I}}$	$V_{\text{CM\_AUX}}$ input bias current <sup>(8)</sup>	All gains	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$\pm 1$	$\pm 10$	nA
			$T_A = -65^\circ\text{C}$ to $+150^\circ\text{C}$			$\pm 20$	
<b>DIGITAL I/O</b>							
$V_{\text{IH}}$	Input logic high	$T_A = -65^\circ\text{C}$ to $+150^\circ\text{C}$		$V_{\text{DD}} - 0.6$			V
$V_{\text{IL}}$	Input logic low	$T_A = -65^\circ\text{C}$ to $+150^\circ\text{C}$				0.5	V
$V_{\text{OH}}$	Output logic high				$V_{\text{DD}}$		V
$V_{\text{OL}}$	Output logic low				0		V
$R_{\text{Hi\_Z}}$	Output resistance	High-impedance mode			5		M $\Omega$
$I_{\text{in}}$	Input bias current				<1		$\mu\text{A}$
$F_{\text{SCLK}}$	SCLK rate					10	MHz



## 5.5 Electrical Characteristics (续)

Unless otherwise noted, all limits are specified at  $T_A = 25^\circ\text{C}$ , input  $CM = 2.5\text{ V}$ ,  $V_{CM} = 1.2\text{ V}$ ,  $V_{CM\_Aux} = 1.2\text{ V}$ , single-ended input drive,  $V_{CC} = 5\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ ,  $R_L = 100\text{-}\Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\text{ V}_{PP}$  differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see [表 8-1](#) for abbreviations used).<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
F <sub>SCLK_DT</sub>	SCLK duty cycle		45%	50%	55%	

## 5.5 Electrical Characteristics (续)

Unless otherwise noted, all limits are specified at  $T_A = 25^\circ\text{C}$ , input  $\text{CM} = 2.5\text{ V}$ ,  $V_{\text{CM}} = 1.2\text{ V}$ ,  $V_{\text{CM\_Aux}} = 1.2\text{ V}$ , single-ended input drive,  $V_{\text{CC}} = 5\text{ V}$ ,  $V_{\text{DD}} = 3.3\text{ V}$ ,  $R_L = 100\text{-}\Omega$  differential (both main and auxiliary outputs),  $V_{\text{OUT}} = 0.7\text{ V}_{\text{PP}}$  differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see 表 8-1 for abbreviations used).<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
<b>POWER REQUIREMENTS</b>							
$I_{\text{S1}}$	Supply current, $V_{\text{CC}}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		195	210	225	mA
		$T_A = -65^\circ\text{C}$ to $+150^\circ\text{C}$				230	
$I_{\text{S1\_off}}$	Supply current, $V_{\text{CC}}$ aux off	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			150	165	mA
		$T_A = -65^\circ\text{C}$ to $+150^\circ\text{C}$				170	
$I_{\text{DD}}$	Supply current, $V_{\text{DD}}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			180	350	$\mu\text{A}$
		$T_A = -65^\circ\text{C}$ to $150^\circ\text{C}$				400	
<b>BANDWIDTH LIMITING FILTER SPECIFICATIONS</b>							
	Pass band tolerance, – 3 dB bandwidth	All gains	20 MHz	0%	20%		
			100 MHz	0%	20%		
			200 MHz	0%	20%		
			350 MHz		$\pm 25\%$		
			650 MHz		$\pm 25\%$		
			750 MHz		$\pm 25\%$		
		Preamp LG, 0-dB ladder	350 MHz		$\pm 10\%$		
			650 MHz		$\pm 10\%$		
			750 MHz		$\pm 10\%$		

- (1) *Electrical Characteristics* table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .
- (2) Limits are 100% production tested at  $25^\circ\text{C}$  unless otherwise specified. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values can vary over time and also depends on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (4) Recovery time is the slower of the main and auxiliary outputs. Output swing of  $700\text{ mV}_{\text{PP}}$  shifted up or down by 50% ( $0.35\text{ V}$ ) by introducing an offset. Measured values correspond to the time required to return to within  $\pm 1\%$  of  $0.7\text{ V}_{\text{PP}}$  ( $\pm 7\text{ mV}$ ).
- (5) Distortion data taken under single ended input condition.
- (6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
- (7) Specified by design.
- (8) Positive current is current flowing into the device.

## 5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{\text{S}}$	SDIO setup time	25			ns
$t_{\text{H}}$	SDIO hold time	25			ns
$t_{\text{CES}}$	$\overline{\text{CS}}$ enable setup time (from $\overline{\text{CS}}$ asserted to rising edge of SCLK)	25			ns
$t_{\text{CDS}}$	$\overline{\text{CS}}$ disable setup time (from $\overline{\text{CS}}$ deasserted to rising edge of SCLK)	25			ns
$t_{\text{IAG}}$	Inter-access gap	3			SCLK cycles

### 5.7 Typical Characteristics

at input  $CM = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\text{ V}_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

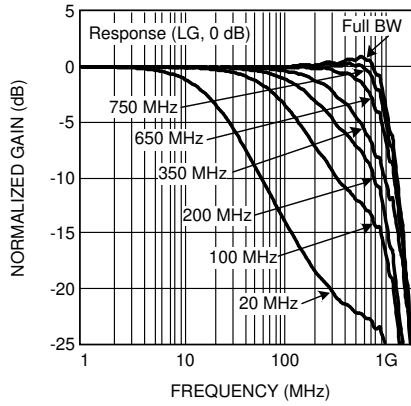


图 5-1. Response (LG, 0-dB)

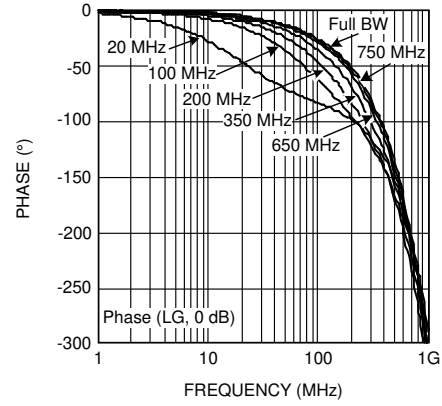


图 5-2. Phase (LG, 0-dB)

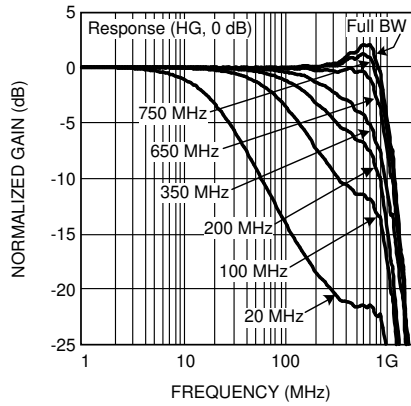


图 5-3. Response (HG, 0-dB)

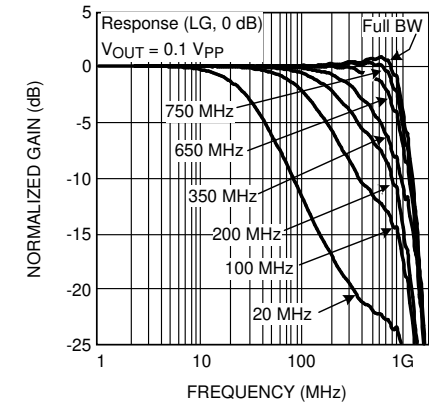


图 5-4. Small Signal Response (LG, 0-dB)

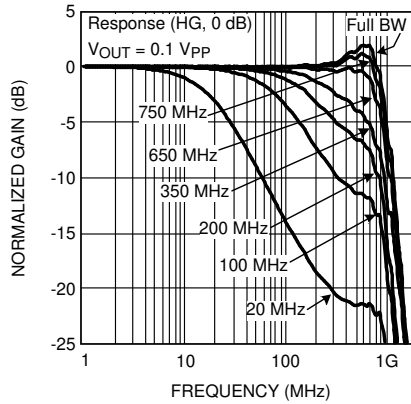


图 5-5. Small Signal Response (HG, 0-dB)

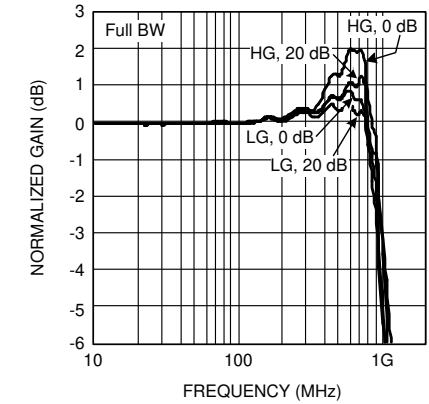


图 5-6. Response vs Gain

### 5.7 Typical Characteristics (continued)

at input  $V_{CM} = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\ V_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

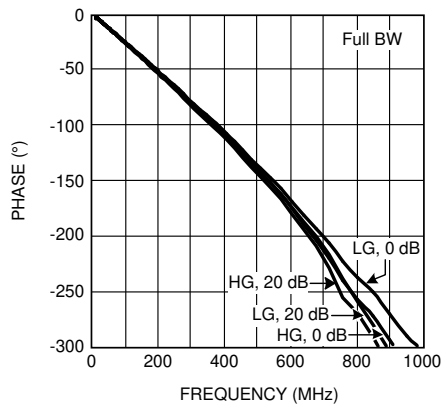


图 5-7. Phase vs Gain

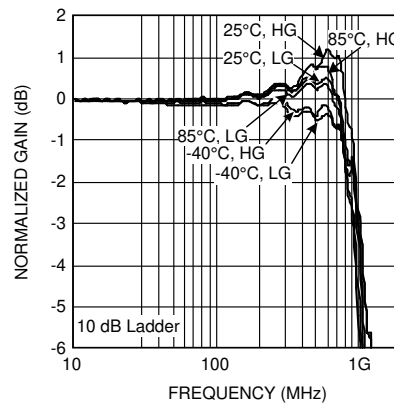


图 5-8. Response Over Temperature

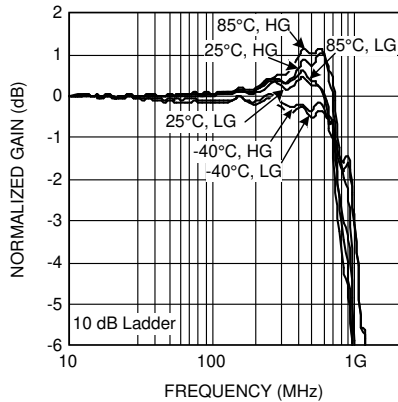


图 5-9. Auxiliary Response Over Temperature

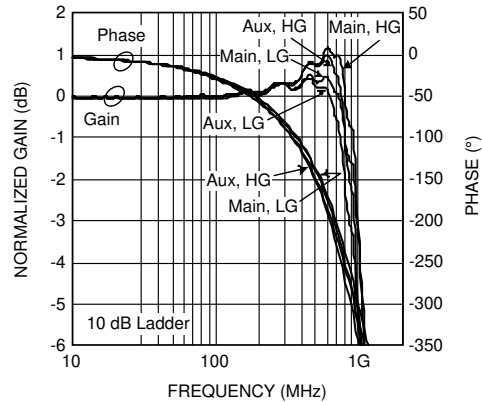


图 5-10. Main vs Auxiliary Response

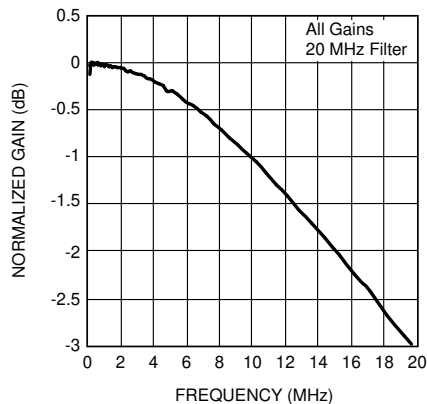


图 5-11. Response vs Gain

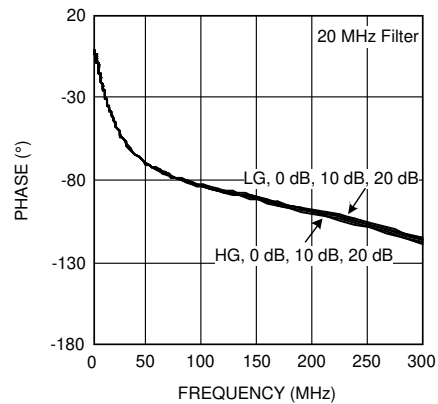


图 5-12. Phase vs Gain

### 5.7 Typical Characteristics (continued)

at input  $V_{CM} = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\ V_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

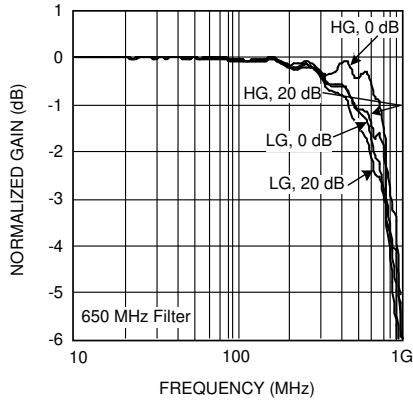


图 5-13. Response vs Gain

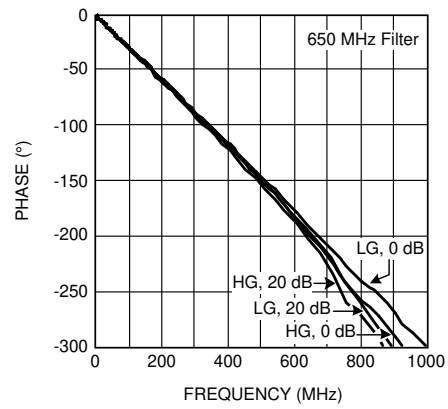


图 5-14. Phase vs Gain

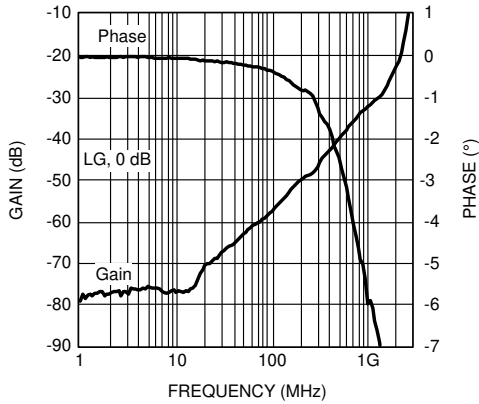


图 5-15. Balance Error

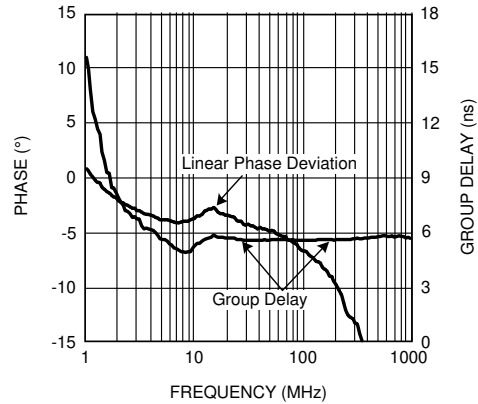


图 5-16. Linear Phase Deviation and Group Delay

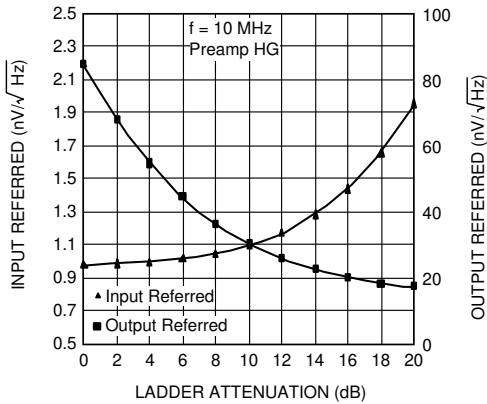


图 5-17. Noise vs Ladder Attenuation

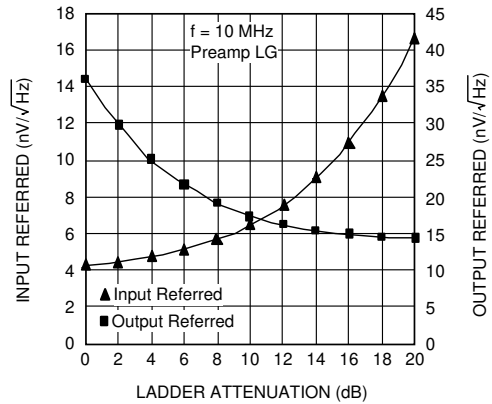


图 5-18. Noise vs Ladder Attenuation

### 5.7 Typical Characteristics (continued)

at input  $V_{CM} = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\ V_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

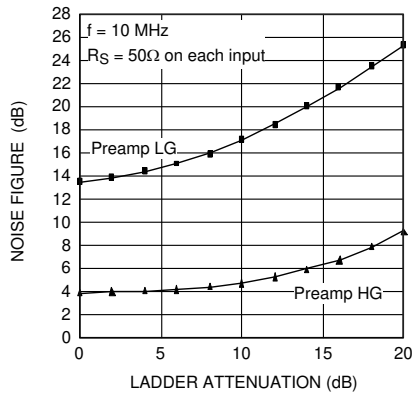


图 5-19. Noise Figure vs Gain

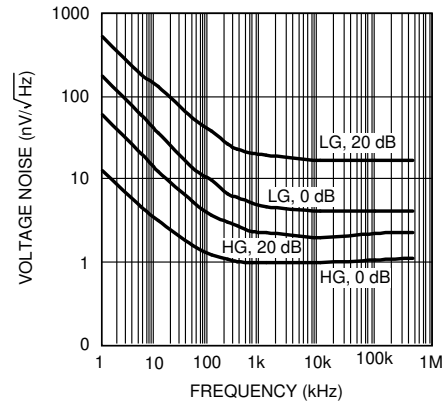


图 5-20. Input Voltage Noise vs Frequency

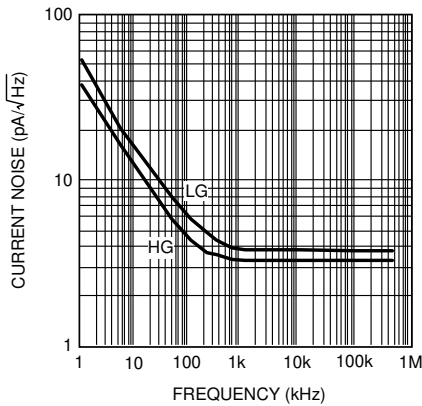


图 5-21. Input Current Noise vs Frequency

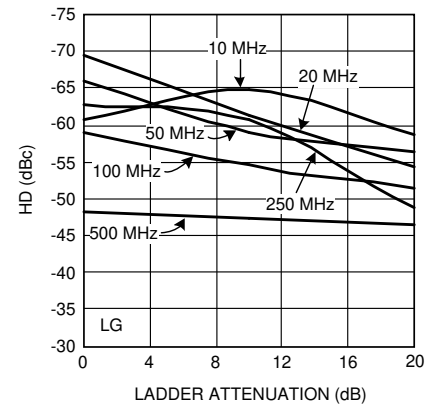


图 5-22. HD2 vs Ladder Attenuation

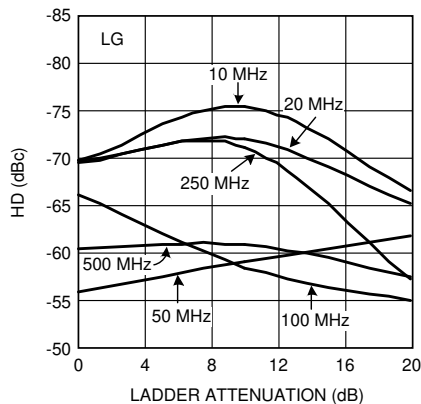


图 5-23. HD3 vs Ladder Attenuation

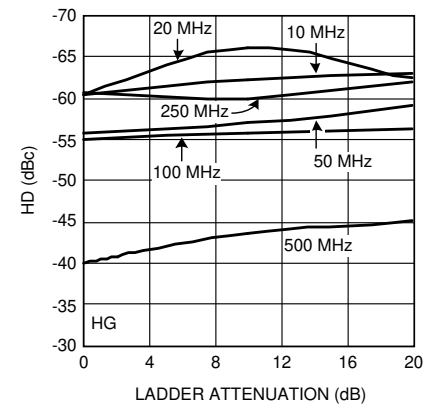


图 5-24. HD2 vs Ladder Attenuation

### 5.7 Typical Characteristics (continued)

at input  $V_{CM} = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7 V_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

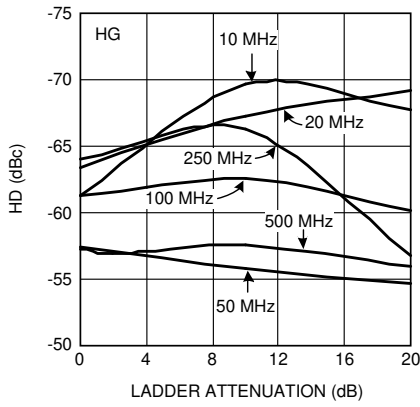


图 5-25. HD3 vs Ladder Attenuation

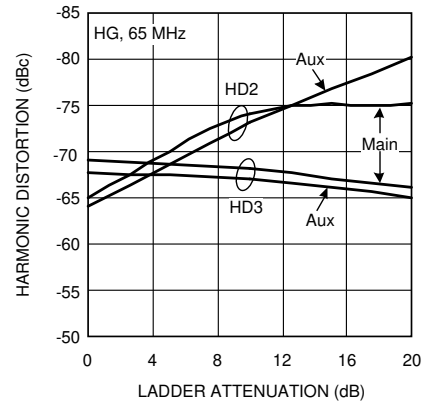


图 5-26. Main and Auxiliary Distortion Comparison

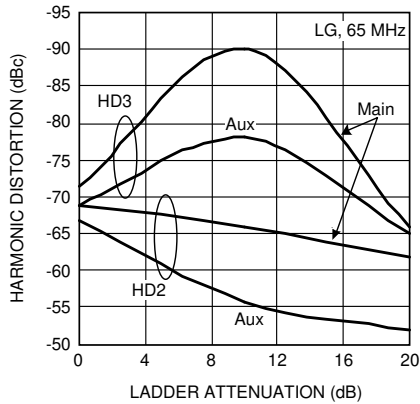


图 5-27. Main and Auxiliary Distortion Comparison

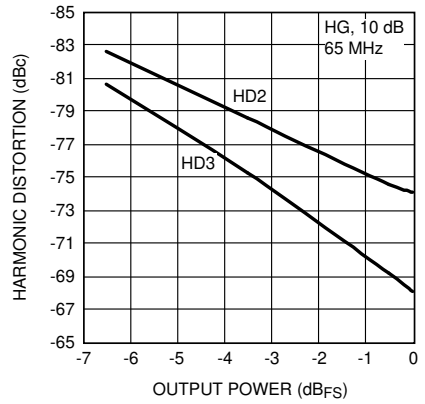


图 5-28. Distortion vs Output Power

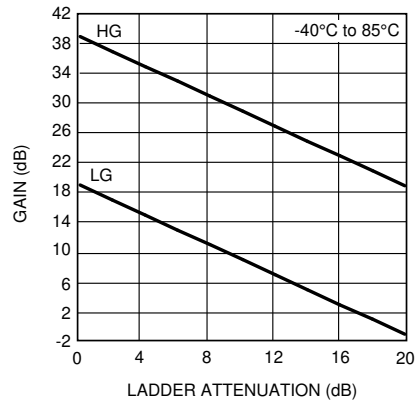


图 5-29. Gain vs Ladder Attenuation

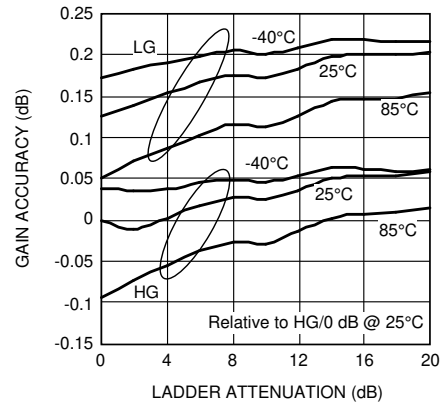


图 5-30. Gain Accuracy vs Ladder Attenuation

### 5.7 Typical Characteristics (continued)

at input  $V_{CM} = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\ V_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

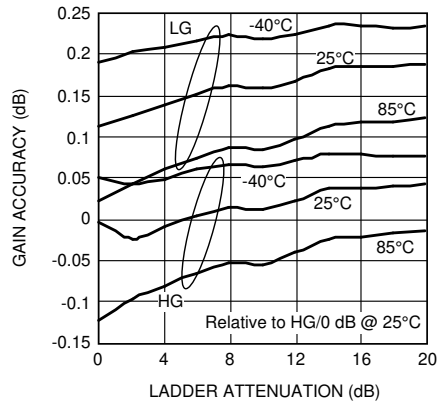


图 5-31. Auxiliary Gain Accuracy vs Ladder Attenuation

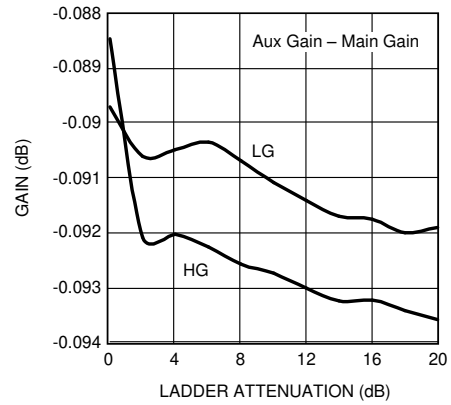


图 5-32. Gain Matching vs Ladder Attenuation

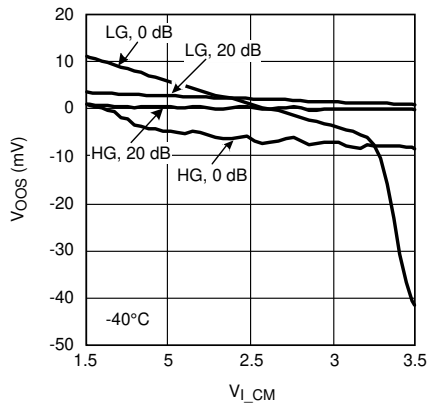


图 5-33.  $A_{V_{CM}}$

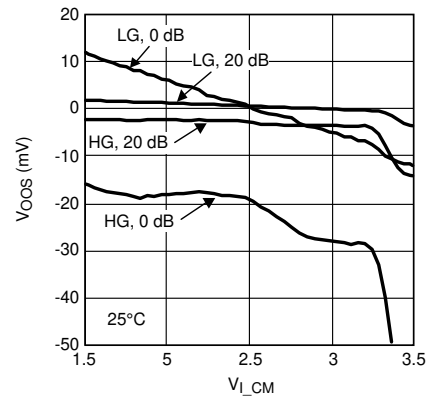


图 5-34.  $A_{V_{CM}}$

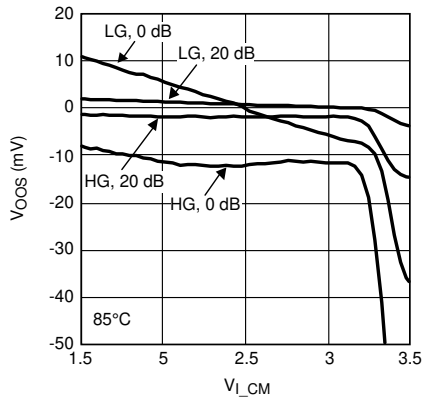


图 5-35.  $A_{V_{CM}}$

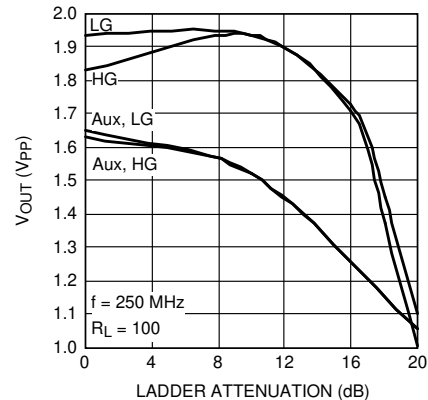


图 5-36. -1-dB Compression vs Ladder Attenuation



### 5.7 Typical Characteristics (continued)

at input  $V_{CM} = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\text{ V}_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

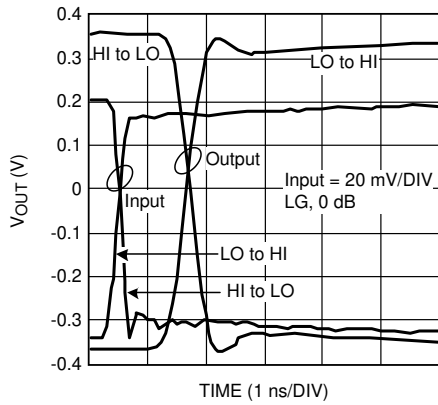


图 5-37. Step Response

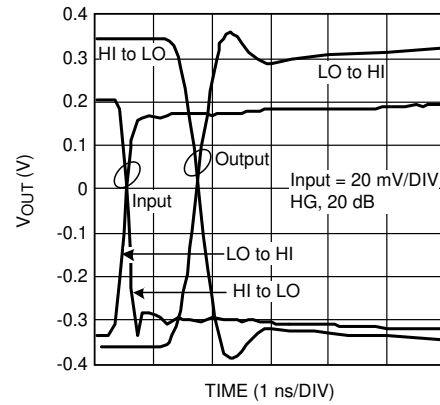


图 5-38. Step Response

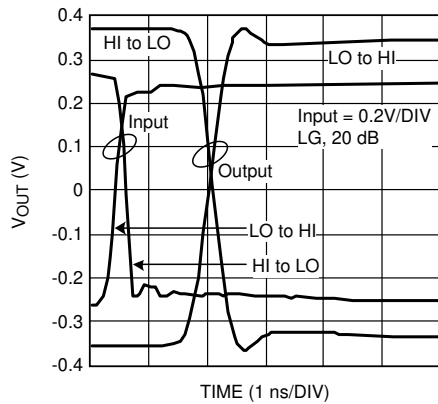


图 5-39. Step Response

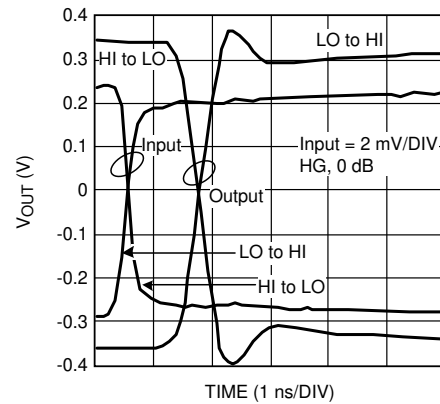


图 5-40. Step Response

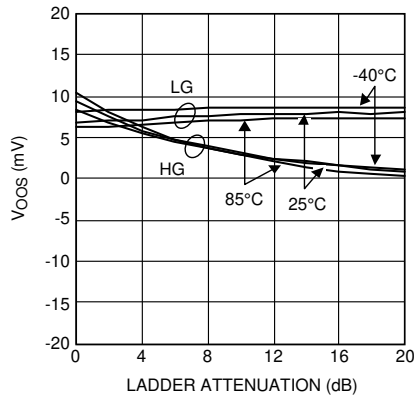


图 5-41. Output Offset Voltage (Typical Unit 1)

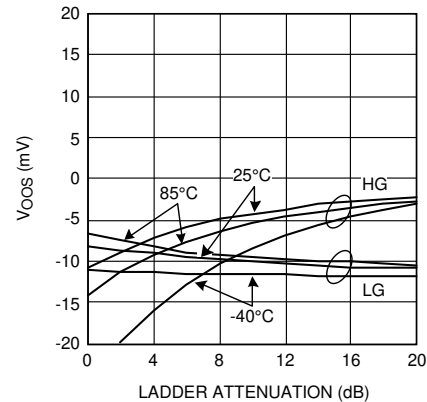


图 5-42. Output Offset Voltage (Typical Unit 2)

### 5.7 Typical Characteristics (continued)

at input  $V_{CM} = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\text{ V}_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

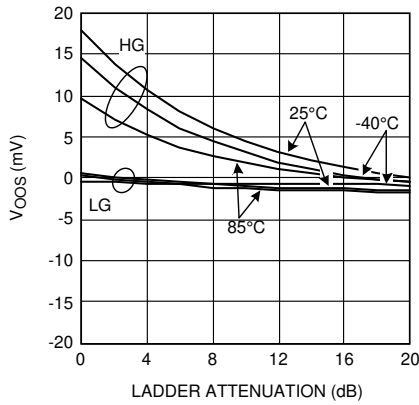


图 5-43. Output Offset Voltage (Typical Unit 3)

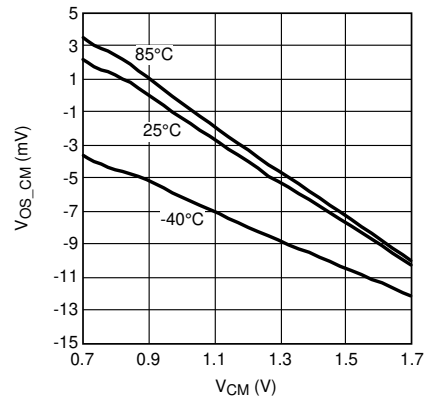


图 5-44.  $V_{OS\_CM}$  vs  $V_{CM}$

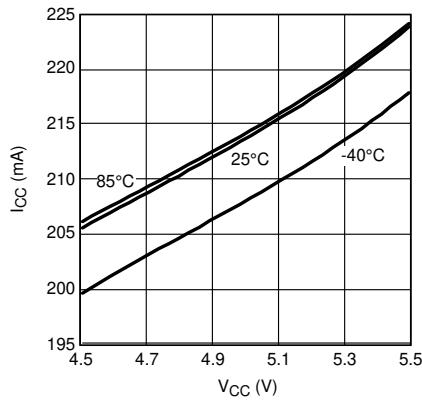


图 5-45. Supply Current vs Supply Voltage

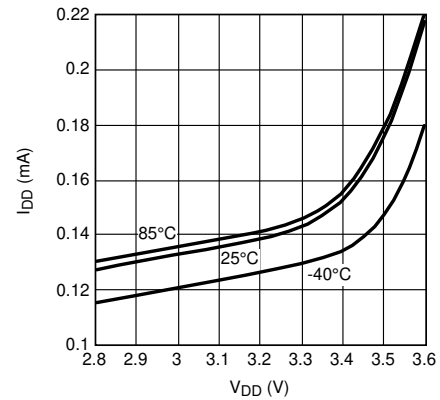


图 5-46. Supply Current vs Supply Voltage

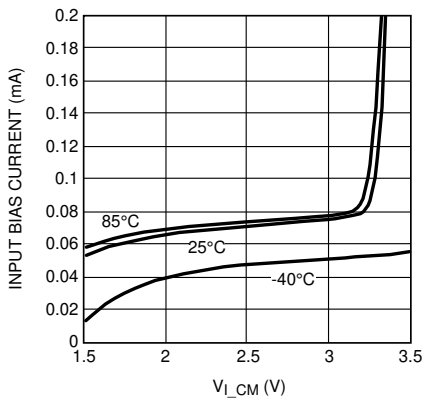


图 5-47. Input Bias Current vs Input CM

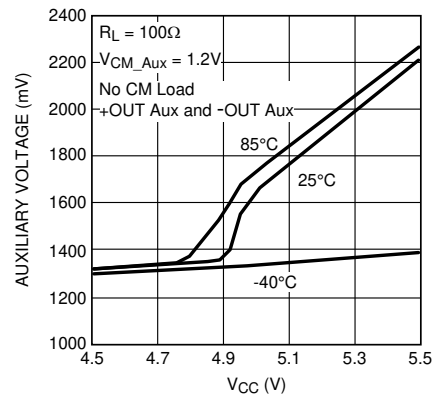


图 5-48. Auxiliary Output Voltage (Hi-Z Mode)

### 5.7 Typical Characteristics (continued)

at input  $V_{CM} = 2.5\text{-V}$ ,  $V_{CM} = 1.2\text{-V}$ ,  $V_{CM\text{ AUX}} = 1.2\text{-V}$ , single-ended input drive,  $V_{CC} = 5\text{-V}$ ,  $V_{DD} = 3.3\text{-V}$ ,  $R_L = 100\ \Omega$  differential (both main and auxiliary outputs),  $V_{OUT} = 0.7\ V_{PP}$  differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

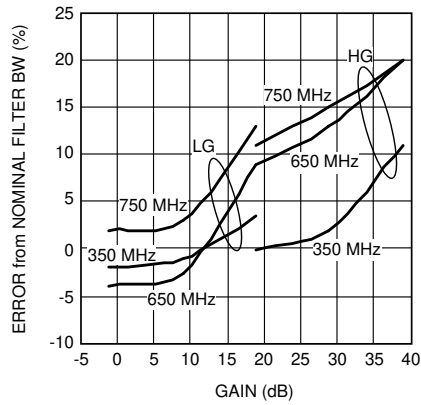


图 5-49. Filter BW vs Gain

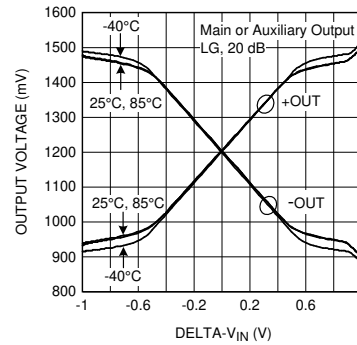


图 5-50. Output vs Input

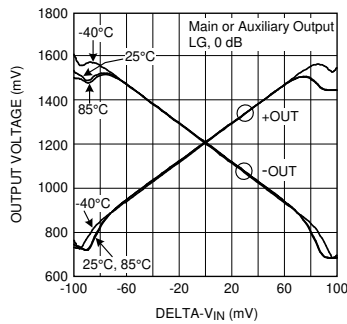


图 5-51. Output vs Input

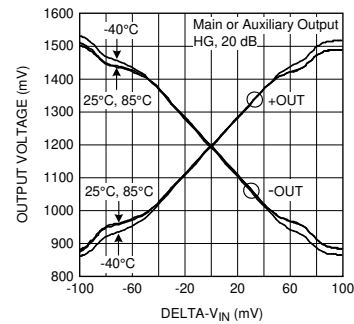


图 5-52. Output vs Input

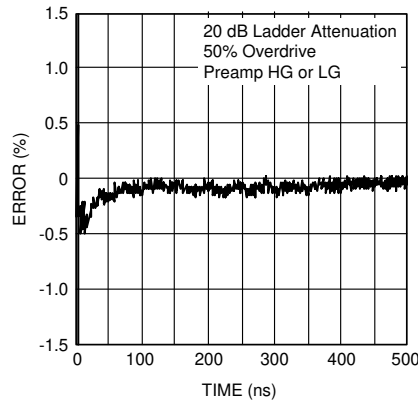


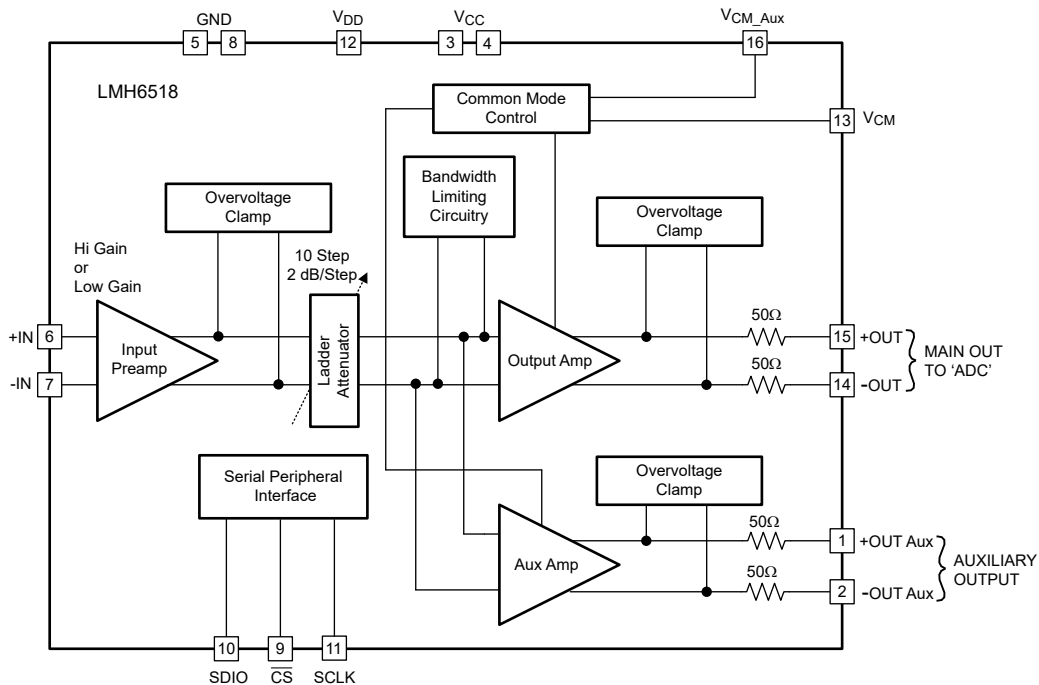
图 5-53. Overdrive Recovery Time (Return to Zero)

## 6 Detailed Description

### 6.1 Overview

The LMH6518 is a digitally-controlled variable gain amplifier (DVGA) that is designed specifically as an oscilloscope analog front end (AFE). This device samples an analog voltage and conditions the voltage for the analog to digital converter (ADC) input. This device is specifically designed to drive TI's giga sample ADCs that have a  $100\text{-}\Omega$  input impedance and  $800\text{ mV}_{PP}$  full-scale input voltage.

### 6.2 Functional Block Diagram



### 6.3 Feature Description

The LMH6518 offers several unique features in addition to being a general purpose digital variable gain amplifier (DVGA).

#### 6.3.1 Input Preamplifier

The LMH6518 has a fully differential preamplifier which has a consistent  $150\text{-k}\Omega$  impedance across all gain settings. The LMH6518 is also driven with a single-ended signal source. The preamplifier has two gain settings. See [§ 7.2.1.2.2](#) for details.

##### 6.3.1.1 Primary Output Amplifier

The LMH6518 has two nearly identical amplifiers. The output amplifier was designed as the primary output amplifier. The output amplifier features an internal  $100\text{-}\Omega$  termination that interfaces with  $100\text{-}\Omega$  input impedance ADCs. The output amplifier has a common-mode voltage control pin that sets the output common-mode voltage of the amplifier.

##### 6.3.1.2 Auxiliary Amplifier

The LMH6518 has a second output amplifier that was designed to provide a trigger signal when used as an oscilloscope AFE. The auxiliary amplifier has all of the features of the output amplifier and provides a duplicate signal for use in trigger circuits. The auxiliary amplifier has a common mode voltage control pin which sets the output common mode of the amplifier.

### 6.3.2 Overvoltage Clamp

The LMH6518 features two levels of clamps used to protect the amplifier and the ADC from voltage transients. These clamps are placed after the input preamplifier and also after the final output amplifier. The clamp voltages are set by the preamp and ladder attenuator logic functions. The SPI bus is used to set and control the preamp (HG or LG) and ladder attenuator (0-dB to 20-dB, 10 states) logic functions.

### 6.3.3 Attenuator

The primary gain control feature of the LMH65418 is the digital attenuator. The attenuator controls the overall gain of the amplifier. The attenuator has a range of 0-dB to 20-dB of attenuation.

### 6.3.4 Digital Control Block

The LMH6518 has digitally controlled gain, as well as digitally controlled voltage clamps and digitally controlled bandwidth. If the block is not used, this block can also disable the auxiliary amplifier. [节 6.5.1](#) has details on the digital control registers and programming.

## 6.4 Device Functional Modes

### 6.4.1 Primary Amplifier

The main functional mode of the LMH6518 is as an AFE providing gain, voltage clamping, and frequency limiting. In this mode, the gain, bandwidth, and voltage swing are all programmable using the SPI control block.

### 6.4.2 Auxiliary Output

The secondary functional mode of the LMH6518 is the auxiliary output. This output is nearly identical to the primary amplifier. The only difference is that the auxiliary output has slightly lower distortion performance. The auxiliary output was designed to provide a trigger signal when used as an oscilloscope AFE.

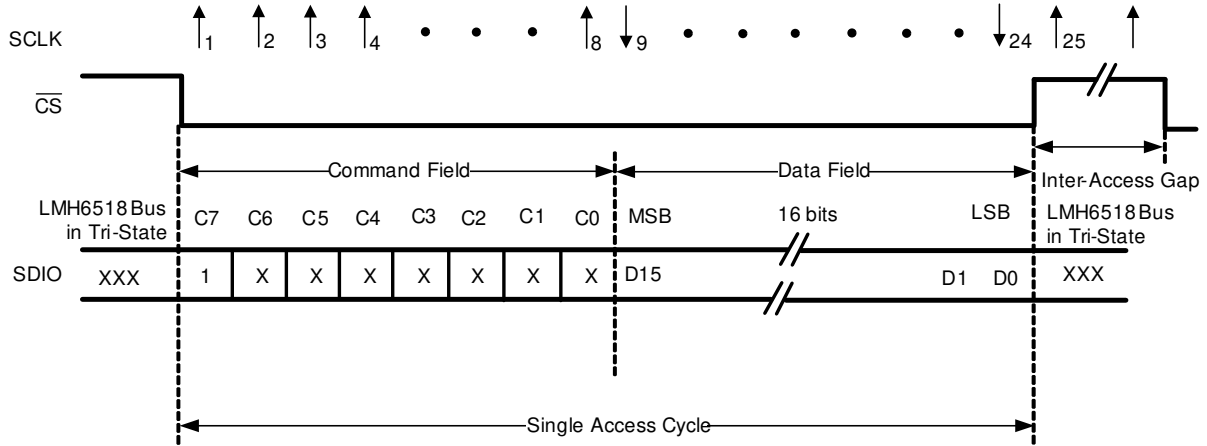
## 6.5 Programming

### 6.5.1 Logic Functions

The following LMH6518 functions are controlled using the SPI-compatible bus:

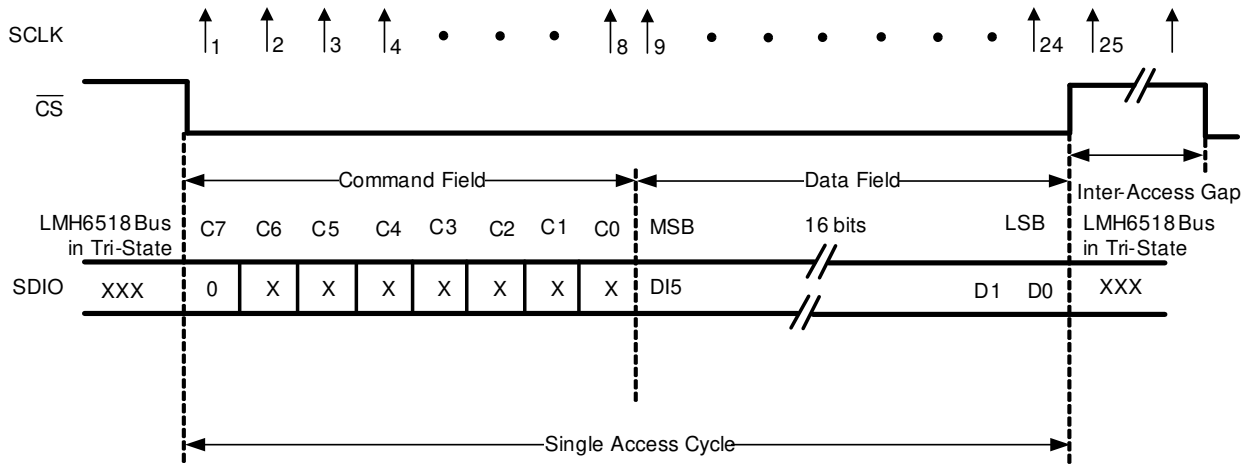
- Filters (20 MHz, 100 MHz, 200 MHz, 350 MHz, 650 MHz, 750 MHz, or full bandwidth)
- Power mode (full power or auxiliary high impedance, Hi-Z)
- Preamp (HG or LG)
- Attenuation ladder (0 dB to 20 dB, 10 states)
- LMH6518 state *write* or *read* back

The SPI bus uses 3.3-V logic. *SDIO* is the serial digital input-output that writes to or reads back from the LMH6518. *SCLK* is the bus clock with chip-select function controlled by  $\overline{CS}$ .



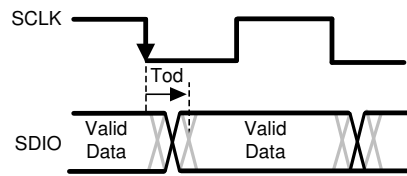
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**图 6-1. Serial Interface Protocol, Read Operation**

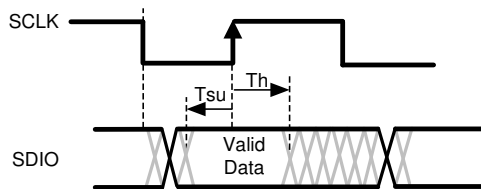


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**图 6-2. Serial Interface Protocol, Write Operation**



**图 6-3. Read Timing**



**图 6-4. Write Timing**

**表 6-1. Data Field**

							FILTER					PREAMP	LADDER ATTENUATION			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
X	0	0	0	0	0 = Full power 1 = Aux Hi-Z	0	See 表 6-3			0	0 = LG 1 = HG	See 表 6-4				

**备注**

Bits D5, D9, and D11 to D14 must be 0. Otherwise, device operation is undefined and specifications are not valid.

**表 6-2. Default Power-On Reset Condition**

							FILTER					PREAMP	LADDER ATTENUATION			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	

**表 6-3. Filter Selection Data Field**

FILTER			BANDWIDTH (MHz)
D8	D7	D6	
0	0	0	Full
0	0	1	20
0	1	0	100
0	1	1	200
1	0	0	350
1	0	1	650
1	1	0	750
1	1	1	Unallowed

**备注**

All filters are low-pass, single pole roll-off and operate on both main and auxiliary outputs. These filters are intended as signal path bandwidth and noise limiting.

表 6-4. Ladder Attenuation Data Field

LADDER ATTENUATION				BANDWIDTH (dB)
D3	D2	D1	D0	
0	0	0	0	0
0	0	0	1	-2
0	0	1	0	-4
0	0	1	1	-6
0	1	0	0	-8
0	1	0	1	-10
0	1	1	0	-12
0	1	1	1	-14
1	0	0	0	-16
1	0	0	1	-18
1	0	1	0	-20
1	0	1	1	Unallowed
1	1	0	0	Unallowed
1	1	0	1	Unallowed
1	1	1	0	Unallowed
1	1	1	1	Unallowed

## 备注

An *unallowed* SPI state can result in undefined operation where device behavior is not valid.



## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

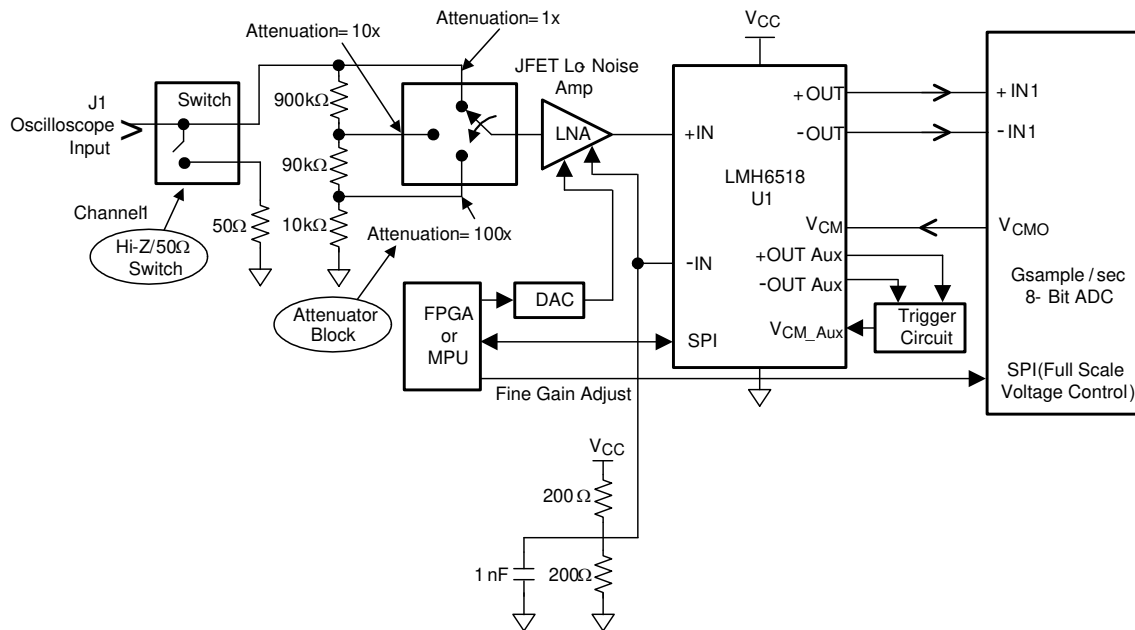
### 7.1 Application Information

The LMH6518 device is an excellent choice for applications that require a differential signal path and drive a differential, high-bandwidth analog-to-digital converter. The LMH6518 has 900 MHz of bandwidth and drives signals up to  $1.8 V_{PP}$ .

Typical applications for the LMH6518 include an oscilloscope AFE, gain control in a radio receiver, and a data-acquisition system.

### 7.2 Typical Application

#### 7.2.1 Oscilloscope Front End



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图 7-1. Digital Oscilloscope Front-End

#### 7.2.1.1 Design Requirements

An oscilloscope is used to sample signals from millivolts to volts. To make the best use of the limited ADC input range, the oscilloscope input circuitry must have a wide gain range.

In this design example, the LMH6518 is driving an ADC12J2700 and has the following requirements:

- Common mode voltage = 1.225-V
- Full scale voltage = 650 mV<sub>PP</sub> to 800 mV<sub>PP</sub>
- Bandwidth = 900-MHz
- Trigger channel
- Spurious free dynamic range = 50-dB

### 7.2.1.2 Detailed Design Procedure

图 7-2 shows a block diagram of the LMH6518 main output signal path.

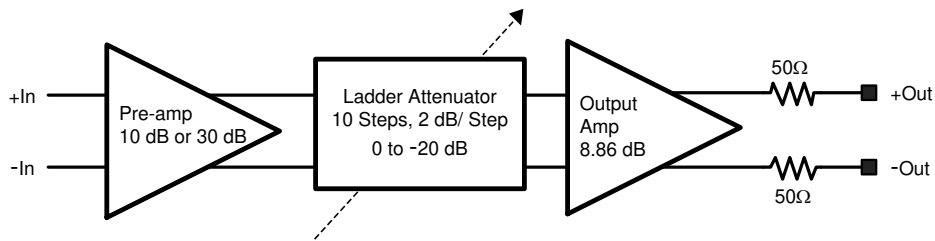


图 7-2. LMH6518 Signal Path Block Diagram

The auxiliary output (not shown) uses another but similar output amplifier that taps into the ladder attenuator output. In this data sheet, preamp gain of 30 dB is referred to as high gain (HG), and preamp gain of 10 dB as low gain (LG).

The LMH6518 2-dB/step gain resolution and 40-dB adjustment range (from  $-1.16$  dB to  $38.8$  dB). These specifications allow this device to be used with the TI GPS ADCs, which have full scale (FS) adjustment through the extended control mode (ECM) to provide near-continuous variability (8.5-mdB resolution) that covers 42.6-dB FS input range using 方程式 1.

$$(20 \times \log \frac{920 \text{ mV}_{PP}}{6.8 \text{ mV}_{PP}} = 42.6 \text{ dB}) \quad (1)$$

TI's GPS ECM control allows the ADC FS to be set using the ADC SPI bus. The ADC FS voltage range is from 560 mV to 840 mV with 9 bits of FS voltage control.

The ADC ECM gain resolution is calculated with 方程式 2.

$$\text{Gain Resolution} = 20 \log \frac{0.56 + \left( \frac{0.84 - 0.56}{2 \times 512} \right)}{0.56 - \left( \frac{0.84 - 0.56}{2 \times 512} \right)} = 8.5 \text{ mdB} \quad (2)$$

However, the *recommended* ADC FS operating range is narrower: from 595 mV to 805 mV with  $700 \text{ mV}_{PP}$  as the midpoint. Raising the value of ADC FS voltage is tantamount to reducing the signal path gain to accommodate a larger input and vice versa, thus providing a method of gain fine-adjust. The ADC ECM gain adjustment is  $-1.21$ -dB, as in 方程式 3.

$$\begin{aligned} & (= 20 \times \log \frac{700 \text{ mV}}{805 \text{ mV}}) \text{ to } +1.41 \text{ dB} \\ & (= 20 \times \log \frac{700 \text{ mV}}{595 \text{ mV}}) \end{aligned} \quad (3)$$

The ADC FS fine-adjust range of 2.62 dB (= 1.41 dB + 1.21 dB) is larger than the LMH6518 2-dB/step resolution; therefore, there is always at least one LMH6518 gain setting to accommodate any FS signal from 6.8 mV<sub>PP</sub> to 920 mV<sub>PP</sub> at the LMH6518 input, with 0.62-dB (= 2.62-2) overlap.

Assuming a nominal 0.7-V<sub>PP</sub> output, the LMH6518 minimum FS input swing is limited by the maximum signal path gain possible and vice versa with [方程式 4](#).

$$\text{Maximum LMH6518 FS Input } \frac{0.7 V_{PP}}{10^{\left(\frac{(38.8 + 1.41) \text{ dB}}{20}\right)}} = 6.8 \text{ mV}_{PP} \quad (4)$$

(or 8 mV<sub>PP</sub> with no ADC fine adjust in [方程式 5](#))

$$\text{Maximum LMH6518 FS Input } \frac{0.7 V_{PP}}{10^{\left(\frac{(-1.16 - 1.21) \text{ dB}}{20}\right)}} = 920 \text{ mV}_{PP} \quad (5)$$

(or 800 mV<sub>PP</sub> with no ADC FS adjust)

To accommodate a higher FS input, an additional attenuator is required before the LMH6518. This front-end attenuator is shown in the [图 7-1](#) with details shown in [图 7-12](#). The highest minimum attenuation level is determined by the largest FS input signal (FS<sub>max</sub>) in [方程式 6](#).

$$\text{Attenuation (dB)} = 20 \times \log \frac{FS_{MAX} (V_{PP})}{800 \text{ mV}_{PP}} \quad (6)$$

Therefore, to accommodate 80 V<sub>PP</sub>, a 40-dB minimum attenuation is required before the LMH6518.

In a typical oscilloscope application, the voltage range encountered is from 1 mV/DIV to 10 V/DIV with eight vertical divisions visible on the screen. One of the primary concerns in a digital oscilloscope is SNR that translates to display trace width to thickness. Typically, oscilloscope manufacturers require the noise level to be low enough so that the *no-input* visible trace width is less than 1% of FS. Experience shows that this corresponds to a minimum SNR of 52 dB.

The factors that influence SNR are:

- Scope front-end noise (Front-end attenuator + scope probe Hi-Z buffer which is discussed later in this data sheet and shown in [图 7-1](#))
- LMH6518
- ADC

The LMH6518 related SNR factors are:

- Bandwidth
- Preamp used (Preamp HG or LG)
- Ladder attenuation
- Signal level

SNR increases with the inverse square root of the bandwidth. Therefore, reducing bandwidth from 450 MHz to 200 MHz for example, improves SNR by 3.5-dB, as seen in [方程式 7](#).

$$\left(20 \times \log \frac{\sqrt{450 \text{ MHz}}}{\sqrt{200 \text{ MHz}}}\right) = 3.5 \text{ dB} \quad (7)$$

The other factors listed previously, preamp and ladder attenuation, depend on the signal level and also impact SNR. The combined effect of these factors is summarized in 图 7-3, where SNR is plotted as a function of the LMH6518 FS input voltage (assuming scope bandwidth of 200-MHz) and not including the ADC and the front-end noise.

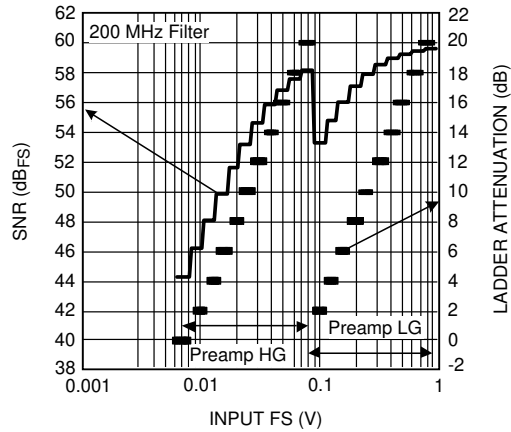


图 7-3. LMH6518 SNR and Ladder Attenuation Used vs Input

As 图 7-3 shows, SNR of at least 52 dB is maintained for FS inputs greater than 24 mV<sub>PP</sub> (3 mV/DIV on a scope) assuming the LMH6518 internal 200-MHz filter is enabled. Most oscilloscope manufacturers relax the SNR specifications to 40 dB for the highest gain (lowest scope voltage setting). From 图 7-3, the LMH6518 minimum SNR is 43.5 dB, thereby meeting the relaxed SNR specification for the lower range of scope front panel voltages.

In 图 7-3, the step change in SNR near Input FS of 90 mV<sub>PP</sub> is the transition point from preamp LG to preamp HG with a subsequent 3-dB difference due to the preamp HG to 20-dB ladder attenuation lower output noise compared to preamp LG to 2-ddB ladder attenuation noise. Judicious choice of front-end attenuators maintains the 52-dB SNR specification for scope FS inputs  $\geq 24$  mV<sub>PP</sub> by confining the LMH6518 gain range to the lower 30.5-dB using 方程式 8 from the total range of 40-dB ( $= 38.8 - (-1.16)$ ) is possible.

$$\left( = 20 \times \log \frac{0.8 V_{PP}}{24 \text{ mV}_{PP}} \right) \quad (8)$$

For example, to cover the range of 1 mV/DIV to 10 V/DIV (80-dB range), 表 7-1 lists a configuration that affords good SNR.

表 7-1. Oscilloscope Example Including Front-End Attenuators

ROW	SCOPE FS INPUT (V <sub>PP</sub> )	S, SCOPE VERTICAL SCALE (V/DIV)	PREAMP	LADDER ATTENUATION RANGE (dB)	A, FRONT-END ATTENUATION (V/V)	MINIMUM SNR (dB) WITH 200 MHz FILTER
1	8 m to 24 m	1 m to 3 m	HG	0 to 10	1	44
2	24 m to 80 m	3 m to 10 m	HG	10 to 20	1	52
3	80 m to 0.8	10 m to 0.1	LG	0 to 20	1	53.4
4	0.8 to 8	0.1 to 1	LG	0 to 20	10	53.4
5	8 to 80	1 to 10	LG	0 to 20	100	53.4

In 表 7-1, the highest FS input in row 5, column 2 (80 V<sub>PP</sub>), and the LMH6518 highest FS input allowed (0.8 V<sub>PP</sub>) set the front-end attenuator value with 方程式 9.

$$100\times \left( = \frac{80 V_{PP}}{0.8 V_{PP}} \right)$$

(9)

The 100 × attenuator allows high-SNR operation down to 30.5-dB, as explained earlier, or 2.4 V<sub>PP</sub> at scope input. In that same table, rows 1 to 3 with no front-end attenuation (1 ×) cover the scope FS input range from 8 mV<sub>PP</sub> to 800 mV<sub>PP</sub>. That leaves the scope FS input range of 0.8 V<sub>PP</sub> to 2.4 V<sub>PP</sub>. If the 100 × attenuator is used for the entire scope FS range of 0.8 V<sub>PP</sub> to 80 V<sub>PP</sub>, SNR dips below 52-dB for a portion of that range. Another attenuation level is thus required to maintain the SNR specification requirement of 52 dB.

One possible attenuation partitioning is to select the additional attenuator value to cover a 20 dB range above 0.8 V<sub>PP</sub> FS (to 8 V<sub>PP</sub>) with the 100 × attenuator covering the remaining 20-dB range from 8 V<sub>PP</sub> to 80 V<sub>PP</sub>. Mapping 8 V<sub>PP</sub> FS scope input to 0.8 V<sub>PP</sub> at LMH6518 input means the additional attenuator is 10 ×, as shown in [表 7-1](#), row 4. The remaining scope input range of 8 V<sub>PP</sub> to 80 V<sub>PP</sub> is then covered by the 100 × front-end attenuator derived earlier. The entire scope input range is now covered with SNR maintained approximately 52 dB for a scope FS input ≥ 24 mV<sub>PP</sub>, as shown in [表 7-1](#).

#### 7.2.1.2.1 Settings and ADC SPI Code (ECM)

Covering the range from 1 mV/div to 10 V/div requires the following adjustment within the digital oscilloscope:

- Front-end attenuator
- LMH6518 preamp
- LMH6518 ladder attenuation
- ADC FS value (ECM)

The LMH6518 product folder contains a spreadsheet that helps calculate the front-end attenuator, LMH6518 preamp gain (HG or LG), ladder attenuation, and ADC FS setting based on the scope vertical scale (S in V/div).

The following step-by-step procedure explains the operations performed by the spreadsheet based on the scope vertical scale setting (S in V/div) and front-end attenuation A (from [表 7-1](#)). A numerical example is also worked out for more clarification:

1. Determine the required signal path gain, K, with [方程式 10](#):

$$K = 20 \times \log \frac{0.95 \times 700 \text{ mV}_{PP}}{8 \times S(\text{V/div})} = -21.6 + 20 \times \log \frac{A}{S(\text{V/div})} \quad (10)$$

Assuming the full-scale signal occupies 95% of the 0.7 V<sub>PP</sub> FS for 5% overhead that occupies eight vertical scope divisions.

Required condition:  $-2.37 \text{ dB} \leq K \leq 40.3 \text{ dB}$

Example: With S = 110 mV/div, [表 7-1](#) shows that A = 10 V/V in [方程式 11](#).

$$\rightarrow K = -21.6 + 20 \times \log \frac{10}{110 \text{ mV}} = 17.57 \text{ dB} \quad (11)$$

2. Determine the LMH6518 gain, G:

G is the closest LMH6518 gain to the value of K where

- $G = (38.8 - 2n)\text{dB}; n = 0, 1, 2, \dots, 20$

For this example, the closest G to K = 17.57 dB is 16.8 dB (with n = 11). The next LMH6518 gain, 18.8 dB (with n = 10) is incorrect as 16.8 is closer. If 18.8 dB were mistakenly selected, the ADC FS setting is out of range. Therefore, G = 16.8 dB

3. Determine preamp (HG or LG) and ladder attenuation:

- If  $G \geq 18.8 \text{ dB} \rightarrow$  Preamp is HG and ladder attenuation =  $38.8 - G$
- If  $G < 18.8 \text{ dB} \rightarrow$  Preamp is LG and ladder attenuation =  $18.8 - G$

For this example, with G = 16.8 → *Preamp LG and Ladder Attenuation = 2 dB (= 18.8 to 16.8)*.

4. Determine the required ADC FS voltage,  $FS_E$ , with [方程式 12](#):

$$FS_E = \frac{S \times 8}{A} \times 1.05 \times 10^{\frac{G}{20}} \tag{12}$$

The 1.05 factor is to add 5% FS overhead margin to avoid ADC overdrive with [方程式 13](#).

$$FS_E = \frac{S \times 8}{10} \times 1.05 \times 10^{\frac{16.8}{20}} = 639.3 \text{ mV} \tag{13}$$

Required condition:  $0.56 \text{ V} \leq FS_E \leq 0.84 \text{ V}$

Recommend condition:  $0.595 \text{ V} \leq FS_E \leq 0.805 \text{ V}$  for optimum ADC FS

5. Determine the ADC ECM code ratio with [方程式 14](#):

$$ECM \text{ (ratio)} = \frac{FS_E - 0.56}{0.28} \tag{14}$$

where

- $0.28 \text{ V} = (0.84 - 0.56) \text{ V}$
- $0.56 \text{ V}$  is the lower end of the ADC FS adjustability

For this example:

$$ECM \text{ (ratio)} = \frac{0.6393 - 0.56}{0.28} = 0.283$$

Required condition:  $0 \leq ECM \text{ (ratio)} \leq 1$

6. Determine the ECM binary code sent on ADC SPI bus:

- Convert the ECM value represented by the ratio calculated previously, to binary:
- $ECM \text{ (binary)} = DEC2BIN\{ECM(\text{ratio}) \times 511, 9\}$   
where *DEC2BIN* is a spreadsheet function that converts the decimal ECM ratio, from step 5, multiplied by 511 distinct levels, into binary 9 bits.

**备注**

The web-based spreadsheet computes ECM without the use of *DEC2BIN* function to ease use by all spreadsheet users who do not have this function installed.

For this example:  $ECM \text{ (binary)} = DEC2BIN(0.283 \times 511, 9) = 010010000$ . This number is sent to the ADC on the SPI bus to program the ADC to proper FS voltage.

**7.2.1.2.2 Input and Output Considerations**

The LMH6518 ideal input and output conditions, considered individually, are listed in [表 7-2](#).

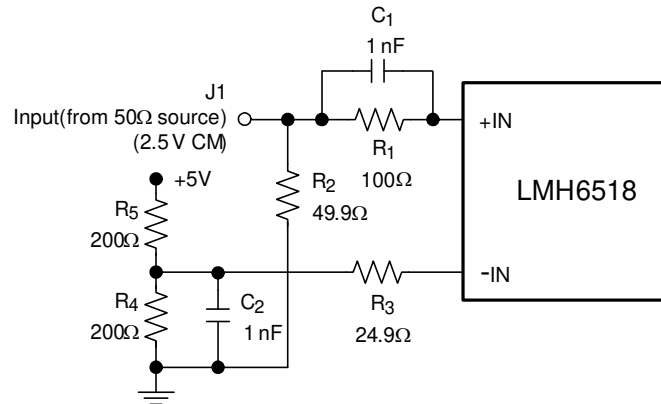
**表 7-2. LMH6518 Ideal Input and Output Conditions**

IMPEDANCE FROM EACH INPUT TO GROUND ( $\Omega$ )	COMMON MODE INPUT (V)	DIFFERENTIAL INPUT ( $V_{PP}$ )	LOAD IMPEDANCE ( $\Omega$ )	DIFFERENTIAL OUTPUT (V)	COMMON MODE OUTPUT (V)
$\leq 50$	1.5 to 3.1	$< 0.8$	100 (differential) and 50 (single-ended)	$< 0.77$	0.95 to 1.45

In addition to the individual conditions listed in [表 7-2](#), the input and output terminal conditions must match differentially (that is, +IN to -IN and +OUT to -OUT), as well, for best performance.

The input is differential but is driven single-ended as long as the conditions of [表 7-2](#) are met, and there is good matching between the driven and undriven inputs from DC to the highest frequency of interest. If not, there is a settling time impact among other possible performance degradations. The data-sheet specifications are with

single-ended input, unless specified. 图 7-4 is the recommended bench-test schematic to drive one input and to bias the other input with good matching in mind.

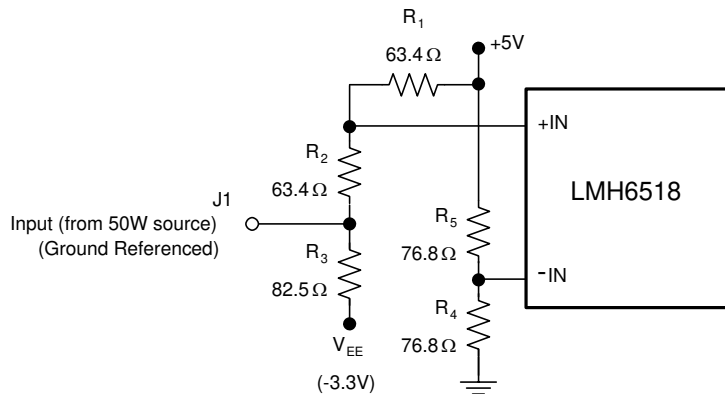


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图 7-4. Recommended Single-Ended Bench-Test Input Drive from 50-Ω Source

With 图 7-4, each LMH6518 input sees 25-Ω to ground at higher frequencies when the capacitors look like shorts. This impedance increases to 125-Ω at DC for both inputs, thereby preserving the required matching at any frequency. This configuration, using properly selected R's and C's, allows four times less biasing power dissipation than when undriven inputs are biased with an effective 25-Ω from the LMH6518 input to ground.

Driving the LMH6518 input from a ground-referenced, 50-Ω source is possible by providing level shift circuitry on the driven input. 图 7-5 shows a circuit where half the input signal reaches the LMH6518 input, while the negative supply voltage ( $V_{EE}$ ) prevents biasing current on the 50-Ω source at J1 while providing 50-Ω termination to the source. The driven input (+IN) is biased to 2.5-V ( $V_{CC}/2$ ) in 图 7-5.



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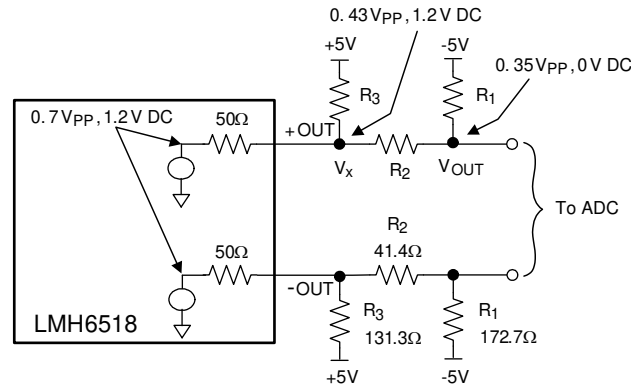
图 7-5. LMH6518 Driven by a Ground-Referenced Source

In 图 7-5, the equivalent impedance from each LMH6518 input to ground is around 38-Ω. The power consumption of this configuration is approximately 0.5 W (in  $R_1 - R_5$ ) which is higher than that of 图 7-4 because of additional power dissipated to perform the level shifting. Additional 50-Ω attenuators is placed between J1 and  $R_2/R_3$  junction in 图 7-5 to accommodate higher input voltages.

Shifting the LMH6518 *output* common mode level is also possible by using a level shift approach similar to that of 图 7-5. The circuit in 图 7-6 shows an implementation where the LMH6518 nominal 1.2-V CM output, set by a



1.2-V on  $V_{CM}$  input from the GPS ADC, is shifted lower for proper interface to different ADCs (which require  $V_{CM} = 0\text{-V}$  and have high input impedance).



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图 7-6. Output CM Shift Scheme

In 图 7-6,  $V_x$  is kept at 1.2-V by proper selection of external resistor values, so that the LMH6518 outputs are not CM-loaded. As was the case with input level shifting, this output-level shifting also consumes additional power (0.58 W).

#### 7.2.1.2.2.1 Output Swing, Clamping, and Operation Beyond Full Scale

One of the major concerns when interfacing to low-voltage ADCs (such as the GPS ADC that the LMH6518 is intended to drive) is to ensure that the ADC input is not violated with excessive drive. For this reason, plus the important requirement that an oscilloscope recovers quickly and gracefully from an overdrive condition, the LMH6518 is fitted with three overvoltage clamps: one at the preamp output, and one each at the main and auxiliary outputs. The preamp clamp is responsible for preventing the preamp from saturation (to minimize recovery time) with large ladder attenuation when preamp output swing is highest. Alternatively, the output clamps perform this function when ladder attenuation is lower. Therefore, the output amplifier is closer to saturation and prolonged recovery (if not properly clamped). The combination of these clamps results in 图 5-50, 图 5-51, 图 5-52, and 图 7-9. With these four graphs, observe where output limiting starts due to the clamp action. LMH6518 owes the fast recovery time ( $< 5\text{ ns}$ ) from 50% overdrive to these clamps.

图 5-50, 图 5-51, 图 5-52, and 图 7-9 in 节 5.7 are used to determine the LMH6518 linear swing beyond full scale. This information sets the overdrive limit for both oscilloscope waveform capture and signal triggering. The preamp clamp is set tighter than the output clamp, evidenced by lower output swing with 20-dB ladder attenuation than with 0 dB. With high ladder attenuation (20 dB) defining the limit, the graphs show that the +OUT and -OUT difference of 0.4-V is well inside the clamp range, thereby providing 0.8  $V_{PP}$  of unhindered output swing. This corresponds to an overdrive capability of approximately  $\pm 7\%$  beyond full scale.

From 图 7-1, the signal path consists of the input impedance switch, the attenuator switch, low-noise amplifier (LNA, JFET amplifier) to drive the LMH6518 input (+IN), and the DAC to provide offset adjust. The LNA must have the following characteristics:

- Set the U1 common-mode level to  $V_{CC} / 2$  (approximately 2.5 V)
- Low drift (1-mV shift at LNA output can translate into 88-mV shift at the LMH6518 output at maximum gain, or approximately 13% of FS)
- Low output impedance ( $\leq 50\ \Omega$ ) to drive U1 for good settling behavior
- Low noise ( $< 0.98\text{ nV}/\sqrt{\text{Hz}}$ ) to reduce the impact on the LMH6518 noise figure. Be aware that 图 7-1 does not show the necessary capacitors across the resistors in the front-end attenuators (see 图 7-12). These capacitors provide frequency response compensation and limit the noise contribution from the resistors so that the resistors do not impact the signal path noise. For more information about front-end attenuator design, including frequency compensation, see 节 8.2.1 for additional resources.

- Gain of 1 V/V (or close to 1 V/V)
- Excellent frequency response flatness from dc to > 500 MHz to 800 MHz to not impact the time domain performance

The undriven input (–IN) is biased to  $V_{CC} / 2$  using a voltage driver. The impedance driving the LMH6518 –IN pin must be closely matched to the LNA output impedance for good settling-time performance.

§ 7.2.2 shows one possible implementation of the LNA buffer along with performance data.

When the LMH6518 auxiliary output is not used, this output can be disabled using the SPI (see § 6.5.1 for the SPI register map). § 5.5 shows that by disabling this output, device power dissipation decreases by the reduction in supply current of approximately 60 mA. 图 7-7 shows that in the absence of heavy common loading, the auxiliary output is at a voltage close to 1.7 V ( $V_{CC} = 5$  V). With higher supply voltages, the auxiliary voltage also increases. Ensure that any circuitry tied to this output is capable of handling the 2.3 V possible under  $V_{CC}$  worst-case condition of 5.5 V.

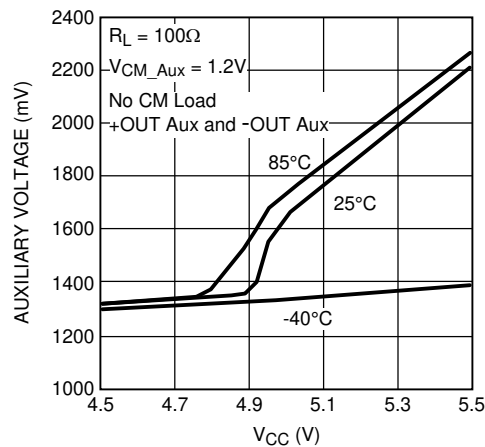


图 7-7. Auxiliary Output Voltage as a Function of  $V_{CC}$

### 7.2.1.2.3 Oscilloscope Trigger Applications

With the auxiliary output of the LMH6518 offering a second output that follows the main one (except for a slightly reduced distortion performance), the oscilloscope trigger function is implemented by tapping this output. The auxiliary common mode is set with the  $V_{CM\_AUX}$  input of the LMH6518. If required, the trigger function is placed at a distance from the main signal path by taking advantage of the differential auxiliary output and rejecting any board-related common-mode interference pick-up at the receive end.

If trigger circuitry is physically close to the LMH6518, the circuit diagram shown in 图 7-8 allows operation using only one of two auxiliary outputs. Unused outputs require proper termination using  $R_1$ ,  $R_{11}$  combination. U3 (DAC101C085) generates a 0-V to 2.5-V trigger level, with 2.4-mV resolution as in 方程式 15 or 0.7% ( $= 2.4\text{-mV} \times 100/0.35 V_{PP}$ ) of FS, which is compared to the LMH6518 +OUT AUX by using an ultra-fast comparator, U2 (LMH7220). The U2 complimentary LVDS output is terminated in the required 100- $\Omega$  load ( $R_{10}$ ), for best performance, where the LVDS trigger output is available.

$$\left( = \frac{2.5\text{V}}{2^{10}} \right) \quad (15)$$

The LMH7220 offset voltage ( $\pm 9.5$  mV) and offset voltage drift ( $\pm 50\text{-}\mu\text{V}/^\circ\text{C}$ ) error is 5.9 LSB of the trigger DAC (U3) as in 方程式 16.

$$(9.5 \text{ mV} + 50 \frac{\mu\text{V}}{^{\circ}\text{C}} \times 100^{\circ}\text{C}) = 1.45 \text{ mV} \approx 5.9 \text{ LSB}$$

(16)

The offset voltage related portion of this error is nulled, if necessary, during the oscilloscope initial calibration. To do so, the LMH6518 input is terminated properly with no input applied and U3 output is adjusted around  $V_{CM\_Aux}$  voltage ( $1.2 \text{ V} \pm 10 \text{ mV}$ ) while looking for the U2 output transition. The U3 output, relative to  $V_{CM\_Aux}$  at transition corresponds to the U2 offset error, which is factored into the trigger readings and thus eliminated, leaving only the offset voltage temperature drift component ( $= 2 \text{ LSB}$ ).

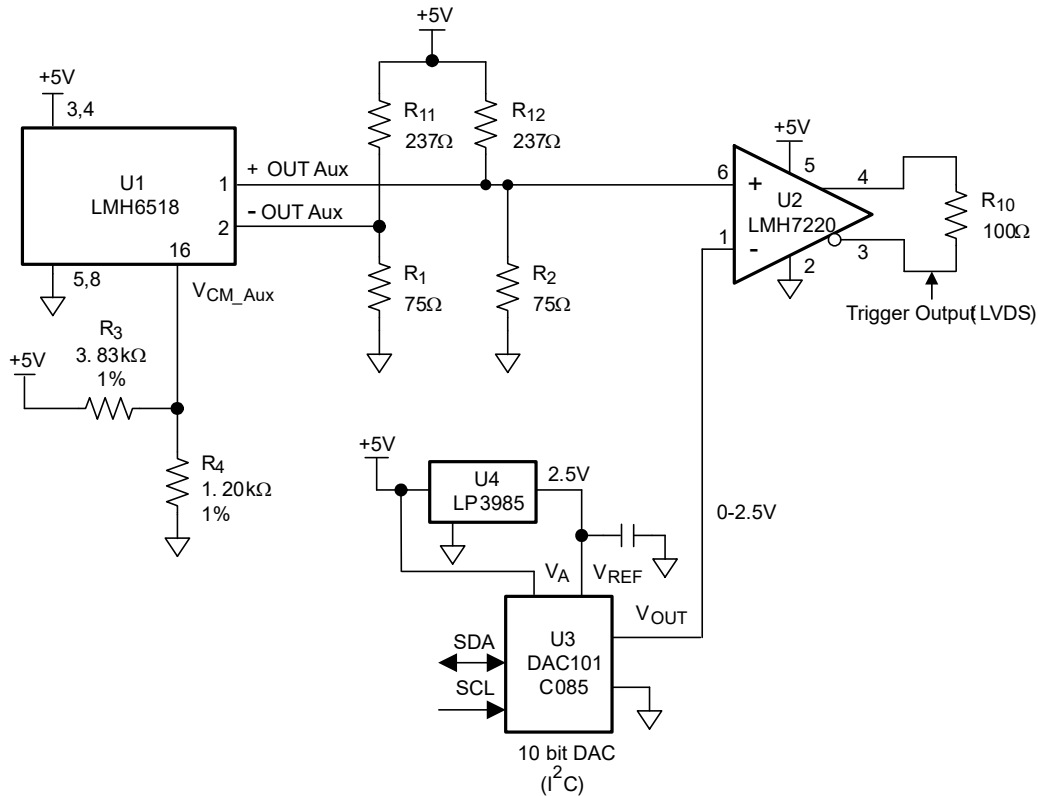


图 7-8. Single-Ended Trigger From the LMH6518 Auxiliary Output

The U2 minimum toggle rate specification of 750Mbps with  $\pm 50\text{-mV}$  overdrive allows the oscilloscope to trigger on repetitive waveforms much greater than the 500-MHz oscilloscope bandwidth applications, when the input signal is at least 14.3% of FS swing with [方程式 17](#).

$$\left( = \frac{50 \text{ mV}}{\frac{0.7 \text{ V}}{2}} \times 100 \right)$$

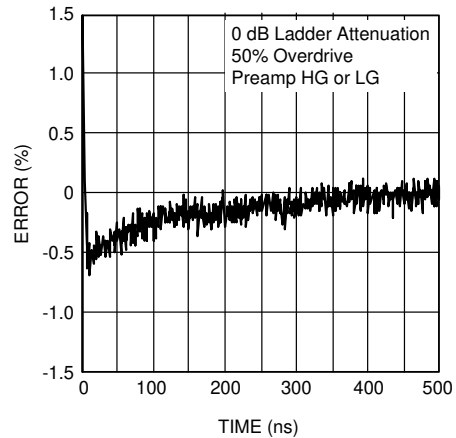
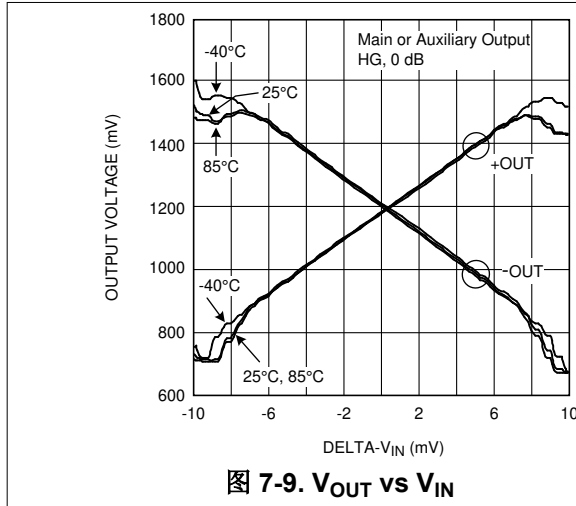
(17)

The worst-case, single-event, minimum-discernible pulse duration is set by the LMH7220 propagation delay specification of 3.63 ns (20-mV overdrive).

Both the main and the auxiliary outputs recover gracefully and quickly from a 50% overdrive condition, as tabulated in [节 5.5](#) under overdrive recovery time. However, overdrive conditions beyond 50% can result in longer recovery times due to the interaction between an internal clamp and the common-mode feedback loop that sets the output common-mode voltage. This long recovery time can have an impact on both the displayed waveform and the oscilloscope trigger. The result is a loss of trigger pulse or visual distortion of the displayed

waveform. To avoid this scenario, the oscilloscope must detect an excessive overdrive and go into trigger-loss mode. Done in this way, the oscilloscope display shows the last waveform that did not violate the overdrive condition. Preferably, there is a visual indicator on the screen that alerts the user of the excessive condition, and returns the display to normal after the condition is corrected.

### 7.2.1.3 Application Curves



### 7.2.2 JFET LNA Implementation

图 7-11 shows the schematic drawing for a possible implementation of the LNA buffer.

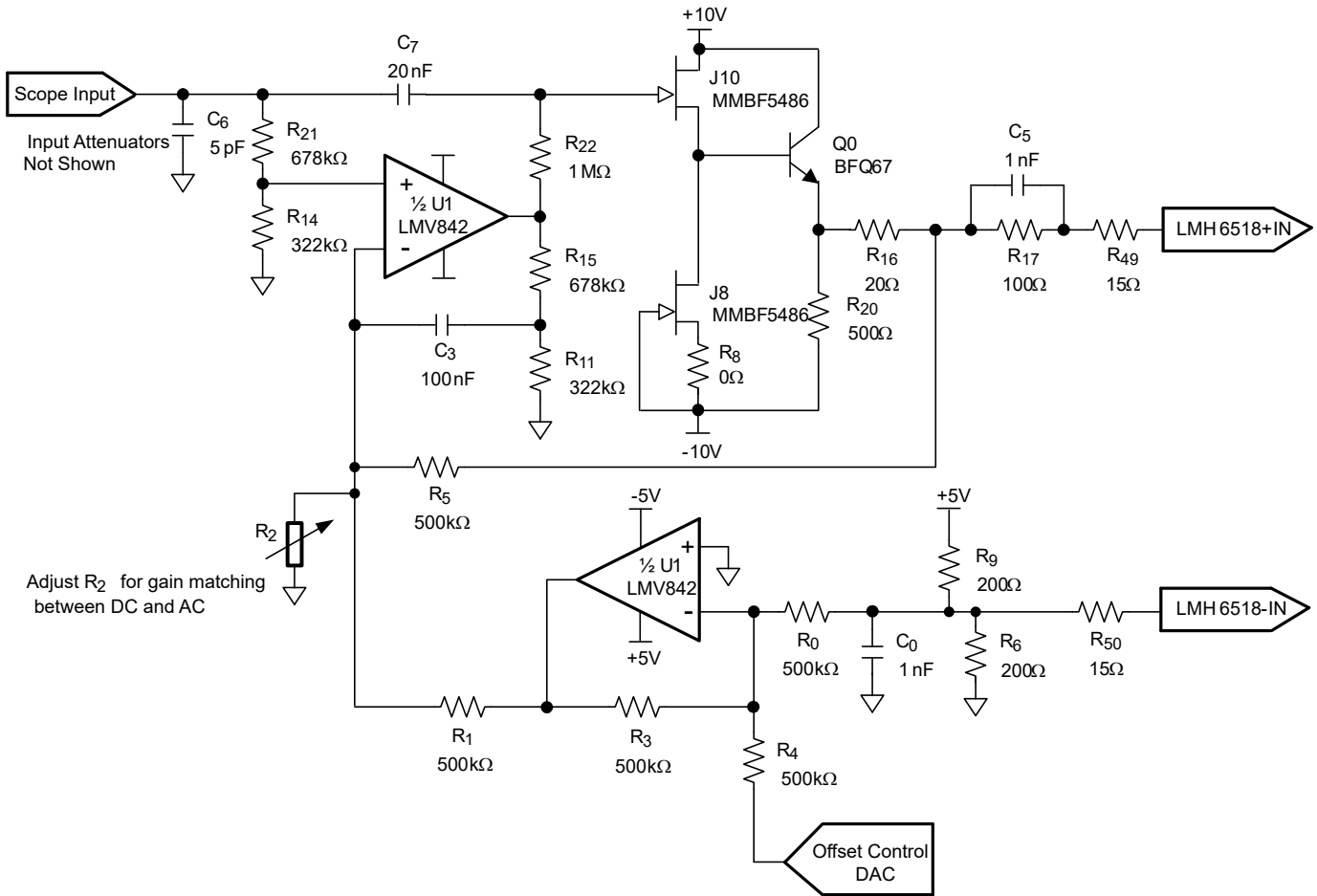


图 7-11. JFET LNA Implementation

### 7.2.2.1 Design Requirements

This circuit uses an N-Channel JFET (J10) in source-follower configuration to buffer the input signal with J8 acting as a constant current source. This buffer presents a fixed input impedance ( $1\text{ M}\Omega \parallel 10\text{ pF}$ ) with a gain close to  $1\text{-V/V}$ .

The signal path is ac-coupled through  $C_7$  with dc (and low frequency) at LMH6518 +IN maintained through the action of U1. NPN transistor Q0 is an emitter follower which isolates the buffer from the load (LMH6518 input and board traces).

The undriven input of the LMH6518 (-IN) is biased to 2.5-V by  $R_6$ ,  $R_9$  voltage divider. The lower half of U1 inverts this voltage and the upper half of U1 compares this voltage to the combination of the driven output level at LMH6518 +IN and the scaled version of scope input at  $R_{14}$ ,  $R_{21}$  junction, and adjusts J10 Gate accordingly to set the LMH6518 +IN. This control loop has a frequency response that covers dc to a few Hz, limited by roll-off capacitor  $C_3$  and  $R_{15}$  combination (first order approximation). DC and low-frequency gain is given by 方程式 18.

$$\text{Gain (DC)} = \frac{R_{14}}{R_{14} + R_{21}} \left( 1 + \frac{R_5}{R_1 \parallel R_2} \right) \cong 1\text{ V/V} \quad (18)$$

With the values in 图 7-11  $\rightarrow R_2$  approximately  $452\text{ k}\Omega$ .

For a flat frequency response, the dc (low frequency) gain requires lowering to match the less-than-1 V/V ac (high frequency) path gain through the JFETs. This is done by increasing the value of  $R_2$ .

Choose values of  $R_{15}$  and  $R_{11}$  so that the frequency response at J10 Gate (and consequently the output) remain flat when  $C_7$  starts to conduct as in [方程式 19](#).

$$\frac{R_{21}}{R_{14}} = \frac{R_{15}}{R_{11}} \quad (19)$$

Offset correction is done by varying the voltage at  $R_4$ , using a DAC or equivalent as shown, to shift the LMH6518 +IN voltage relative to -IN. The result is a circuit which shifts the ground referenced scope input to 2.5-V ( $V_{CC} / 2$ ) CM with adjustable offset and without any JFET or BJT related offsets.

The front-end attenuator (not shown) lower leg resistance is increased for proper divider-ratio to account for the 1-M $\Omega$  shunt due to the series combination of  $R_{21}$  and  $R_{14}$ . For example, a 10:1 front-end attenuator is formed by a series 900 k $\Omega$  and a shunt 111 k $\Omega$  for a scope BNC input impedance of 1 M $\Omega$  (= 900 K + (111 K || 1 M)).

[表 7-3](#) lists other possible JFET candidates that fall in the range of speed ( $f_t$ ) and low-noise requirement.

表 7-3. Selected JFET Candidates Specifications

COMPANY	PART NUMBER	V <sub>P</sub> (V)	I <sub>dss</sub> (mA)	gm (mS)	INPUT C (pF)	NOISE <sup>(1)</sup> (nV/RtHz)	BREAK DOWN (V)	CALCULATED f <sub>t</sub> (MHz)
Interfet	IF140	- 2.2	10	5.5	2.3	4	- 20	380
Interfet	IF142	- 2.2	10	5.5	2.3	4	- 25	380
Interfet	2N5397/8	- 2.5	13	8	5	2.5	- 25	254
Interfet	2N5911/2	- 2.5	13	8	5	2.5	—	254
Interfet	J308/9/10	- 2.3	21	17	5.8	—	- 25	466
Philips	BF513	- 3	15	10	5	—	—	318
Fairchild	MMBF5486	- 4	14	7	4	2.5	- 25	278
Vishay Siliconix	SST441	- 3.5	13	6	3.5	4	- 35	272

(1) Noise data at approximately I<sub>dss</sub> / 2.

The LNA noise can degrade the scope SNR if comparable to the input-referred noise of the LMH6518. LNA noise is influenced by the following operating conditions:

1. JFET equivalent input noise
2. BJT base current

Reducing either *a* or *b* above, or both, reduces noise. One way to reduce *a* is to increase R<sub>8</sub> (currently set to 0 Ω). This reduces the noise impact of J8 but requires a JFET which has a higher I<sub>dss</sub> rating to maintain the operating current of J10, so that the J10 noise contribution is minimized. Reducing the BJT base current is accomplished with increasing R<sub>20</sub> at the expenses of higher rise and fall times. A higher β also reduces the base current (keep in mind that β and f<sub>t</sub> at the operating collector current is what matters).

图 7-13 shows the impact of the JFET buffer noise on SNR, compared to SNR in 图 7-3, assuming either 3-nV/√ Hz or 1.5-nV/√ Hz buffer noise for comparison.

### 7.2.2.2 Detailed Design Procedure

#### 7.2.2.2.1 Attenuator Design

图 7-12 shows a front-end attenuator designed to work with 图 7-11.

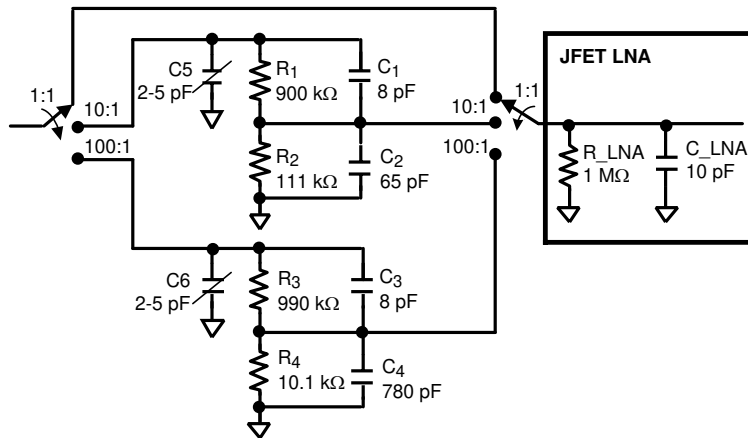


图 7-12. Front-End Attenuator for JFET LNA Implementation

$R_{LNA}$  and  $C_{LNA}$  are the input impedance components of the JFET LNA. The 10:1 and 100:1 attenuators bottom resistors ( $R_2$  and  $R_4$ ) are adjusted higher to compensate for the LNA  $1-M\Omega$  input impedance, compared to the case where a high-input-impedance LNA is used. The two switches used on the input and output of the attenuator block are low-capacitance, high-isolation switches to reduce any speed or crosstalk impact. Capacitors  $C_1$  to  $C_4$  provide the proper frequency response (and step response) by creating zeros that flatten the response for wide-band operation. For the 10:1 attenuator,  $R_1C_1 = R_2C_2$ . The same applies to the 100:1 attenuator. The shunt capacitors,  $C_1$  to  $C_4$ , have an important other benefit in that these capacitors roll off the resistor thermal noise at a low frequency (low-pass response,  $-3$ -dB down at approximately 20-kHz), thereby eliminating any significant noise contribution from the attenuation resistors. Otherwise, the channel noise is dominated by the attenuator resistor thermal noise. Adjust trimmer capacitors  $C_5$  and  $C_6$  to match the input capacitance regardless of attenuator used.

### 7.2.2.3 Application Curve

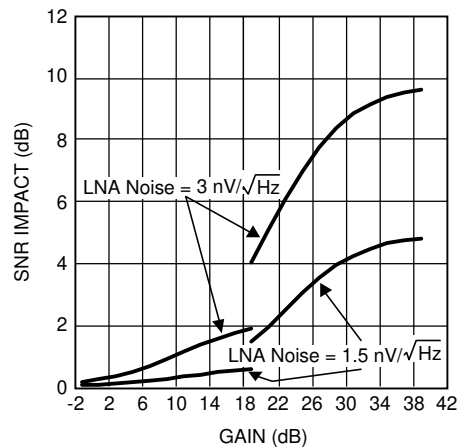


图 7-13. LNA Buffer SNR Impact

## 7.3 Power Supply Recommendations

The LMH6581 requires two power supplies. The analog signal path is powered by a single 5-V ( $\pm 5\%$ ) supply and the digital control is powered by a single 3.3-V ( $\pm 5\%$ ) supply. The 5-V supply must be capable of providing the 230-mA of quiescent current plus any load current. Make sure that the loads of both amplifiers are included.

The 3.3-V digital supply requires only a small, 400- $\mu$ A current.

Place supply bypass capacitors at pins 3, 4, and 12. Low-ESR, ceramic capacitors of 0.01- $\mu$ F are recommended.

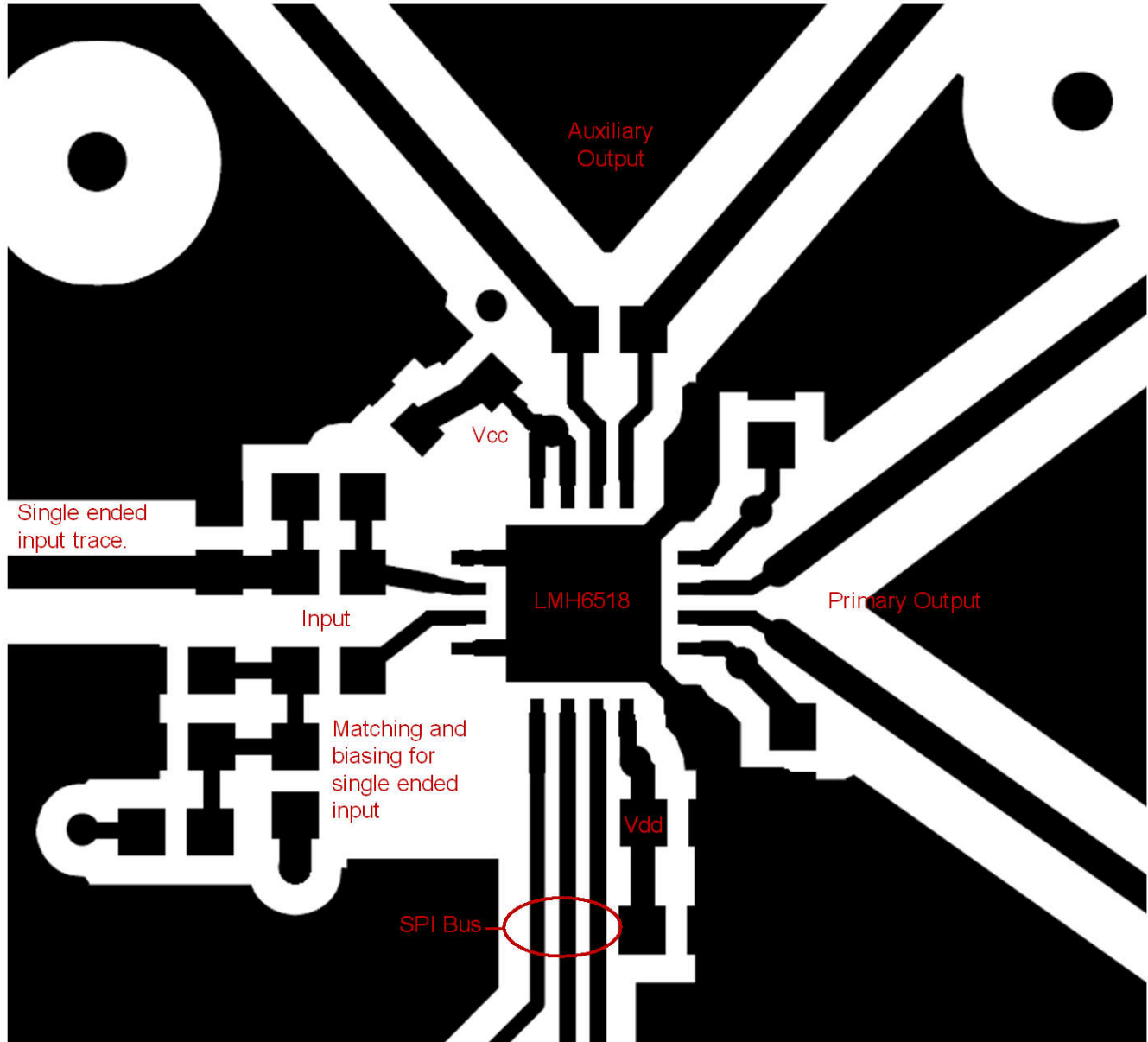


## 7.4 Layout

### 7.4.1 Layout Guidelines

Layout is critical to achieve specified performance. Circuit symmetry is necessary for good HD2 performance. Input traces must have impedance-controlled transmission lines. To reduce output to input coupling, use ground plane to fill between the amplifier input and output traces. Output termination resistors are provided on chip internally to the LMH6518. When driving an ADC, the ADC must be placed physically close to the LMH6518 output pins. Use controlled impedance transmission lines if the ADC must be placed farther than 10 mm from the amplifier output pins.

### 7.4.2 Layout Example



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图 7-14. LMH6518 Layout Schematic

## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 第三方产品免责声明

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#### 8.1.2 Device Nomenclature

表 8-1. Definition of Terms and Specifications

TERM	DEFINITION
$A_{V\_CM}$ (dB)	Change in output offset voltage ( $\Delta V_{OOS}$ ) with respect to the change in input common-mode voltage ( $\Delta V_{I\_CM}$ )
$A_{V\_DIFF}$ (dB)	Gain with 100- $\Omega$ differential load
CM	Common mode
CMRR (dB)	Common-mode rejection defined as: $A_{V\_DIFF}$ (dB) - $A_{V\_CM}$ (dB)
CMRR_CM	Common-mode rejection relative to $V_{CM}$ defined as: $\Delta V_{OOS} / \Delta V_{CM}$
HG	Preamp high gain
Ladder	Ladder attenuator setting (0 dB to 20 dB)
LG	Preamp low gain
Max Gain	Gain = 38.8 dB
Min Gain	Gain = -1.16 dB
+OUT	Positive main output
-OUT	Negative main output
+OUT AUX	Positive auxiliary output
-OUT AUX	Negative auxiliary output
PB	Phase balance defined as the phase difference between the complimentary outputs relative to 180°
PSRR	Input-referred $V_{OOS}$ shift divided by change in $V_{CC}$
PSRR_CM	Output common-mode voltage change ( $\Delta V_{O\_CM}$ ) with respect to $V_{CC}$ voltage change ( $\Delta V_{CC}$ )
$V_{CM}$	Input pin voltage that sets main output CM
$V_{CM\_Aux}$	Input pin voltage that sets auxiliary output CM
$V_{I\_CM}$	Input CM voltage (average of +IN and -IN)
$\Delta V_{IN}$ (V)	Differential voltage across device inputs
$V_{OOS}$	DC offset voltage. Differential output voltage measured with inputs shorted together to $V_{CC} / 2$
$V_{O\_CM}$	Output common-mode voltage (dc average of $V_{+OUT}$ and $V_{-OUT}$ )
$V_{OS\_CM}$	CM offset voltage: $V_{O\_CM} - V_{CM}$
$\Delta V_{O\_CM}$	Variation in output common-mode voltage ( $V_{O\_CM}$ )
$\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$	Balance error. Measure of the output swing balance of +OUT and -OUT, as reflected on the output common-mode voltage ( $V_{O\_CM}$ ), relative to the differential output swing ( $V_{OUT}$ ). Calculated as output common-mode voltage change ( $\Delta V_{O\_CM}$ ) divided by the output differential voltage change ( $\Delta V_{OUT}$ , which is nominally around 700 mV <sub>PP</sub> )
$\Delta V_{OUT}$	Change in differential output voltage (corrected for dc offset, $V_{OOS}$ )

### 8.2 Documentation Support

#### 8.2.1 Related Documentation

For related documentation see the following:

*Wideband Amplifiers* by Peter Staric and Erik Margan, published by Springer (2006). (Section 5.2)

#### 8.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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## 8.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision D (September 2016) to Revision E (July 2024)</b>	<b>Page</b>
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Updated text for clarity in <i>Pin Configurations and Functions</i> .....	3
• Updated note 1 text for clarity in the <i>Absolute Maximum Ratings</i> .....	4
• Added note 2 in the <i>Absolute Maximum Ratings</i> .....	4
• Added new row for maximum dc output <i>Absolute Maximum Ratings</i> .....	4
• Updated last sentence in paragraph for clarity in <i>Layout Guidelines</i> .....	41

<b>Changes from Revision C (July 2013) to Revision D (September 2016)</b>	<b>Page</b>
• 添加了 <i>ESD</i> 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Added <i>Thermal Information</i> table.....	4
• Changed Y-axis unit on Output vs Input <i>Typical Characteristics</i> graphs From: (V) To: (mV).....	11
• Changed Y-axis unit on $V_{OUT}$ vs $V_{IN}$ <i>Application Curves</i> graph From: (V) To: (mV).....	36

<b>Changes from Revision A (March 2013) to Revision B (March 2013)</b>	<b>Page</b>
• 将美国国家半导体数据表的布局更改为 TI 格式.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6518SQ/NOPB	ACTIVE	WQFN	RGH	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ	<a href="#">Samples</a>
LMH6518SQE/NOPB	ACTIVE	WQFN	RGH	16	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ	<a href="#">Samples</a>
LMH6518SQX/NOPB	ACTIVE	WQFN	RGH	16	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



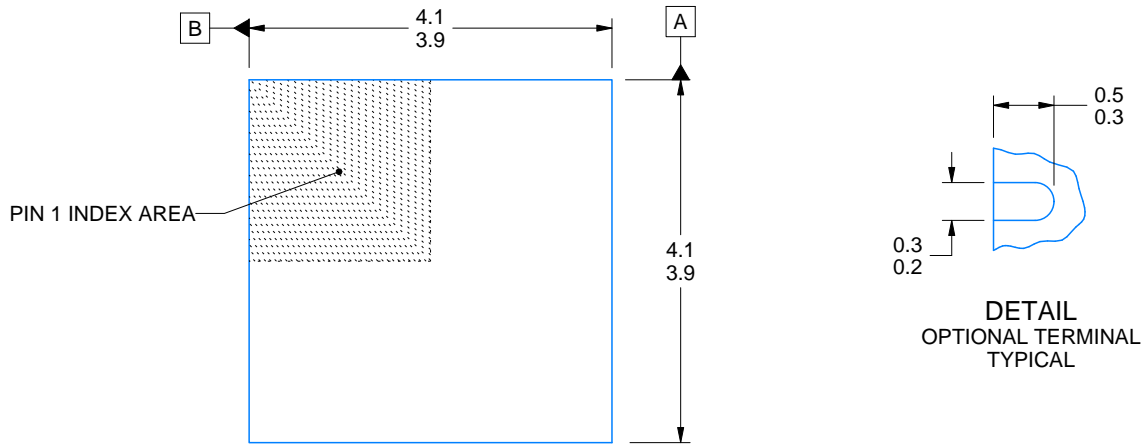
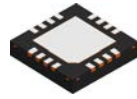
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6518SQ/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6518SQE/NOPB	WQFN	RGH	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6518SQX/NOPB	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

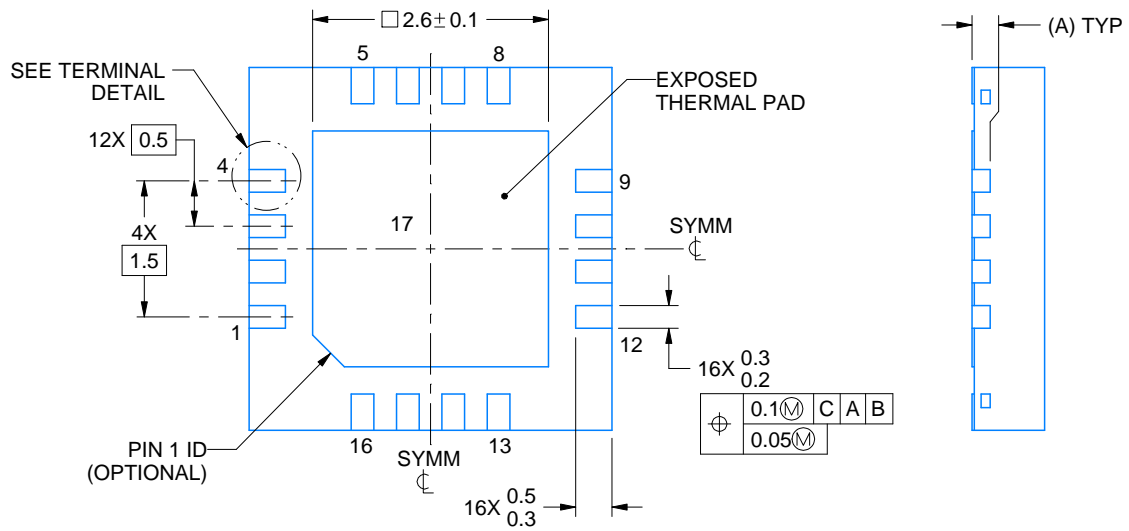
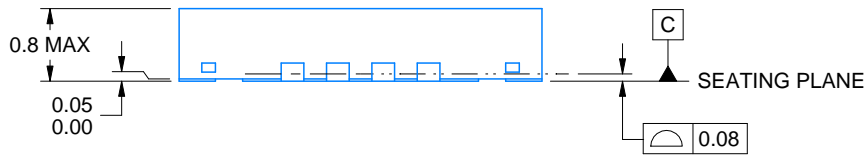
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6518SQ/NOPB	WQFN	RGH	16	1000	208.0	191.0	35.0
LMH6518SQE/NOPB	WQFN	RGH	16	250	208.0	191.0	35.0
LMH6518SQX/NOPB	WQFN	RGH	16	4500	356.0	356.0	36.0



DIM A	
OPT 1	OPT 1
(0.1)	(0.2)



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

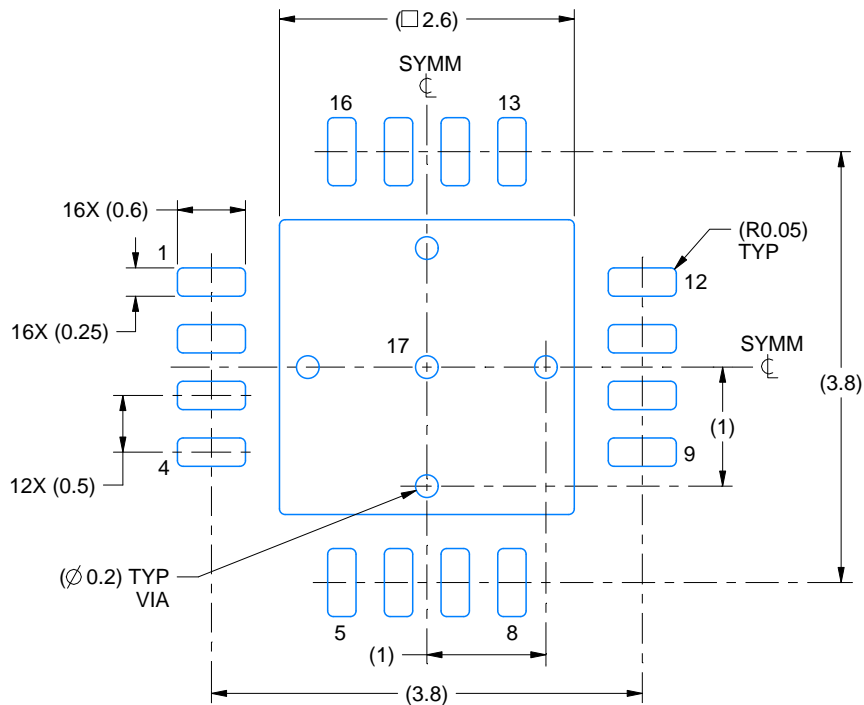


# EXAMPLE BOARD LAYOUT

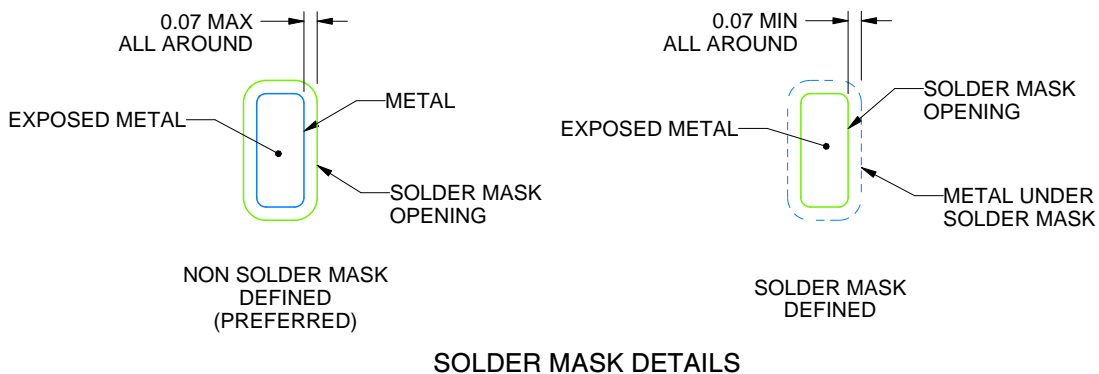
RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

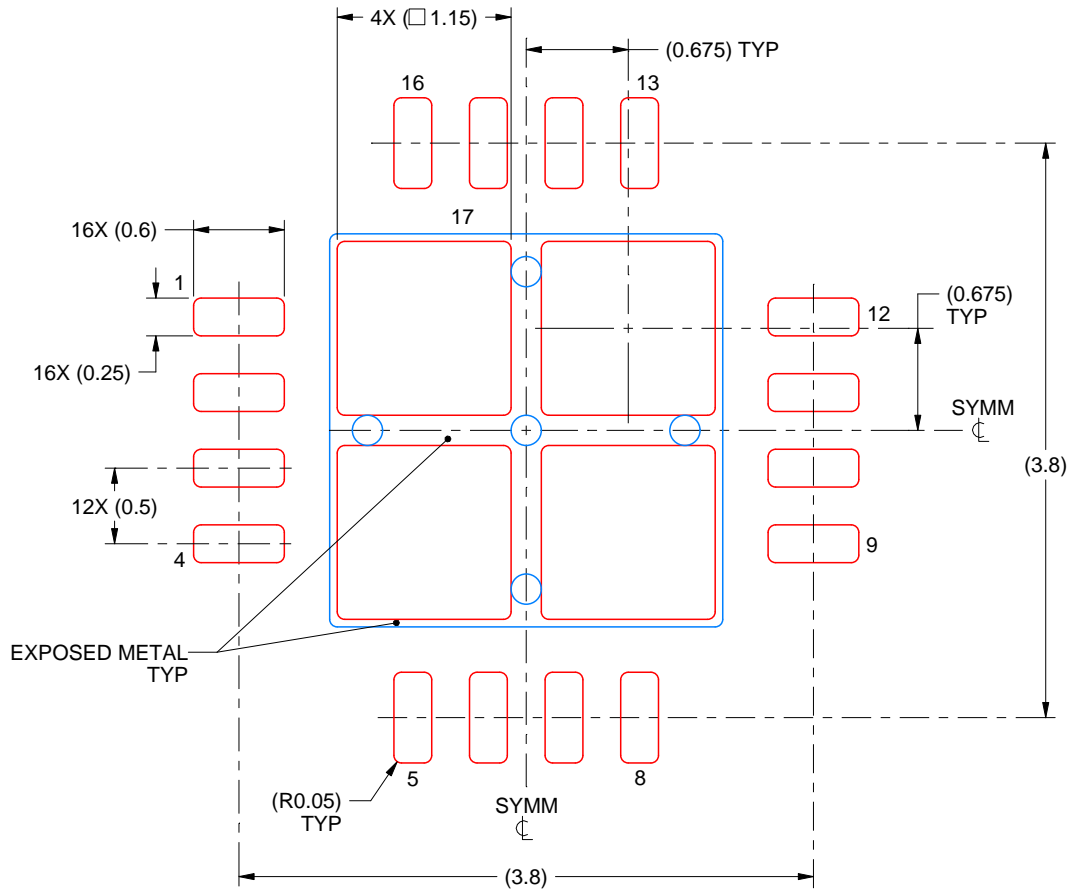
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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