

# LMH6628 Dual Wideband, Low Noise, Voltage Feedback Op Amp

Check for Samples: [LMH6628](#)

## FEATURES

- **Wide Unity Gain Bandwidth: 300MHz**
- **Low Noise:  $2\text{nV}/\sqrt{\text{Hz}}$**
- **Low Distortion:  $-65/-74\text{dBc}$  (10MHz)**
- **Settling Time: 12ns to 0.1%**
- **Wide Supply Voltage Range:  $\pm 2.5\text{V}$  to  $\pm 6\text{V}$**
- **High Output Current:  $\pm 85\text{mA}$**
- **Improved Replacement for CLC428**

## APPLICATIONS

- **High Speed Dual Op Amp**
- **Low Noise Integrators**
- **Low Noise Active Filters**
- **Driver/receiver for Transmission Systems**
- **High Speed Detectors**
- **I/Q Channel Amplifiers**

## DESCRIPTION

The Texas Instruments LMH6628 is a high speed dual op amp that offers a traditional voltage feedback topology featuring unity gain stability and slew enhanced circuitry. The LMH6628's low noise and very low harmonic distortion combine to form a wide dynamic range op amp that operates from a single (5V to 12V) or dual ( $\pm 5\text{V}$ ) power supply.

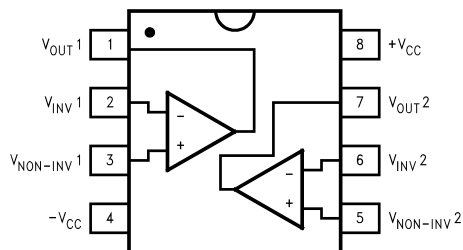
Each of the LMH6628's closely matched channels provides a 300MHz unity gain bandwidth and low input voltage noise density ( $2\text{nV}/\sqrt{\text{Hz}}$ ). Low 2nd/3rd harmonic distortion ( $-65/-74\text{dBc}$  at 10MHz) make the LMH6628 a perfect wide dynamic range amplifier for matched I/Q channels.

With its fast and accurate settling (12ns to 0.1%), the LMH6628 is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of hi resolution analog-to-digital converters. Combining the LMH6628's two tightly matched amplifiers in a single 8-pin SOIC package reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

The LMH6628 is fabricated using TI's VIP10™ complimentary bipolar process.

To reduce design times and assist in board layout, the LMH6628 is supported by an evaluation board (CLC730036).

## Connection Diagram



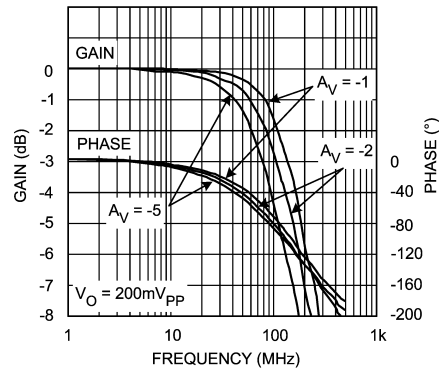
**Figure 1. 8-Pin SOIC, Top View**



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**Figure 2. Inverting Frequency Response**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	Human Body Model	2kV
	Machine Model	200V
Supply Voltage		13.5
Short Circuit Current		See <sup>(4)</sup>
Common-Mode Input Voltage		$V^+ - V^-$
Differential Input Voltage		$V^+ - V^-$
Maximum Junction Temperature		+150°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (soldering 10 sec)		+300°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 1.5k $\Omega$  in series with 100pF. Machine model, 0 $\Omega$  in series with 200pF.
- (4) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

### Operating Ratings<sup>(1)</sup>

Thermal Resistance <sup>(2)</sup>		
Package	( $\theta_{JC}$ )	( $\theta_{JA}$ )
SOIC	65°C/W	145°C/W
Temperature Range	-40°C to +85°C	
Nominal Supply Voltage	$\pm 2.5V$ to $\pm 6V$	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$  and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC board.

**Electrical Characteristics<sup>(1)</sup>**

$V_{CC} = \pm 5V$ ,  $A_V = +2V/V$ ,  $R_F = 100\Omega$ ,  $R_G = 100\Omega$ ,  $R_L = 100\Omega$ ; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Frequency Domain Response</b>						
GB	Gain Bandwidth Product	$V_O < 0.5V_{PP}$		200		MHz
SSBW	-3dB Bandwidth, $A_V = +1$	$V_O < 0.5V_{PP}$	180	300		MHz
SSBW	-3dB Bandwidth, $A_V = +2$	$V_O < 0.5V_{PP}$		100		MHz
GFL	Gain Flatness	$V_O < 0.5V_{PP}$				
GFP	Peaking	DC to 200MHz		0.0		dB
GFR	Rolloff	DC to 20MHz		.1		dB
LPD	Linear Phase Deviation	DC to 20MHz		.1		deg
<b>Time Domain Response</b>						
TR	Rise and Fall Time	1V Step		4		ns
TS	Settling Time	2V Step to 0.1%		12		ns
OS	Overshoot	1V Step		1		%
SR	Slew Rate	4V Step	300	550		V/ $\mu$ s
<b>Distortion And Noise Response</b>						
HD2	2nd Harmonic Distortion	1V <sub>PP</sub> , 10MHz		-65		dBc
HD3	3rd Harmonic Distortion	1V <sub>PP</sub> , 10MHz		-74		dBc
$V_N$	Equivalent Input Noise Voltage					
		1MHz to 100MHz		2		nV/ $\sqrt{Hz}$
$I_N$	Current	1MHz to 100MHz		2		pA/ $\sqrt{Hz}$
XTLKA	Crosstalk	Input Referred, 10MHz		-62		dB
<b>Static, DC Performance</b>						
$G_{OL}$	Open-Loop Gain		56 <b>53</b>	63		dB
$V_{IO}$	Input Offset Voltage			$\pm 5$	$\pm 2$ <b><math>\pm 2.6</math></b>	mV
$DV_{IO}$	Average Drift			5		$\mu$ V/ $^{\circ}$ C
$I_{BN}$	Input Bias Current			$\pm 7$	$\pm 20$ <b><math>\pm 30</math></b>	$\mu$ A
$DI_{BN}$	Average Drift			150		nA/ $^{\circ}$ C
$I_{OS}$	Input Offset Current			0.3	$\pm 6$	$\mu$ A
$I_{OSD}$	Average Drift			5		nA/ $^{\circ}$ C
PSRR	Power Supply Rejection Ratio		60 <b>46</b>	70		dB
CMRR	Common-Mode Rejection Ratio		57 <b>54</b>	62		dB
$I_{CC}$	Supply Current	Per Channel, $R_L = \infty$	7.5 <b>7.0</b>	9	12 <b>12.5</b>	mA
<b>Miscellaneous Performance</b>						
$R_{IN}$	Input Resistance	Common-Mode		500		k $\Omega$
		Differential-Mode		200		k $\Omega$
$C_{IN}$	Input Capacitance	Common-Mode		1.5		pF
		Differential-Mode		1.5		pF
$R_{OUT}$	Output Resistance	Closed-Loop		.1		$\Omega$

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where  $T_J > T_A$ . See Note 6 for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

**Electrical Characteristics<sup>(1)</sup> (continued)**

$V_{CC} = \pm 5V$ ,  $A_V = +2V/V$ ,  $R_F = 100\Omega$ ,  $R_G = 100\Omega$ ,  $R_L = 100\Omega$ ; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_O$	Output Voltage Range	$R_L = \infty$		$\pm 3.8$		V
$V_{OL}$		$R_L = 100\Omega$	$\pm 3.2$ <b><math>\pm 3.1</math></b>	$\pm 3.5$		V
CMIR	Input Voltage Range	Common- Mode		$\pm 3.7$		V
$I_O$	Output Current		$\pm 50$	$\pm 85$		mA

### Typical Performance Characteristics

( $T_A = +25^\circ$ ,  $A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_f = 100\Omega$ ,  $R_L = 100\Omega$ , unless specified)

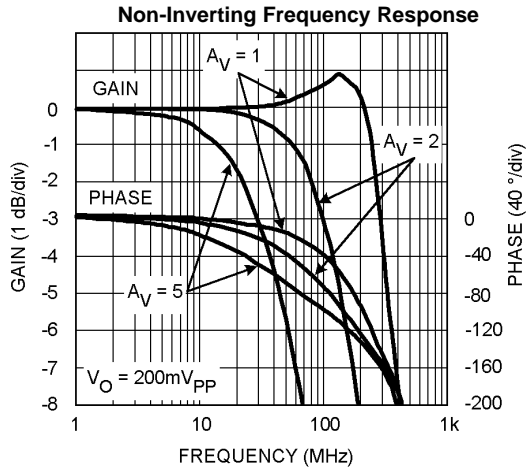


Figure 3.

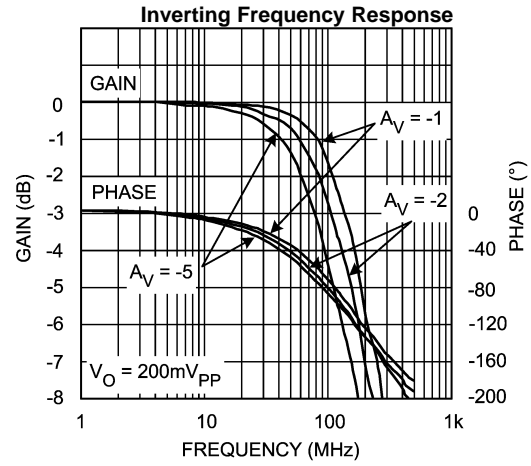


Figure 4.

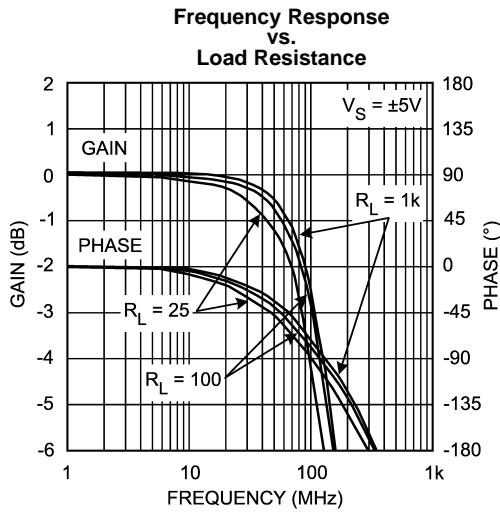


Figure 5.

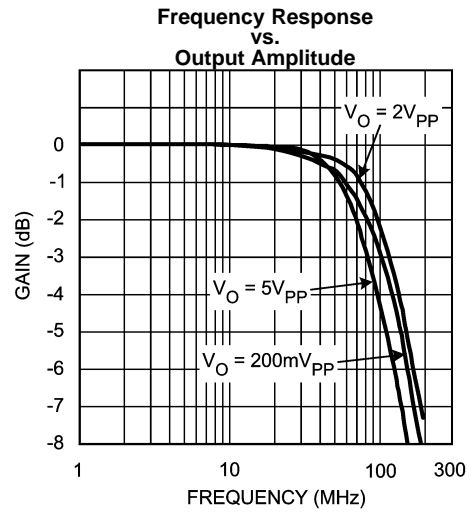


Figure 6.

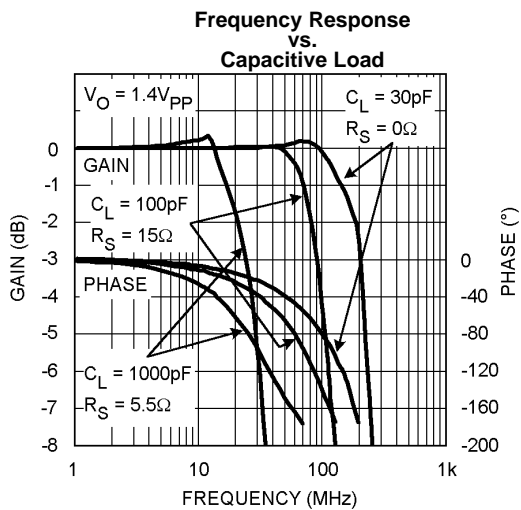


Figure 7.

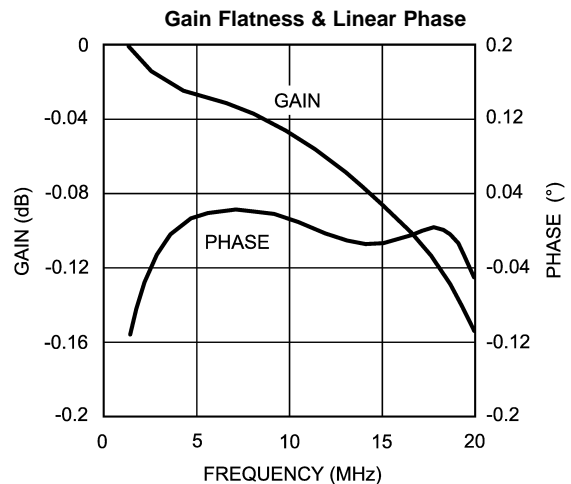


Figure 8.

**Typical Performance Characteristics (continued)**

( $T_A = +25^\circ$ ,  $A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_f = 100\Omega$ ,  $R_L = 100\Omega$ , unless specified)

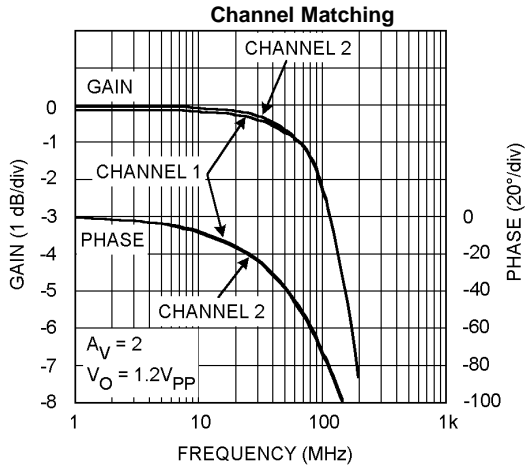


Figure 9.

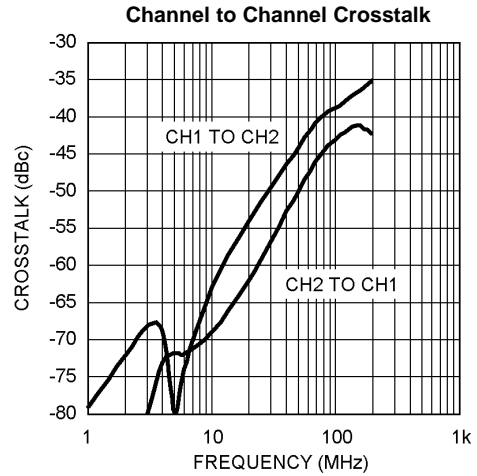


Figure 10.

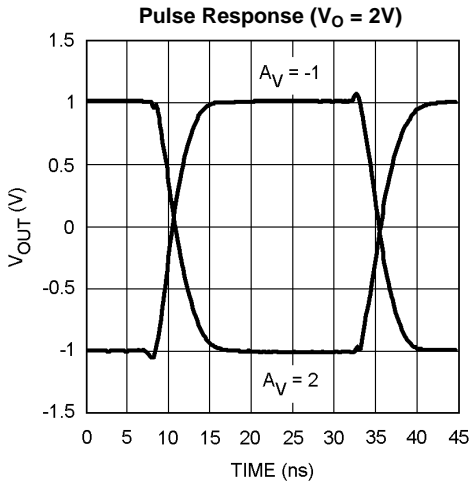


Figure 11.

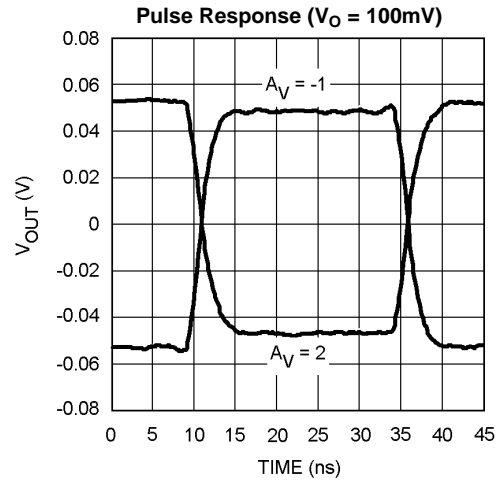


Figure 12.

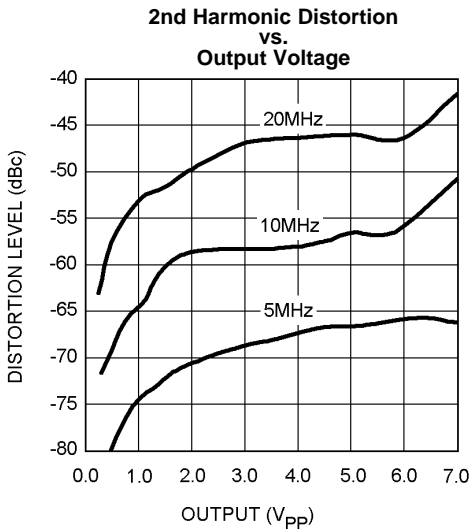


Figure 13.

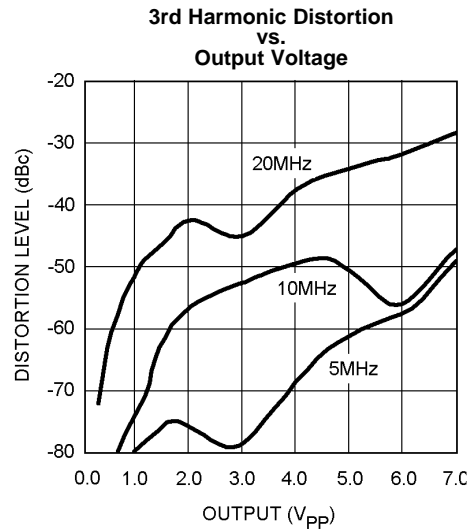


Figure 14.

Typical Performance Characteristics (continued)

( $T_A = +25^\circ$ ,  $A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_F = 100\Omega$ ,  $R_L = 100\Omega$ , unless specified)

2nd & 3rd Harmonic Distortion vs. Frequency

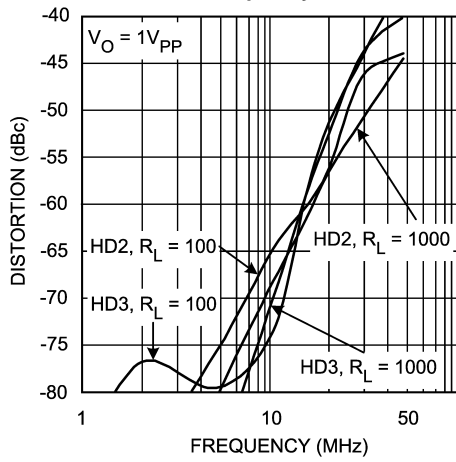


Figure 15.

PSRR and CMRR ( $\pm 5V$ )

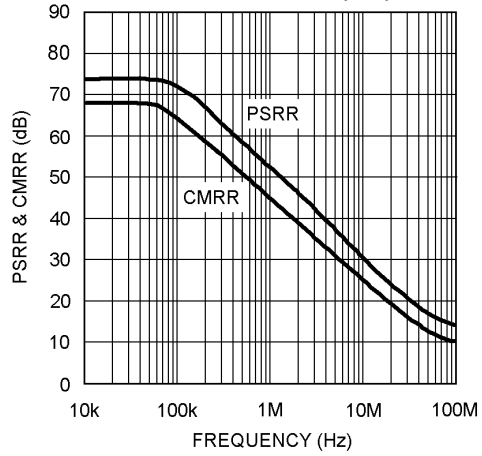


Figure 16.

PSRR and CMRR ( $\pm 2.5V$ )

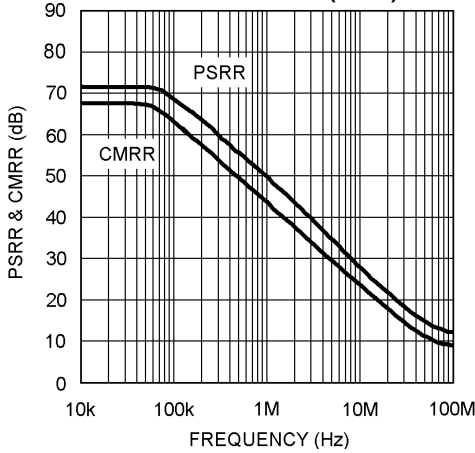


Figure 17.

Closed Loop Output Resistance ( $\pm 2.5V$ )

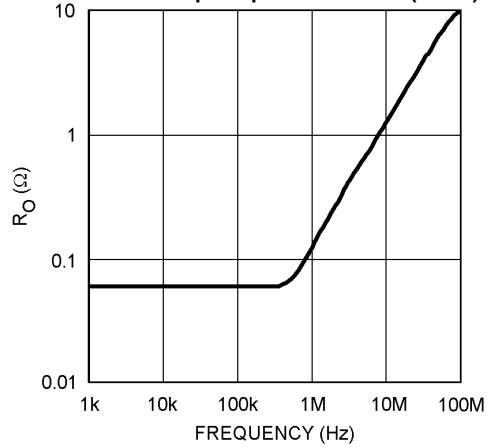


Figure 18.

Closed Loop Output Resistance ( $\pm 5V$ )

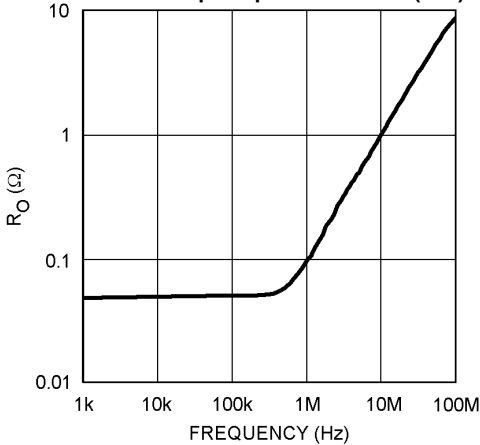


Figure 19.

Open Loop Gain & Phase ( $\pm 2.5V$ )

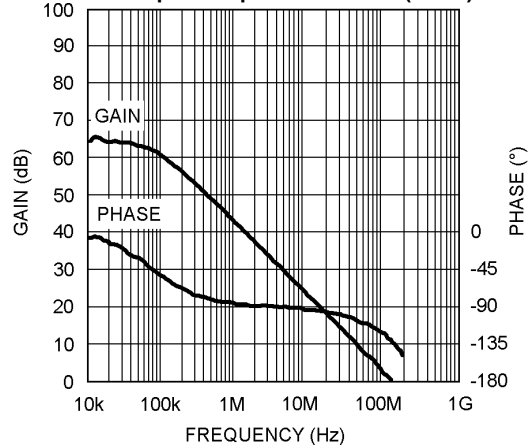


Figure 20.

**Typical Performance Characteristics (continued)**

( $T_A = +25^\circ$ ,  $A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_f = 100\Omega$ ,  $R_L = 100\Omega$ , unless specified)

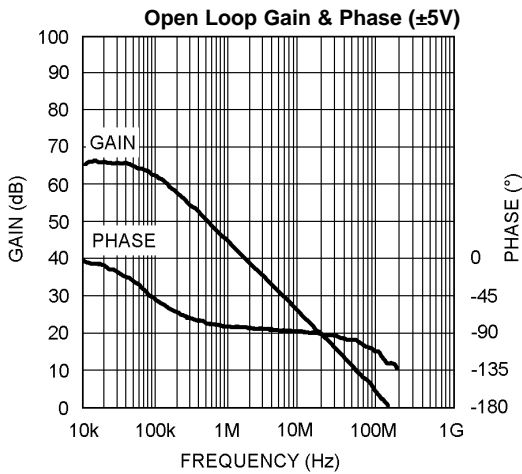


Figure 21.

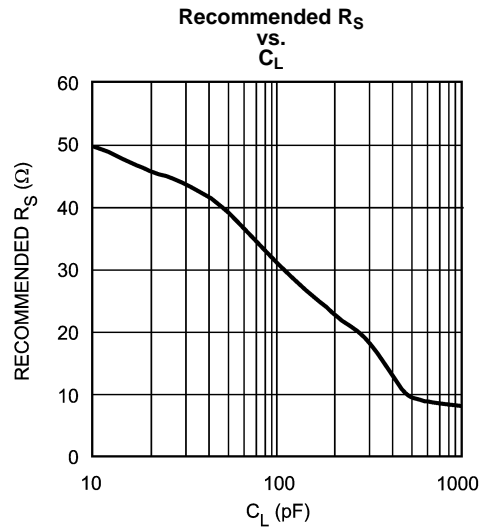


Figure 22.

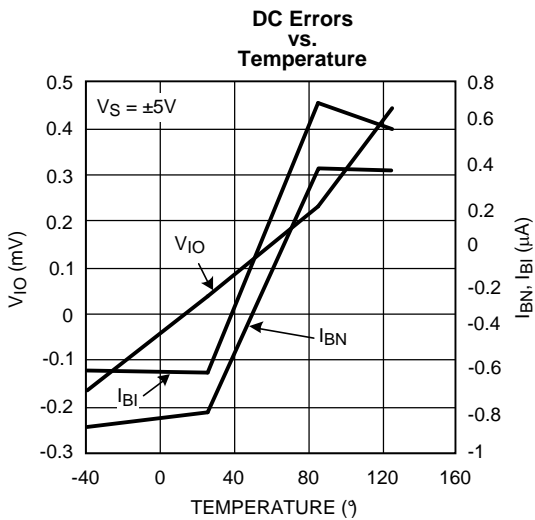


Figure 23.

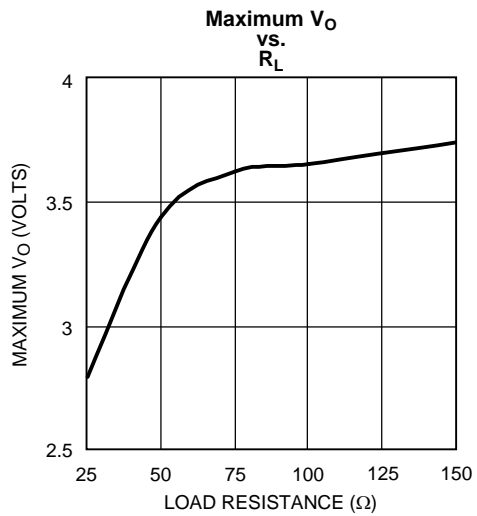
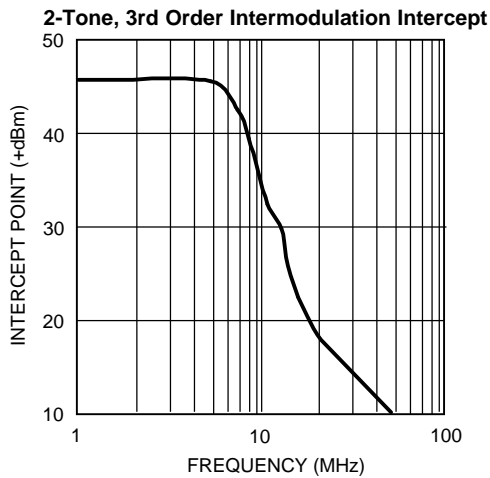


Figure 24.

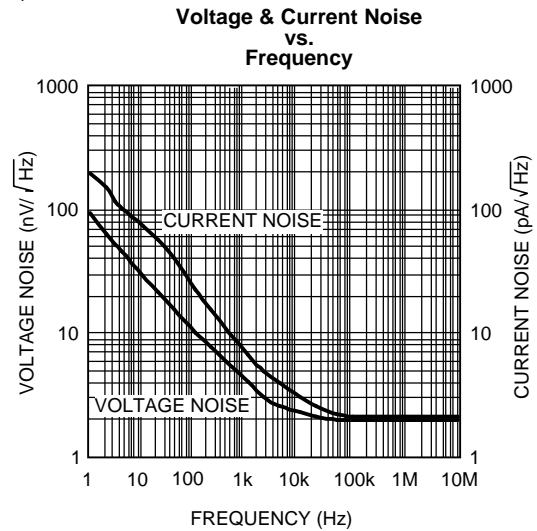


**Typical Performance Characteristics (continued)**

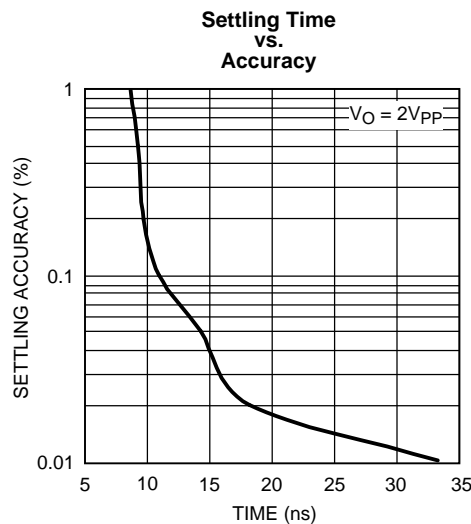
( $T_A = +25^\circ$ ,  $A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_f = 100\Omega$ ,  $R_L = 100\Omega$ , unless specified)



**Figure 25.**



**Figure 26.**



**Figure 27.**

## APPLICATION SECTION

### LOW NOISE DESIGN

Ultimate low noise performance from circuit designs using the LMH6628 requires the proper selection of external resistors. By selecting appropriate low valued resistors for  $R_F$  and  $R_G$ , amplifier circuits using the LMH6628 can achieve output noise that is approximately the equivalent voltage input noise of  $2nV/\sqrt{Hz}$  multiplied by the desired gain ( $A_V$ ).

### DC BIAS CURRENTS AND OFFSET VOLTAGES

Cancellation of the output offset voltage due to input bias currents is possible with the LMH6628. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage ( $V_{OS}$ ) multiplied by the desired gain ( $A_V$ ). Application Note OA-7 ([SNOA365](#)) offers several solutions to further reduce the output offset.

### OUTPUT AND SUPPLY CONSIDERATIONS

With  $\pm 5V$  supplies, the LMH6628 is capable of a typical output swing of  $\pm 3.8V$  under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than  $50\Omega$ , the output swing will be limited by the LMH6628's output current capability, typically 85mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See [Figure 22](#).

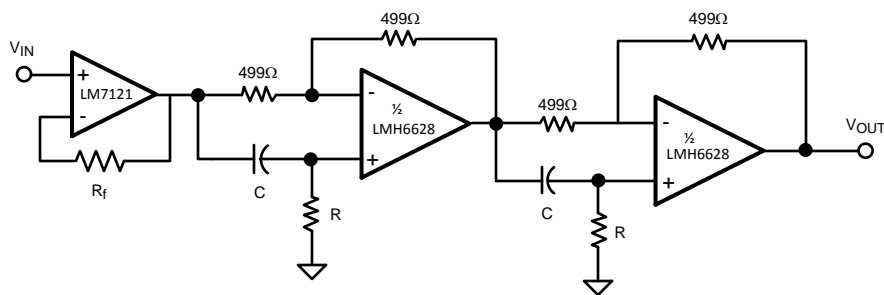
### LAYOUT

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of  $0.1\mu F$  should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 ([SNOA367](#)) for more information. Texas Instruments suggests the CLC730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

### ANALOG DELAY CIRCUIT (ALL-PASS NETWORK)

The circuit in [Figure 28](#) implements an all-pass network using the LMH6628. A wide bandwidth buffer (LM7121) drives the circuit and provides a high input impedance for the source. As shown in [Figure 29](#), the circuit provides a 13.1ns delay (with  $R = 40.2\Omega$ ,  $C = 47pF$ ).  $R_F$  and  $R_G$  should be of equal and low value for parasitic insensitive operation.



**Figure 28. Circuit That Implements an All-pass Network Using the LMH6628**

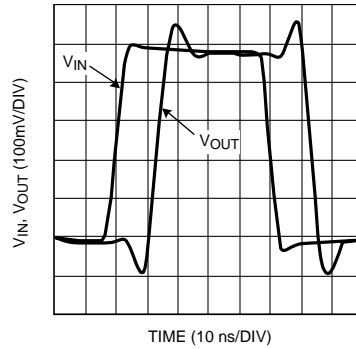


Figure 29. Delay Circuit Response to 0.5V Pulse

The circuit gain is +1 and the delay is determined by the following equations.

$$\tau_{\text{delay}} = 2(2RC + T_d) \tag{1}$$

$$T_d = \frac{1}{360} \frac{d\phi}{df}; \tag{2}$$

where  $T_d$  is the delay of the op amp at  $A_V = +1$ .

The LMH6628 provides a typical delay of 2.8ns at its  $-3\text{dB}$  point.

### FULL DUPLEX DIGITAL OR ANALOG TRANSMISSION

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The LMH6628's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in Figure 30, one of the LMH6628's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier  $A_2$  ( $B_2$ ) is connected across R and forms differential amplifier for the signals transmitted by driver  $A_2$  ( $B_2$ ). If  $R_F$  equals  $R_G$ , receiver  $A_2$  ( $B_1$ ) will then reject the signals from driver  $A_1$  ( $B_1$ ) and pass the signals from driver  $B_1$  ( $A_1$ ).

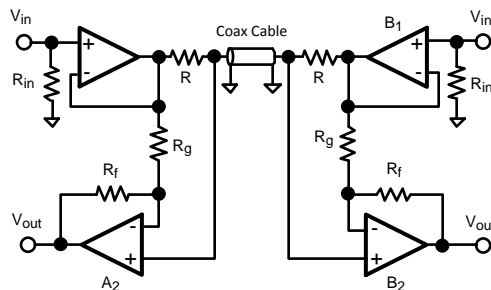


Figure 30. Full Duplex Transmit and Receive Using the LMH6628

The output of the receiver amplifier will be:

$$V_{\text{out}_{A(B)}} = \frac{1}{2} V_{\text{in}_{A(B)}} \left[ 1 - \frac{R_f}{R_g} \right] + \frac{1}{2} V_{\text{in}_{B(A)}} \left[ 1 + \frac{R_f}{R_g} \right] \tag{3}$$

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of Figure 31 shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

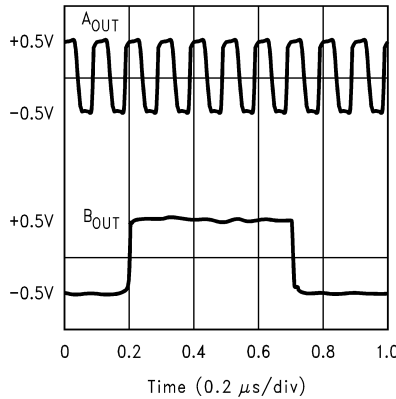


Figure 31. Simultaneous Reception of Signals Transmitted at 1MHz and 10MHz

**POSITIVE PEAK DETECTOR**

The LMH6628's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in Figure 32.

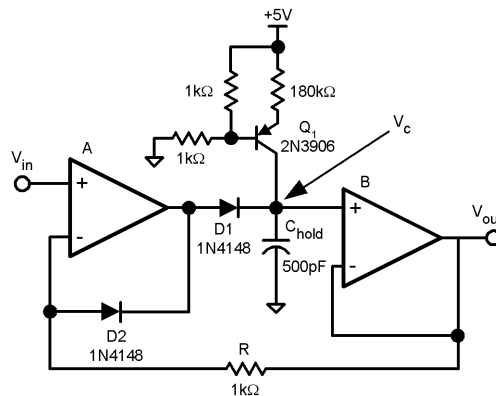


Figure 32. LMH6628's Dual Amplifiers Used to Implement a Unity-Gain Peak Detector Circuit

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging C<sub>hold</sub>. A plot of the circuit's performance is shown in Figure 33 with a 1MHz sinusoidal input.

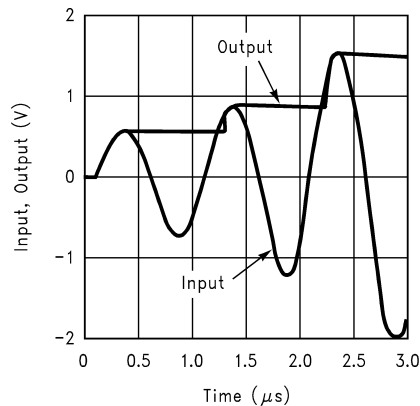


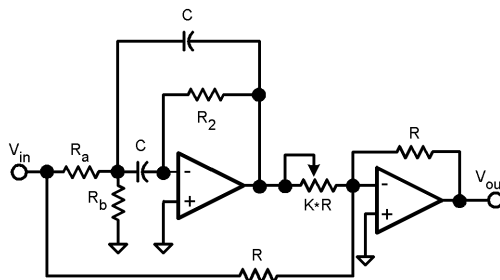
Figure 33. Circuit's Performance With a 1MHz Sinusoidal Input

A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D2 prevents negative saturation when  $V_{IN}$  is less than  $V_C$ . A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

### ADJUSTABLE OR BANDPASS EQUALIZER

A "boost" equalizer can be made with the LMH6628 by summing a bandpass response with the input signal, as shown in [Figure 34](#).



**Figure 34. "Boost" Equalizer Made With the LMH6628 by Summing a Bandpass Response With the Input Signal**

The overall transfer function is shown in [Equation 4](#).

$$\frac{V_{out}}{V_{in}} = \left[ \frac{R_b}{K(R_a + R_b)} \right] \frac{s2Q\omega_o}{s^2 + s \frac{\omega_o}{Q} + \omega_o^2} -1 \quad (4)$$

To build a boost circuit, use the design equations [Equation 5](#) and [Equation 6](#).

$$\frac{R_2 C}{2} = \frac{Q}{\omega_o} \quad (5)$$

$$2C (R_a || R_b) = \frac{1}{Q\omega_o} \quad (6)$$

Select  $R_2$  and  $C$  using [Equation 5](#). Use reasonable values for high frequency circuits -  $R_2$  between  $10\Omega$  and  $5k\Omega$ ,  $C$  between  $10pF$  and  $2000pF$ . Use [Equation 6](#) to determine the parallel combination of  $R_a$  and  $R_b$ . Select  $R_a$  and  $R_b$  by either the  $10\Omega$  to  $5k\Omega$  criteria or by other requirements based on the impedance  $V_{in}$  is capable of driving. Finish the design by determining the value of  $K$  from [Equation 7](#).

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}} (\omega_o) = \frac{R_2}{2KR_a} -1 \quad (7)$$

[Figure 35](#) shows an example of the response of the circuit of [Figure 34](#), where  $f_o$  is  $2.3MHz$ . The component values are as follows:  $R_a=2.1k\Omega$ ,  $R_b = 68.5\Omega$ ,  $R_2 = 4.22k\Omega$ ,  $R = 500\Omega$ ,  $KR = 50\Omega$ ,  $C = 120pF$ .

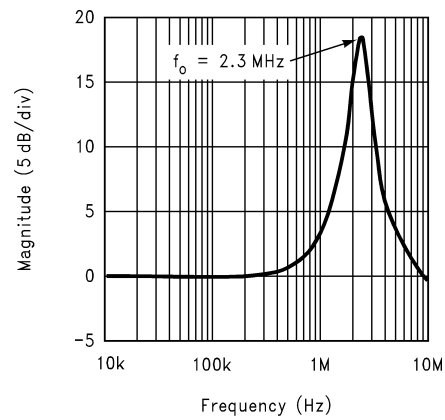


Figure 35. Example of Response of Circuit of [Figure 34](#), Where  $f_o$  is 2.3MHz

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**REVISION HISTORY**

<b>Changes from Revision C (March 2013) to Revision D</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<a href="#">14</a>

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**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMH6628MA/NOPB</a>	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 28MA
LMH6628MA/NOPB.A	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 28MA
<a href="#">LMH6628MAX/NOPB</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 28MA
LMH6628MAX/NOPB.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 28MA

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6628MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6628MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMH6628MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6628MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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