LMV331 单路、LMV393 双路、LMV339 四路通用低电压比较器

1 特性

- 2.7V 和 5V 性能
- 低电源电流
  - LMV331 26 µA 典型值
  - LMV393 50 µA 典型值
  - LMV339 100 µA 典型值
- 输入共模电压范围包括接地
- 低输出饱和电压 150mV 典型值
- 集电极开路输出可实现最大限度灵活性

2 应用

- 扫地机器人
- 服务器 PSU
- 无绳电动工具
- 电器
- 楼宇自动化
- 工厂自动化与控制

3 说明

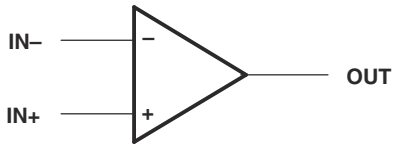
LMV393 和 LMV339 器件分别是双路和四路比较器的低电压（2.7V 至 5.5V）版本，它们的工作电压范围为 5V 至 30V。LMV331 是单路比较器。

LMV331、LMV339 和 LMV393 是颇具成本效益的器件，适用于在便携式消费类电子产品的电路设计中要求低电压运行、低功耗和节省空间的应用。无需消耗全部的电源电流，这类器件便可达到或超出常见 LM339 和 LM393 器件的规格。

器件信息

器件型号	封装（引脚）(1)	本体尺寸（标称值）(2)
LMV339（四通道）	SOIC (14)	3.91mm × 8.65mm
	TSSOP (14)	4.40mm × 5.00mm
	X2QFN (14)	2.00mm x 2.00mm
LMV393（双通道）	SOIC (8)	3.91mm × 4.90mm
	TSSOP (8)	3.00mm × 4.40mm
LMV331（单通道）	SC-70 (5)	1.25mm x 2.00mm
	SOT-23 (5)	1.60mm x 2.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）

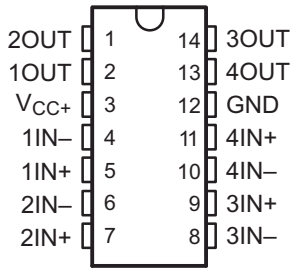


简化版原理图

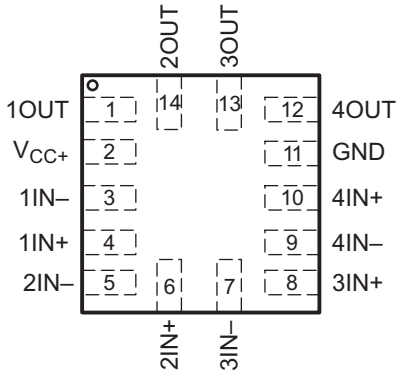
Table of Contents

4 Pin Configuration and Functions

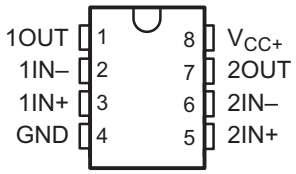
LMV339 . . . D OR PW PACKAGE
(TOP VIEW)



LMV339 . . . RUC PACKAGE
(TOP VIEW)



LMV393 . . . D, DDU, DGK OR PW PACKAGE
(TOP VIEW)



LMV331 . . . DBV OR DCK PACKAGE
(TOP VIEW)

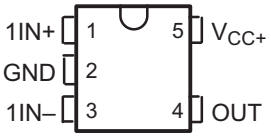


表 4-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	LMV331	LMV393	LMV339			
	DBV, DCK	D, DGK , PW	D, PW	RUC		
1IN – , 2IN – , 3IN – , 4IN –	3	2, 6	4, 6, 8, 10	3, 5, 7, 9	I	Comparator negative input pin
1IN+ , 2IN+, 3IN+, 4IN+	1	3, 5	5, 7, 9, 11	4, 6, 8, 10	I	Comparator positive input pin
GND	2	4	12	11	I	Ground
1OUT, 2OUT, 3OUT, 4OUT	4	1, 7	2, 1, 14, 13	1, 14, 13, 12	O	Comparator output pin
V_{CC+}	5	8	3	2	I	Supply Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			5.5	V
V_{ID}	Differential input voltage(3)			±5.5	V
V_I	Input voltage range (either input)		0	V_{CC+}	V
	Duration of output short circuit (one amplifier) to ground(4)	At or below T_A = 25°C, V_{CC} ≤ 5.5V	Unlimited		
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN –.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)	2.7	5.5	V
V_{OUT}	Output voltage		V_{CC+} + 0.3	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		LMV339			LMV393				LMV331		UNIT
		D	PW	RUC	D	DDU	DGK	PW	DBV	DCK	
		14 PINS			8 PINS				5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136	155	216	168	210	216	222	224	238	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	51.3	—	—	—	—	—	—	
$R_{\theta JB}$	Junction-to-board thermal resistance	—	—	59.0	—	—	—	—	—	—	
ψ_{JT}	Junction-to-top characterization parameter	—	—	1.2	—	—	—	—	—	—	
ψ_{JB}	Junction-to-board characterization parameter	—	—	59.0	—	—	—	—	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics, V_{CC+} = 2.7V

V_{CC+} = 2.7V, GND = 0V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		+0.5	7	mV
α_{VIO}	Average temperature coefficient of input offset voltage		–40°C to 125°C		5		μV/°C
I_{IB}	Input bias current		25°C		0.005	250	nA
			–40°C to 125°C			400	
I_{IO}	Input offset current		25°C		0.001	50	nA
			–40°C to 125°C			150	
I_O	Output current (sinking)	$V_O \leqslant$ 1.5V	25°C	5	23		mA
	Output Leakage Current		25°C		0.003		μA
			–40°C to 125°C			1	
V_{ICR}	Common-mode input voltage range		25°C		–0.1 to 2		V
V_{SAT}	Saturation voltage	$I_O \leqslant$ 1.5mA	25°C		150		mV
I_{CC}	Supply current	LMV331	25°C		26	100	μA
		LMV393 (both comparators)	25°C		50	140	
		LMV339 (all four comparators)	25°C		100	200	

5.6 Switching Characteristics, V_{CC+} = 2.7V

T_A = 25°C, V_{CC+} = 2.7V, R_L = 5.1kΩ, GND = 0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PHL}	Propagation delay high to low level output switching	Input overdrive = 10mV	1000	ns
		Input overdrive = 100mV	350	
t_{PLH}	Propagation delay low to high level output switching	Input overdrive = 10mV	500	ns
		Input overdrive = 100mV	400	

5.7 Electrical Characteristics, V_{CC+} = 5V

V_{CC+} = 5V, GND = 0V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		+0.5	7	mV
			–40°C to 125°C			9	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C		5		μV/°C
I_{IB}	Input bias current		25°C		0.005	250	nA
			–40°C to 125°C			400	
I_{IO}	Input offset current		25°C		0.001	50	nA
			–40°C to 125°C			150	
I_O	Output current (sinking)	$V_O \leqslant$ 1.5V	25°C	10	84		mA
	Output Leakage Current		25°C		0.003		μA
			–40°C to 125°C			1	
V_{ICR}	Common-mode input voltage range		25°C		–0.1 to 4.2		V
A_{VD}	Large-signal differential voltage gain		25°C	20	50		V/mV
V_{SAT}	Saturation voltage	$I_O \leqslant$4 mA	25°C		150	400	mV
			–40°C to 125°C			700	
I_{CC}	Supply current	LMV331	25°C		26	120	μA
			–40°C to 125°C			150	
		LMV393 (both comparators)	25°C		50	200	
			–40°C to 125°C			250	
		LMV339 (all four comparators)	25°C		100	300	
			–40°C to 125°C			350	

5.8 Switching Characteristics, V_{CC+} = 5V

T_A = 25°C, V_{CC+} = 5V, R_L = 5.1kΩ, GND = 0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PHL}	Propagation delay high to low level output switching	Input overdrive = 10mV	600	ns
		Input overdrive = 100mV	200	
t_{PLH}	Propagation delay low to high level output switching	Input overdrive = 10mV	450	ns
		Input overdrive = 100mV	300	

5.9 Typical Characteristics

Unless otherwise specified, VS = +5V, single supply, TA = 25°C

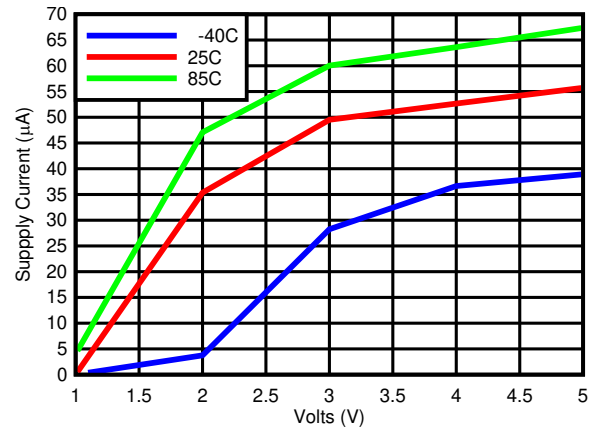


图 5-1. Supply Current vs Supply Voltage Output High

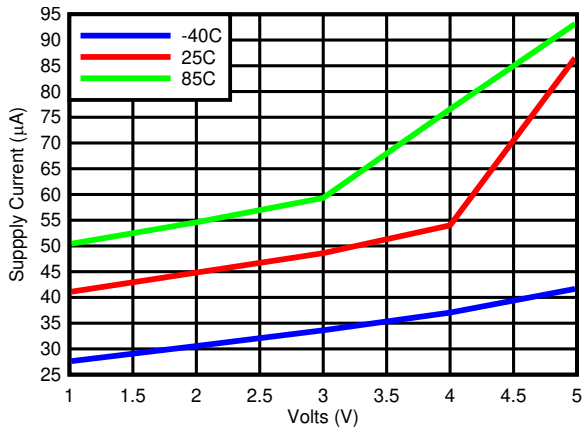


图 5-2. Supply Current vs Supply Voltage Output Low

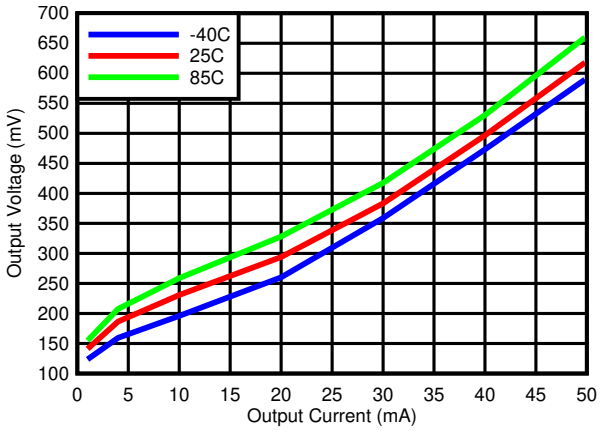


图 5-3. Output Voltage vs Output Current

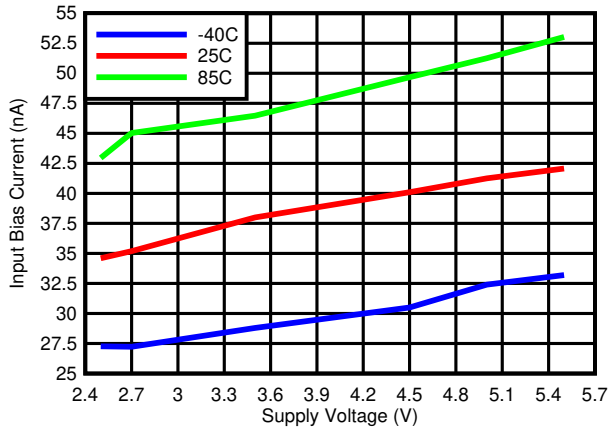


图 5-4. Input Bias Current vs Supply Voltage

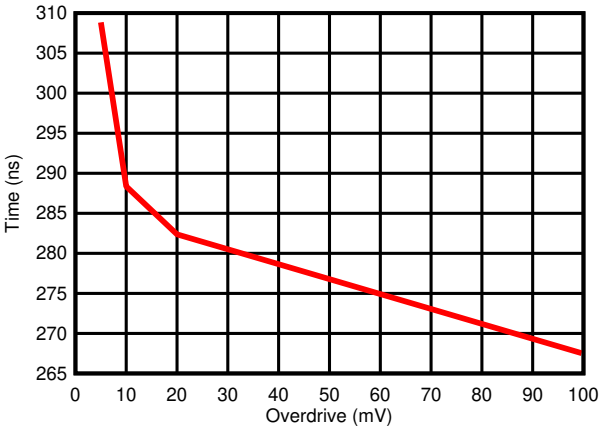


图 5-5. Response Time vs Input Overdrives Negative Transition (V_{CC}=5V)

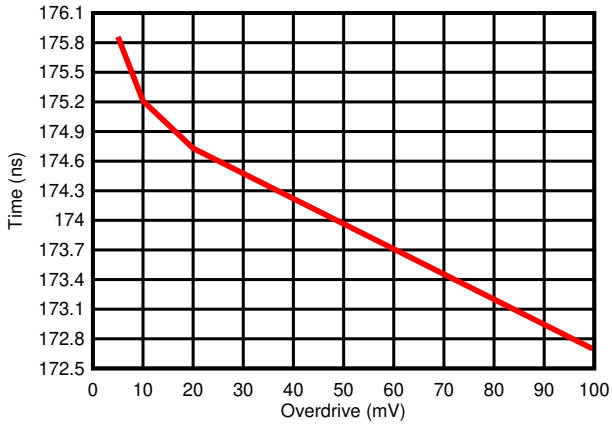


图 5-6. Response Time vs Input Overdrives Positive Transition (V_{CC} = 5V)

5.9 Typical Characteristics (continued)

Unless otherwise specified, VS = +5V, single supply, TA = 25°C

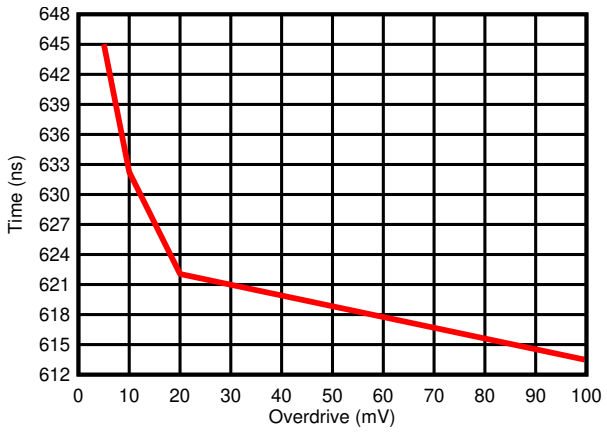


图 5-7. Response Time vs Input Overdrives Negative Transition (V_{CC} = 2.7V)

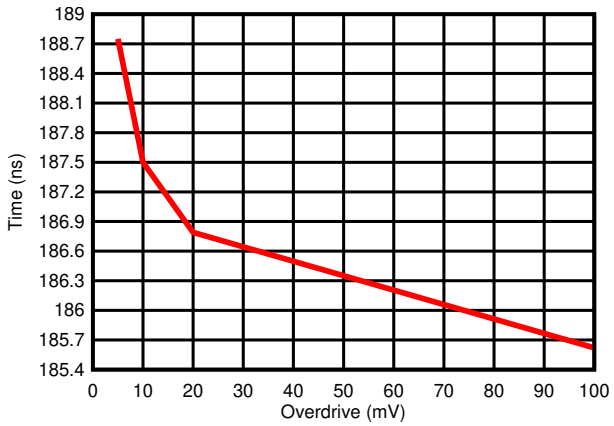


图 5-8. Response Time vs Input Overdrives Positive Transition (V_{CC} = 2.7V)

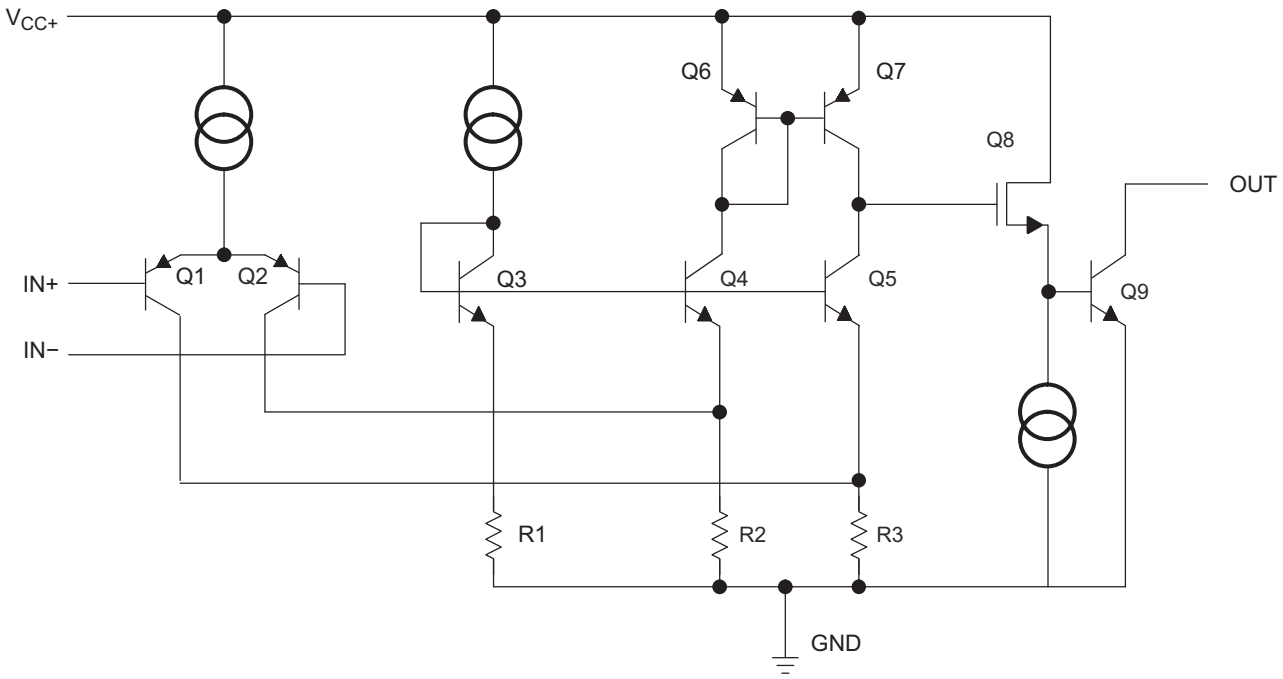
6 Detailed Description

6.1 Overview

The LMV331, LMV393 and LMV339 family of comparators have the ability to operate up to 5V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to it's low Iq and fast response.

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

6.2 Functional Block Diagram



6.3 Feature Description

The LMV331, LMV393 and LMV339 consists of a PNP input, whose Vbe creates a limit on the input common mode voltage capability, allowing LMV33x to accurately function from ground to V_{CC} – Vbe(about 700mV) differential input. This enables much head room for modern day supplies of 3.3V and 5.0V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. Please see 图 5-3 for V_{OL} values with respect to the output current.

6.4 Device Functional Modes

6.4.1 Voltage Comparison

The LMV33x operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputs a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

LMV331, LMV393, and LMV339 typically is used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LMV331, LMV393, and LMV33 is an ecxellent choice for level shifting to a higher or lower voltage.

7.2 Typical Application

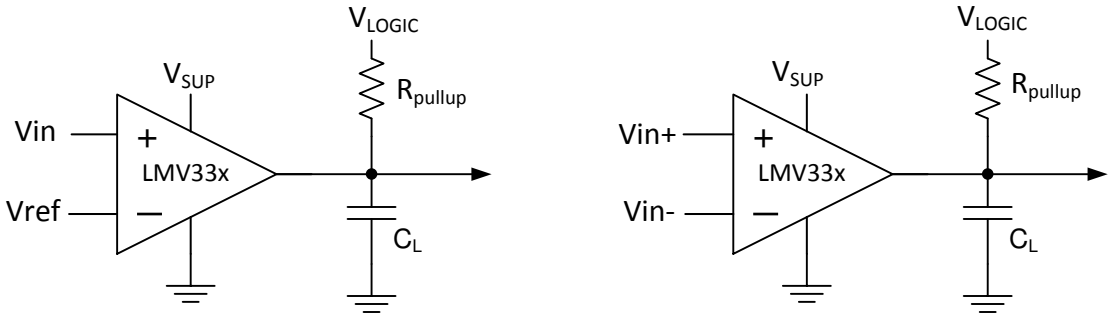


图 7-1. Typical Application Schematic

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to 4.2V
Supply Voltage	2.7V to 5V
Logic Supply Voltage (R_{PULLUP} Voltage)	1V to 5V
Output Current (V_{LOGIC}/R_{PULLUP})	1μA to 20mA
Input Overdrive Voltage	100mV
Reference Voltage	2.5V
Load Capacitance (C_L)	15pF

7.2.2 Detailed Design Procedure

When using LMV331, LMV393, and LMV33 in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

7.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If operating temperature is above or below 25°C the V_{ICR} can range from 0V to V_{CC} – 0.7V. This limits the input voltage range to as high as V_{CC} – 0.7V and as low as 0V. Operation outside of this range can yield incorrect comparisons.

Below is a possible list of input voltage situation and the outcomes:

1. When both IN- and IN+ are both within the common mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

7.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison; the Overdrive Voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 图 7-2 show positive and negative response times with respect to overdrive voltage.

7.2.2.3 Output and Drive Current

Output current is determined by the pull-up resistance (Rpullup) and Vlogic voltage, refer to 图 7-1. The output current produces a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use 图 5-3 to determine V_{OL} based on the output current.

The output current can also effect the transient response. This is explained in the next section.

7.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The positive response time (τ_p) is approximately $\tau_P = R_{PULLUP} \times C_L$
- The negative response time (τ_N) is approximately $\tau_N = R_{CE} \times C_L$
  - R_{CE} can be determine by taking the slope of 图 5-3 in it's linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

7.2.3 Application Curves

The following curves were generated with 5V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1kΩ, and 50pF scope probe.

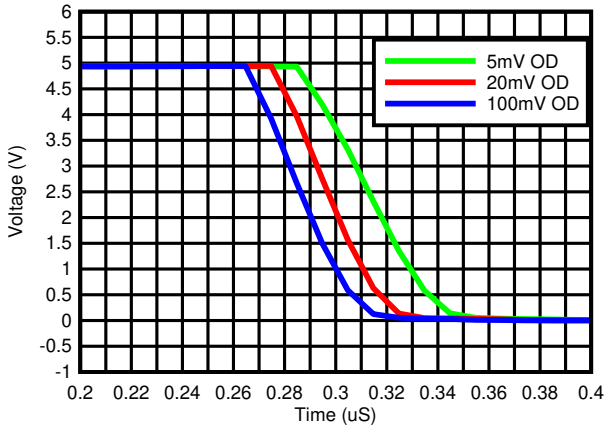


图 7-2. Response Time for Various Overdrives (Negative Transition)

8 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, a bypass capacitor is recommended on the supply pin to reject any variation on the supply voltage. This variation cause temporary fluctuations in the comparator's input common mode range and create an inaccurate comparison.

9 Layout

9.1 Layout Guidelines

For accurate comparator applications without hysteresis, a stable power supply is necessary with minimized noise and glitches, which can affect the high level input common mode voltage range. To achieve this, add a bypass capacitor between the supply voltage and ground. This can be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

9.2 Layout Example

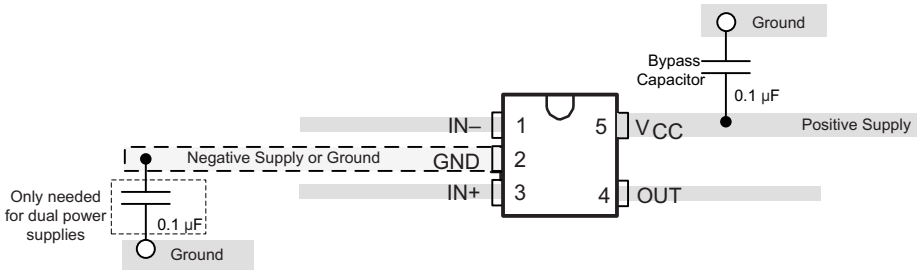


图 9-1. LMV331 Layout Example

10 Device and Documentation Support

10.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV331	Click here	Click here	Click here	Click here	Click here
LMV393	Click here	Click here	Click here	Click here	Click here
LMV339	Click here	Click here	Click here	Click here	Click here

11 Trademarks

所有商标均为其各自所有者的财产。

12 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision U (October 2020) to Revision V (May 2025) **Page**

- 更新了*器件信息*表 1
- Corrected incorrect *Feature Description* text about input voltage conditions for output sinking 9

Changes from Revision T (January 2015) to Revision U (October 2020) **Page**

- 更新了整个文档中的表、图和交叉参考的编号格式 1

Changes from Revision S (January 2015) to Revision T (January 2015) **Page**

- 添加了*应用*、*器件信息*表、*引脚功能*表、*ESD 等级*表、*热性能信息*表、*典型特性*、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1
- 删除了*订购信息*表请参阅数据表末尾的可订购产品附录 1

Changes from Revision R (May 2012) to Revision S (January 2015) **Page**

- Updated operating temperature range 4

Changes from Revision Q (April 2012) to Revision R (May 2012) **Page**

- Added RUC to marking list (table later removed in T) 3

Changes from Revision P (March 2012) to Revision Q (April 2012) **Page**

- Corrected the Top Side Marking for RUC package, RT_ (table removed in T) 3

Changes from Revision O (February 2012) to Revision P (March 2012) **Page**

- Corrected typo in Ordering Information Table for Top Side Marking, R9_ (table removed in T) 3

Changes from Revision N (April 2011) to Revision O (February 2012) **Page**

- Changed V_I in the *Absolute Maximum Ratings* from 5.5V to V_{CC+} 4

Changes from Revision M (November 2005) to Revision N (April 2011) **Page**

- 将文档格式从 Quicksilver 变更为 DocZone 1
- Added RUC package pin out drawing 3

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV331IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)
LMV331IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)
LMV331IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)
LMV331IDBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)
LMV331IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)
LMV331IDBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	(R1IF, R1IK)
LMV331IDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)
LMV331IDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)
LMV331IDCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)
LMV331IDCKRE4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)
LMV331IDCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)
LMV331IDCKT	Obsolete	Production	SC70 (DCK) | 5	-	-	Call TI	Call TI	-40 to 125	(R2F, R2R)
LMV339ID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	LMV339I
LMV339IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV339I
LMV339IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV339I
LMV339IDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV339I
LMV339IDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV339I
LMV339IPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	MV339I
LMV339IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I
LMV339IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I
LMV339IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I
LMV339IPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I
LMV393ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	MV393I
LMV393IDDUR	Obsolete	Production	VSSOP (DDU) | 8	-	-	Call TI	Call TI	-40 to 125	RABR
LMV393IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(R9B, R9Q, R9R)
LMV393IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(R9B, R9Q, R9R)
LMV393IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(R9B, R9Q, R9R)
LMV393IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV393IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 125	MV393I
LMV393IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IPWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LMV331, LMV393 :

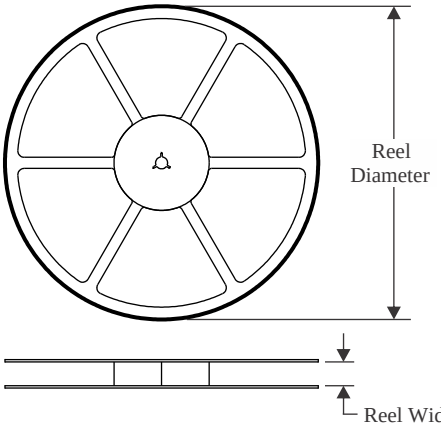
- Automotive : LMV331-Q1, LMV393-Q1

NOTE: Qualified Version Definitions:

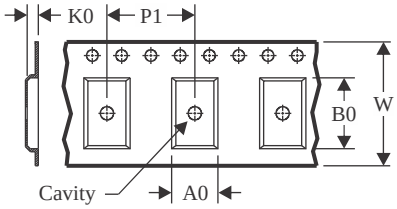
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

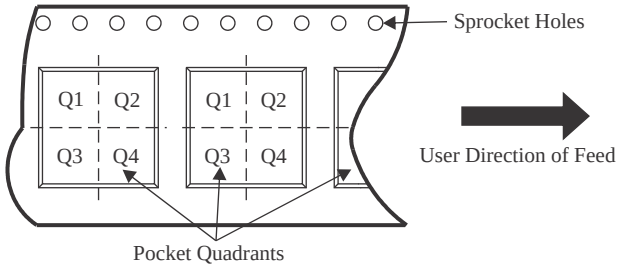


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

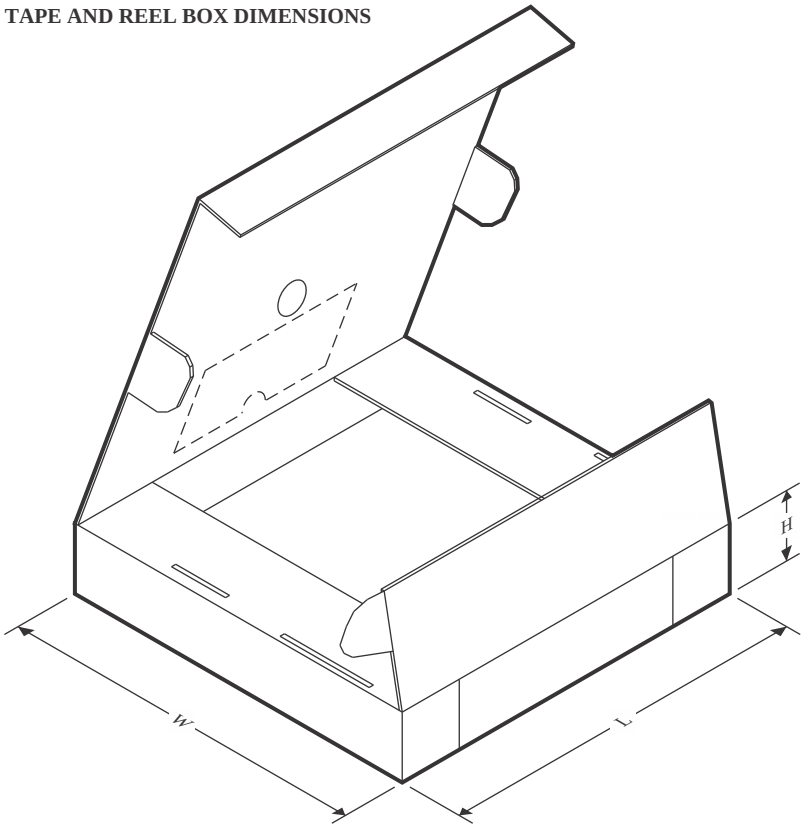
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.17	3.23	1.37	4.0	8.0	Q3
LMV331IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV331IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV331IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV339IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV339IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV339IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV393IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LMV393IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LMV393IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

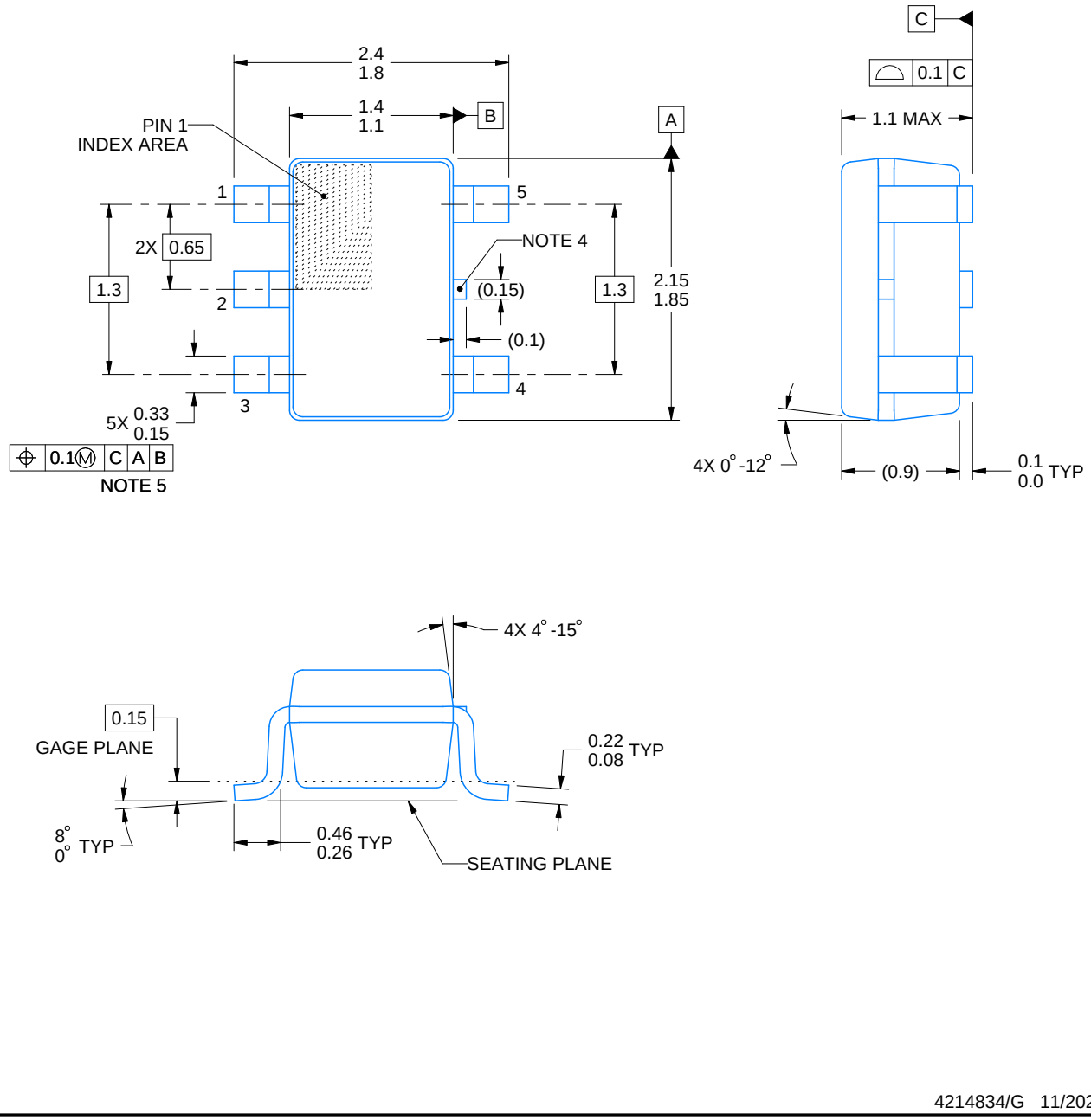
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV331IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV331IDBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV331IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV331IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV339IDR	SOIC	D	14	2500	353.0	353.0	32.0
LMV339IDRG4	SOIC	D	14	2500	353.0	353.0	32.0
LMV339IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LMV393IDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
LMV393IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LMV393IDR	SOIC	D	8	2500	353.0	353.0	32.0
LMV393IDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LMV393IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
LMV393IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

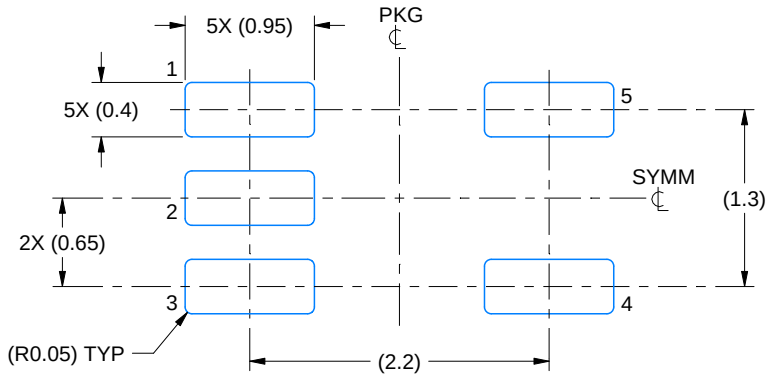
SMALL OUTLINE TRANSISTOR



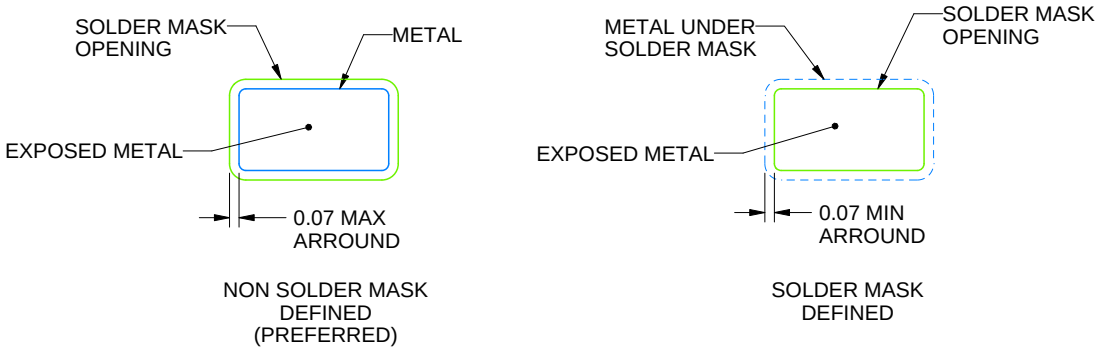
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

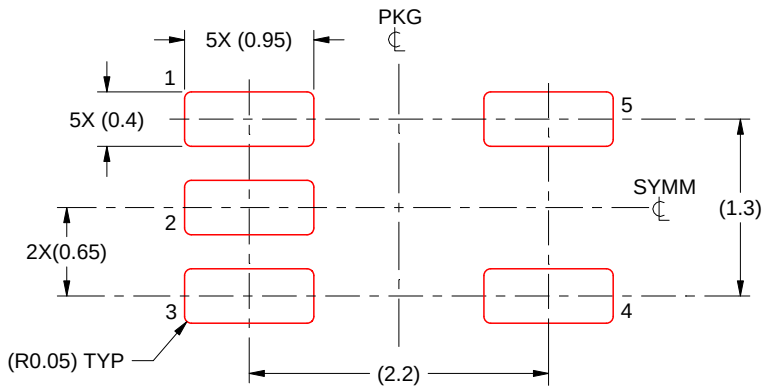


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

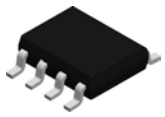


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

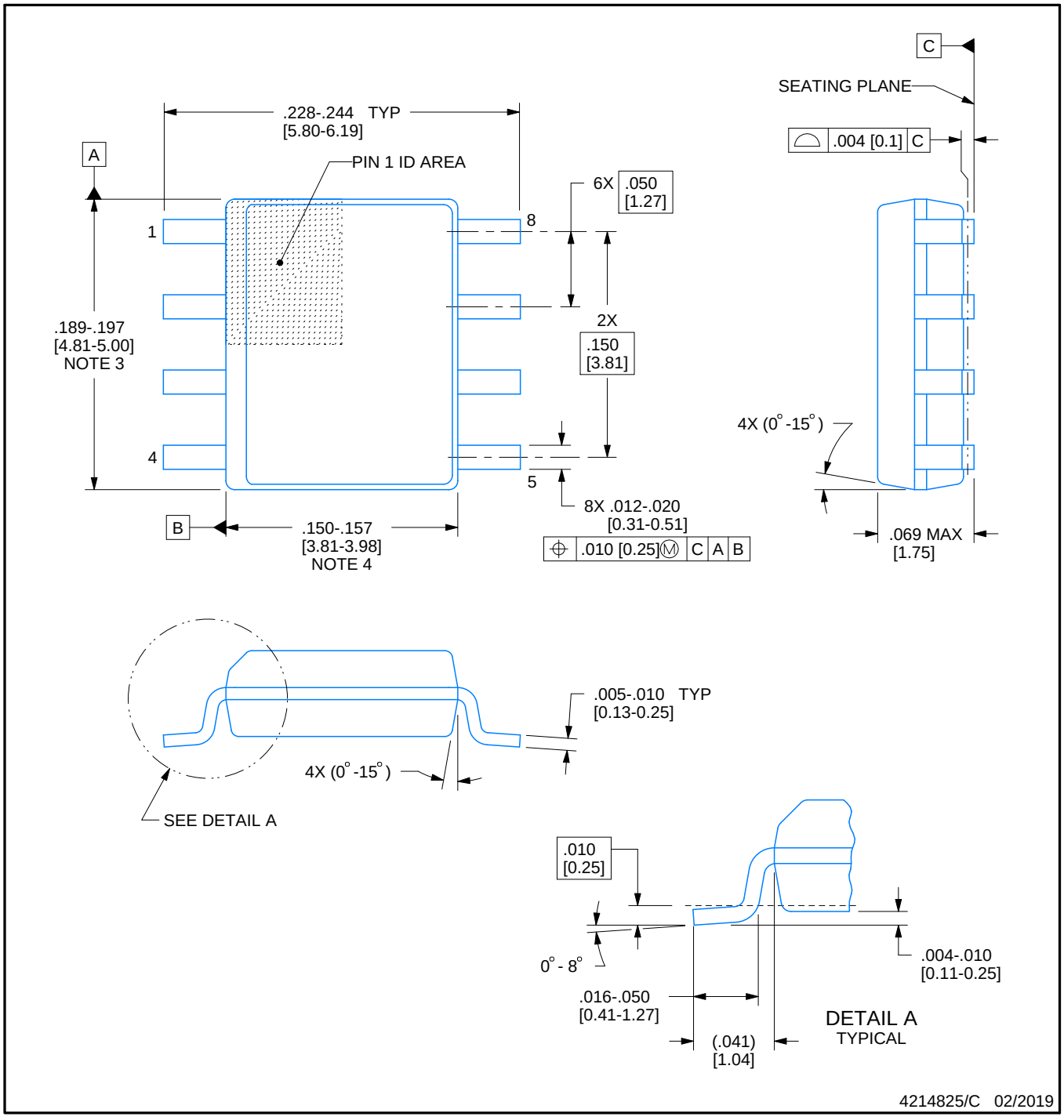


PACKAGE OUTLINE

D0008A

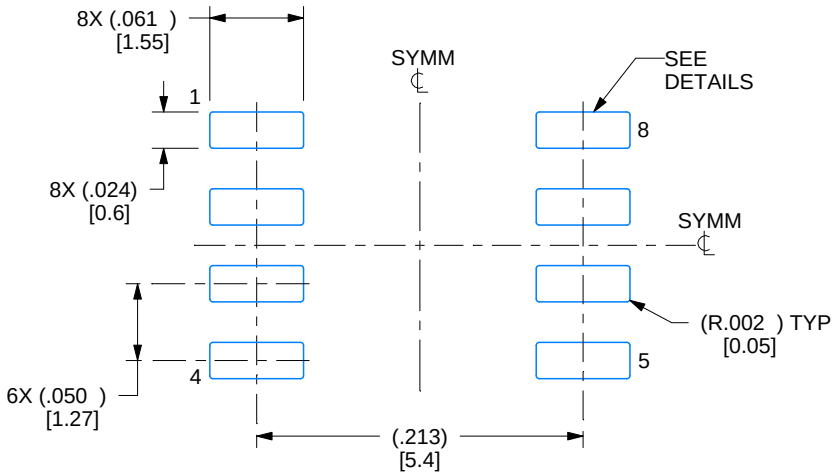
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

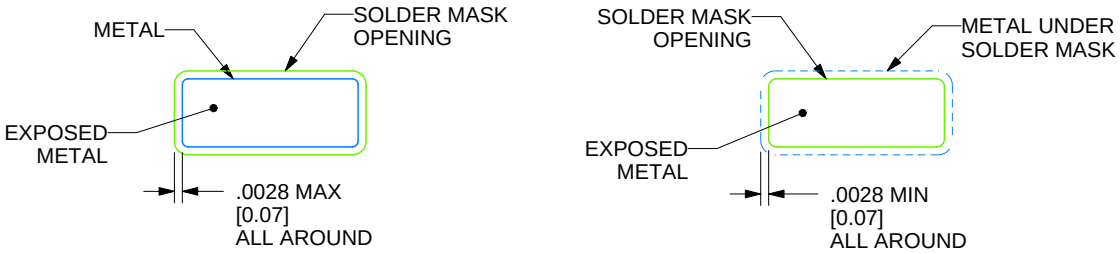


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

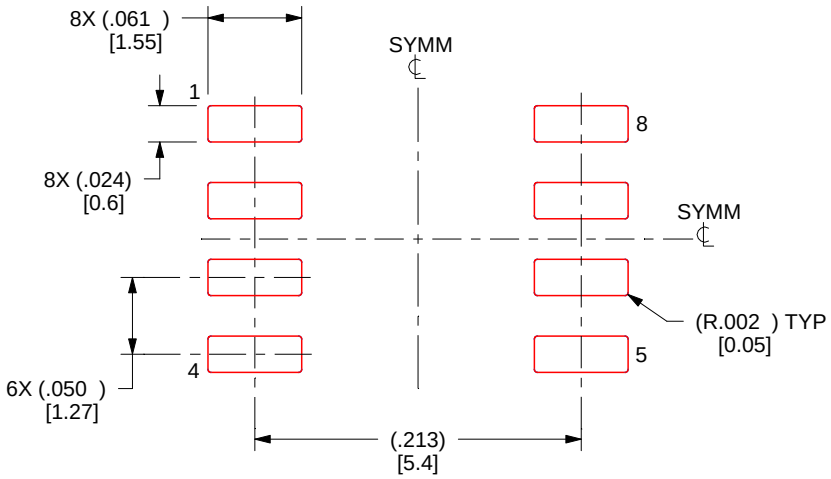
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

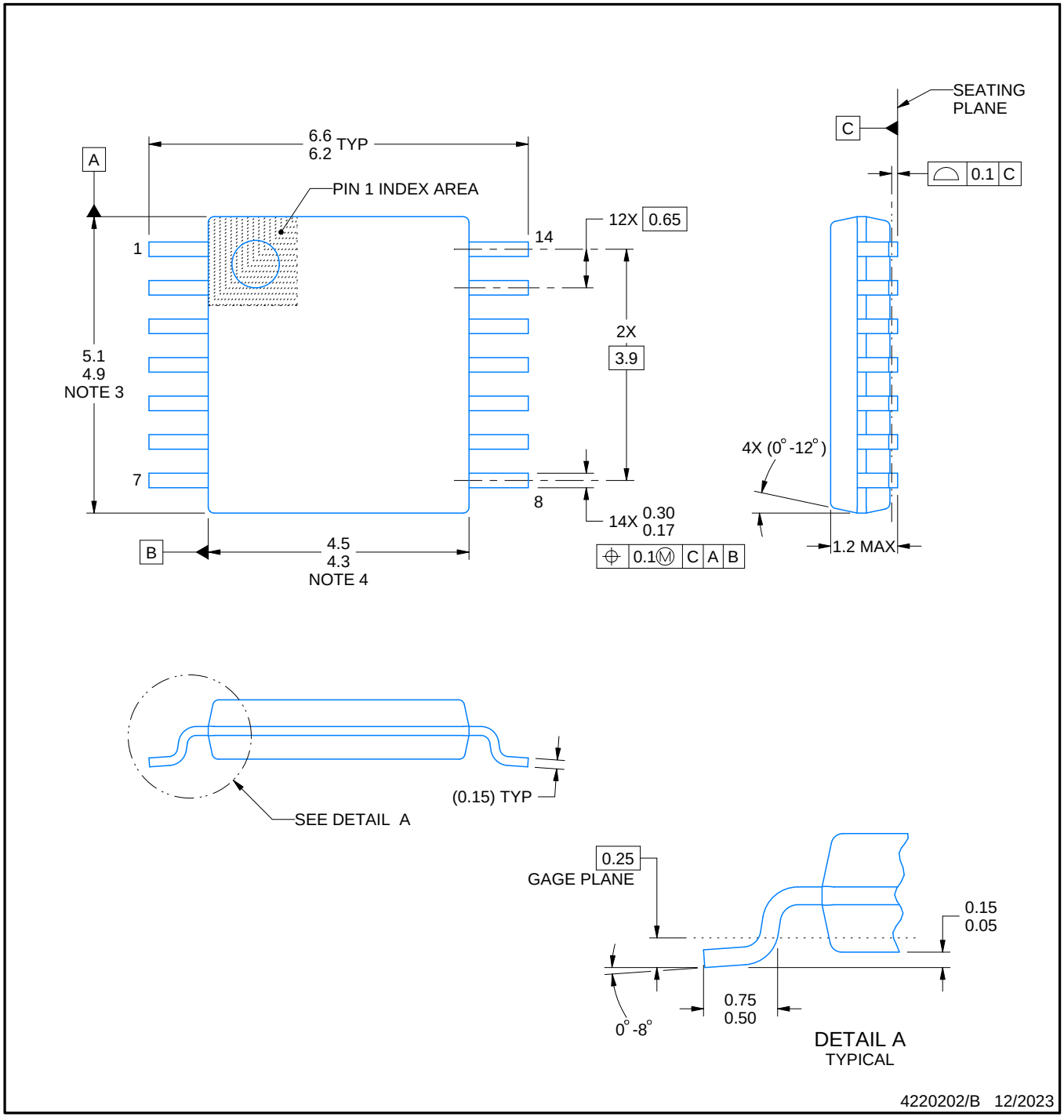
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

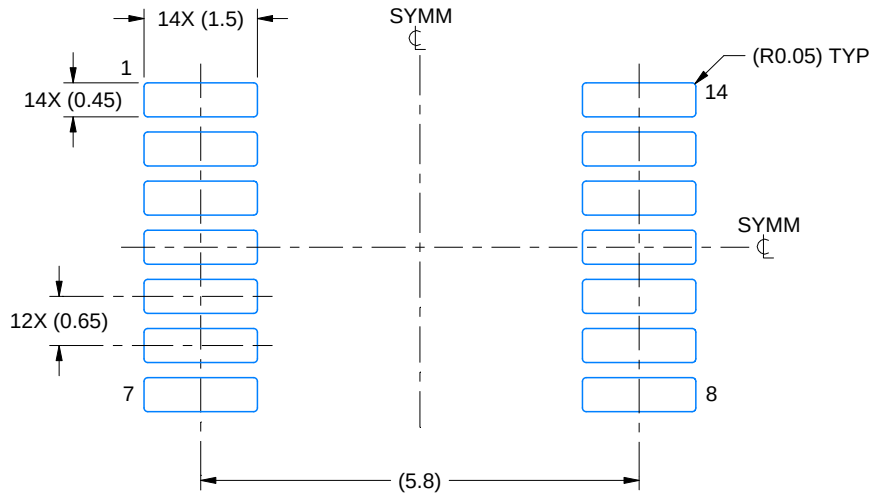
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

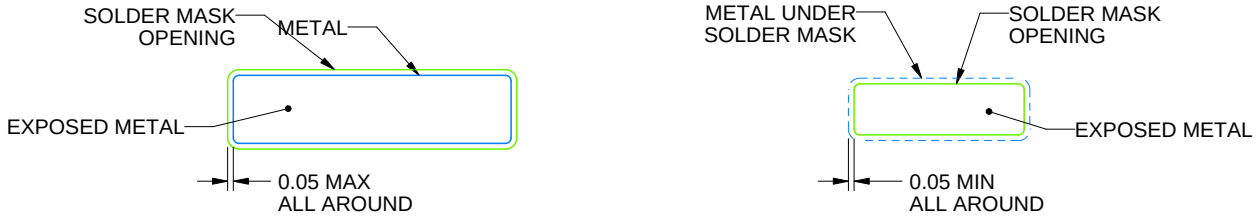


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

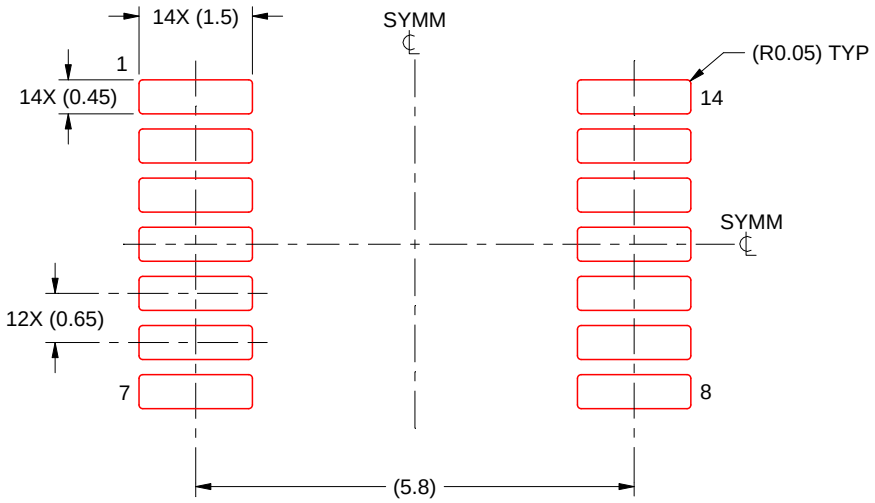


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

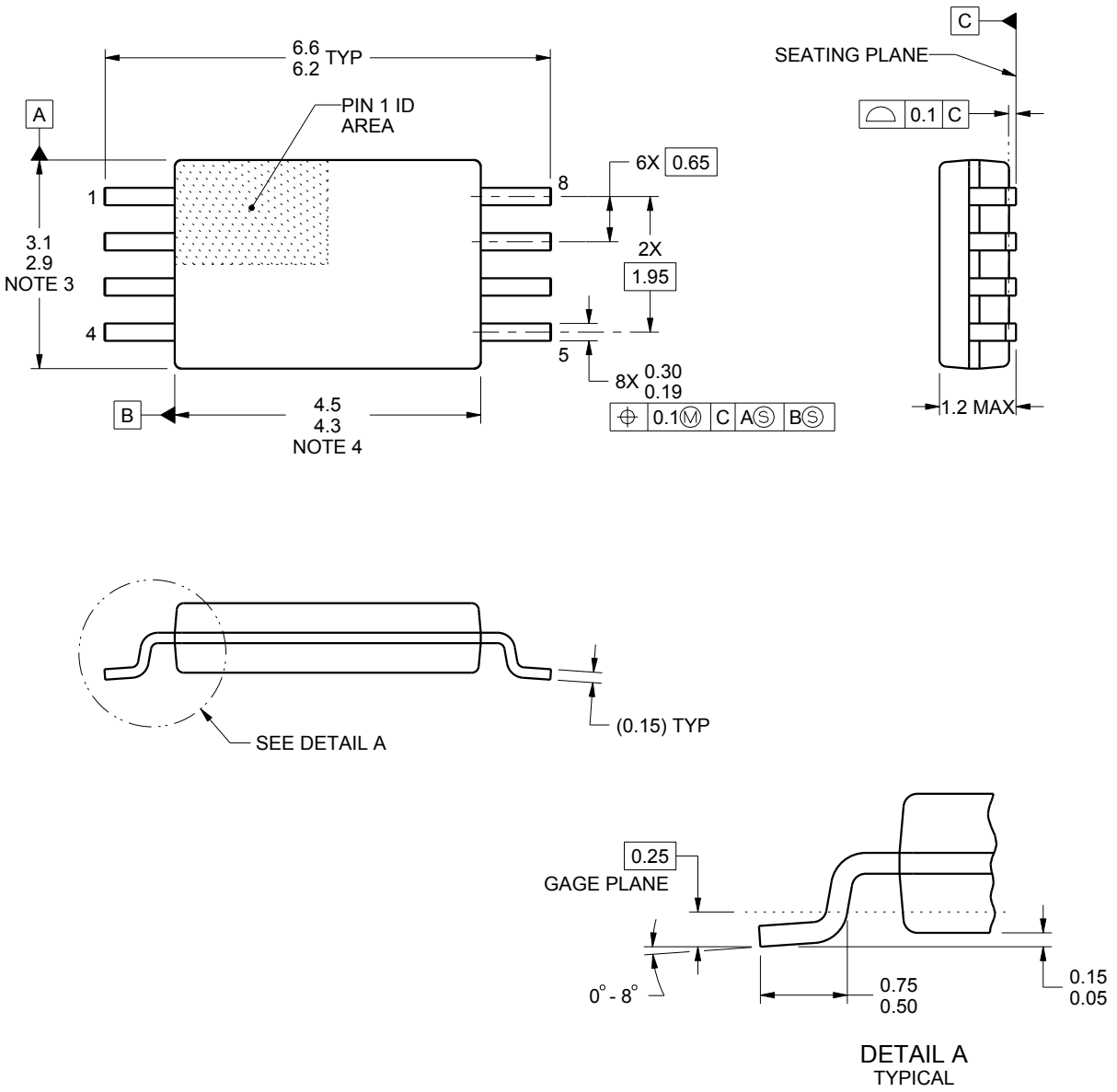
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

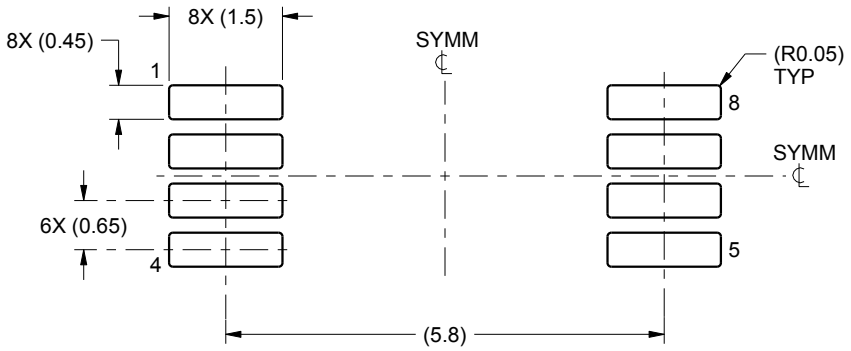
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

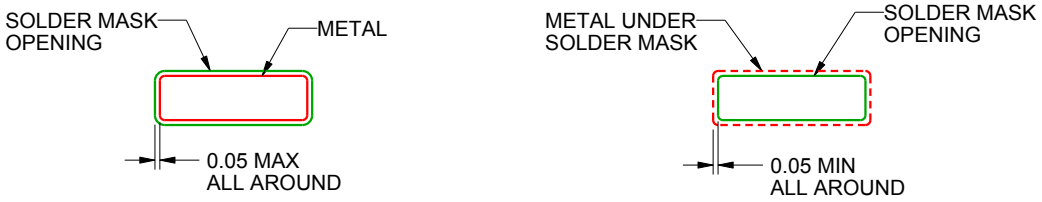


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

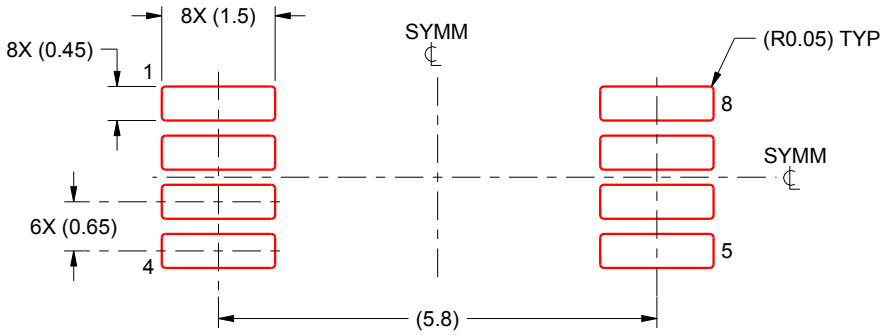


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

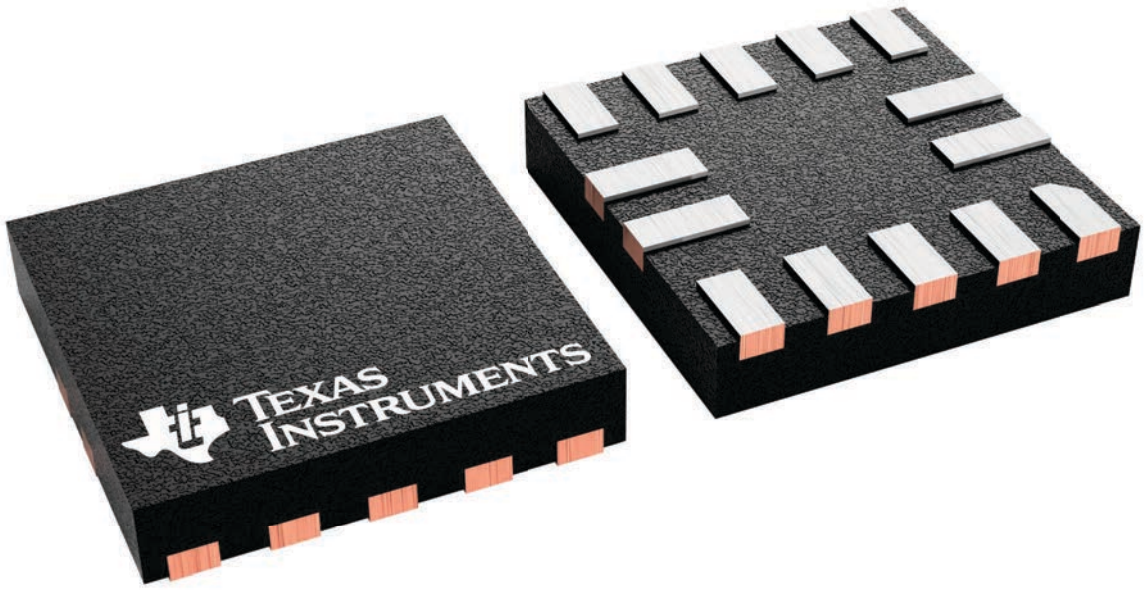
RUC 14

X2QFN - 0.4 mm max height

2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

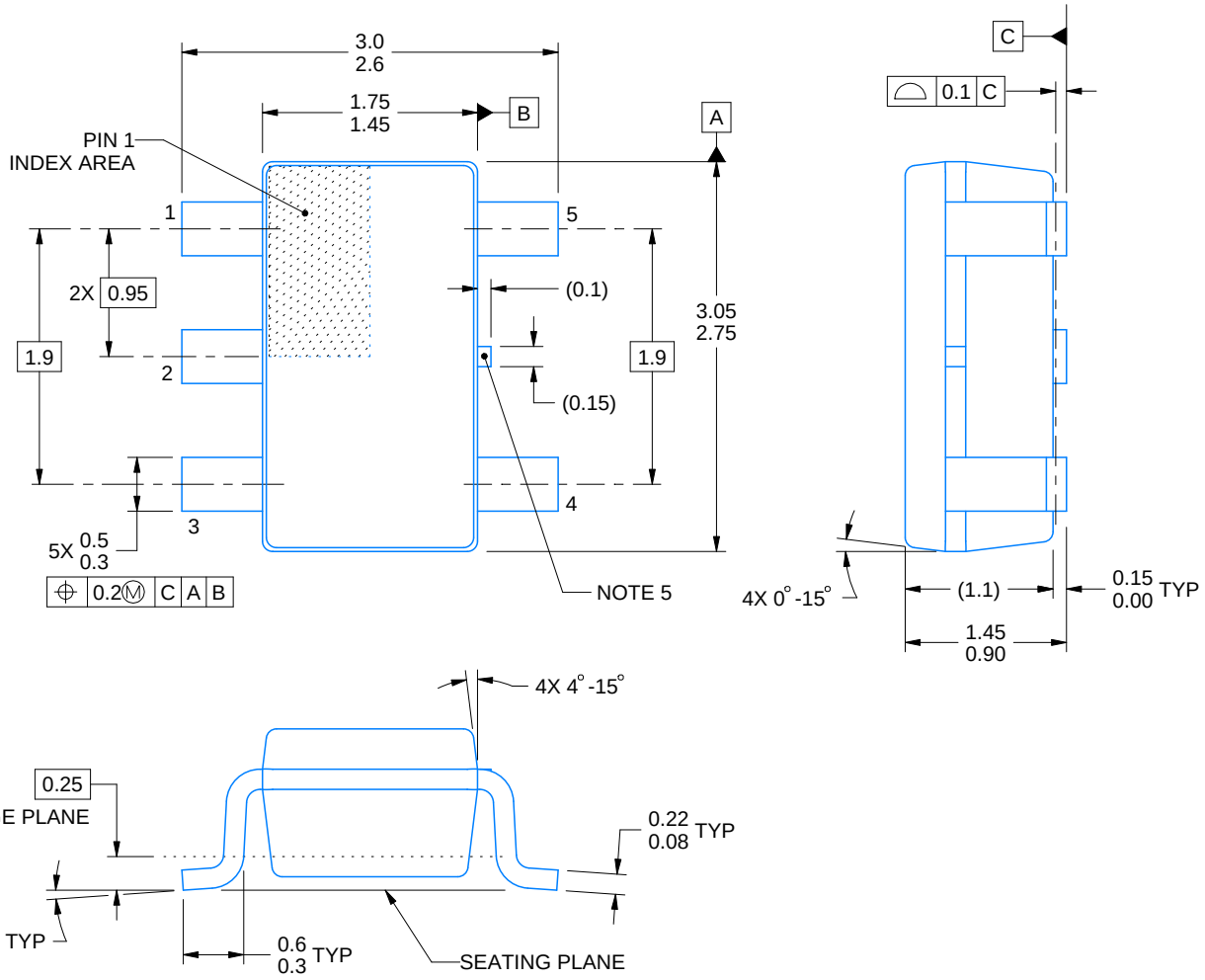


PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

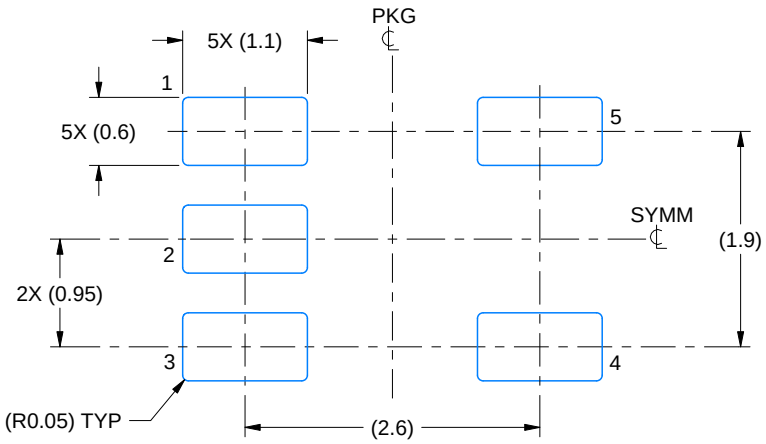
SMALL OUTLINE TRANSISTOR



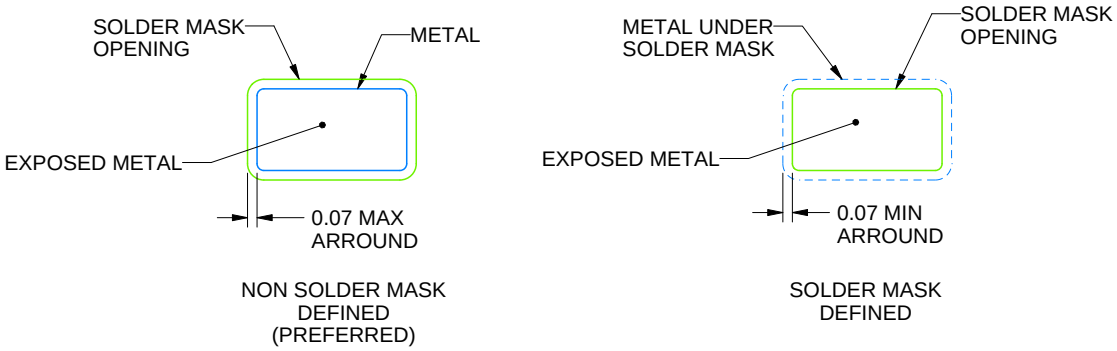
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

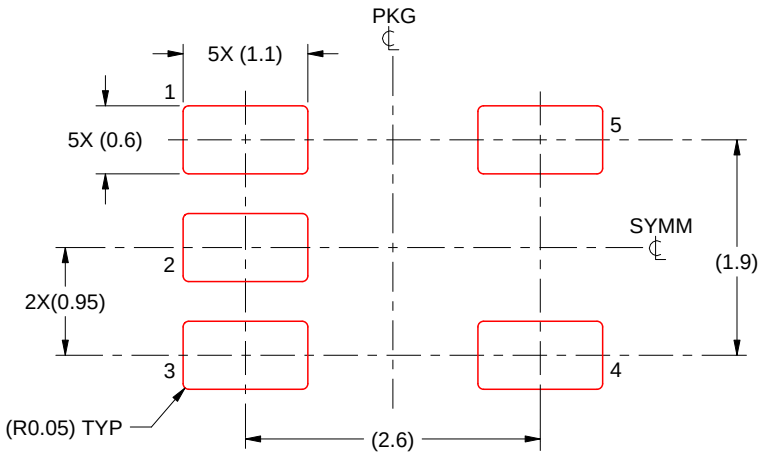


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

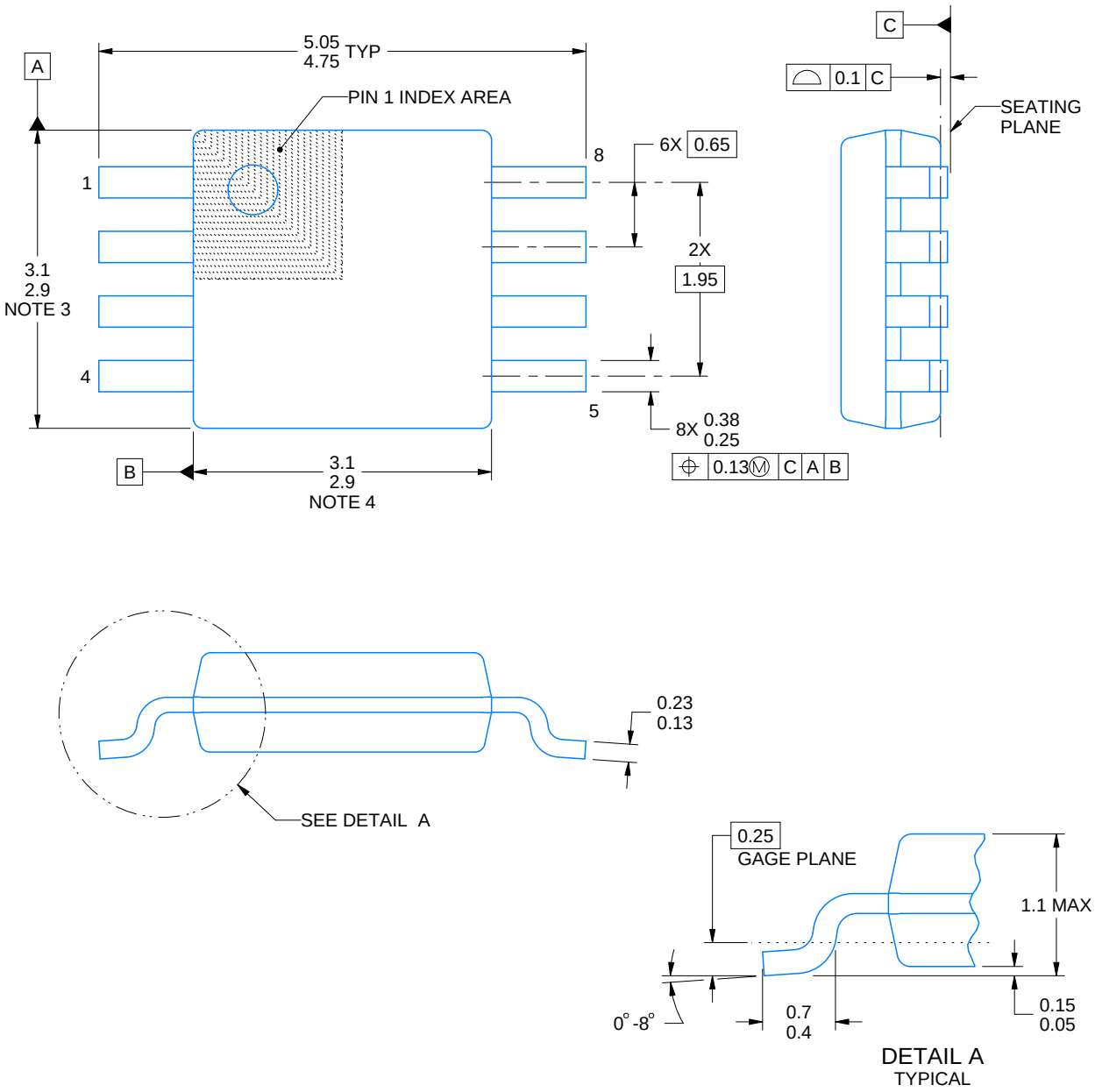
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

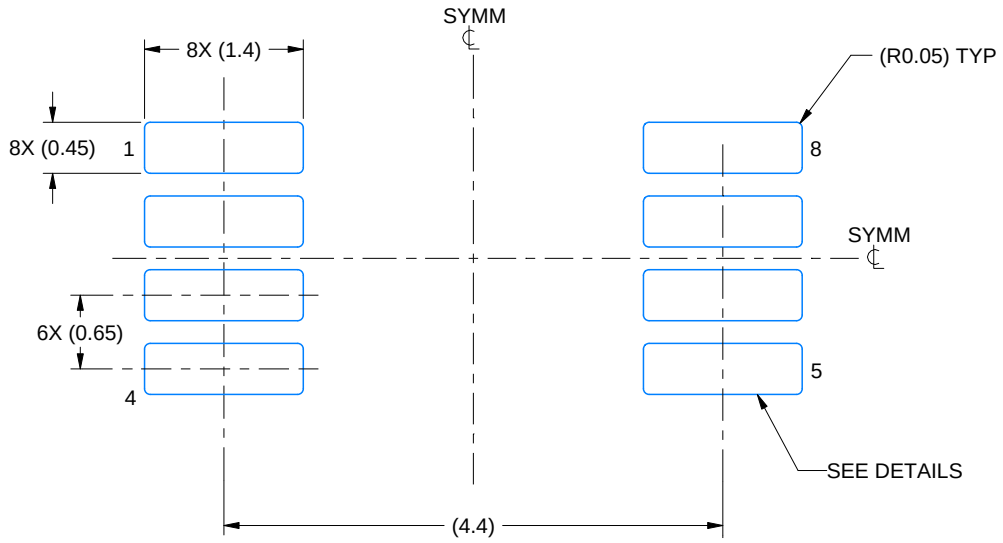
SMALL OUTLINE PACKAGE



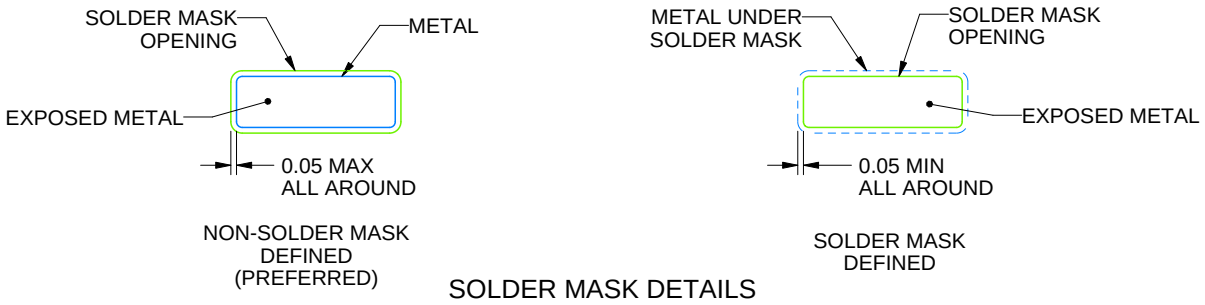
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

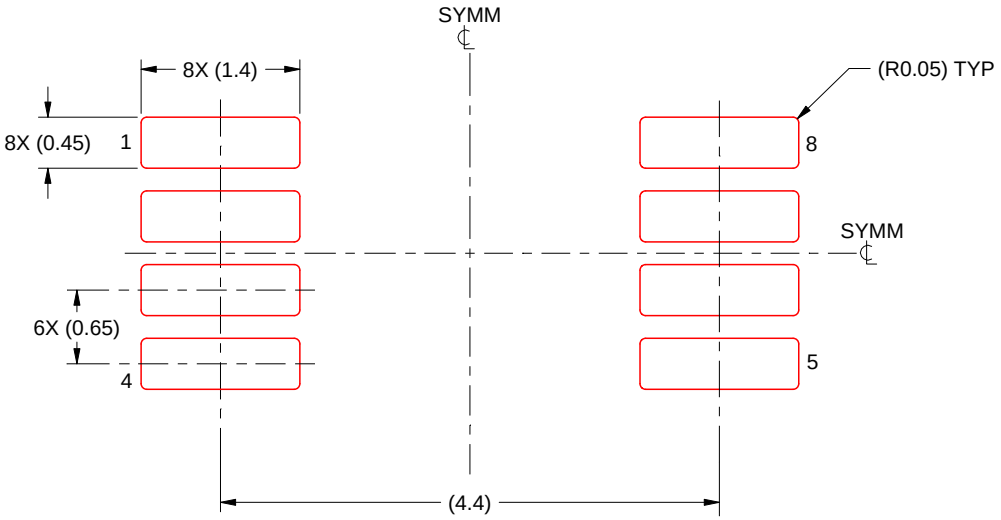


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



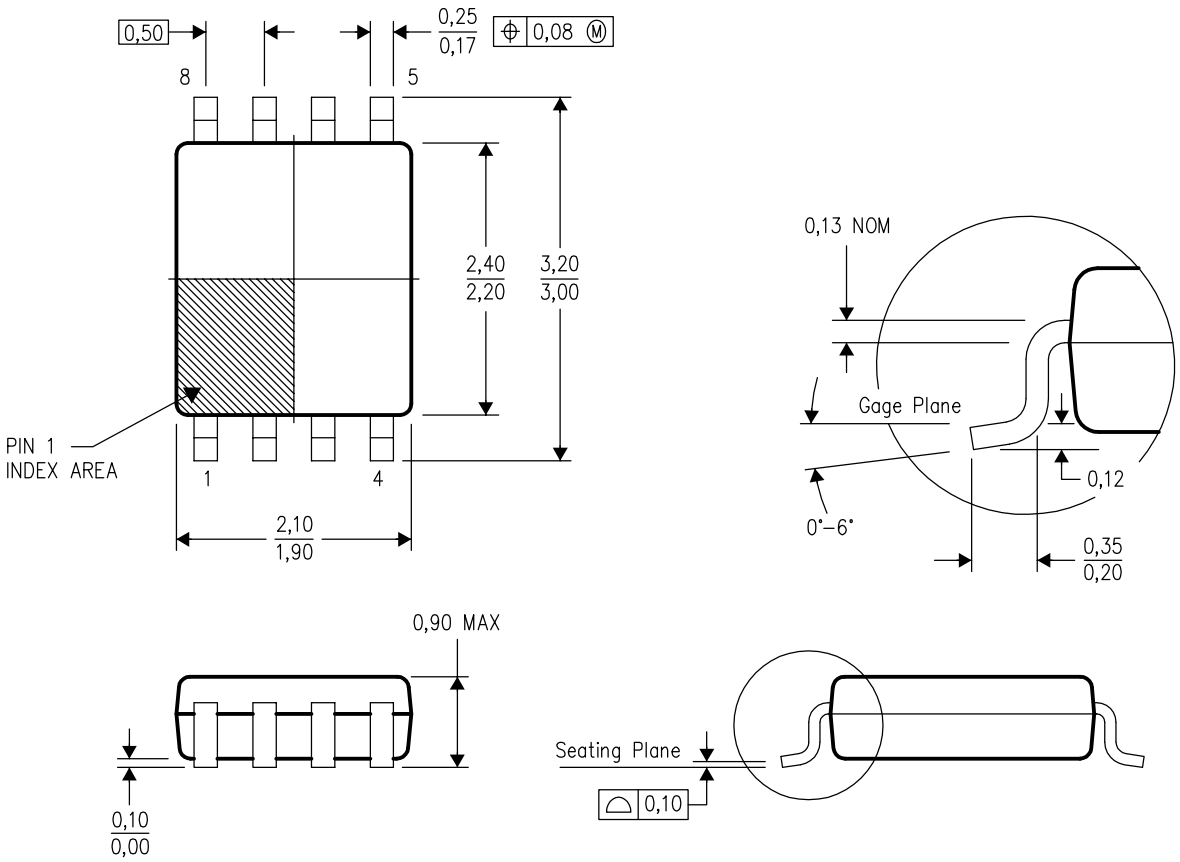
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

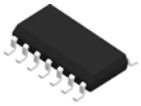
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4205140/A 05/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation CA.

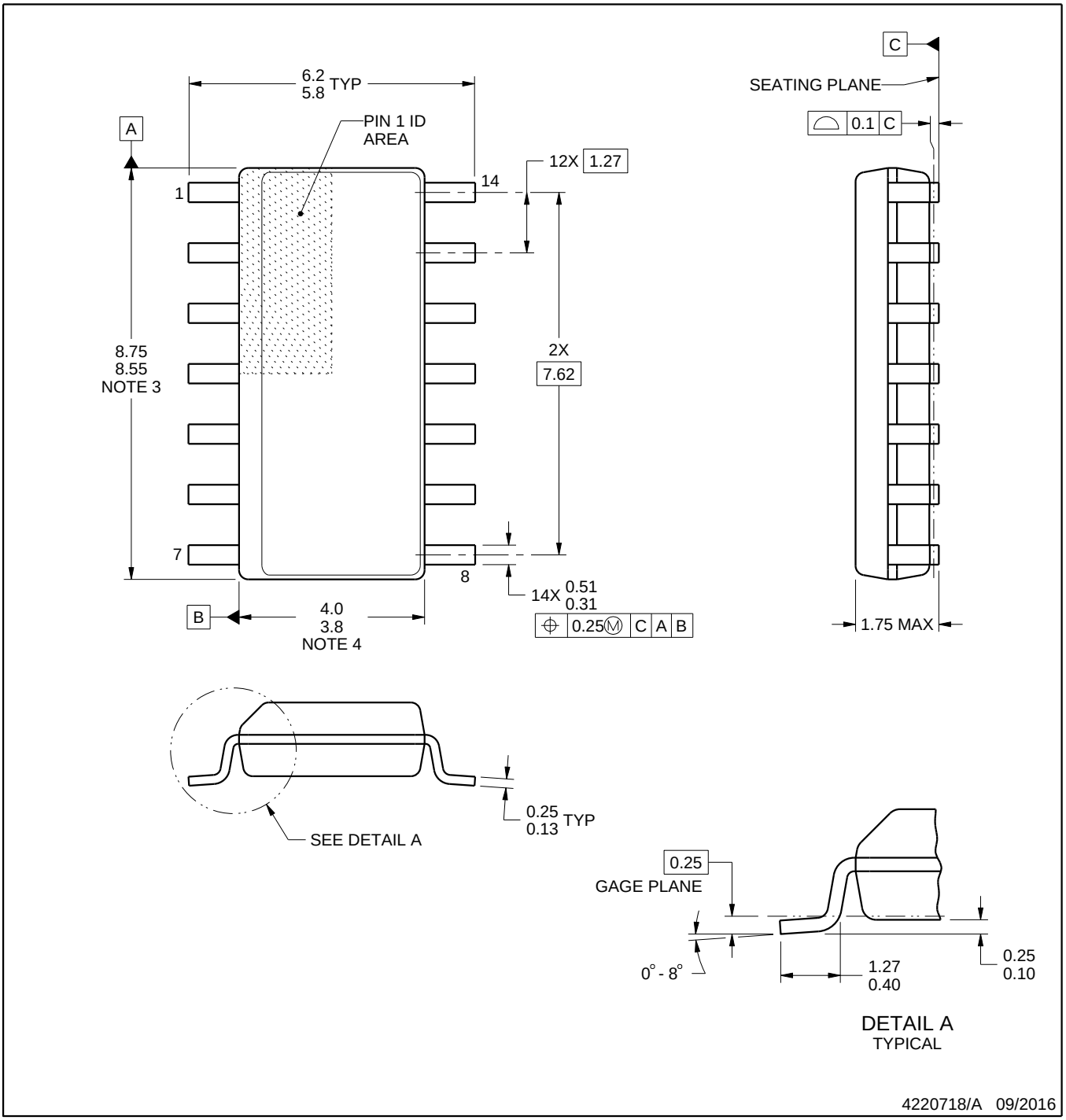


PACKAGE OUTLINE

D0014A

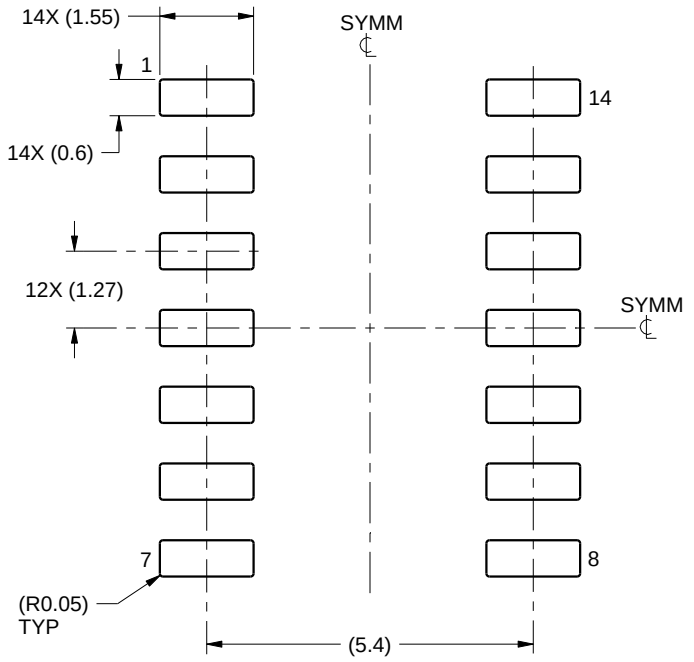
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

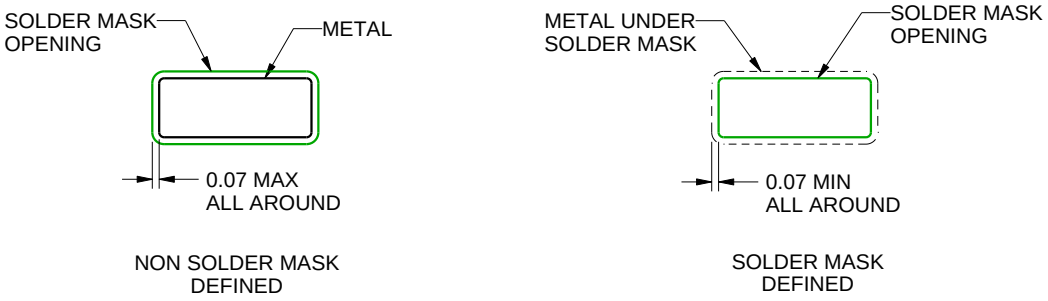


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

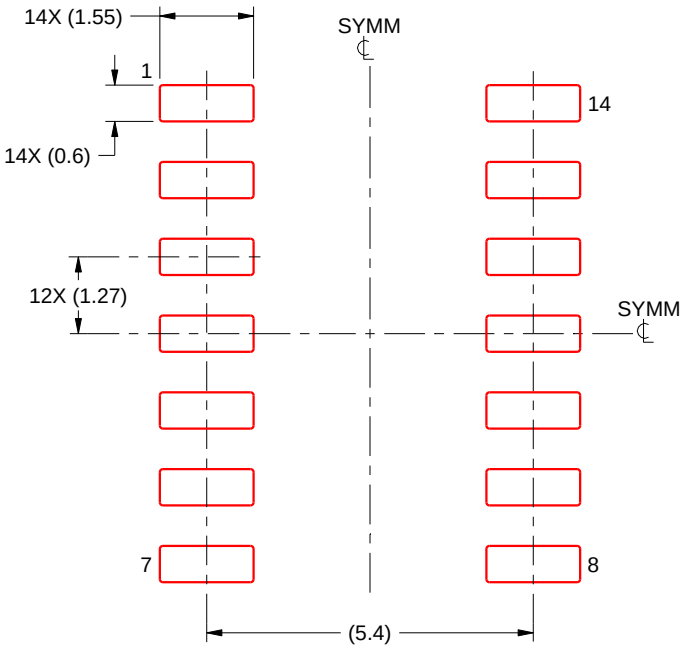
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月