MCT8316A 高速无传感器梯形控制集成 FET BLDC 驱动器

1 特性

- 采用集成无传感器电机控制算法的三相 BLDC 电机驱动器
  - 无代码高速梯形控制
  - 支持高达 3kHz（电气频率）
  - 非常短的启动时间（< 50ms）
  - 快速减速 (< 150ms)
  - 支持 120° 或 150° 调制，以改善声学性能
  - 通过正向重新同步和反向驱动支持风力机
  - 模拟，PWM，频率或基于 I^2C 的速度输入
  - 主动消磁支持减少功率损耗
  - 可配置的电机启动和停止选项
  - 可选闭环速度控制
  - 抗电压浪涌保护可防止过压
  - 通过 DACOUT 进行变量监控
- 4.5V 至 35V 工作电压（绝对最大值 40V）
- 高输出电流能力：8A 峰值
- 低 MOSFET 导通状态电阻
  - T_A = 25°C 时，$R_{DS(ON)}$ (HS + LS) 为 95mΩ
- 低功耗睡眠模式
  - V_{VM} = 24V、T_A = 25°C 时为 3μA（最大值）
- 速度环路精度：3% 使用内部时钟，1% 使用外部时钟参考
- 灵活的器件配置选项
  - MCT8316AV：I^2C 接口 (EEPROM)
  - MCT8316AT：基于硬件引脚的配置
- 支持高达 100kHz 的 PWM 频率，以支持低电感电机
- 不需要外部电流检测电阻器
- 内置 3.3V ±5%、20mA LDO 稳压器
- 内置 3.3V/5V、170mA 降压稳压器
- 专用 DRVOFF 引脚以禁用（高阻态）输出
- 展频和压摆率，用于降低 EMI
- 整套集成保护特性
  - 电源欠压锁定 (UVLO)
  - 电机锁定检测（5 种不同类型）
  - 过流保护 (OCP)
  - 热警告和热关断 (OTW/TSD)
  - 故障条件指示引脚 (nFAULT)
  - 可选择通过 I^2C 接口进行故障诊断

2 应用

- 无刷直流 (BLDC) 电机模块
- 机器人真空吸水电机
- 电机周期燃油泵
- 电器风扇和泵
- 汽车风扇和风机
- 医用 CPAP 风机

3 说明

MCT8316A 为需要高速运行（高达 3kHz 电气）或极快启动速度（< 50ms）的客户提供了一个单芯片无代码无传感器梯形解决方案，此解决方案适用于峰值电流高达 8A 的 12V 至 24V 无刷直流电机。MCT8316A 集成了三个 1/2H 桥，具有 40V 的绝对最大电压和 95mΩ 的超低 $R_{DS(ON)}$（高侧 + 低侧）。可调降压稳压器和 LDO 的电源管理系列能够为器件生成 3.3V 或 5.0V 电压轨，可用于为外部电路供电。

无传感器梯形控制功能具有很高的可配置性，通过寄存器设置 (MCT8316AV) 或硬件引脚 (MCT8316AT) 完成，范围从电机启动行为到闭环运行。MCT8316AV 的寄存器设置可在非易失性 EEPROM 中设置，从而允许器件在配置后独立运行。该器件通过 PWM 输入、模拟电压、可变频率方波或 I^2C 命令接收速度命令。MCT8316A 集成多种保护特性，旨在出现故障事件时保护该器件、电机和系统。

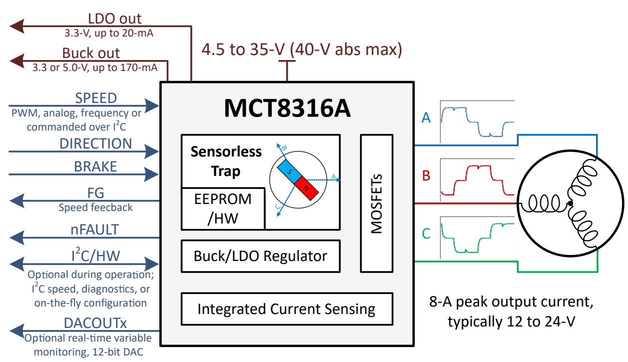
器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
MCT8316A1V	VQFN (40)	7.00mm x 5.00mm
MCT8316A1T	VQFN (40)	7.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

参考文档：

- 请参阅 E2E 常见问题解答中的阐释。
- 请参阅 MCT8316A 调优指南
- 请参阅 MCT8316A EVM GUI



简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision A (December 2021) to Revision B (February 2022) **Page**

- 更新了 E2E 链接........ 1

Changes from Revision * (August 2021) to Revision A (December 2021) **Page**

- 将器件状态更新为“量产数据”........ 1

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5 Device Comparison Table

DEVICE	PACKAGES	INTERFACE	BUCK REGULATOR
MCT8316AV	40-pin VQFN (7x5 mm)	I^2C	Yes
MCT8316AT		Hardware	

表 5-1. MCT8316AV (I^2C variant) vs MCT8316AT (Hardware variant) configuration comparison

Parameter	MCT8316AV (I^2C variant)	MCT8316AT (Hardware variant)
Initial Speed Detect (ISD) Parameters		
ISD Enable	ISD_EN (2 settings)	Enable
Brake Enable	BRAKE_EN (2 settings)	Disable
Hi-Z Enable	HIZ_EN (2 settings)	Disable
Reverse Drive Enable	RVS_DR_EN (2 settings)	Enable
Resynchronization Enable	RESYNC_EN (2 settings)	Enable
Stationary Brake Enable	STAT_BRK_EN (2 settings)	Enable
Stationary Detect Threshold	STAT_DETECT_THR (8 settings)	25-mV
Brake Mode	BRK_MODE(2 settings)	Low side
Brake Configuration	BRK_CONFIG (2 settings)	N/A since BRAKE_EN is set to Disable
Brake Current Threshold	BRK_CURR_THR (8 settings)	
Brake Time	BRK_TIME (16 settings)	
Hi-Z Time	HIZ_TIME (16 settings)	N/A since HIZ_EN is set to Disable
Stationary Brake Time	STARTUP_BRK_TIME (8 settings)	RMP_1, RMP_2 pins (12 settings)
Motor Start-up Parameters		
Start-up Method	MTR_STARTUP (4 settings)	RMP_1 pin (2 settings)
Align Ramp Rate	ALIGN_RAMP_RATE (16 settings)	RMP_1, RMP_2 pins (4 settings)
Align Time	ALIGN_TIME (16 settings)	RMP_1, RMP_2 pins (16 settings)
Align Duty	ALIGN_DUTY (8 settings)	20%
Align Current Threshold	ALIGN_CURR_THR (16 settings)	ILIMIT_1, ILIMIT_2 pins (7 settings)
IPD Clock Frequency	IPD_CLK_FREQ (8 settings)	CONFIG_1 pin (4 settings)
IPD Current Threshold	IPD_CURR_THR (16 settings)	ILIMIT_1, ILIMIT_2 pins (7 settings)
IPD Release Mode	IPD_RLS_MODE (2 settings)	Tristate
IPD Advance Angle	IPD_ADV_ANGLE (4 settings)	30º
IPD Repeat Times	IPD_REPEAT (4 settings)	RMP_1, RMP_2 pins (2 settings)
First Cycle Frequency	SLOW_FIRST_CYC_FREQ (16 settings)	RMP_1, RMP_2 pins (18 settings)
Open Loop Parameters		
Open Loop Current Limit Configuration	OL_ILIMIT_CONFIG (2 settings)	Open loop current limit defined by OL_ILIMIT
Open Loop Duty Cycle	OL_DUTY (8 settings)	RMP_1, RMP_2 pins (4 settings)
Open Loop Current Limit	OL_ILIMIT (16 settings)	ILIMIT_1, ILIMIT_2 pins (7 settings)
Open Loop Acceleration A1	OL_ACC_A1 (32 settings)	RMP_1, RMP_2 pins (16 settings)
Open Loop Acceleration A2	OL_ACC_A2 (32 settings)	Same value as OL_ACC_A1
Open to Closed Loop Handoff Threshold	OPN_CL_HANDOFF_THR (32 settings)	RMP_1, RMP_2 pins (2 settings)
Auto Handoff	AUTO_HANDOFF (2 settings)	RMP_1, RMP_2 pins (2 settings)
First Cycle Frequency Select	FIRST_CYCLE_FREQ_SEL (2 settings)	Defined by SLOW_FIRST_CYC_FREQ
Minimum Duty	MIN_DUTY (16 settings)	CONFIG_3 pin (4 settings)
Closed Loop Parameters		
Commutation Type	COMM_CONTROL (2 options)	120º commutation
Closed Loop Acceleration Rate	CL_ACC (32 settings)	RMP_1, RMP_2 pins (16 settings)
Closed Loop Deceleration Rate	CL_DEC (32 settings)	Same value as CL_ACC

表 5-1. MCT8316AV (I^2C variant) vs MCT8316AT (Hardware variant) configuration comparison (continued)

Parameter	MCT8316AV (I^2C variant)	MCT8316AT (Hardware variant)
PWM Switching Frequency	PWM_FREQ_OUT (32 settings)	CONFIG_1 pin (8 settings)
PWM Modulation	PWM_MODUL (3 settings)	Mixed modulation
PWM Mode	PWM_MODE (2 settings)	Single-ended mode
Lead Angle Polarity	LD_ANGLE_POLARITY	Positive
Lead Angle	LD_ANGLE(256 settings)	LDANGLE pin (16 settings)
Dynamic Degauss Enable	DYN_DEGAUSS_EN (2 settings)	RMP_1, RMP_2 pins (2 settings)
BEMF Threshold	BEMF_THRESHOLD1 and BEMF_THRESHOLD2 (64 settings)	LDANGLE pin (16 settings)
Fast Start-up Enable	INTEG_ZC_METHOD (2 settings)	RMP_1, RMP_2 pin (2 settings)
Speed/ Power Loop Enable	CLOSED_LOOP_MODE (4 settings)	Disable
Maximum Speed	MAX_SPEED (65536 settings)	N/A since CLOSED_LOOP_MODE is set to Disable
Speed/ Power Loop Max. Duty Cycle	SPD_POWER_V_MAX (8 settings)	
Speed/ Power Loop Min. Duty Cycle	SPD_POWER_V_MIN (8 settings)	
Speed/ Power Loop Kp	SPD_POWER_KP (1024 settings)	
Speed/ Power Loop Ki	SPD_POWER_KI (4096 settings)	
Power Regulation Mode	CONST_POWER_MODE (4 settings)	
Maximum Power	MAX_POWER (1024 settings)	
Constant Power Limit Hysteresis	CONST_POWER_LIMIT_HYST (4 settings)	
Fast Deceleration Enable	FAST_DECEL_EN (2 settings)	Disable
Fast Deceleration Current Limit	FAST_DECEL_CURR_LIM (16 settings)	N/A since FAST_DECEL_EN is set to Disable
Fast Deceleration Speed Delta	FAST_BRK_DELTA (8 settings)	
Fast Deceleration Duty Threshold	FAST_DEC_DUTY_THR (8 settings)	
Fast Deceleration Duty Window	FAST_DEC_DUTY_WIN (8 settings)	
Dynamic Brake Current Limit Enable	DYNAMIC_BRK_CURR (2 settings)	
Dynamic Brake Current Low Limit	DYN_BRK_CURR_LOW_LIM (16 settings)	
FG Signal Configuration Parameters		
FG Output Mode Select	FG_SEL (3 settings)	Output FG in open and closed loop
FG division factor	FG_DIV (16 settings)	Divide by 1 (2-pole motor)
FG Configuration	FG_CONFIG (2 settings)	FG active as long as motor is driven
FG BEMF Threshold	FG_BEMF_THR (8 settings)	N/A since FG_CONFIG is set to FG active as long as motor is driven
Motor Stop Configuration Parameters		
Motor Stop Method	MTR_STOP (5 settings)	Recirculation mode
Motor Brake Time	MTR_STOP_BRK_TIME (16 settings)	1000-ms
Active Spin-down Brake Duty Cycle Threshold	ACT_SPIN_BRK_THR (8 settings)	N/A since MTR_STOP set to recirculation mode
Brake Duty Threshold	BRAKE_DUTY_THRESHOLD (8 settings)	Immediate
AVS Enable	AVS_EN (2 settings)	Enable
Fault Protection Parameters		
Cycle-by-Cycle(CBC) Current Limit	CBC_ILIMIT (16 settings)	ILIMIT_2 pin (7 settings)
CBC Current Limit Mode	CBC_ILIMIT_MODE (9 settings)	Auto recovery next PWM cycle; nFault active; driver is in recirculation state
Lock Current Limit Mode	LOCK_ILIMIT_MODE (9 settings)	Disable
Lock Current Limit	LOCK_ILIMIT (16 settings)	N/A since LOCK_ILIMIT_MODE is set to Disable
Lock Current Deglitch Time	LOCK_ILIMIT_DEG (16 settings)	
CBC Limit Retry PWM Cycles	CBC_RETRY_PWM_CYC (4 settings)	N/A since CBC_ILIMIT_MODE is set to Auto recovery next PWM cycle

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表 5-1. MCT8316AV (I^{2}C variant) vs MCT8316AT (Hardware variant) configuration comparison (continued)

Parameter	MCT8316AV (I^{2}C variant)	MCT8316AT (Hardware variant)
Motor Lock Mode	MTR_LCK_MODE (9 settings)	Automatic recovery after tCLK_RETRY; driver is tristated
Lock Retry Time	LCK_RETRY (8 settings)	5s
Abnormal Speed Enable	LOCK1_EN (2 settings)	Enable
Loss of Sync Enable	LOCK2_EN (2 settings)	Enable
No Motor Enable	LOCK3_EN (2 settings)	Enable
Abnormal Speed Threshold	LOCK_ABN_SPEED (8 settings)	CONFIG_3 pin (4 settings)
Number of Times Sync Lost	LOSS_SYNC_TIMES (8 settings)	Trigger after losing sync 5 times
No Motor Threshold	NO_MTR_THR (8 settings)	25-mV
Overvoltage Threshold	MAX_VM_MOTOR (8 settings)	No Limit
Overvoltage Mode	MAX_VM_MODE (2 settings)	N/A since MAX_VM_MOTOR set to No Limit
Undervoltage Threshold	MIN_VM_MOTOR (8 settings)	No Limit
Undervoltage Mode	MIN_VM_MODE (2 settings)	N/A since MIN_VM_MOTOR set to No Limit
Automatic Retry Attempts	AUTO_RETRY_TIMES (8 settings)	No Limit
150º Commutation Parameters		
150º Two Phase Step 0 Duty	TWOPH_STEP0 (8 settings)	N/A since COMM_CONTROL set to 120º commutation
150º Two Phase Step 1 Duty	TWOPH_STEP1 (8 settings)	
150º Two Phase Step 2 Duty	TWOPH_STEP2 (8 settings)	
150º Two Phase Step 3 Duty	TWOPH_STEP3 (8 settings)	
150º Two Phase Step 4 Duty	TWOPH_STEP4 (8 settings)	
150º Two Phase Step 5 Duty	TWOPH_STEP5 (8 settings)	
150º Two Phase Step 6 Duty	TWOPH_STEP6 (8 settings)	
150º Two Phase Step 7 Duty	TWOPH_STEP7 (8 settings)	
150º Three Phase Step 0 Duty	THREEPH_STEP0 (8 settings)	
150º Three Phase Step 1 Duty	THREEPH_STEP1 (8 settings)	
150º Three Phase Step 2 Duty	THREEPH_STEP2 (8 settings)	
150º Three Phase Step 3 Duty	THREEPH_STEP3 (8 settings)	
150º Three Phase Step 4 Duty	THREEPH_STEP4 (8 settings)	
150º Three Phase Step 5 Duty	THREEPH_STEP5 (8 settings)	
150º Three Phase Step 6 Duty	THREEPH_STEP6 (8 settings)	
150º Three Phase Step 7 Duty	THREEPH_STEP7 (8 settings)	
Miscellaneous Algorithm Parameters		
Open to Closed Loop Handoff Cycles	OL_HANDOFF_CYC (4 settings)	RMP_1, RMP_2 pins (2 settings)
Blanking Time	TBLANK (16 settings)	CONFIG_1 pin (5 settings)
Lead Angle for 150º commutation	LEAD_ANGLE_150DEG_ADV (4 settings)	N/A since COMM_CONTROL is set to 120º commutation
Gate Driver Parameters		
Slew Rate	SLEW_RATE (4 settings)	SLEW_RATE pin(4 settings)
Overvoltage Level	OVP_SEL (2 settings)	32-V
Overvoltage Enable	OVP_EN (2 settings)	Enable
Overtemperature Warning Reporting Enable	OTW_REP (2 settings)	Disable
OCP Retry Time	OCP_RETRY (2 settings)	500-ms
OCP Level	OCP_LVL (2 settings)	CONFIG_2 pin (2 settings)
OCP Mode	OCP_MODE (4 settings)	CONFIG_2 pin (2 settings)
BEMF Comparator Threshold	BEMF_THR (2 settings)	
Active Asynchronous Rectification Enable	EN_AAR (2 settings)	CONFIG_2 pin (2 settings)

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表 5-1. MCT8316AV (I²C variant) vs MCT8316AT (Hardware variant) configuration comparison (continued)

Parameter	MCT8316AV (I²C variant)	MCT8316AT (Hardware variant)
Active Synchronous Rectification Enable	EN_ASR (2 settings)	Same as EN_AAR
Current Sense Amplifier Gain	CSA_GAIN (4 settings)	ILIMIT pin(4 settings)
Delay Compensation Enable	DELAY_COMP_EN (2 settings)	CONFIG_2 pin (2 settings)
Delay Target	TARGET_DELAY (16 settings)	0-µs
Buck Slew Rate	BUCK_SR (2 settings)	1000-V/µs
Buck Power Sequencing Disable	BUCK_PS_DIS (2 settings)	Disabled if BUCK_SEL set to 3.3V; else enabled
Buck Current Limit	BUCK_CL (2 settings)	600-mA
Buck Voltage Selection	BUCK_SEL (4 settings)	SLEW_RATE pin (2 settings)
Buck Disable	BUCK_DIS (2 settings)	Enable
Pin and Device Configuration Parameters		
Register address of variable to be monitored on DACOUT1 pin	DACOUT1_VAR_ADDR (12-bit)	N/A
Register address of variable to be monitored on DACOUT1 pin	DACOUT2_VAR_ADDR (12-bit)	N/A
Brake Configuration	BRAKE_INPUT (3 settings)	BRAKE pin input
Direction Configuration	DIR_INPUT (3 settings)	DIR pin input
Speed Input Mode	SPD_CTRL_MODE (4 settings)	Speed input in analog mode
SOx Pin	DAC_SOX_CONFIG (4 settings)	N/A
Pin 36 and 37 Configuration	DAC_XTAL_CONFIG (2 settings)	N/A
Spread Spectrum Modulation	SSM_CONFIG (2 settings)	Enable
Device Mode	DEV_MODE (2 settings)	Standby
Speed PWM Input Range	SPD_PWM_RANGE_SELECT (2 settings)	325-Hz to 95-kHz
Clock Source	CLK_SEL (3 settings)	Internal oscillator
External Clock Mode Enable	EXT_CLK_EN (2 settings)	N/A since CLK_SEL set to Internal Oscillator
External Clock Configuration	EXT_CLK_CONFIG (8 settings)	N/A since CLK_SEL set to Internal Oscillator

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6 Pin Configuration and Functions

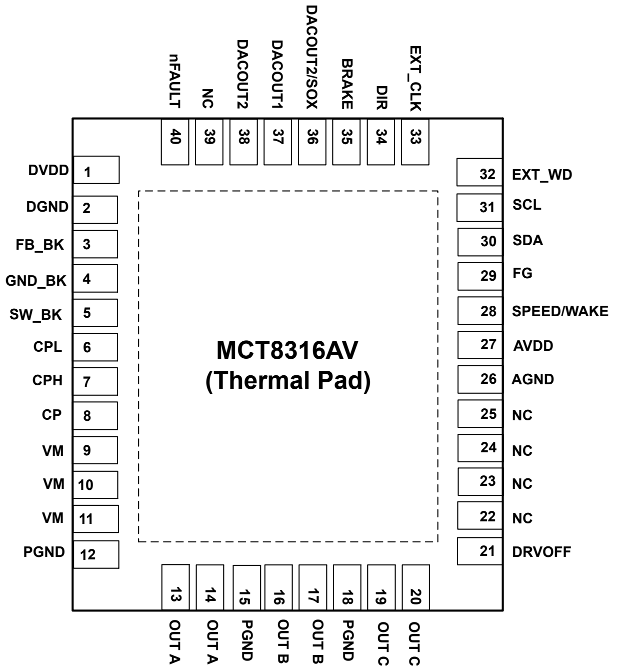

图 6-1. MCT8316AV 40-Pin VQFN With Exposed Thermal Pad Top View

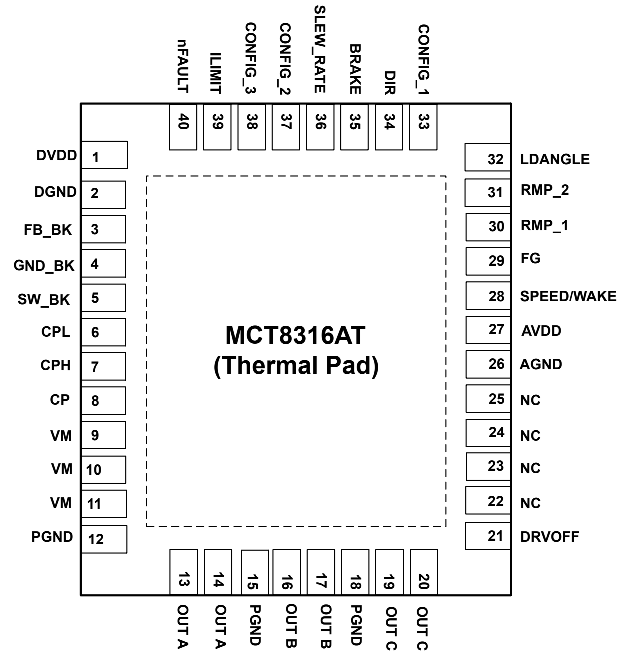

图 6-2. MCT8316AT 40-Pin VQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN	40-pin Package		TYPE(1)	DESCRIPTION
NAME	MCT8316AV	MCT8316AT		
AGND	26	26	GND	Device analog ground. Refer Layout Guidelines for connections recommendation.
AVDD	27	27	PWR O	3.3-V internal regulator output. Connect a X5R or X7R, 1-μF, 6.3-V ceramic capacitor between the AVDD1 and AGND pins. This regulator can source up to 20 mA externally.
BRAKE	35	35	I	High → brake the motor Low → normal operation Connect to PGND via 10-kΩ resistor, if not used
CONFIG_1	-	33	I	Connect resistor to GND for parameter configuration.
CONFIG_2	-	37	I	Connect resistor to GND for parameter configuration.
CONFIG_3	-	38	I	Connect resistor to GND for parameter configuration.
CP	8	8	PWR	Charge pump output. Connect a X5R or X7R, 1-μF, 16-V ceramic capacitor between the CP and VM pins.
CPH	7	7	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
CPL	6	6	PWR	
DACOUT2/ SOX	36	-	O	Multipurpose pin: DAC output when configured as DACOUT2 CSA output configured as SOX
DACOUT1	37	-	O	DAC output DACOUT1
DACOUT2	38	-	O	DAC output DACOUT2
DGND	2	2	GND	Device digital ground. Refer Layout Guidelines for connections recommendation.

表 6-1. Pin Functions (continued)

PIN	40-pin Package		TYPE(1)	DESCRIPTION
NAME	MCT8316A V	MCT8316A T		
DIR	34	34	I	Direction of motor spinning; When low, phase driving sequence is OUT A → OUT B → OUT C When high, phase driving sequence is OUT A → OUT C → OUT B Connect to PGND via 10-kΩ resistor, if not used
DRVOFF	21	21	I	Coast (Hi-Z) all six MOSFETs.
DVDD	1	1	PWR	1.5-V internal regulator output. Connect a X5R or X7R, 1-μF, 6.3-V ceramic capacitor between the DVDD and DGND pins.
EXT_CLK	33	-	I	External clock reference input in external clock reference mode.
EXT_WD	32	-	I	External watchdog input.
FB_BK	3	3	PWR I/O	Feedback for buck regulator. Connect to buck regulator output after the inductor/ resistor.
FG	29	29	O	Motor speed indicator output. Open-drain output requires an external pull-up resistor to 1.8 to 5-V.
GND_BK	4	4	GND	Buck regulator ground. Refer Layout Guidelines for connections recommendation.
ILIMIT	-	39	I	Connect resistor to GND for parameter configuration.
LDANGLE	-	32	I	Connect resistor to GND for parameter configuration.
NC	22, 23, 24, 25, 39	22, 23, 24, 25	-	No connection, open
nFAULT	40	40	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8V to 5.0V.
OUTA	13, 14	13, 14	PWR O	Half bridge output A
OUTB	16, 17	16, 17	PWR O	Half bridge output B
OUTC	19, 20	19, 20	PWR O	Half bridge output C
PGND	12, 15, 18	12, 15, 18	GND	Device power ground. Refer Layout Guidelines for connections recommendation.
RMP_1	-	30	I	Connect resistor to GND for parameter configuration.
RMP_2	-	31	I	Connect resistor to GND for parameter configuration.
SCL	31	-	I	I^2C clock input
SDA	30	-	I/O	I^2C data line
SLEW_RATE	-	36	I	Connect resistor to GND for parameter configuration.
SPEED/ WAKE	28	28	I	Device speed input; supports analog, frequency or PWM speed input. The speed pin input can be configured through SPD_CTRL_MODE.
SW_BK	5	5	PWR	Buck switch node. Connect this pin to an inductor or resistor.
VM	9, 10, 11	9, 10, 11	PWR I	Device and motor power supply. Connect to motor supply voltage; bypass to GND with a 0.1-μF capacitor plus one bulk capacitor. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
Thermal pad			GND	Must be connected to ground

(1) I = input, O = output, GND = groung pin, PWR = power, NC = no connect

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	40	V
Power supply voltage ramp (VM)		4	V/μs
Voltage difference between ground pins (GND_BK,DGND, PGND, AGND)	–0.3	0.3	V
Charge pump voltage (CPH, CP)	–0.3	V_{VM} + 6	V
Charge pump negative switching pin voltage (CPL)	–0.3	V_{VM} +0.3	V
Switching regulator pin voltage (FB_BK)	–0.3	5.75	V
Switching node pin voltage (SW_BK)	–0.3	V_{VM} +0.3	V
Analog regulators pin voltage (AVDD)	–0.3	4	V
Analog regulators pin voltage (DVDD)	–0.3	1.7	V
Logic pin input voltage (BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SCL, SDA, SPEED)	–0.3	6	V
Open drain pin output voltage (nFAULT, FG)	–0.3	6	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_{VM} + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	35	V
I_{OUT} [1]	Peak output winding current	OUTA, OUTB, OUTC			8	A
V_{IN_LOGIC}	Logic input voltage	BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SPEED, SDA, SCL	–0.1		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT, FG	–0.1		5.5	V
I_{OD}	Open drain output current capability	nFAULT, FG			5	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating Junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC[(1)]		MCT8316A RGF (VQFN) 40 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6 V, V_{SPEED} = 0, T_A = 25 °C		3	5	µA
		V_{SPEED} = 0, T_A = 125 °C		3.5	7	µA
I_{VMS}	VM standby mode current	V_{VM} > 6 V, V_{SPEED} > V_{EN_SB}, DRVOFF = High, T_A = 25 °C, L_{BK} = 47 uH, C_{BK} = 22 µF		8	15	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EN_SB}, DRVOFF = High, R_{BK} = 22 Ω, C_{BK} = 22 µF		25	28	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EN_SB}, DRVOFF = High, L_{BK} = 47 uH, C_{BK} = 22 µF		8	15	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EN_SB}, DRVOFF = High, R_{BK} = 22 Ω, C_{BK} = 22 µF		25	28	mA
I_{VM}	VM operating mode current	V_{VM} > 6 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), T_J = 25 °C, L_{BK} = 47 uH, C_{BK} = 22 µF, No Motor Connected		11	18	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), T_J = 25 °C, R_{BK} = 22 Ω, C_{BK} = 22 µF, No Motor Connected		27	30	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), L_{BK} = 47 uH, C_{BK} = 22 µF, No Motor Connected		11	17	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), R_{BK} = 22 Ω, C_{BK} = 22 µF, No Motor Connected		28	30	mA
V_{AVDD}	Analog regulator voltage	0 mA ≤ I_{AVDD} ≤ 30 mA	3.125	3.3	3.465	V
I_{AVDD}	External analog regulator load				20	mA
V_{DVDD}	Digital regulator voltage		1.4	1.55	1.65	V
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM	4.0	4.7	5.5	V
f_{CP}	Charge pump switching frequency			400		kHz

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at T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK REGULATOR						
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF)	V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 170 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 170 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 170 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA $\leq I_{BK} \leq$ 170 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA $\leq I_{BK} \leq$ 170 mA		V_{VM} – I_{BK}*(R_{LBK} +2) (1)		V
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF)	V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 20 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 20 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 20 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA $\leq I_{BK} \leq$ 20 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA $\leq I_{BK} \leq$ 20 mA		V_{VM} – I_{BK}*(R_{LBK} +2)(1)		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF)	V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 10 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 10 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 10 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA $\leq I_{BK} \leq$ 10 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA $\leq I_{BK} \leq$ 10 mA		V_{VM} – I_{BK}*(R_{BK} +2)		V
V_{BK_RIP}	Buck regulator ripple voltage	V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 170 mA, Buck regulator with inductor, L_{BK} = 47 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 20 mA, Buck regulator with inductor, L_{BK} = 22 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA $\leq I_{BK} \leq$ 10 mA, Buck regulator with resistor; R_{BK} = 22 Ω, C_{BK} = 22 µF	–100		100	mV

at T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BK}	External buck regulator load	L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			170	mA
		L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			170 – I_{AVDD}	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			20	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			20 – I_{AVDD}	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			10	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			10 – I_{AVDD}	mA
f_{SW_BK}	Buck regulator switching frequency	Regulation Mode	20		535	kHz
		Linear Mode	20		535	kHz
V_{BK_UV}	Buck regulator undervoltage lockout	V_{BK} rising, BUCK_SEL = 00b	2.7	2.8	2.95	V
		V_{BK} falling, BUCK_SEL = 00b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 01b	4.3	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 01b	4.1	4.2	4.35	V
		V_{BK} rising, BUCK_SEL = 10b	2.7	2.8	2.95	V
		V_{BK} falling, BUCK_SEL = 10b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 11b	4.3	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 11b	4.1	4.2	4.35	V
$V_{BK\_UV\_HYS}$	Buck regulator undervoltage lockout hysteresis	Rising to falling threshold	90	200	400	mV
I_{BK_CL}	Buck regulator Current limit threshold	BUCK_CL = 0b	360	600	910	mA
		BUCK_CL = 1b	80	150	250	mA
I_{BK_OCP}	Buck regulator Overcurrent protection trip point		2	3	4	A
t_{BK_RETRY}	Overcurrent protection retry time		0.7	1	1.3	ms
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		95	125	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		105	130	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		140	185	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		145	190	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, SLEW_RATE = 00b	13	25	45	V/us
		V_{VM} = 24 V, SLEW_RATE = 01b	30	50	80	V/us
		V_{VM} = 24 V, SLEW_RATE = 10b	80	125	185	V/us
		V_{VM} = 24 V, SLEW_RATE = 11b	130	200	280	V/us
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %	V_{VM} = 24 V, SLEW_RATE = 00b	14	25	45	V/us
		V_{VM} = 24 V, SLEW_RATE = 01b	30	50	80	V/us
		V_{VM} = 24 V, SLEW_RATE = 10b	80	125	185	V/us
		V_{VM} = 24 V, SLEW_RATE = 11b	110	200	280	V/us
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24 V, SR = 25 V/µs		1800	3400	ns
		V_{VM} = 24 V, SR = 50 V/µs		1100	1550	ns
		V_{VM} = 24 V, SR = 125 V/µs		650	1000	ns
		V_{VM} = 24 V, SR = 200 V/µs		500	750	ns

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at T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPEED INPUT - PWM MODE						
f_{PWM}	PWM input frequency		0.01		95	kHz
Res_{PWM}	PWM input resolution	f_{PWM} = 0.01 to 0.35 kHz	11	12	13	bits
		f_{PWM} = 0.35 to 2 kHz	12	13	14	bits
		f_{PWM} = 2 to 3.5 kHz	11	11.5	12	bits
		f_{PWM} = 3.5 to 7 kHz	13	13.5	14	bits
		f_{PWM} = 7 to 14 kHz	12	12.5	13	bits
		f_{PWM} = 14 to 29.2 kHz	11	11.5	12	bits
		f_{PWM} = 29.3 to 60 kHz	10	10.5	11	bits
		f_{PWM} = 60 to 95 kHz	8	9	10	bits
SPEED INPUT - ANALOG MODE						
V_{ANA_FS}	Analog full-speed voltage		2.95	3	3.05	V
V_{ANA_RES}	Analog voltage resolution			732		μV
SPEED INPUT - FREQUENCY MODE						
f_{PWM_FREQ}	PWM input frequency range	Duty cycle = 50%	3		32767	Hz
SLEEP MODE						
V_{EN_SL}	Analog voltage to enter sleep mode	SPD_CTRL_MODE = 00b (analog mode)			40	mV
V_{EX_SL}	Analog voltage to exit sleep mode	SPD_CTRL_MODE = 00b (analog mode)	2.2			V
t_{DET_ANA}	Time needed to detect wake up signal on SPEED pin	SPD_CTRL_MODE = 00b (analog mode) V_{SPEED} > V_{EX_SL}	0.5	1	1.5	μs
t_{WAKE}	Wakeup time from sleep mode	V_{SPEED} > V_{EX_SL} to DVDD voltage available, SPD_CTRL_MODE = 01b (PWM mode)		3	5	ms
$t_{EX\_SL\_DR\_ANA}$	Time taken to drive motor after exiting from sleep mode	SPD_CTRL_MODE = 00b (analog mode) V_{SPEED} > V_{EN_SL}, ISD detection disabled			20	ms
t_{DET_PWM}	Time needed to detect wake up signal on SPEED pin	SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} > V_{DIG_IH}	0.5	1	1.5	μs
t_{WAKE_PWM}	Wakeup time from sleep mode	V_{SPEED} > V_{DIG_IH} to DVDD voltage available and release nFault, SPD_CTRL_MODE = 01b (PWM mode)		3	5	ms
$t_{EX\_SL\_DR\_PWM}$	Time taken to drive motor after wakeup from sleep state	SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} > V_{DIG_IH}, ISD detection disabled			20	ms
$t_{DET\_SL\_ANA}$	Time needed to detect sleep command	SPD_CTRL_MODE = 00b (analog mode) V_{SPEED} < V_{EN_SL}	0.5	1	2	ms
$t_{DET\_SL\_PWM}$	Time needed to detect sleep command	SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} < V_{DIG_IL}, SLEEP_TIME = 00b	0.035	0.05	0.065	ms
		SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} < V_{DIG_IL}, SLEEP_TIME = 01b	0.14	0.2	0.26	ms
		SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} < V_{DIG_IL}, SLEEP_TIME = 10b	14	20	26	ms
		SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} < V_{DIG_IL}, SLEEP_TIME = 11b	140	200	260	ms
$t_{DET\_SL\_FREQ}$	Time needed to detect sleep command	SPD_CTRL_MODE = 11b (Frequency mode) V_{SPEED} < V_{DIG_IL}		4000		ms
t_{EN_SL}	Time needed to stop driving motor after detecting sleep command	V_{SPEED} < V_{EN_SL} (analog mode) or V_{SPEED} < V_{DIG_IL} (PWM mode)		1	2	ms

at T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STANDBY MODE						
V_{EN_SB}	Analog voltage to enter standby mode	SPD_CTRL_MODE = 00b (analog mode)			40	mV
V_{EX_SB}	Analog voltage to exit standby mode	SPD_CTRL_MODE = 00b (analog mode)	170			mV
$t_{EX\_SB\_DR\_ANA}$	Time taken to drive motor after exiting standby mode	SPD_CTRL_MODE = 00b (analog mode) V_{SPEED} > V_{EN_SB}, ISD detection disabled			6	ms
$t_{EX\_SB\_DR\_PWM}$	Time taken to drive motor after exiting standby mode	SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} > V_{DIG_IH}, ISD detection disabled			6	ms
$t_{DET\_SB\_ANA}$	Time needed to detect standby mode	SPD_CTRL_MODE = 00b (analog mode) V_{SPEED} < V_{EN_SB}	0.5	1	2	ms
$t_{EN\_SB\_PWM}$	Time needed to detect standby command	SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} < V_{DIG_IL}, SLEEP_TIME = 00b	0.035	0.05	0.065	ms
		SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} < V_{DIG_IL}, SLEEP_TIME = 01b	0.14	0.2	0.26	ms
		SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} < V_{DIG_IL}, SLEEP_TIME = 10b	14	20	26	ms
		SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} < V_{DIG_IL}, SLEEP_TIME = 11b	140	200	260	ms
$t_{EN\_SB\_FREQ}$	Time needed to detect standby mode	SPD_CTRL_MODE = 11b (Frequency mode), V_{SPEED} < V_{DIG_IL}		4000		ms
$t_{EN\_SB\_DIG}$	Time needed to detect standby mode	SPD_CTRL_MODE = 10b (I2C mode), SPEED_CMD = 0		1	2	ms
t_{EN_SB}	Time needed to stop driving motor after detecting standby command	V_{SPEED} < V_{EN_SL} (analog mode) or V_{SPEED} < V_{DIG_IL} (PWM mode) or SPEED_CMD = 0 (I2C mode)		1	2	ms
LOGIC-LEVEL INPUTS (BRAKE, DIR, EXT_CLK, EXT_WD, SCL, SDA, SPEED)						
V_{IL}	Input logic low voltage	AVDD = 3 to 3.6 V			0.25*AVDD	V
V_{IH}	Input logic high voltage	AVDD = 3 to 3.6 V	0.65*AVDD			V
V_{HYS}	Input hysteresis		50	500	800	mV
I_{IL}	Input logic low current	AVDD = 3 to 3.6 V	-0.15		0.15	μA
I_{IH}	Input logic high current	AVDD = 3 to 3.6 V	-0.3		0	μA
R_{PD_SPEED}	Input pulldown resistance	SPEED pin To GND	0.6	1	1.4	MΩ
R_{PD}	Input pulldown resistance	To GND	90	100	110	kΩ
OPEN-DRAIN OUTPUTS (nFAULT, FG)						
V_{OL}	Output logic low voltage	I_{OD} =-5 mA			0.4	V
I_{OZ}	Output logic high current	V_{OD} = 3.3 V	0		0.5	μA
I^2C Serial Interface						
V_{I2C_L}	LOW-level input voltage		-0.5		0.3*AVDD	V
V_{I2C_H}	HIGH-level input voltage		0.7*AVDD		5.5	V
V_{I2C_HYS}	Hysterisis		0.05*AVDD			V
V_{I2C_OL}	LOW-level output voltage	open-drain at 2mA sink current	0		0.4	V
I_{I2C_OL}	LOW-level output current	V_{I2C_OL} = 0.6V			6	mA
I_{I2C_IL}	Input current on SDA and SCL		-10[2]		10[2]	μA
C_i	Capacitance for SDA and SCL				10	pF

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at T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{of}	Output fall time from V_{I2C_H}(min) to V_{I2C_L}(max)	Standard Mode			250(3)	ns
		Fast Mode			250(3)	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Fast Mode	0		50(4)	ns
OSCILLATOR						
f_{OSCREF}	External clock reference	EXT_CLK_CONFIG = 000b		8		kHz
		EXT_CLK_CONFIG = 001b		16		kHz
		EXT_CLK_CONFIG = 010b		32		kHz
		EXT_CLK_CONFIG = 011b		64		kHz
		EXT_CLK_CONFIG = 100b		128		kHz
		EXT_CLK_CONFIG = 101b		256		kHz
		EXT_CLK_CONFIG = 110b		512		kHz
		EXT_CLK_CONFIG = 111b		1024		kHz
EEPROM						
EE_{Prog}	Programing voltage		1.35	1.5	1.65	V
EE_{RET}	Retention	T_A = 25 ℃		100		Years
		T_J = -40 to 150 ℃	10			Years
EE_{END}	Endurance	T_J = -40 to 150 ℃	1000			Cycles
		T_J = -40 to 85 ℃	20000			Cycles
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	VM rising	4.3	4.4	4.5	V
		VM falling	4.1	4.2	4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold	140	200	350	mV
t_{UVLO}	Supply undervoltage deglitch time		3	5	7	µs
V_{OVP}	Supply overvoltage protection (OVP)	Supply rising, OVP_EN = 1, OVP_SEL = 0	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	31.8	33	34.3	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	19	21	22	V
V_{OVP_HYS}	Supply overvoltage protection (OVP)	Rising to falling threshold, OVP_SEL = 1	0.9	1	1.1	V
		Rising to falling threshold, OVP_SEL = 0	0.7	0.8	0.9	V
t_{OVP}	Supply overvoltage deglitch time		2.5	5	7	µs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising	2.25	2.5	2.75	V
		Supply falling	2.2	2.4	2.6	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	65	100	150	mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.5	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold	180	200	240	mV
I_{OCP}	Overcurrent protection trip point	OCP_LVL = 0b	10	16	20	A
		OCP_LVL = 1b	15	24	28	A

at T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OCP}	Overcurrent protection deglitch time	OCP_DEG = 00b	0.1	0.3	0.7	µs
		OCP_DEG = 01b	0.2	0.6	1.2	µs
		OCP_DEG = 10b	0.6	1.25	1.8	µs
		OCP_DEG = 11b	1	1.6	2.5	µs
t_{RETRY}	Overcurrent protection retry time	OCP_RETRY = 0	4	5	6	ms
		OCP_RETRY = 1	425	500	575	ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	160	170	180	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	25	30	35	°C
T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	175	185	195	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_J)	25	30	35	°C
T_{TSD}	Thermal shutdown temperature (FET)	Die temperature (T_J)	170	180	190	°C
T_{TSD_HYS}	Thermal shutdown hysteresis (FET)	Die temperature (T_J)	20	25	30	°C

(1) R_{LBK} is resistance of inductor L_{BK}
(2) If AVDD is switched off, I/O pins must not obstruct the SDA and SCL lines.
(3) The maximum tf for the SDA and SCL bus lines (300 ns) is longer than the specified maximum tof for the output stages (250 ns). This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
(4) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns

7.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Standard-mode						
f_{SCL}	SCL clock frequency		0		100	kHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4			µs
t_{LOW}	LOW period of the SCL clock		4.7			µs
t_{HIGH}	HIGH period of the SCL clock		4			µs
t_{SU_STA}	Set-up time for a repeated START condition		4.7			µs
t_{HD_DAT}	Data hold time (2)	I2C bus devices	0 (3)		(4)	µs
t_{SU_DAT}	Data set-up time		250			ns
t_r	Rise time for both SDA and SCL signals				1000	ns
t_f	Fall time of both SDA and SCL signals (3) (6) (7) (8)				300	ns
t_{SU_STO}	Set-up time for STOP condition		4			µs
t_{BUF}	Bus free time between STOP and START condition		4.7			µs
C_b	Capacitive load for each bus line (9)				400	pF
t_{VD_DAT}	Data valid time (10)				3.45 (4)	µs
t_{VD_ACK}	Data valid acknowledge time (11)				3.45 (4)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V
Fast-mode						
f_{SCL}	SCL clock frequency		0		400	KHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	0.6			µs

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{LOW}	LOW period of the SCL clock		1.3			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU_STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD_DAT}	Data hold time (2)		0 (3)		(4)	µs
t_{SU_DAT}	Data set-up time		100 (5)			ns
t_r	Rise time for both SDA and SCL signals		20		300	ns
t_f	Fall time of both SDA and SCL signals (3) (6) (7) (8)		20 x (AVDD/ 5.5V)		300	ns
t_{SU_STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between STOP and START condition		1.3			µs
C_b	Capacitive load for each bus line (9)				400	pF
t_{VD_DAT}	Data valid time (10)				0.9 (4)	µs
t_{VD_ACK}	Data valid acknowledge time (11)				0.9 (4)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V

(1) All values referred to $V_{IH(min)}$ ($0.3V_{DD}$) and $V_{IL(max)}$ levels (see Table 9).
(2) t_{HD_DAT} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
(3) A device must internally provice a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum t_{HD_DAT} could be 3.45 us and .9 us for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_DAT} or t_{VD_ACK} by a transistion time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
(5) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement t_{SU_DAT} 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period if the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + t_{SU_DAT} = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
(6) If mixed with Hs-mode devices, faster fall times according to Table 10 are allowed.
(7) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(8) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
(9) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
(10) t_{VD_DAT} = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
(11) t_{VD_ACK} = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, dependging on which one is worse).

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7.7 Typical Characteristics

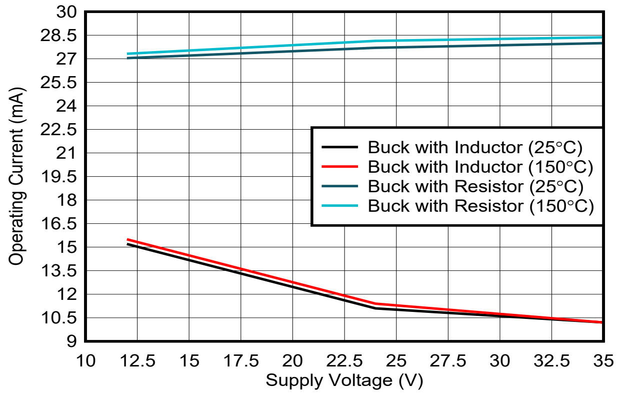

图 7-1. Supply current over supply voltage

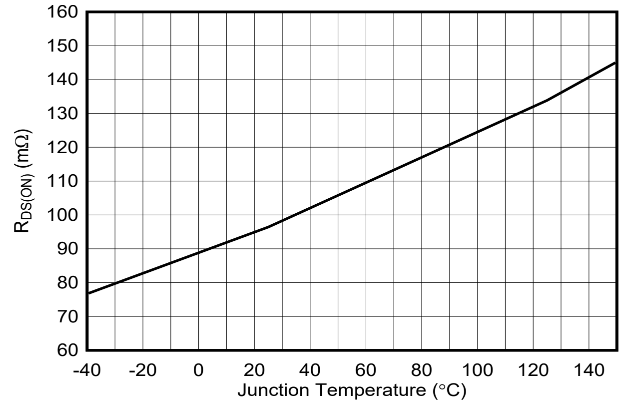

图 7-2. $R_{DS(ON)}$ (high and low side combined) for MOSFETs over temperature

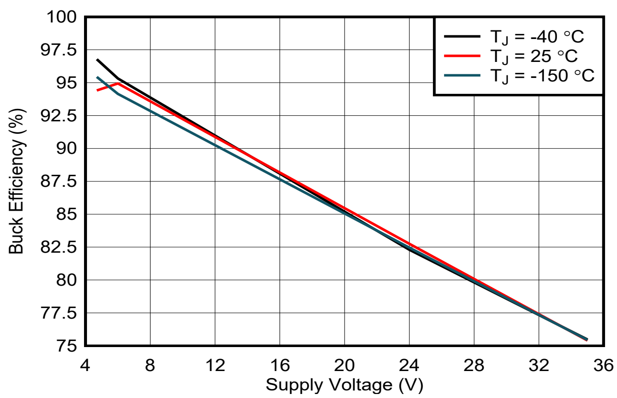

图 7-3. Buck regulator efficiency over supply voltage

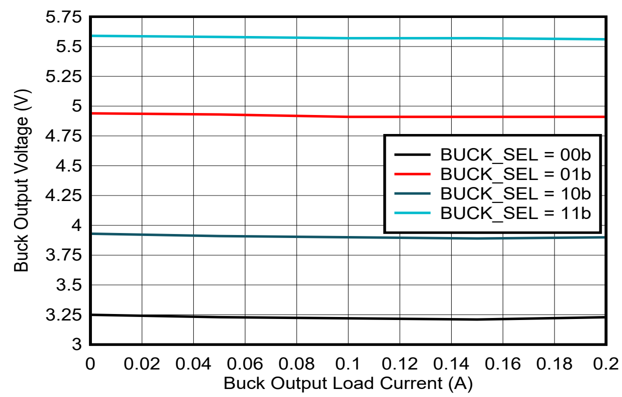

图 7-4. Buck regulator output voltage over load current

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8 Detailed Description

8.1 Overview

The MCT8316A provides a single-chip, code-free sensorless trapezoidal solution for customers requiring high speed operation (up to 3 kHz electrical speed) or very fast startup time (< 50ms) for 12- to 24-V brushless-DC motors requiring up to 8-A peak phase currents.

The MCT8316A integrates three 1/2-H bridges with 40-V absolute maximum capability and a very low $R_{DS(ON)}$ of 95-mΩ (high-side + low-side) to enable high power drive capability. Current is sensed using an integrated current sensing circuit which eliminates the need for external sense resistors. Power management features of an adjustable buck regulator and LDO generate the necessary voltage rails for the device and can be used to power external circuits.

Sensorless trapezoidal control is highly configurable through register settings (MCT8316AV) or hardware pins (MCT8316AT) ranging from motor start-up behavior to closed loop operation. Register settings can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. MCT8316A allows for a high level of monitoring; any variable in the algorithm can be displayed and observed as an analog output via two 12-bit DACs. This feature provides an effective method to tune speed loops as well as motor acceleration. The device receives a speed command through a PWM input, analog voltage, frequency input or I^2C command.

In-built protection features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD undervoltage lockout (AVDD_UV), buck regulator UVLO, motor lock detection and overtemperature warning and shutdown (OTW and TSD). Fault events are indicated by the nFAULT pin with detailed fault information available in the registers.

The MCT8316A device is available in a 0.5-mm pin pitch, VQFN surface-mount package. The VQFN package size is 7 mm × 5 mm with a height of 1 mm.

8.2 Functional Block Diagram

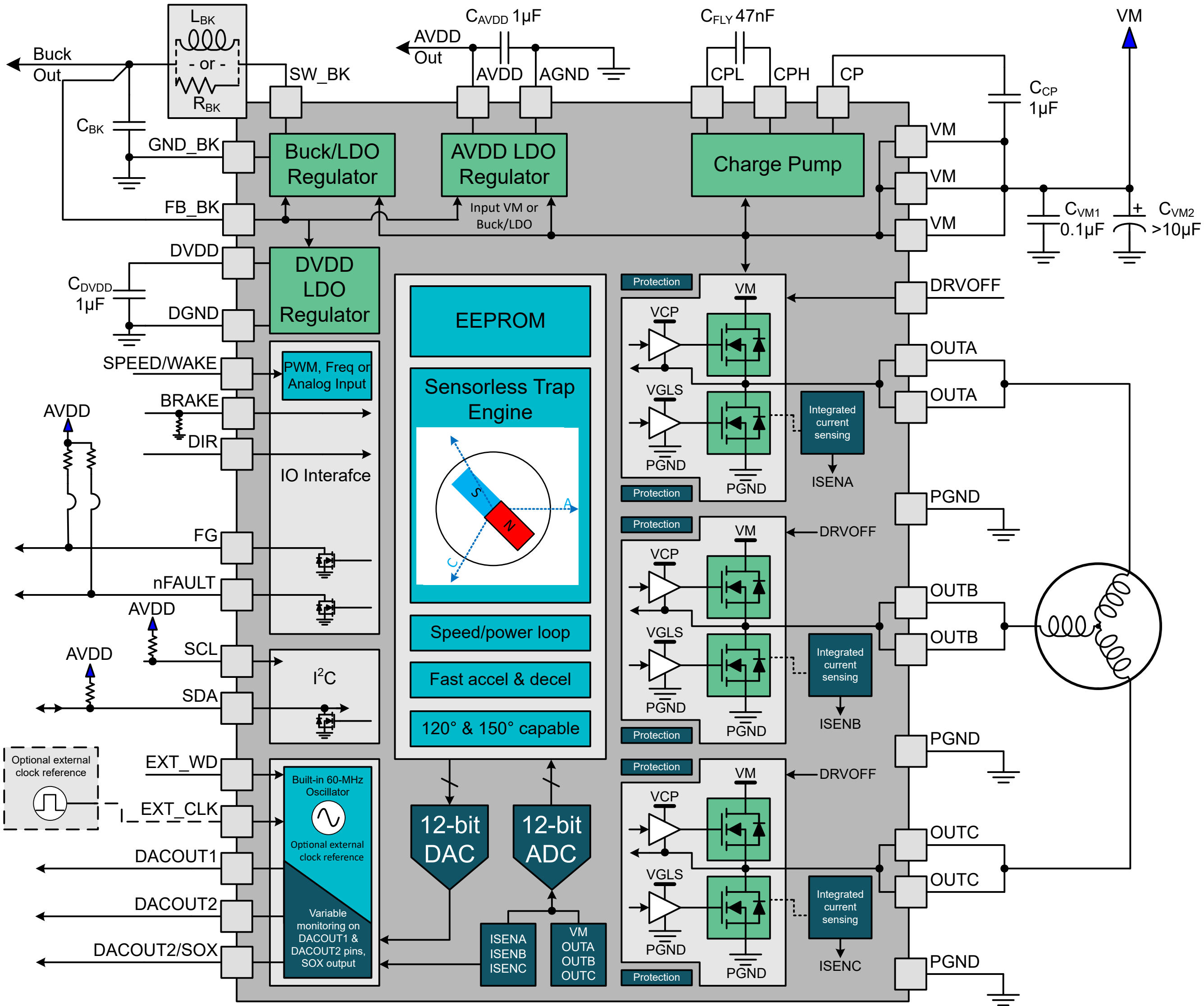

图 8-1. MCT8316AV Functional Block Diagram

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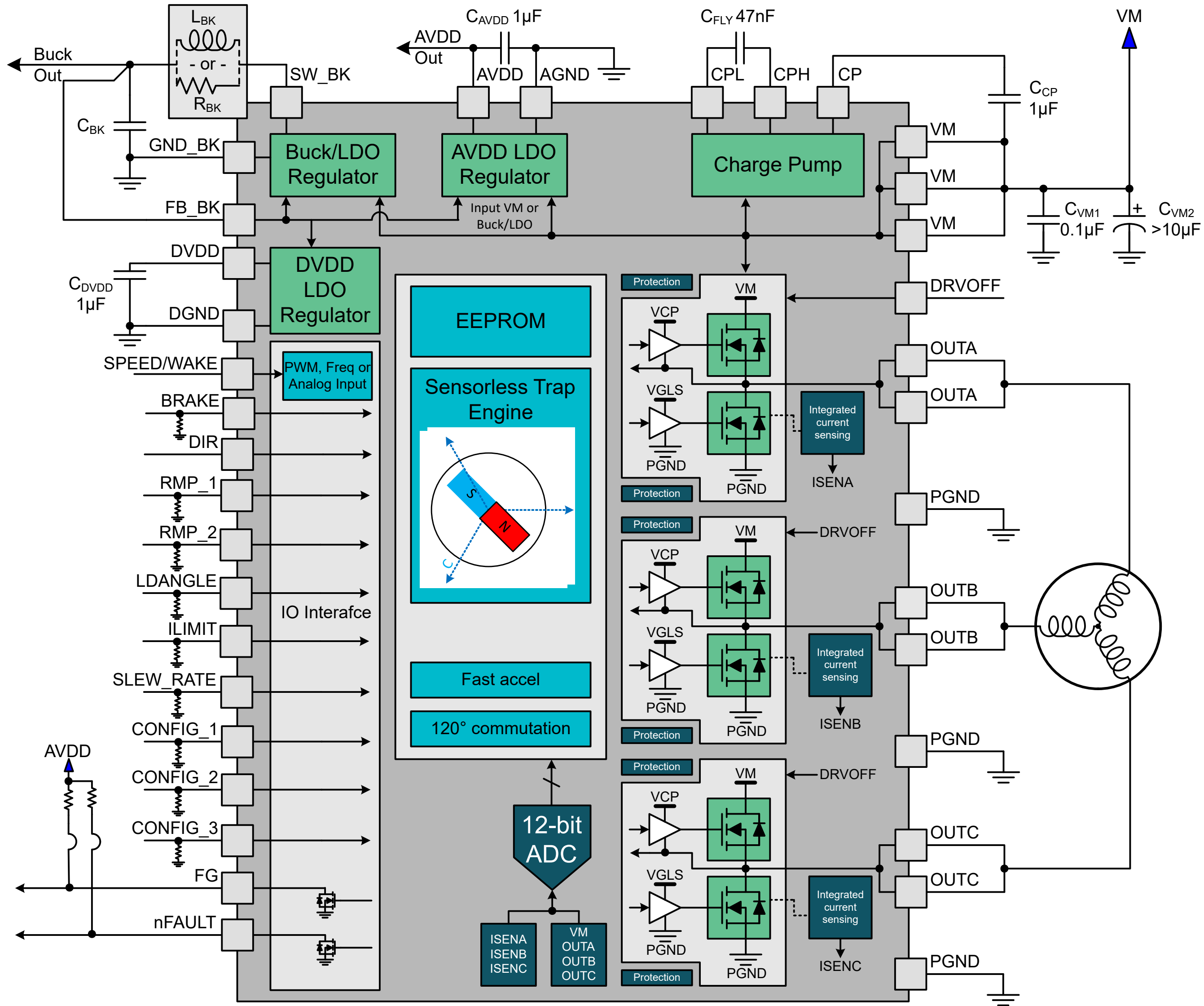

图 8-2. MCT8316AT Functional Block Diagram

8.3 Feature Description

8.3.1 Output Stage

The MCT8316A consists of an integrated 95-mΩ (combined high-side and low-side FETs' on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

8.3.2 Device Interface Modes

The MCT8316A family of devices supports two different interface versions, I^2C (MCT8316AV) and hardware (MCT8316AT) to provide end application design suited for either flexibility or simplicity. The two interface versions share the same 40-pin VQFN package with significant overlap in power and certain I/O pins (like FG, nFAULT, DIR, BRAKE, SPEED/WAKE) positions - this compatibility lets application designers evaluate with one interface version and potentially switch to another with minimal modifications to their design. The I^2C version (MCT8316AV) allows controlling the motor operation and system through BRAKE, DIR, DRVOFF, EXT_CLK, EXT_WD and SPEED/WAKE . MCT8316AV also provides different signals for monitoring algorithm variables, speed, fault and phase current feedback through DACOUT1, DACOUT2, FG, nFAULT and SOX. The hardware version (MCT8316AT) allows controlling the motor operation and system through BRAKE, DIR, SPEED/WAKE, DRVOFF and allows configuring system/algorithm parameters through CONFIG_1, CONFIG_2, CONFIG_3, LDANGLE, ILIMIT, RMP_1, RMP_2, SLEW_RATE. MCT8316AT also provides different signals for monitoring speed and fault feedback through FG and nFAULT.

8.3.2.1 Interface - Control and Monitoring

Motor Control Signals

- When BRAKE pin is driven 'High', MCT8316A enters brake state. Low-side braking (see Low-Side Braking) is implemented during this brake state. MCT8316A decreases output speed to value defined by BRAKE_DUTY_THRESHOLD before entering brake state. As long as BRAKE is driven 'High', MCT8316A stays in brake state. Brake pin input can be overwritten by configuring BRAKE_INPUT over the I^2C interface.
- The DIR pin decides the direction of motor spin; when driven 'High', the sequence is OUT A → OUT C → OUT B, and when driven 'Low' the sequence is OUT A → OUT B → OUT C. DIR pin input can be overwritten by configuring DIR_INPUT over the I^2C interface.
- When DRVOFF pin is driven 'High', MCT8316A stops driving the motor by turning OFF all MOSFETs (coast state). When DRVOFF is driven 'Low', MCT8316A returns to normal state of operation, as if it was restarting the motor (see DRVOFF Functionality). DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active. Entry and exit from sleep or standby condition is controlled by SPEED pin.
- SPEED/WAKE pin is used to control motor speed and wake up MCT8316A from sleep mode. SPEED pin can be configured to accept PWM, frequency or analog input signals. It is used to enter and exit from sleep and standby mode (see 表 8-19).

External Oscillator and Watchdog Signals (Optional)

- EXT_CLK pin may be used to provide an external clock reference (see External Clock Source (Available for MCT8316AV)).
- EXT_WD pin may be used to provide an external watchdog signal (see External Watchdog (Available only in MCT836AV)).

Output Signals

- DACOUT1 outputs internal variable defined by address in register DACOUT1_VAR_ADDR, the output of DACOUT1 is refreshed every PWM cycle (see DAC outputs).
- DACOUT2 outputs internal variable defined by address in register DACOUT2_VAR_ADDR, the output of DACOUT2 is refreshed every PWM cycle (see DAC outputs).
- FG pin provides pulses which are proportional to motor speed (see FG Configuration).
- nFAULT pin provides fault status in device or motor operation.
- SOX pin provides the output of one of the current sense amplifiers.

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8.3.2.2 I²C Interface

The MCT8316AV supports an I²C serial communication interface that allows an external controller to send and receive data. This I²C interface lets the external controller configure the EEPROM and read detailed fault and motor state information. The I²C bus is a two-wire interface using the SCL and SDA pins which are described as follows:

- The SCL pin is the clock signal input.
- The SDA pin is the data input and output.

8.3.2.3 Hardware Interface - Pin Configuration

MCT8316AT allows configuration of motor control algorithm and driver parameters through the pull-down resistors connected to the device configuration pins, RMP_1, RMP_2, LDANGLE, CONFIG_1, ILIMIT, SLEW_RATE, CONFIG_2 and CONFIG_3. This allows quick and easy configuration of the MCT8316 motor control and gate driver parameters without the need for EEPROM programming through I²C interface. The parameters that can be configured by each device configuration pin are detailed in 表 8-1 .

表 8-1. Pin configurable parameters

Pin	Configurable Parameters
RMP_1, RMP_2	Start-up method, open loop acceleration rate, closed loop acceleration rate, first cycle frequency, align time, dynamic degauss enable, fast start-up enable, stationary brake time, auto handoff enable, handoff threshold, open loop duty, align ramp rate
LDANGLE	Lead angle or BEMF threshold
CONFIG_1	PWM switching frequency, ZC detection blanking time, IPD clock frequency
ILIMIT, SLEW_RATE	CBC limit, open loop, align and IPD current limit, buck output voltage selection, phase output voltage slew rate
CONFIG_2	OCP level, OCP mode, AAR enable, delay compensation enable
CONFIG_3	Abnormal speed, minimum duty

RMP_1 and RMP_2 pins are used to set the start-up method (Double Align or IPD), open loop acceleration rate A1 (OL_ACC_A1 in Hz/s), closed loop acceleration rate (CL_ACC in V/s), startup brake time (STARTUP_BRK_TIME in ms), first cycle frequency (SLOW_FIRST_CYCLE_FREQ in Hz) and align time (ALIGN_TIME in ms, if Double Align is selected).

RMP_1 is used to set the start-up method and the inertia profile of the motor-load system. Inertia profiles range from ultra-high inertia (like ceiling fans) to ultra-high acceleration (like fuel pumps) with some example applications for each type of inertia profile given in 表 8-2. Once the inertia profile is chosen using RMP_1 pin, RMP_2 pin is used to set parameters like CL_ACC, OL_ACC_A1, STARTUP_BRK_TIME, SLOW_FIRST_CYC_FREQ, ALIGN_TIME (if applicable).

Based on the inertia profile and CL_ACC chosen, other parameters including IPD repeat times (IPD_REPEAT), dynamic degauss enable (DYN_DEGAUSS_EN), auto handoff enable (AUTO_HANDOFF), handoff threshold (OPN_CL_HANDOFF_THR), OL duty (OL_DUTY), align ramp rate (ALIGN_RAMP_RATE) and fast start-up enable (INTEG_ZC_METHOD) are auto-selected as per Tables through 12-11. Note that Open loop acceleration rate A2 (OL_ACC_A2 in Hz/s²) is set to the same value as that of OL_ACC_A1.

表 8-2. Resistor values for configuring parameters on RMP_1 pin

Level	Resistor value, RMP_1	MTR_STARTUP	RMP_2 configuration classification based on motor-load inertia or acceleration rate	ALIGN_RAMP_RATE (V/s)	CL_ACC (V/s)	OL_DUTY (%)
0	Tied to GND	Double Align	Ultra-high inertia	10	1, 2	15
1	4.7kΩ, ±5%		Very high inertia		5, 10	
2	10kΩ, ±5%		High inertia	100	15, 20	20
3	15kΩ, ±5%		Low acceleration		25, 50	
4	22kΩ, ±5%		Medium acceleration	500	75, 100	25
5	30kΩ, ±5%		High acceleration		150, 200	
6	39kΩ, ±5%		Very high acceleration	1000	250, 500	40
7	51kΩ, ±5%		Ultra-high acceleration		1000, 32767	
8	62kΩ, ±5%	IPD	Ultra-high inertia	10	1, 2	15
9	75kΩ, ±5%		Very high inertia		5, 10	
10	91kΩ, ±5%		High inertia	100	15, 20	20
11	110kΩ, ±5%		Low acceleration		25, 50	
12	150kΩ, ±5%		Medium acceleration	500	75, 100	25
13	200kΩ, ±5%		High acceleration		150, 200	
14	240kΩ, ±5%		Very high acceleration	1000	250, 500	40
15	300kΩ, ±5%		Ultra-high acceleration		1000, 32767	

表 8-3. Parameter values on RMP_2 pin for ultra-high inertia applications

Level	Resistor value, RMP_2	ALIGN_TIME (ms)	DYN_DEGAUSS_EN	SLOW_FIRST_CYC_FREQ (Hz)	STARTUP_BRK_TIME (ms)	CL_ACC (V/s)	OL_ACC_A1 (Hz/s)
0	Tied to GND	10000	N	0.01	5000	1	0.005
1	4.7kΩ, ±5%	6000	N				
2	10kΩ, ±5%	10000	N	0.025			
3	15kΩ, ±5%	6000	N				
4	22kΩ, ±5%	4000	N	0.05	2000		
5	30kΩ, ±5%	2000	N				
6	39kΩ, ±5%	4000	N	0.075			
7	51kΩ, ±5%	2000	N				
8	62kΩ, ±5%	6000	N	0.025	1000	2	0.025
9	75kΩ, ±5%	4000	N				
10	91kΩ, ±5%	6000	N	0.05			
11	110kΩ, ±5%	4000	N				
12	150kΩ, ±5%	2000	N	0.075	500		
13	200kΩ, ±5%	1000	N				
14	240kΩ, ±5%	2000	N	0.1			
15	300kΩ, ±5%	1000	N				

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For all resistor values in 表 8-3, AUTO_HANDOFF is enabled (1b), OPN_CL_HANDOFF_THR is 600Hz, INTEG_ZC_METHOD is disabled (0b), IPD_REPEAT is 3.

表 8-4. Parameter values on RMP_2 pin for very high inertia applications

Level	Resistor value, RMP_2	ALIGN_TIME (ms)	DYN_DEGAUSS_EN	SLOW_FIRST_CYC_FREQ (Hz)	STARTUP_BRK_TIME (ms)	CL_ACC (V/s)	OL_ACC_A1 (Hz/s)
0	Tie to GND	6000	N	0.05	1000	5	0.05
1	4.7kΩ, ±5%	4000	N				
2	10kΩ, ±5%	6000	N	0.075			
3	15kΩ, ±5%	4000	N				
4	22kΩ, ±5%	2000	N	0.1	500		
5	30kΩ, ±5%	1000	N				
6	39kΩ, ±5%	2000	N	0.25			
7	51kΩ, ±5%	1000	N				
8	62kΩ, ±5%	4000	N	0.25	500	10	0.5
9	75kΩ, ±5%	2000	N				
10	91kΩ, ±5%	4000	N	0.5			
11	110kΩ, ±5%	2000	N				
12	150kΩ, ±5%	1000	N	0.5	250		
13	200kΩ, ±5%	750	N				
14	240kΩ, ±5%	1000	N	0.75			
15	300kΩ, ±5%	750	N				

For all resistor values in 表 8-4, AUTO_HANDOFF is enabled (1b), OPN_CL_HANDOFF_THR is 600Hz, INTEG_ZC_METHOD is disabled (0b), IPD_REPEAT is 3.

表 8-5. Parameter values on RMP_2 pin for high inertia applications

Level	Resistor value, RMP_2	ALIGN_TIME (ms)	DYN_DEGAUSS_EN	SLOW_FIRST_CYC_FREQ (Hz)	STARTUP_BRK_TIME (ms)	CL_ACC (V/s)	OL_ACC_A1 (Hz/s)
0	Tie to GND	4000	N	0.25	500	15	1
1	4.7kΩ, ±5%	2000	N				
2	10kΩ, ±5%	4000	N	0.5			
3	15kΩ, ±5%	2000	N				
4	22kΩ, ±5%	1000	N	0.5	250		
5	30kΩ, ±5%	750	N				
6	39kΩ, ±5%	1000	N	0.75			
7	51kΩ, ±5%	750	N				
8	62kΩ, ±5%	2000	N	0.5	250	20	2.5
9	75kΩ, ±5%	1000	N				
10	91kΩ, ±5%	2000	N	0.75			
11	110kΩ, ±5%	1000	N				
12	150kΩ, ±5%	750	N	1	100		
13	200kΩ, ±5%	500	N				
14	240kΩ, ±5%	750	N	2			
15	300kΩ, ±5%	500	N				

For all resistor values in 表 8-5, AUTO_HANDOFF is enabled (1b), OPN_CL_HANDOFF_THR is 600Hz, INTEG_ZC_METHOD is disabled (0b), IPD_REPEAT is 3.

表 8-6. Parameter values on RMP_2 pin for low acceleration applications

Level	Resistor value, RMP_2	ALIGN_TIME (ms)	DYN_DEGAUSS_EN	SLOW_FIRST_CYC_FREQ (Hz)	STARTUP_BRK_TIME (ms)	CL_ACC (V/s)	OL_ACC_A1 (Hz/s)
0	Tie to GND	2000	N	0.5	250	25	5
1	4.7kΩ, ±5%	1000	Y				
2	10kΩ, ±5%	2000	N	0.75			
3	15kΩ, ±5%	1000	Y				
4	22kΩ, ±5%	750	N	1	100		
5	30kΩ, ±5%	500	Y				
6	39kΩ, ±5%	750	N	2			
7	51kΩ, ±5%	500	Y				
8	62kΩ, ±5%	1000	N	0.5	100	50	10
9	75kΩ, ±5%	750	Y				
10	91kΩ, ±5%	1000	N	0.75			
11	110kΩ, ±5%	750	Y				
12	150kΩ, ±5%	500	N	1	75		
13	200kΩ, ±5%	300	Y				
14	240kΩ, ±5%	500	N	2			
15	300kΩ, ±5%	300	Y				

For all resistor values in 表 8-6, AUTO_HANDOFF is enabled (1b), OPN_CL_HANDOFF_THR is 600Hz, INTEG_ZC_METHOD is disabled (0b), IPD_REPEAT is 3.

表 8-7. Parameter values on RMP_2 pin for medium acceleration applications

Level	Resistor value, RMP_2	ALIGN_TIME (ms)	DYN_DEGAUSS_EN	SLOW_FIRST_CYC_FREQ (Hz)	STARTUP_BRK_TIME (ms)	CL_ACC (V/s)	OL_ACC_A1 (Hz/s)
0	Tie to GND	750	N	0.5	100	75	25
1	4.7kΩ, ±5%	500	Y				
2	10kΩ, ±5%	750	N	0.75			
3	15kΩ, ±5%	500	Y				
4	22kΩ, ±5%	300	N	1	75		
5	30kΩ, ±5%	200	Y				
6	39kΩ, ±5%	300	N	2			
7	51kΩ, ±5%	200	Y				
8	62kΩ, ±5%	500	N	0.5	75	100	50
9	75kΩ, ±5%	300	Y				
10	91kΩ, ±5%	500	N	0.75			
11	110kΩ, ±5%	300	Y				
12	150kΩ, ±5%	200	N	1	50		
13	200kΩ, ±5%	100	Y				
14	240kΩ, ±5%	200	N	2			
15	300kΩ, ±5%	100	Y				

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For all resistor values in 表 8-7, AUTO_HANDOFF is enabled (1b), OPN_CL_HANDOFF_THR is 600Hz, INTEG_ZC_METHOD is disabled (0b), IPD_REPEAT is 3.

表 8-8. Parameter values on RMP_2 pin for high acceleration applications

Level	Resistor value, RMP_2	ALIGN_TIME (ms)	DYN_DEGAUSS_EN	SLOW_FIRST_CYC_FREQ (Hz)	STARTUP_BRK_TIME (ms)	CL_ACC (V/s)	OL_ACC_A1 (Hz/s)
0	Tie to GND	500	N	0.5	75	150	100
1	4.7kΩ, ±5%	300	Y				
2	10kΩ, ±5%	500	N	0.75			
3	15kΩ, ±5%	300	Y				
4	22kΩ, ±5%	200	N	1	50		
5	30kΩ, ±5%	100	Y				
6	39kΩ, ±5%	200	N	2			
7	51kΩ, ±5%	100	Y				
8	62kΩ, ±5%	300	N	1	50	200	150
9	75kΩ, ±5%	200	Y				
10	91kΩ, ±5%	300	N	2			
11	110kΩ, ±5%	200	Y				
12	150kΩ, ±5%	100	N	2	25		
13	200kΩ, ±5%	75	Y				
14	240kΩ, ±5%	100	N	3			
15	300kΩ, ±5%	75	Y				

For all resistor values in 表 8-8, AUTO_HANDOFF is enabled (1b), OPN_CL_HANDOFF_THR is 600Hz, INTEG_ZC_METHOD is disabled (0b), IPD_REPEAT is 3.

表 8-9. Parameter values on RMP_2 pin for very high acceleration applications

Level	Resistor value, RMP_2	ALIGN_TIME (ms)	DYN_DEGAUSS_EN	SLOW_FIRST_CYC_FREQ (Hz)	STARTUP_BRK_TIME (ms)	CL_ACC (V/s)	OL_ACC_A1 (Hz/s)
0	Tie to GND	200	N	1	50	250	200
1	4.7kΩ, ±5%	100	Y				
2	10kΩ, ±5%	200	N	2			
3	15kΩ, ±5%	100	Y				
4	22kΩ, ±5%	75	N	3	25		
5	30kΩ, ±5%	50	Y				
6	39kΩ, ±5%	75	N	5			
7	51kΩ, ±5%	50	Y				
8	62kΩ, ±5%	100	Y	5	25	500	500
9	75kΩ, ±5%	75	Y				
10	91kΩ, ±5%	100	Y	10			
11	110kΩ, ±5%	75	Y				
12	150kΩ, ±5%	50	Y	10	10		
13	200kΩ, ±5%	25	Y				
14	240kΩ, ±5%	50	Y	15			
15	300kΩ, ±5%	25	Y				

For resistor values from (0-51)kΩ in 表 8-9, AUTO_HANDOFF is enabled (1b), OPN_CL_HANDOFF_THR is 600Hz, INTEG_ZC_METHOD is disabled (0b), IPD_REPEAT is 3.

For resistor values from (62-300)kΩ in 表 8-9, AUTO_HANDOFF is disabled (0b), OPN_CL_HANDOFF_THR is 20Hz, INTEG_ZC_METHOD is enabled (1b), IPD_REPEAT is 1.

表 8-10. Parameter values on RMP_2 pin for ultra-high acceleration applications

Level	Resistor value, RMP_2	ALIGN_TIME (ms)	DYN_DEGAUSS_EN	SLOW_FIRST_CYC_FREQ (Hz)	STARTUP_BRK_TIME (ms)	CL_ACC (V/s)	OL_ACC_A1 (Hz/s)
0	Tie to GND	50	Y	15	10	1000	1000
1	4.7kΩ, ±5%	25	Y				
2	10kΩ, ±5%	50	Y	25			
3	15kΩ, ±5%	25	Y				
4	22kΩ, ±5%	10	Y	25	5		
5	30kΩ, ±5%	5	Y				
6	39kΩ, ±5%	10	Y	50			
7	51kΩ, ±5%	5	Y				
8	62kΩ, ±5%	25	Y	25	5	32767	2000
9	75kΩ, ±5%	10	Y				
10	91kΩ, ±5%	25	Y	50			
11	110kΩ, ±5%	10	Y				
12	150kΩ, ±5%	5	Y	75	2		
13	200kΩ, ±5%	2	Y				
14	240kΩ, ±5%	5	Y	100			
15	300kΩ, ±5%	2	Y				

For all resistor values in 表 8-10, AUTO_HANDOFF is disabled (0b), OPN_CL_HANDOFF_THR is 20Hz, INTEG_ZC_METHOD is enabled (1b), IPD_REPEAT is 1.

For example, consider the use-case of MTR_STARTUP – Double Align, CL_ACC – 75V/s, STARTUP_BRK_TIME – 75ms, SLOW_FIRST_CYC_FREQ – 1Hz, ALIGN_TIME – 200ms. Here, RMP_1 pin needs a pull-down resistor of 22kΩ to set start-up method to double align and select medium acceleration inertia profile (corresponding to CL_ACC of 75V/s). RMP_2 pin needs a pull-down resistor of 30kΩ to select the required CL_ACC, STARTUP_BRK_TIME, SLOW_FIRST_CYC_FREQ and ALIGN_TIME. Note that the DYN_DEGAUSS_EN is set to enabled (1b) with this RMP_2 resistor value. If DYN_DEGAUSS_EN needs to be disabled (0b), RMP_2 pull-down resistor can be set to 22kΩ, but this will increase the STARTUP_BRK_TIME to 300ms instead. Depending on the parameter that can be set to adjacent values, an optimal resistor setting can be picked from the appropriate table for a given inertia profile.

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LDANGLE pin is used to set the lead angle (LD_ANGLE in degrees) as per 表 8-11, if INTEG_ZC_METHOD is set to 0b. If INTEG_ZC_METHOD is set to 1b, LDANGLE is pin is used to configure the BEMF threshold (BEMF_THRESHOLD1 and BEMF_THRESHOLD2) for integration based ZC method for fast start-up as per 表 8-11.

表 8-11. Resistor values for configuring parameters on LDANGLE pin

Level	Resistor value, LDANGLE	LD_ANGLE (deg.)	BEMF_THRESHOLD1 and BEMF_THRESHOLD2
0	Tie to GND	0	200
1	4.7kΩ, ±5%	2	300
2	10kΩ, ±5%	4	400
3	15kΩ, ±5%	6	500
4	22kΩ, ±5%	8	600
5	30kΩ, ±5%	10	700
6	39kΩ, ±5%	12	800
7	51kΩ, ±5%	14	1000
8	62kΩ, ±5%	16	1200
9	75kΩ, ±5%	18	1400
10	91kΩ, ±5%	20	1600
11	110kΩ, ±5%	22	1800
12	150kΩ, ±5%	24	2100
13	200kΩ, ±5%	26	2400
14	240kΩ, ±5%	28	2700
15	300kΩ, ±5%	30	3000

CONFIG_1 pin is used to set the PWM switching frequency (PWM_FREQ_OUT in kHz), ZC detection blanking time (TBLANK in μs) and IPD clock frequency (IPD_CLK_FREQ in Hz) as per 表 8-12.

表 8-12. Resistor values for configuring parameters on CONFIG_1 pin

<table>
<tr><th>Level</th><th>Resistor value, CONFIG_1</th><th>TBLANK (μs)</th><th>PWM_FREQ_OUT (kHz)</th><th>IPD_CLK_FREQ (Hz)</th></tr>
<tr><td>0</td><td>Tie to GND</td><td>10</td><td rowspan="2">10</td><td rowspan="4">500</td></tr>
<tr><td>1</td><td>4.7kΩ, ±5%</td><td>8</td></tr>
<tr><td>2</td><td>10kΩ, ±5%</td><td>10</td><td rowspan="2">20</td></tr>
<tr><td>3</td><td>15kΩ, ±5%</td><td>8</td></tr>
<tr><td>4</td><td>22kΩ, ±5%</td><td>8</td><td rowspan="2">25</td><td rowspan="4">1000</td></tr>
<tr><td>5</td><td>30kΩ, ±5%</td><td>6</td></tr>
<tr><td>6</td><td>39kΩ, ±5%</td><td>8</td><td rowspan="2">40</td></tr>
<tr><td>7</td><td>51kΩ, ±5%</td><td>6</td></tr>
<tr><td>8</td><td>62kΩ, ±5%</td><td>6</td><td rowspan="2">50</td><td rowspan="4">2000</td></tr>
<tr><td>9</td><td>75kΩ, ±5%</td><td>4</td></tr>
<tr><td>10</td><td>91kΩ, ±5%</td><td>6</td><td rowspan="2">60</td></tr>
<tr><td>11</td><td>110kΩ, ±5%</td><td>4</td></tr>
<tr><td>12</td><td>150kΩ, ±5%</td><td>4</td><td rowspan="2">75</td><td rowspan="4">5000</td></tr>
<tr><td>13</td><td>200kΩ, ±5%</td><td>2</td></tr>
<tr><td>14</td><td>240kΩ, ±5%</td><td>4</td><td rowspan="2">100</td></tr>
<tr><td>15</td><td>300kΩ, ±5%</td><td>2</td></tr>
</table>

ILIMIT and **SLEW_RATE** pins are used to set the cycle-by-cycle (CBC) current limit (ILIMIT in A), CSA_GAIN (in V/A), Open Loop (OL_ILIMIT in A), align (ALIGN_CURR_THR in A) and IPD current limit (IPD_CURR_THR in A) as per 表 8-13 and 表 8-14 . For a given resistor (configuration) value for ILIMIT pin, there are two different values of OL_ILIMIT(ALIGN_CURR_THR and IPD_CURR_THR) that can be chosen(Limit_0 or Limit_1). After choosing between Limit_0 and Limit_1, SLEW_RATE pin pull-down resistor value is selected based on the buck output voltage level (BUCK_SEL, either 3.3V or 5V) and phase output slew rate(SLEW_RATE in V/μs) as per 表 8-14.

表 8-13. Resistor values for configuring parameters on ILIMIT pin

Level	Resistor value, ILIMIT	ILIMIT (A)	CSA_GAIN (V/A)	Open loop, align current, IPD current selection	OL_ILIMIT, ALIGN_CURR_THR, IPD_CURR_THR (A)
0	Tie to GND	0.5	1.2	Limit_0	0.25
				Limit_1	0.42
1	4.7kΩ, ±5%	1	0.6	Limit_0	0.5
				Limit_1	1
2	10kΩ, ±5%	1.33	0.6	Limit_0	0.5
				Limit_1	0.83
3	15kΩ, ±5%	2.67	0.3	Limit_0	1
				Limit_1	2
4	22kΩ, ±5%	3.33	0.3	Limit_0	1.33
				Limit_1	2.67
5	30kΩ, ±5%	4	0.15	Limit_0	2
				Limit_1	3.33
6	39kΩ, ±5%	4.67	0.15	Limit_0	2
				Limit_1	2.67
7	51kΩ, ±5%	4.67	0.15	Limit_0	3.33
				Limit_1	4
8	62kΩ, ±5%	5.33	0.15	Limit_0	2.67
				Limit_1	4
9	75kΩ, ±5%	6	0.15	Limit_0	2
				Limit_1	2.67
10	91kΩ, ±5%	6	0.15	Limit_0	3.33
				Limit_1	4
11	110kΩ, ±5%	6	0.15	Limit_0	4.67
				Limit_1	5.33
12	150kΩ, ±5%	7.33	0.15	Limit_0	2.67
				Limit_1	3.33
13	200kΩ, ±5%	7.33	0.15	Limit_0	4
				Limit_1	4.67
14	240kΩ, ±5%	7.33	0.15	Limit_0	5.33
				Limit_1	6
15	300kΩ, ±5%	8	0.15	Limit_0	4
				Limit_1	6

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表 8-14. Resistor values for configuring parameters on SLEW_RATE pin

Level	Resistor value, SLEW_RATE	BUCK_SEL	SLEW_RATE (V/μs)	Open loop, align current, IPD current selection
0	Tie to GND	3.3V	25	Limit_0
1	4.7kΩ, ±5%			Limit_1
2	10kΩ, ±5%		50	Limit_0
3	15kΩ, ±5%			Limit_1
4	22kΩ, ±5%		125	Limit_0
5	30kΩ, ±5%			Limit_1
6	39kΩ, ±5%		200	Limit_0
7	51kΩ, ±5%			Limit_1
8	62kΩ, ±5%	5V	25	Limit_0
9	75kΩ, ±5%			Limit_1
10	91kΩ, ±5%		50	Limit_0
11	110kΩ, ±5%			Limit_1
12	150kΩ, ±5%		125	Limit_0
13	200kΩ, ±5%			Limit_1
14	240kΩ, ±5%		200	Limit_0
15	300kΩ, ±5%			Limit_1

For example, consider the use-case of ILIMIT – 4.67A, OL_ILIMIT – 3.33A, BUCK_SEL – 3.3V, SLEW_RATE – 125V/μs. From 表 8-13, ILIMIT pin needs a pull-down resistor of 51kΩ, whereas OL_ILIMIT selection is Limit_0. So, SLEW_RATE pin needs a pull-down resistor of 22kΩ, from 表 8-14.

Similarly, consider the use-case of ILIMIT – 7.33A, OL_ILIMIT – 4.67A, BUCK_SEL – 5V, SLEW_RATE – 25V/μs. Here, ILIMIT pin needs a pull-down resistor of 200kΩ, whereas OL_ILIMIT selection is Limit_1 from 表 8-13. So, SLEW_RATE pin needs a pull-down resistor of 75kΩ from 表 8-14.

CONFIG_2 pin is used to set the OCP level (OCP_LVL as either 10 or 15A) and mode (OCP_MODE as either latched or retry after 500ms), Active Asynchronous Rectification (AAR) enable (EN_AAR) and delay compensation enable (DELAY_COMP_EN) as per 表 8-15.

表 8-15. Resistor values for configuring parameters on CONFIG_2 pin

Level	Resistor value, CONFIG_2	OCP_LVL (A)	DELAY_COMP_EN	EN_AAR	OCP_MODE
0	Tie to GND	10	Disable	Disable	Latched
1	4.7kΩ, ±5%	15			
2	10kΩ, ±5%	10	Enable		
3	15kΩ, ±5%	15			
4	22kΩ, ±5%	10	Disable	Enable	
5	30kΩ, ±5%	15			
6	39kΩ, ±5%	10	Enable		
7	51kΩ, ±5%	15			

表 8-15. Resistor values for configuring parameters on CONFIG_2 pin (continued)

Level	Resistor value, CONFIG_2	OCP_LVL (A)	DELAY_COMP_EN	EN_AAR	OCP_MODE
8	62kΩ, ±5%	10	Disable	Disable	Retry after 500ms
9	75kΩ, ±5%	15			
10	91kΩ, ±5%	10	Enable		
11	110kΩ, ±5%	15			
12	150kΩ, ±5%	10	Disable	Enable	
13	200kΩ, ±5%	15			
14	240kΩ, ±5%	10	Enable		
15	300kΩ, ±5%	15			

CONFIG_3 is used to set the abnormal speed threshold (LOCK_ABN_SPEED in Hz) and minimum duty cycle (MIN_DUTY in %) as per 表 8-16.

表 8-16. Resistor values for configuring parameters on CONFIG_3 pin

Level	Resistor value, CONFIG_3	MIN_DUTY (%)	ABN_SPEED (Hz)
0	Tie to GND	2.5	1000
1	4.7kΩ, ±5%	5	
2	10kΩ, ±5%	7.5	
3	15kΩ, ±5%	10	
4	22kΩ, ±5%	2.5	2000
5	30kΩ, ±5%	5	
6	39kΩ, ±5%	7.5	
7	51kΩ, ±5%	10	
8	62kΩ, ±5%	2.5	3000
9	75kΩ, ±5%	5	
10	91kΩ, ±5%	7.5	
11	110kΩ, ±5%	10	
12	150kΩ, ±5%	2.5	4000
13	200kΩ, ±5%	5	
14	240kΩ, ±5%	7.5	
15	300kΩ, ±5%	10	

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8.3.3 Step-Down Mixed-Mode Buck Regulator

The MCT8316A has an integrated mixed-mode buck regulator in conjunction with AVDD to supply regulated 3.3 V or 5 V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4 V or 5.7 V for supporting the extra headroom for external LDO for generating a 3.3 V or 5 V supplies. The output voltage of the buck is set by BUCK_SEL.

The buck regulator has a low quiescent current of ~1-2 mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

表 8-17. Recommended settings for Buck Regulator

Buck Mode	Buck output voltage	Max output current from AVDD (I_{AVDD_MAX})	Max output current from Buck (I_{BK_MAX})	Buck current limit	AVDD power sequencing
Inductor - 47 µH	3.3 V or 4 V	20 mA	170 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Not supported (BUCK_PS_DIS = 1b)
Inductor - 47 µH	5 V or 5.7 V	20 mA	170 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Supported (BUCK_PS_DIS = 0b)
Inductor - 22 µH	5 V or 5.7 V	20 mA	20 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1b)
Inductor - 22 µH	3.3 V or 4 V	20 mA	20 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0b)
Resistor - 22 Ω	5 V or 5.7 V	20 mA	10 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1b)
Resistor - 22 Ω	3.3 V or 4 V	20 mA	10 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0b)

8.3.3.1 Buck in Inductor Mode

The buck regulator in MCT8316A is primarily designed to support low inductance of 47-µH and 22-µH. A 47-µH inductor allows the buck regulator to operate up to 170-mA load current support, whereas applications requiring current up to 20-mA can use a 22-µH inductor which saves component size.

图 8-3 shows the connection of buck regulator in inductor mode.

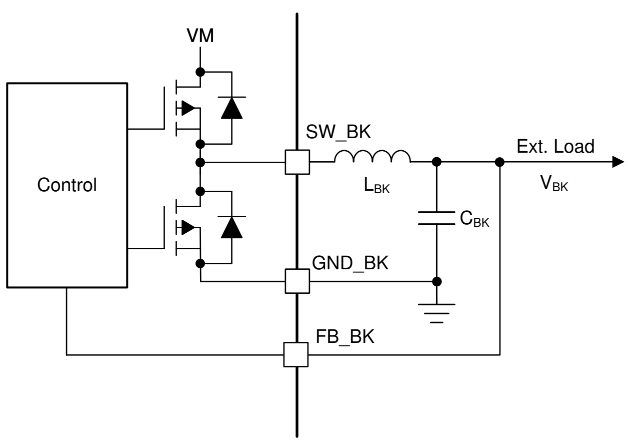

图 8-3. Buck (Inductor Mode)

8.3.3.2 Buck in Resistor mode

If the external load requirement is less than 10-mA, the inductor can be replaced with a resistor. In resistor mode the power is dissipated across the external resistor and the efficiency is lower than buck in inductor mode.

图 8-4 shows the connection of buck in resistor mode.

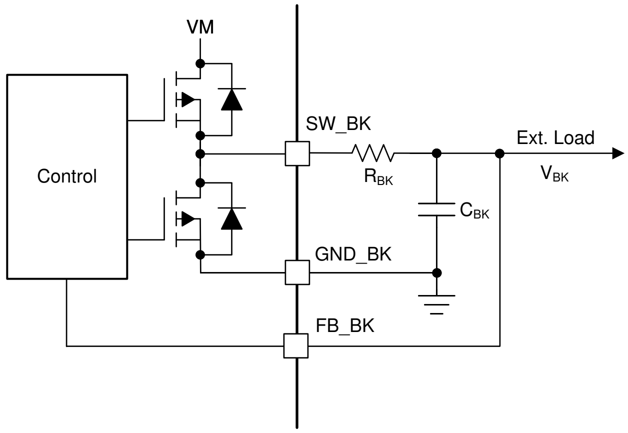

图 8-4. Buck (Resistor Mode)

8.3.3.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to supply an external LDO to generate standard 3.3-V or 5-V output rail with higher accuracies. The buck output voltage should be configured to 4-V or 5.7-V to provide extra headroom to support the external LDO for generating 3.3-V or 5-V rail as shown in 图 8-5. This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

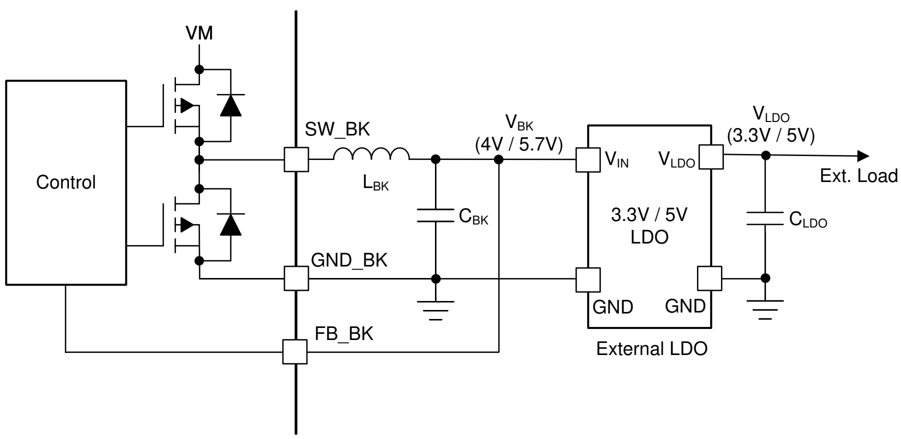

图 8-5. Buck Regulator with External LDO

8.3.3.4 AVDD Power Sequencing from Buck Regulator

The AVDD LDO has an option of using the power supply from mixed mode buck regulator to reduce the device power dissipation. The power sequencing mode allows on-the-fly changeover of AVDD LDO input from DC mains (VM) to buck output (V_{BK}) as shown in 图 8-6. This sequencing can be configured through the BUCK_PS_DIS bit . Power sequencing is supported only when buck output voltage is set to 5-V or 5.7-V.

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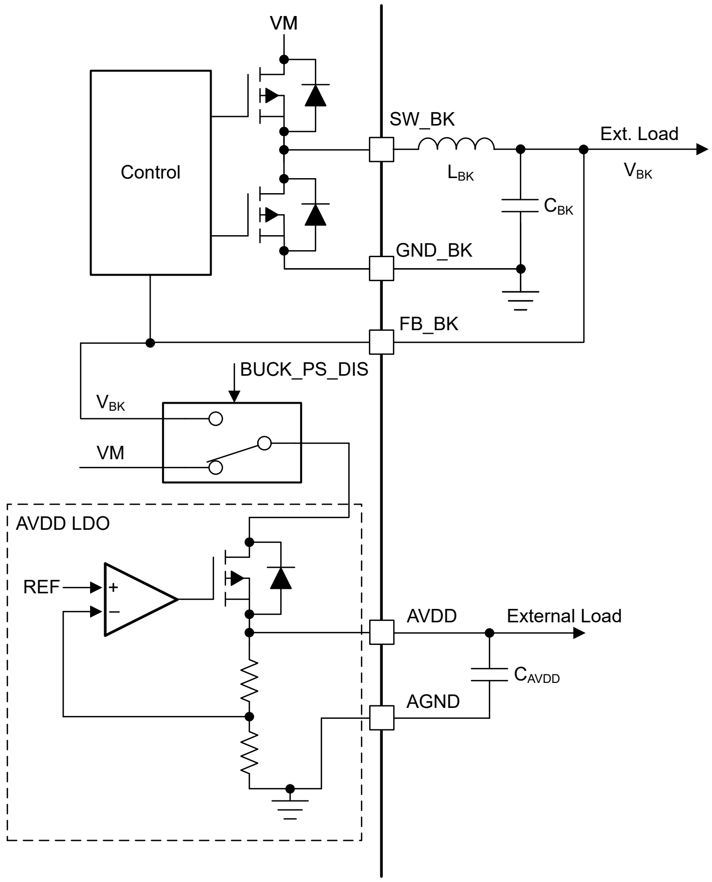

图 8-6. AVDD Power Sequencing from Mixed Mode Buck Regulator

8.3.3.5 Mixed Mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage (V_{BK_REF}) which is internally generated depending on the buck-output voltage setting (BUCK_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ($V_{BK} < V_{BK\_REF}$) or low ($V_{BK} > V_{BK\_REF}$), the high-side power FET of the buck turns on and off respectively. An independent current control loop monitors the current in high-side power FET (I_{BK}) and turns off the high-side FET when the current becomes higher than the buck current limit (I_{BK_CL}). This implements a current limit control for the buck regulator. 图 8-7 shows the architecture of the buck and various control/protection loops.

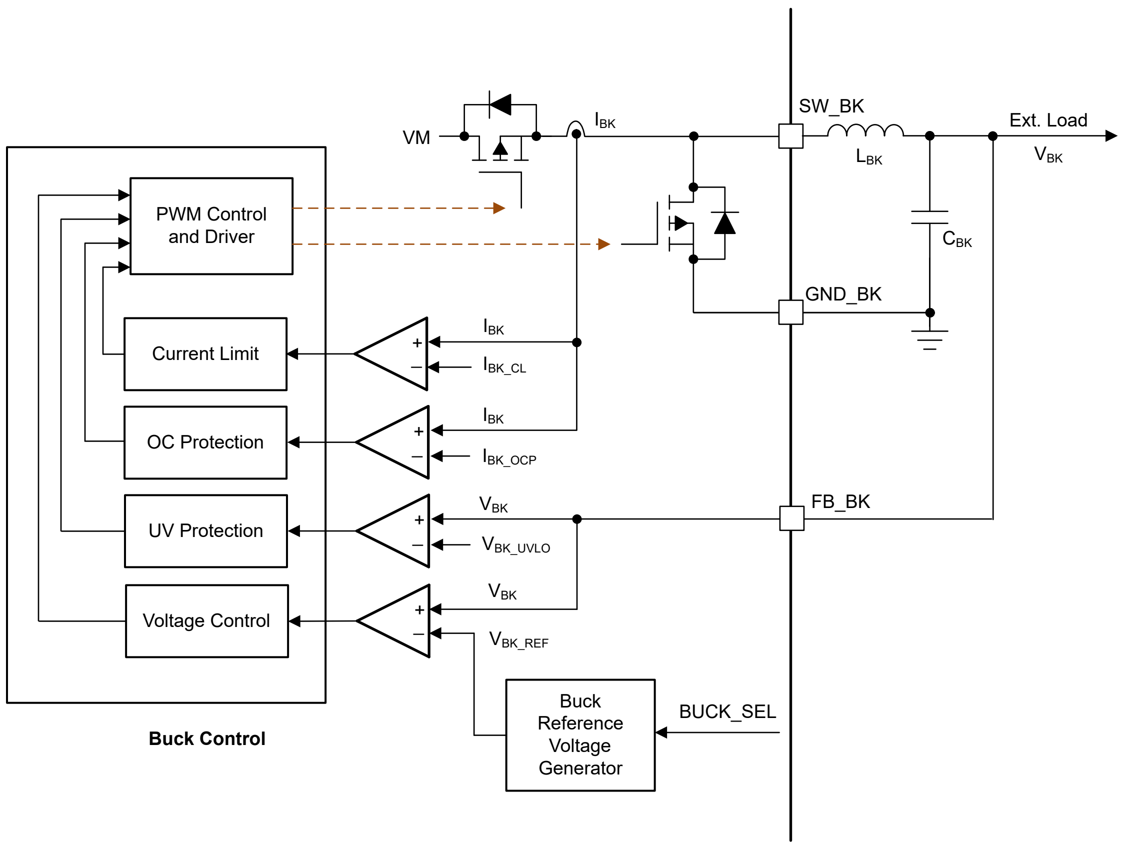

图 8-7. Buck Operation and Control Loops

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8.3.3.6 Buck Undervoltage Protection

If at any time the voltage on the FB_BK pin (buck regulator output) falls lower than the V_{BK_UVLO} threshold, both the high-side and low-side MOSFETs of the buck regulator are disabled . MCT8316A goes into reset state whenever buck UV event occurs, since the internal circuitry in MCT8316A is powered from the buck regulator output.

8.3.3.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current through the high-side MOSFET exceeds the I_{BK_OCP} threshold for a time longer than the deglitch time (t_{OCP_DEG}), a buck OCP event is recognized. MCT8316A goes into reset state whenever buck OCP event occurs, since the internal circuitry in MCT8316A is powered from the buck regulator output.

8.3.4 AVDD Linear Voltage Regulator

A 3.3-V, linear regulator is integrated into the MCT8316A family of devicesand is available for use by external circuitry. The AVDD LDO regulator is used for powering up the internal circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 20-mA). The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1-μF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3-V.

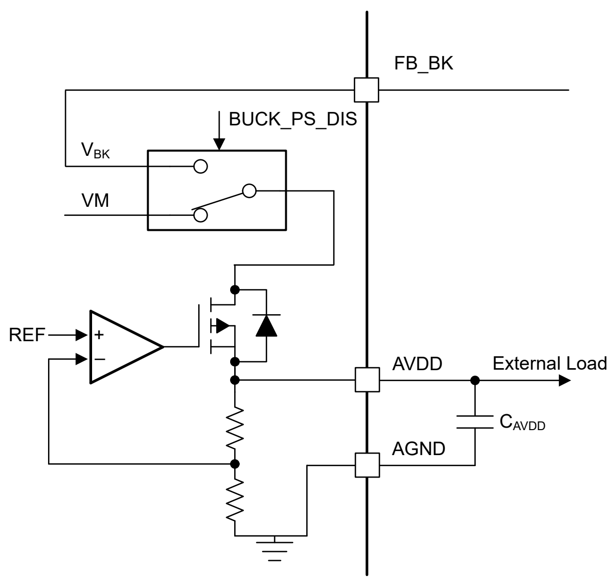

图 8-8. AVDD Linear Regulator Block Diagram

Use 方程式 1 to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply (BUCK_PS_DIS = 1b)

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \tag{1}$$

For example, at a V_{VM} of 24-V, drawing 20-mA out of AVDD results in a power dissipation as shown in 方程式 2.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \tag{2}$$

Use 方程式 3 to calculate the power dissipated in the device by the AVDD linear regulator with buck output as supply (BUCK_PS_DIS = 0b)

$$P = (V_{FB\_BK} - V_{AVDD}) \times I_{AVDD} \tag{3}$$

8.3.5 Charge Pump

Since the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to turn-on the high-side FETs. The MCT8316A integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors(C_{CP}, C_{FLY}) for operation. See the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth).

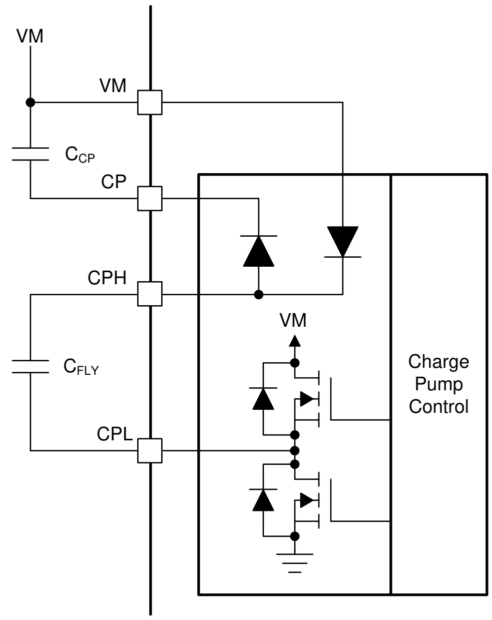

图 8-9. Charge Pump

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8.3.6 Slew Rate Control

An adjustable gate-drive current control for the MOSFETs in the output stage is provided to achieve configurable slew rate for EMI mitigation. The MOSFET VDS slew rate is a critical factor for optimizing radiated emissions, total energy and duration of diode recovery spikes and switching voltage transients related to parasitic elements of the PCB. This slew rate is predominantly determined by the control of the internal MOSFET gate current as shown in 图 8-10.

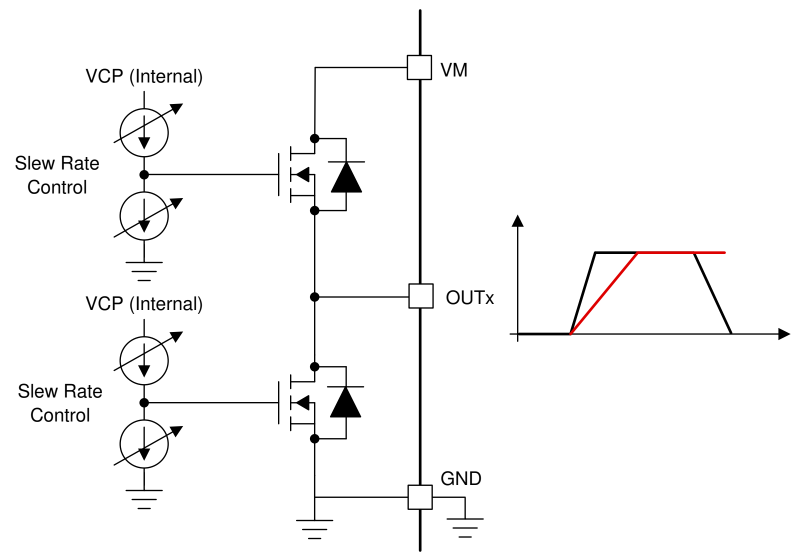

图 8-10. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted through SLEW_RATE settings. Slew rate can be configured as 25-V/µs, 50-V/µs, 125-V/µs or 200-V/µs. The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in 图 8-11.

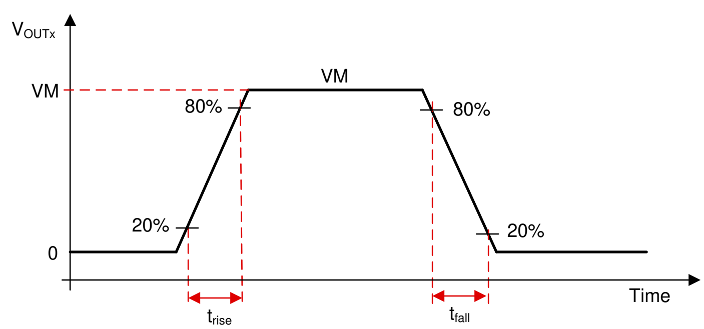

图 8-11. Slew Rate Timings

8.3.7 Cross Conduction (Dead Time)

The device is fully protected against any cross conduction of the MOSFETs. The high-side and low-side MOSFETs are carefully controlled to avoid any shoot-through events by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that the VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in 图 8-12 and 图 8-13 and vice versa.

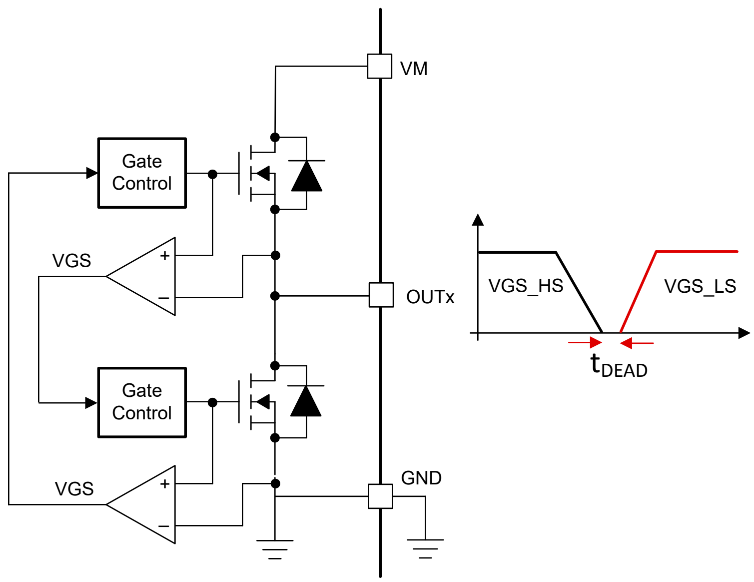

图 8-12. Cross Conduction Protection

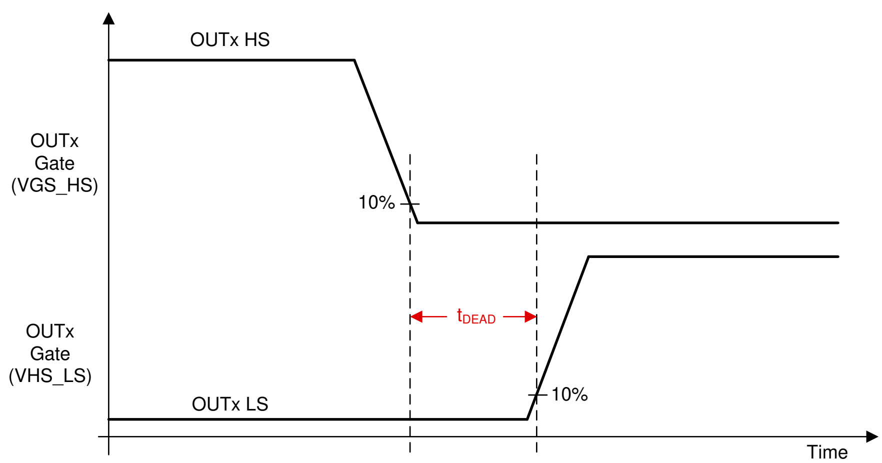

图 8-13. Dead Time

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8.3.8 SPEED Control

The MCT8316A offers four methods of directly controlling the speed of the motor. The speed control method is configured by SPD_CTRL_MODE. The speed command can be controlled in one of the following four ways.

- PWM input on SPEED pin by varying duty cycle of input signal
- Frequency input on SPEED pin by varying frequency of input signal
- Analog input on SPEED pin by varying amplitude of input signal
- Over I^2C by configuring SPEED_CTRL

The speed can also be indirectly controlled by varying the supply voltage (V_M).

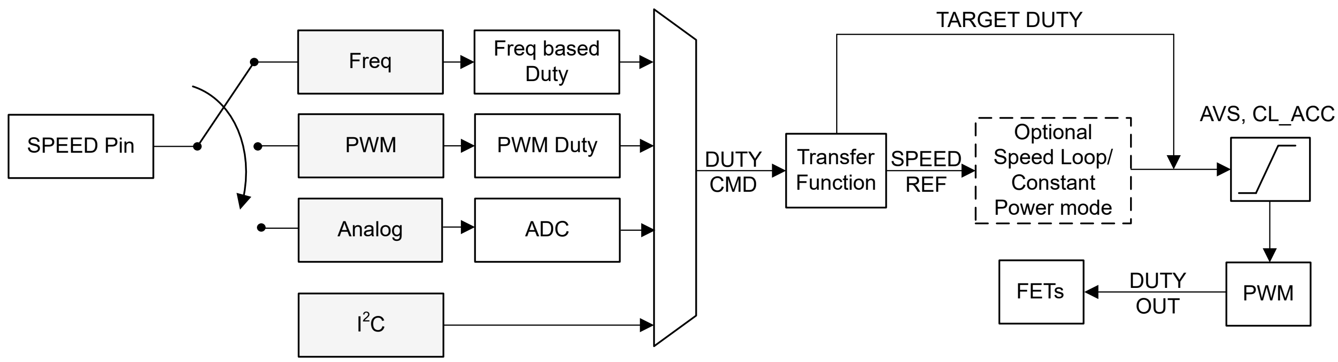

图 8-14. Multiplexing the Speed Command

The signal path from SPEED pin input (or I^2C based speed input) to output duty cycle (DUTY OUT) applied to FETs is shown in 图 8-14.

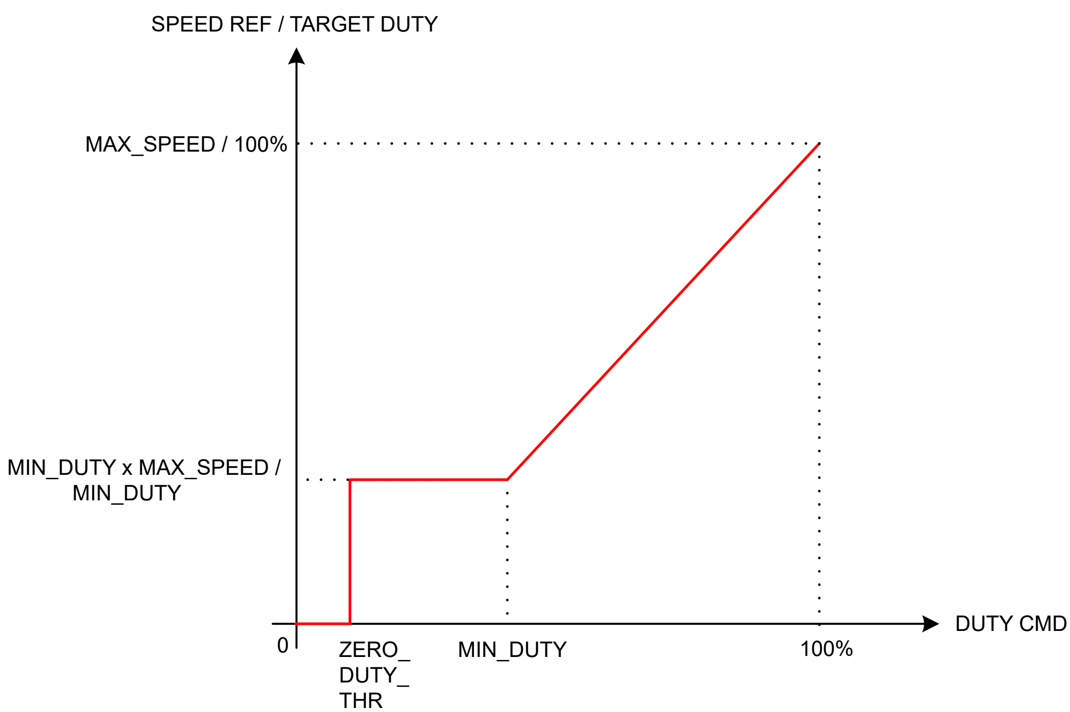

图 8-15. Speed Input Transfer Function

图 8-15 shows the relationship between DUTY CMD and SPEED REF / TARGET DUTY.

When speed loop is enabled, DUTY CMD sets the SPEED REF in Hz. MAX_SPEED sets the SPEED REF at DUTY CMD of 100%. MIN_DUTY sets the minimum SPEED REF (MIN_DUTY x MAX_SPEED). SPEED REF stays clamped at (MIN_DUTY x MAX_SPEED) for ZERO_DUTY_THR < DUTY CMD < MIN_DUTY.

When speed loop is disabled, DUTY CMD sets the TARGET DUTY in % - TARGET DUTY is 100% when DUTY CMD is 100% and TARGET DUTY is equal to MIN_DUTY when DUTY CMD is set to MIN_DUTY. TARGET DUTY stays clamped at MIN DUTY for ZERO_DUTY_THR < DUTY CMD < MIN_DUTY.

ZERO_DUTY_THR sets the DUTY CMD below which SPEED REF/ TARGET DUTY (speed loop enabled/ disabled) is set to zero and motor is in stopped state. AVS, CL_ACC configure the transient characteristics of DUTY OUT; the steady state value of DUTY OUT is directly configured in % through TARGET DUTY (when speed loop is disabled) or through SPEED REF (when speed loop is enabled).

8.3.8.1 Analog-Mode Speed Control

Analog input based speed control can be configured by setting SPD_CTRL_MODE to 00b. In this mode, the duty command (DUTY CMD) varies with the analog voltage input on the SPEED pin(V_{SPEED}). When 0 < V_{SPEED} < V_{EN_SB}, DUTY CMD is set to zero and the motor is stopped. When V_{EN_SB} < V_{SPEED} < V_{ANA_FS}, DUTY CMD varies linearly with V_{SPEED} as shown in 图 8-16 . When V_{SPEED} > V_{ANA_FS}, DUTY CMD is clamped to 100%.

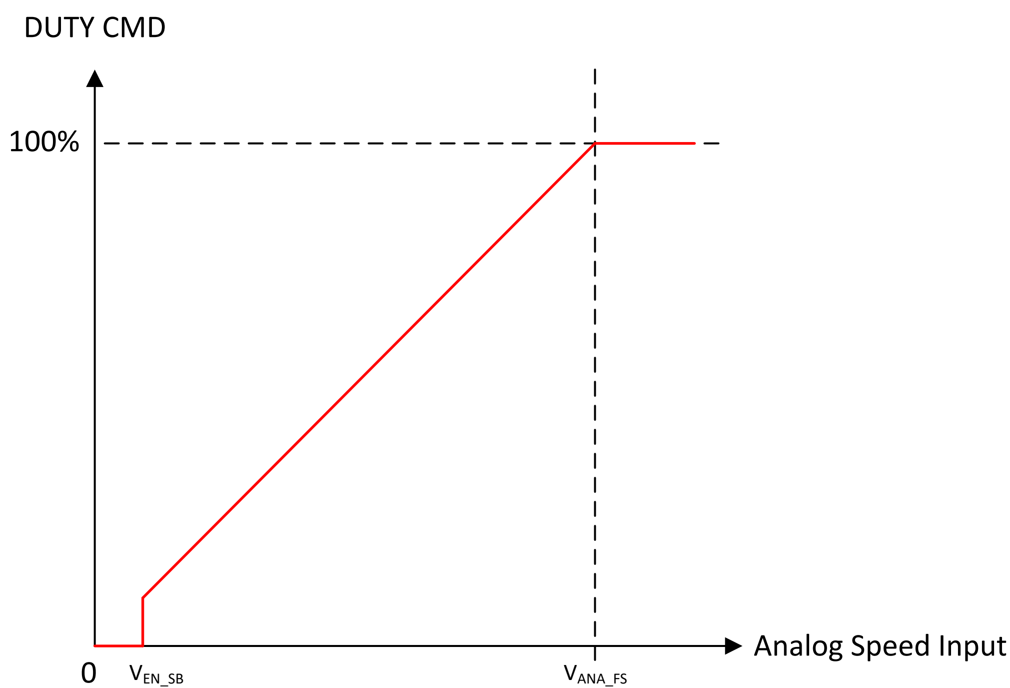

图 8-16. Analog-Mode Speed Control

8.3.8.2 PWM-Mode Speed Control

PWM based speed control can be configured by setting SPD_CTRL_MODE to 01b. In this mode, the PWM duty cycle applied to the SPEED pin can be varied from 0 to 100% and duty command (DUTY CMD) varies linearly with the applied PWM duty cycle. DUTY CMD is set to zero and the motor is stopped when the PWM signal at SPEED pin stays < V_{DIG_IL} for longer than $t_{EN\_SB\_PWM}$. The frequency of the PWM input signal applied to the SPEED pin is defined as f_{PWM} and the range for this frequency can be configured through SPD_PWM_RANGE_SELECT.

备注

f_{PWM} is the frequency of the PWM signal the device can accept at SPEED pin to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phases. The PWM output frequency can be configured through PWM_FREQ_OUT (see 节 8.3.15).

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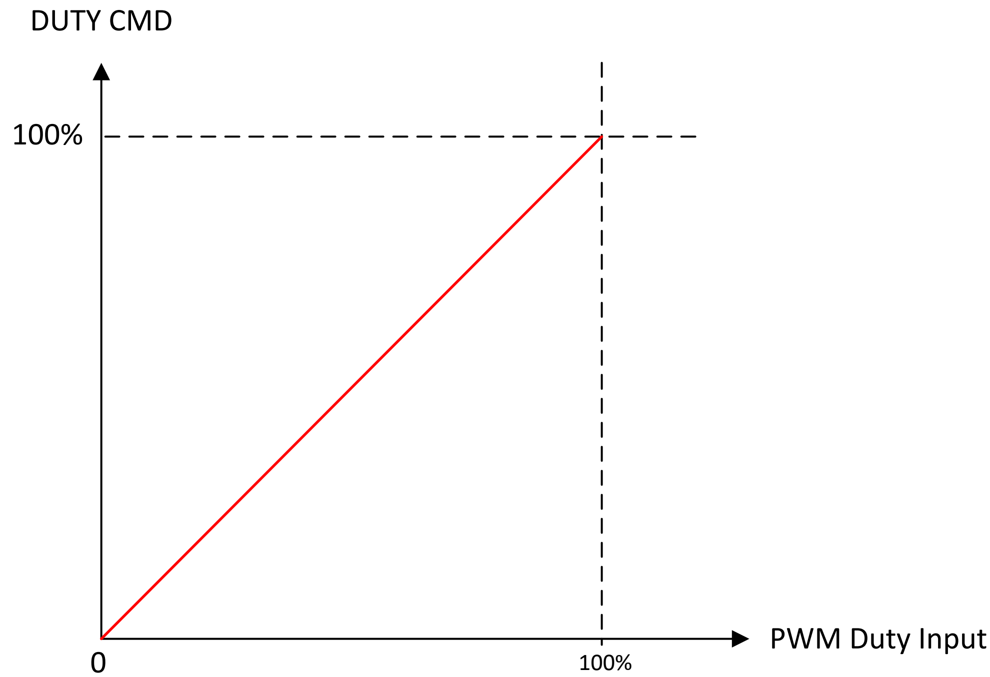

图 8-17. PWM-Mode Speed Control

8.3.8.3 I²C based Speed Control

I²C based serial interface can be used for speed control by setting SPD_CTRL_MODE to 10b. In this mode, the duty command can be written directly into SPEED_CTRL and the SPEED pin can be independently used to control the sleep entry and exit. If SPEED pin input is < V_{EN_SL} for a time longer than SLEEP_TIME, MCT831A enters sleep state irrespective of the I²C duty command in SPEED_CTRL. When SPEED pin > V_{EX_SL}, MCT8316A exits sleep state and speed is controlled through SPEED_CTRL. If SPEED_CTRL is set to 0 and SPEED pin > V_{EX_SL}, MCT8316A is in standby state.

8.3.8.4 Frequency-Mode Speed Control

Frequency based speed control is configured by setting SPD_CTRL_MODE to 11b. In this mode, duty command varies linearly as a function of the frequency of the square wave input at SPEED pin as given in 方程式 4. Input frequency greater than INPUT_MAX_FREQUENCY clamps the duty command to 100%. The duty command is set to zero and the motor is stopped when the frequency signal at SPEED pin stays < V_{DIG_IL} for longer than $t_{EN\_SB\_FREQ}$.

Duty command = Frequency at SPEED pin / INPUT_MAX_FREQUENCY * 100 (4)

8.3.9 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when MCT8316A begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCT8316A includes a number of features to allow for reliable motor start-up under all of these conditions. 图 8-18 shows the motor start-up flow for each of the three initial motor states.

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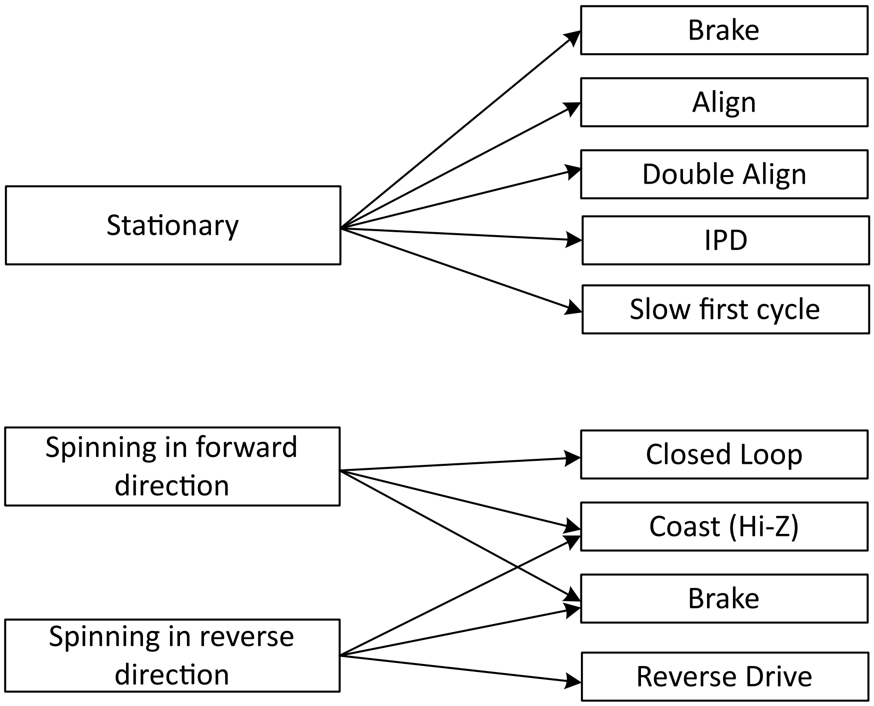

图 8-18. Starting the motor under different initial conditions

备注

"Forward" means "spinning in the same direction as the commanded direction", and "Reverse" means "spinning in the opposite direction as the commanded direction".

8.3.9.1 Case 1 – Motor is Stationary

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCT8316A provides various options to initialize the commutation logic to the motor position and reliably start the motor.

- The align and double align techniques force the motor into alignment by applying a voltage across a particular motor phase to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The slow first cycle method starts the motor by applying a low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

MCT8316A also provides a configurable brake option to ensure the motor is stationary before initiating one of the above start-up methods. Device enters open loop acceleration after going through the configured start-up method.

8.3.9.2 Case 2 – Motor is Spinning in the Forward Direction

If the motor is spinning forward (same direction as the commanded direction) with sufficient speed (BEMF), the MCT8316A resynchronizes with the spinning motor and continues commutation by going directly to closed loop operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. This resynchronization feature can be enabled or disabled through RESYNC_EN. If resynchronization is disabled, the MCT8316A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

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8.3.9.3 Case 3 – Motor is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction (the opposite direction as the commanded direction), the MCT8316A provides several methods to change the direction and drive the motor to the target speed reference in the commanded direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero speed. The motor achieves the shortest possible spin-up time when spinning in the reverse direction.

If reverse drive is not enabled, then the MCT8316A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

备注

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

8.3.10 Motor Start Sequence (MSS)

图 8-19 shows the motor-start sequence implemented in the MCT8316A device.

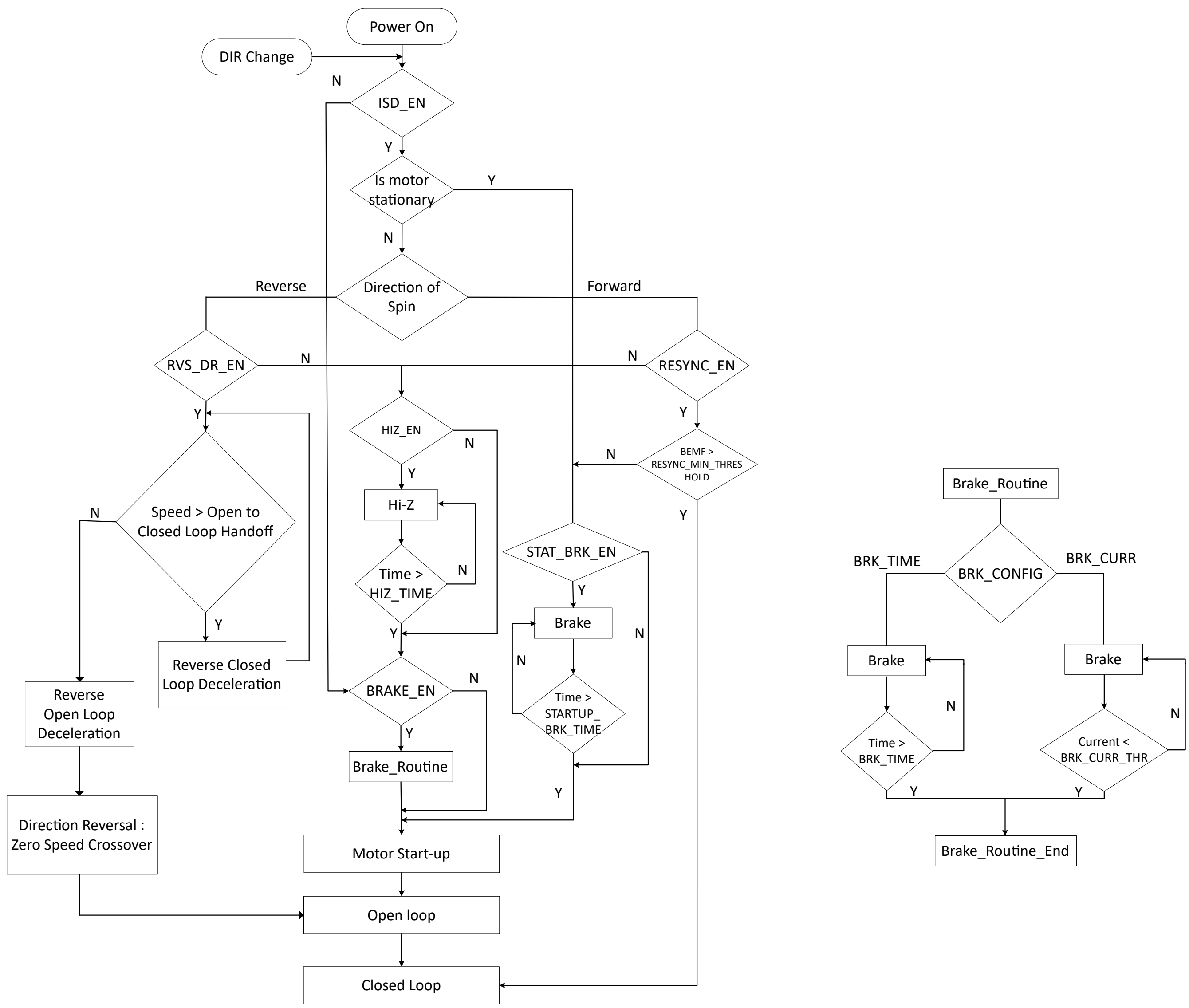

图 8-19. Motor Starting-Up Flow

Power-On State

This is the initial state of the Motor Start Sequence (MSS). The MSS starts in this state on initial power-up or whenever the MCT8316A device comes out of standby or sleep mode.

DIR Change Judgement

In MCT8316A, if direction change command is detected at start of MSS, the motor direction detected in ISD is assumed to be opposite to commanded direction and reverse drive is performed if RVS_DR_EN is set to 1b.

ISD_EN Judgement

After power-on, the MCT8316A MSS enters the ISD_EN judgement where it checks to see if the initial speed detect (ISD) function is enabled (ISD_EN = 1b). If ISD is disabled, the MSS proceeds directly to the BRAKE_EN judgement. If ISD is enabled, MSS advances to the ISD (Is Motor Stationary) state.

ISD State

The MSS determines the initial condition (speed, direction of spin) of the motor (see Initial Speed Detect (ISD)). If motor is deemed to be stationary

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(motor BEMF < STAT_DETECT_THR), the MSS proceeds to STAT_BRK_EN judgement. If the motor is not stationary, MSS proceeds to verify the direction of spin.

STAT_BRK_EN Judgement
The MSS checks if the stationary brake function is enabled (STAT_BRK_EN =1b). If the stationary brake function is enabled, the MSS advances to the stationary brake routine. If the stationary brake function is disabled, the MSS advances to motor start-up state (see 节 8.3.10.4).

Stationary Brake Routine
The stationary brake routine can be used to ensure the motor is completely stationary before attempting to start the motor. The stationary brake is applied by turning on all three low-side driver MOSFETs for a time configured by STARTUP_BRK_TIME.

Direction of Spin Judgement
The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the MCT8316A proceeds to the RESYNC_EN judgement. If the motor is spinning in the reverse direction, the MSS proceeds to the RVS_DR_EN judgement.

RESYNC_EN Judgement
If RESYNC_EN is set to 1b, MCT8316A proceeds to BEMF > RESYNC_MIN_THRESHOLD judgement. If RESYNC_EN is set to 0b, MSS proceeds to HIZ_EN judgement.

BEMF > RESYNC_MIN_THRESHOLD Judgement
If motor speed is such that BEMF > RESYNC_MIN_THRESHOLD, MCT8316A uses the speed and position information from the ISD state to transition to the closed loop state (see Motor Resynchronization) directly. If BEMF < RESYNC_MIN_THRESHOLD, MCT8316A proceeds to STAT_BRK_EN judgement.

RVS_DR_EN Judgement
The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1). If it is enabled, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled, the MSS advances to the HIZ_EN judgement.

Speed > Open to Closed Loop Handoff Judgement
The MSS checks to see if the reverse speed is high enough for MCT8316A to decelerate in closed loop. Till the speed (in reverse direction) is high enough, MSS stays in reverse closed loop deceleration. If speed is too low, then the MSS transitions to reverse open loop deceleration.

Reverse Closed Loop, Open Loop Deceleration and Zero Speed Crossover
The MCT8316A resynchronizes in the reverse direction, decelerates the motor in closed loop till motor speed falls below the handoff threshold. (see *Reverse Drive*). When motor speed in reverse direction is too low, the MCT8316A switches to open-loop, decelerates the motor in open-loop, crosses zero speed, and accelerates in the forward direction in open-loop before entering closed loop operation after motor speed is sufficiently high.

HIZ_EN Judgement
The MSS checks to determine whether the coast (Hi-Z) function is enabled (HIZ_EN =1). If the coast function is enabled, the MSS advances to the coast routine. If the coast function is disabled, the MSS advances to the BRAKE_EN judgement.

Coast (Hi-Z) Routine
The device coasts the motor by turning OFF all six MOSFETs for a certain time configured by HIZ_TIME.

BRAKE_EN Judgement
The MSS checks to determine whether the brake function is enabled (BRAKE_EN =1). If the brake function is enabled, the MSS advances to the brake routine. If the brake function is disabled, the MSS advances to the motor start-up state (see 节 8.3.10.4).

Brake Routine
MCT8316A implements either a time based brake (duration configured by BRK_TIME) or a current based brake (brake applied till phase currents <

	BRK_CURR_THR) based on BRK_CONFIG. Brake is applied either using high-side or low-side MOSFETs based on BRK_MODE configuration.
Closed Loop State	In this state, the MCT8316A drives the motor with trapezoidal control.

8.3.10.1 Initial Speed Detect (ISD)

The ISD function is used to identify the initial condition of the motor and is enabled by setting ISD_EN to 1b. The initial speed, position and direction is determined by sampling the phase voltage through the internal ADC. ISD can be disabled by setting ISD_EN to 0b. If the function is disabled (ISD_EN set to 0b), the MCT8316A does not perform the initial speed detect function and proceeds to check if the brake routine (BRAKE_EN) is enabled.

8.3.10.2 Motor Resynchronization

The motor resynchronization function works when the ISD and resynchronization functions are both enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the commanded direction). The speed and position information measured during ISD are used to initialize the drive state of the MCT8316A, which can transition directly into closed loop state without needing to stop the motor. In the MCT8316A, motor resynchronization can be enabled/disabled through RESYNC_EN bit. If motor resynchronization is disabled, the device proceeds to check if the motor coast (Hi-Z) routine is enabled.

8.3.10.3 Reverse Drive

The MCT8316A uses the reverse drive function to change the direction of the motor rotation when ISD_EN and RVS_DR_EN are both set to 1b and the ISD determines the motor spin direction to be opposite to that of the commanded direction. Reverse drive includes synchronizing with the motor speed in the reverse direction, reverse decelerating the motor through zero speed, changing direction, and accelerating in open loop in forward (or commanded) direction until the device transitions into closed loop in forward direction (see 图 8-20). MCT8316A uses the same parameter values for open to closed loop handoff threshold (OPN_CL_HANDOFF_THR), open loop acceleration rates (OL_ACC_A1, OL_ACC_A2) and open loop current limit (OL_ILIMIT) in the reverse direction as in the forward direction..

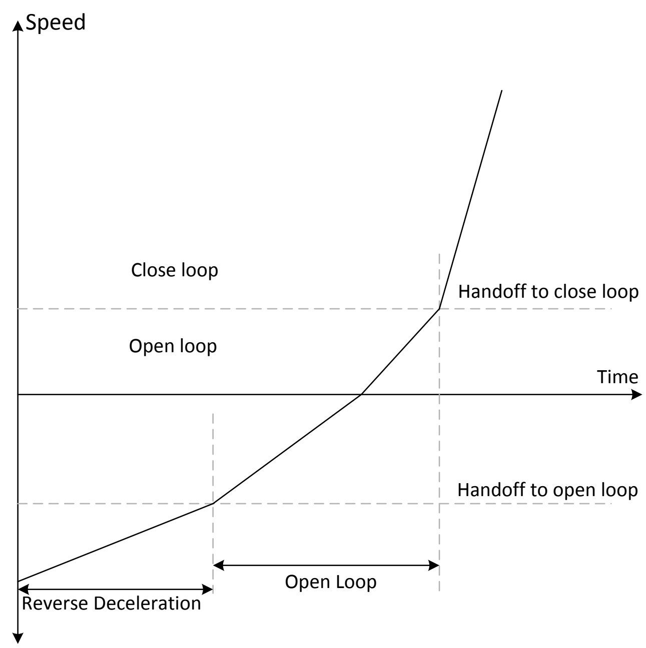

图 8-20. Reverse Drive Function

8.3.10.4 Motor Start-up

There are different options available for motor start-up from a stationary position and these options can be configured by MTR_STARTUP. In align and double align mode, the motor is aligned to a known position by

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injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle.

8.3.10.4.1 Align

Align is enabled by configuring MTR_STARTUP to 00b. The MCT8316A aligns the motor by injecting a DC current using a particular phase pattern (phase-C high-side FET and phase-B low-side FET are ON) - current flowing into phase-B and flowing out from phase-C for a certain time configured by ALIGN_TIME.

The duty cycle during align is defined by ALIGN_DUTY. In MCT8316A, current limit during align is configured through OL_ILIMIT_CONFIG and is determined by ILIMIT or OL_ILIMIT based on configuration of OL_ILIMIT_CONFIG.

A fast change in the phase current during align may result in a sudden change in the driving torque and this could result in acoustic noise. To avoid this, the MCT8316A ramps up duty cycle from 0 to until it reaches ALIGN_DUTY at a configurable rate set by ALIGN_RAMP_RATE. At the end of align routine, the motor will be aligned at the known position.

8.3.10.4.2 Double Align

Double align is enabled by configuring MTR_STARTUP to 01b. Single align is not reliable when the initial position of the rotor is 180^o out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In order to improve the reliabilty of align based start-up, the MCT8316A provides the option of double align start-up. In double align start-up, MCT8316A uses a phase pattern for the second align that is 60^o out of phase with the first align phase pattern in the commanded direction. In double align, relevant parameters like align time, current limit, ramp rate are the same as in the case of single align - two different phase patterns are applied in succession with the same parameters to ensure that the motor will be aligned to a known position irrespective of initial rotor position.

8.3.10.4.3 Initial Position Detection (IPD)

Initial Position Detection (IPD) can be enabled by configuring MTR_STARTUP to 10b. In IPD, inductive sense method is used to determine the initial position of the motor using the spatial variation in the motor inductance.

Align or double align may result in the motor spinning in the reverse direction before starting open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. IPD does not wait for the motor to align with the commutation and therefore can allow for a faster motor start-up sequence. IPD works well when the inductance of the motor varies as a function of position. IPD works by pulsing current in to the motor and hence can generate acoustics which must be taken into account when determining the best start-up method for a particular application.

8.3.10.4.3.1 IPD Operation

IPD operates by sequentially applying six different phase patterns according to the following sequence: BC-> CB-> AB-> BA-> CA-> AC (see 图 8-21). When the current reaches the threshold configured by IPD_CURR_THR, the MCT8316A stops driving the particular phase pattern and measures the time taken to reach the current threshold from when the particular phase pattern was applied. Thus, the time taken to reach IPD_CURR_THR is measured for all six phase patterns - this time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

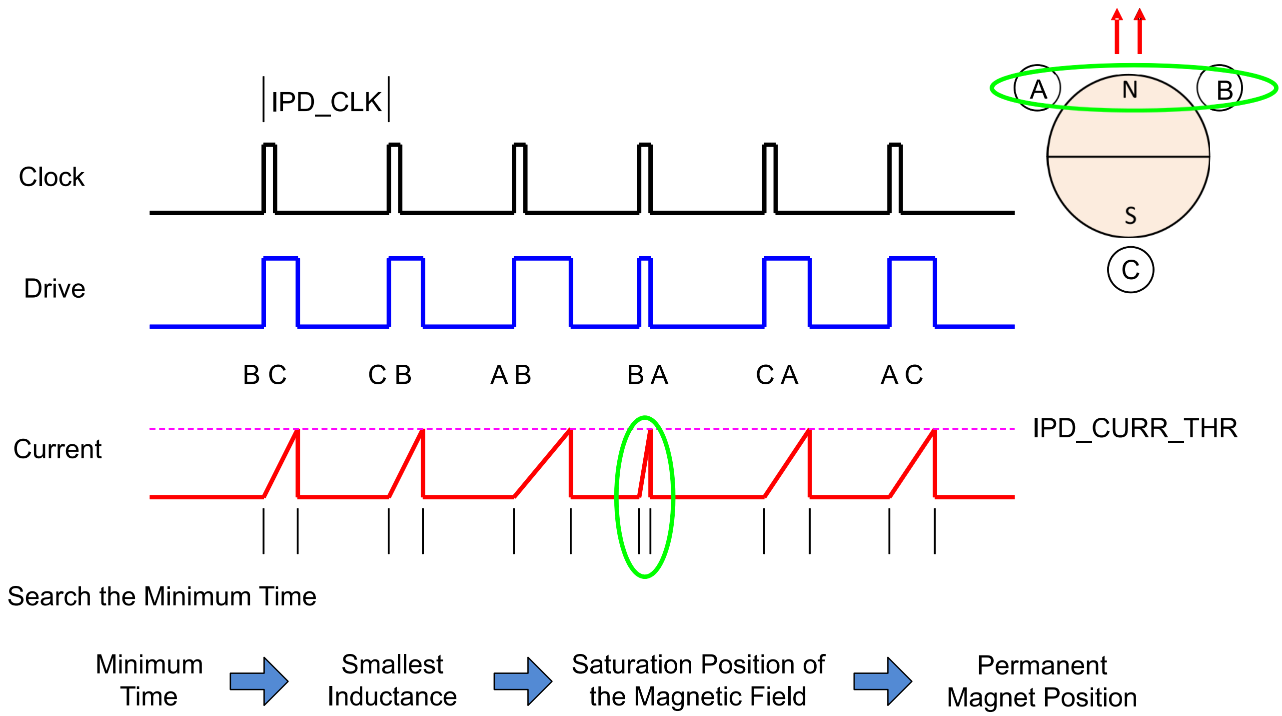

图 8-21. IPD Function

8.3.10.4.3.2 IPD Release Mode

Two modes are available for configuring the way the MCT8316A stops driving the motor when the current threshold is reached. The recirculate (or brake) mode is selected if IPD_RLS_MODE = 0b. In this configuration, the low-side (LSC) MOSFET remains ON to allow the current to recirculate between the MOSFET (LSC) and body diode (LSA) (see 图 8-22). Hi-Z mode is selected if IPD_RLS_MODE = 1b. In Hi-Z mode, both the high-side (HSA) and low-side (LSC) MOSFETs are turned OFF and the current recirculates through the body diodes back to the power supply (see 图 8-23).

In the Hi-Z mode, the phase current has a faster settle-down time, but that can result in a voltage increase on V_M. The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between V_M and GND to absorb the energy. If the voltage surge cannot be contained or if it is unacceptable for the application, recirculate mode must be used. When using the recirculate mode, select the IPD_CLK_FREQ appropriately to give the current in the motor windings enough time to decay to to 0-A before the next IPD phase pattern is applied.

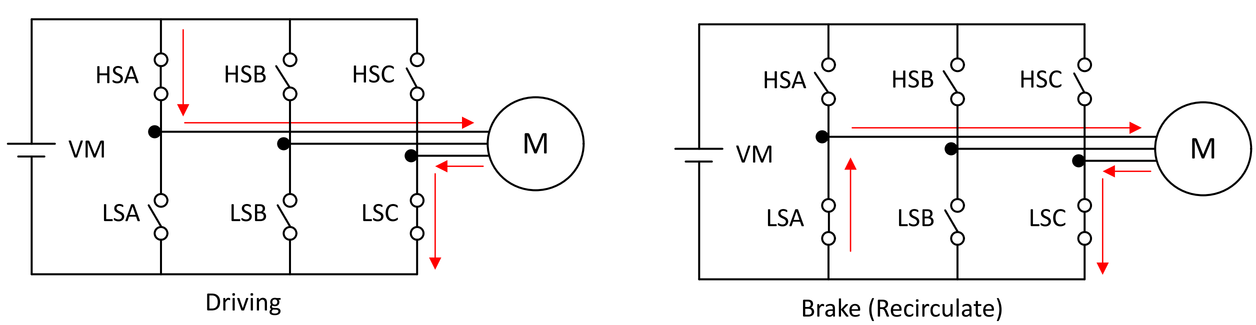

图 8-22. IPD Release Mode 0

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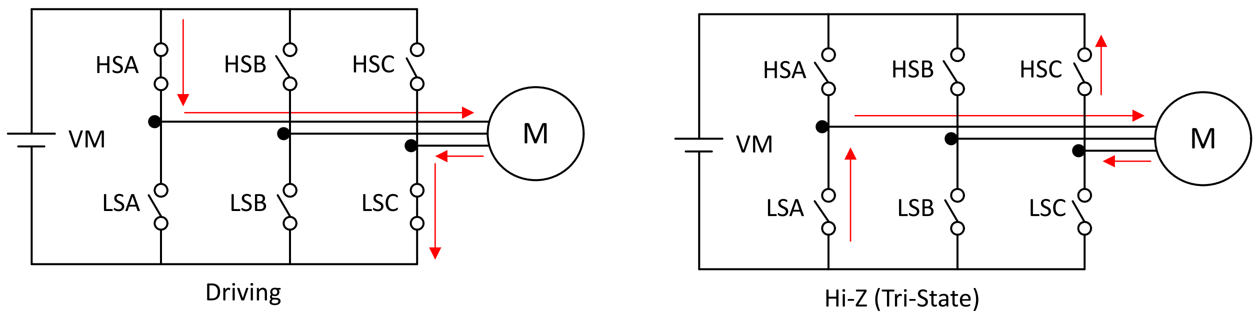

图 8-23. IPD Release Mode 1

8.3.10.4.3.3 IPD Advance Angle

After the initial position is detected, the MCT8316A begins driving the motor in open loop at an angle specified by IPD_ADV_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD_ADV_ANGLE to allow for smooth acceleration in the application (see 图 8-24).

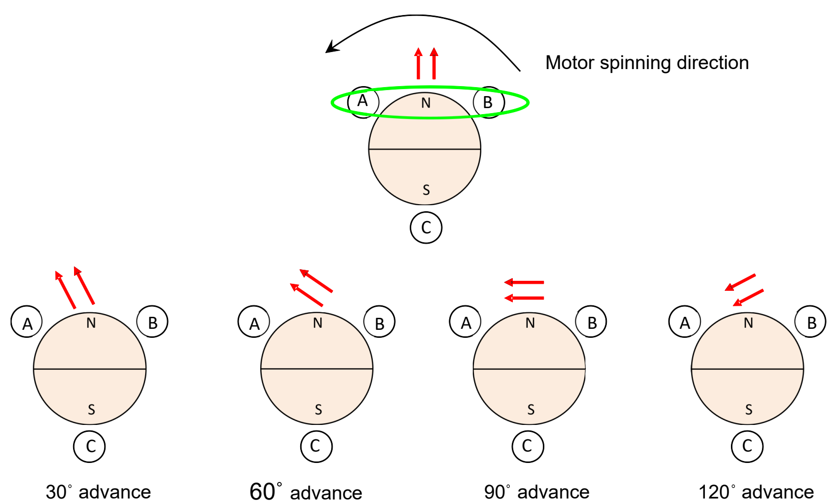

图 8-24. IPD Advance Angle

8.3.10.4.4 Slow First Cycle Startup

Slow First Cycle start-up is enabled by configuring MTR_STARTUP to 11b. In slow first cycle start-up, the MCT8316A starts motor commutation at a frequency defined by SLOW_FIRST_CYCLE_FREQ. The frequency configured is used only for first cycle, and then the motor commutation follows acceleration profile configured by open loop acceleration coefficients A1 and A2. The slow first cycle frequency has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

8.3.10.4.5 Open loop

Upon completing the motor position initialization with either align, double align, IPD or slow first cycle, the MCT8316A begins to accelerate the motor in open loop. During open loop, fixed duty cycle is applied and the cycle by cycle current limit functionality is used to regulate the current.

In MCT8316A, open loop current limit threshold is selected through OL_ILIMIT_CONFIG and is set either by ILIMIT or OL_ILIMIT based on the configuration of OL_ILIMIT_CONFIG. Open loop duty cycle is configured through OL_DUTY. While the motor is in open loop, speed (and commutation instants) is determined by 方程式 5. In MCT8316A, open loop acceleration coefficients, A1 and A2 are configured through OL_ACC_A1 and OL_ACC_A2 respectively. The function of the open-loop operation is to drive the motor to a speed at which the motor generates sufficient BEMF to allow the BEMF zero-crossing based commutation control to accurately drive the motor.

$$\text{Speed (t)} = A1 * t + 0.5 * A2 * t^2 \quad (5)$$

8.3.10.4.6 Transition from Open to Closed Loop

MCT8316A has an internal mechanism to determine the motor speed for transition from open loop commutation to BEMF zero crossing based closed loop commutation. This feature of automatically deciding the open to closed handoff speed can be enabled by configuring AUTO_HANDOFF to 1b. If AUTO_HANDOFF is set to 0b, the open to closed loop handoff speed needs to be configured by OPN_CL_HANDOFF_THR. The closed loop in this section does not refer to closed speed loop - it refers to the commutation control changing from open loop (equation based) to closed loop (BEMF zero crossing based).

8.3.11 Closed Loop Operation

In closed loop operation, the MCT8316A drives the motor using trapezoidal commutation. The commutation instant is determined by the BEMF zero crossing on the phase which is not driven (Hi-Z). The duty cycle of the applied motor voltage is determined by DUTY OUT (see SPEED Control).

8.3.11.1 120º Commutation

In 120º commutation, each phase is driven for 120º and is Hi-Z for 60º within each half electrical cycle as shown in 图 8-25. In 120º commutation there are six different commutation states. 120º commutation can be configured by setting COMM_CONTROL to 00b. MCT8316A supports different modulation modes with 120º commutation which can be configured through PWM_MODUL.

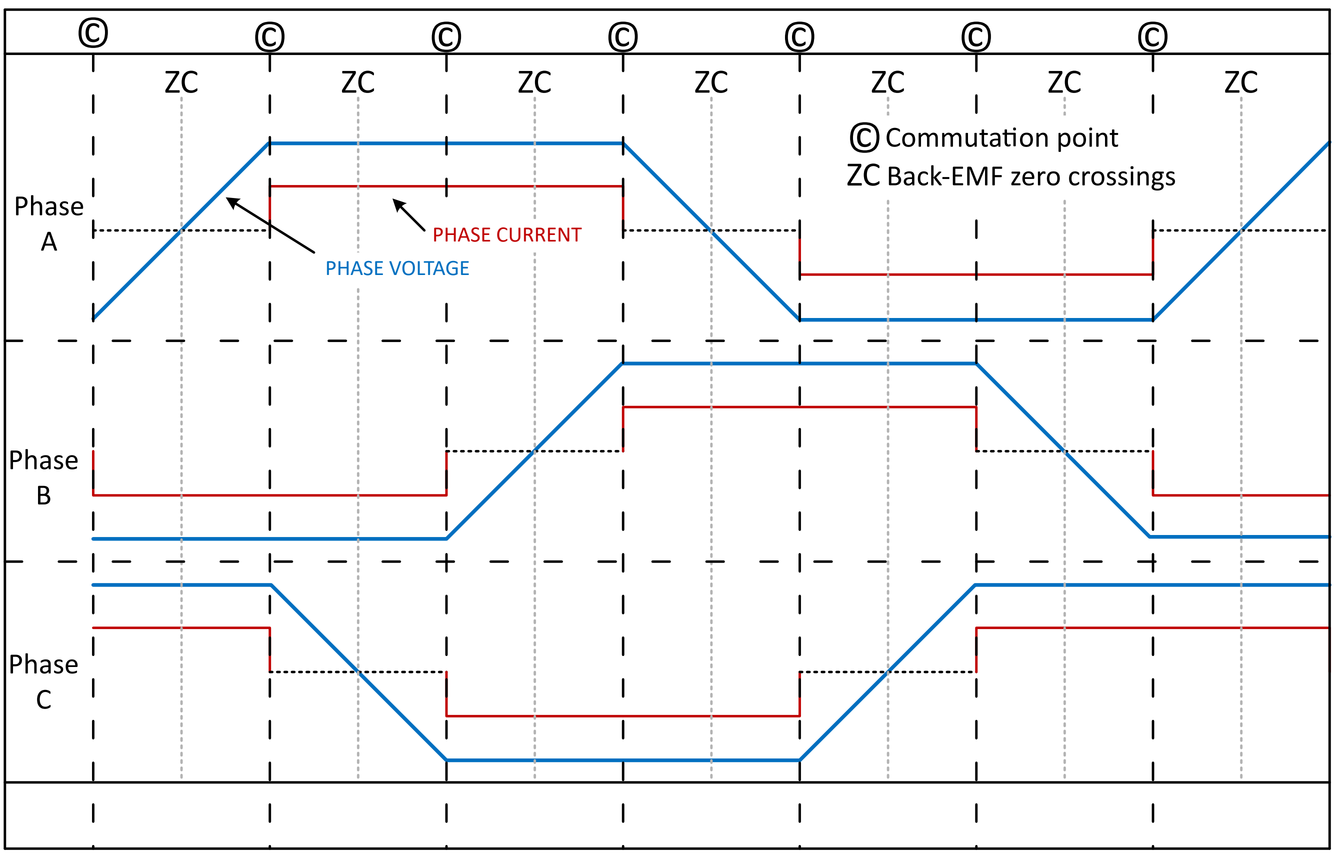

图 8-25. 120º commutation

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8.3.11.1.1 High-Side Modulation

High-side modulation can be configured by setting PWM_MODUL to 00b. In high-side modulation, for a given commutation state, one of the high-side FETs is switching with the commanded duty cycle DUTY_OUT, while the low-side FET is ON with 100% duty cycle (see 图 8-26).

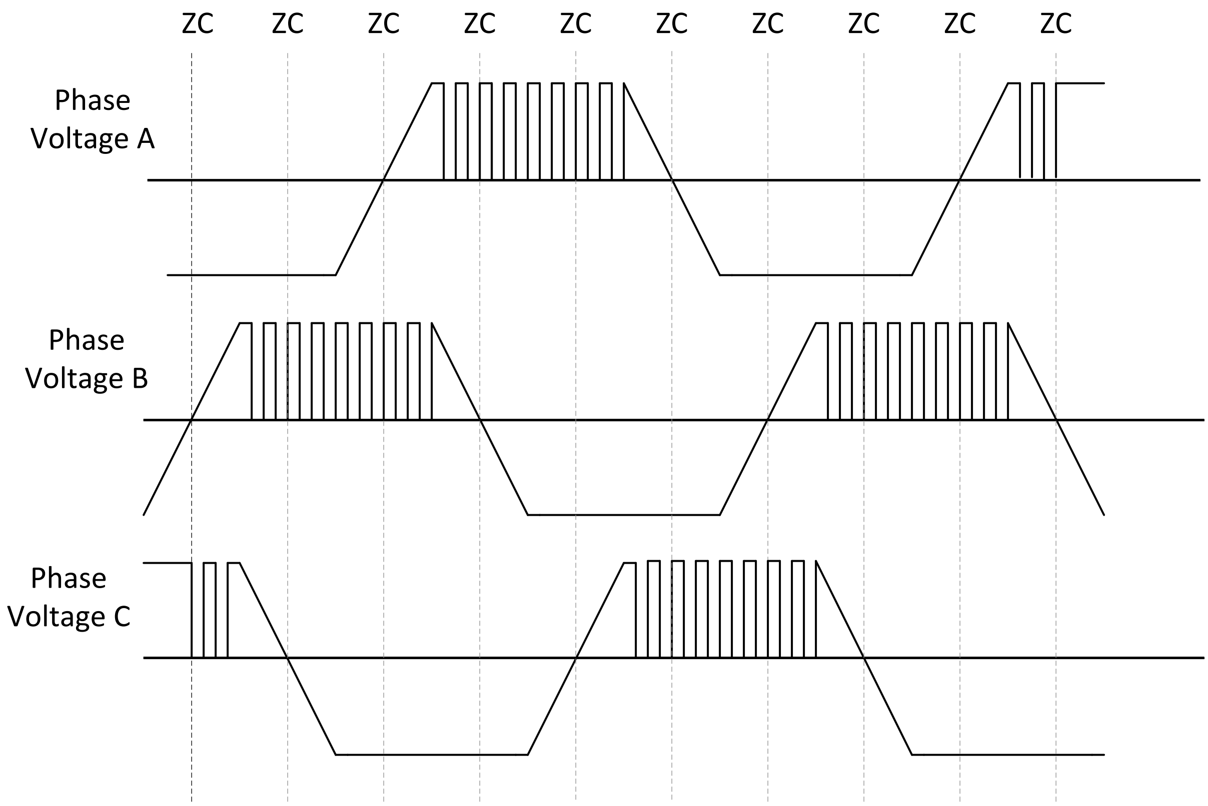

图 8-26. 120° commutation in High Side Modulation Mode

8.3.11.1.2 Low-Side Modulation

Low-side modulation can be configured by setting PWM_MODUL to 01b. In low-side modulation, for a given commutation state, one of the low-side FETs is switching with the commanded duty cycle DUTY_OUT, while the high-side FET is ON with 100% duty cycle (see 图 8-27).

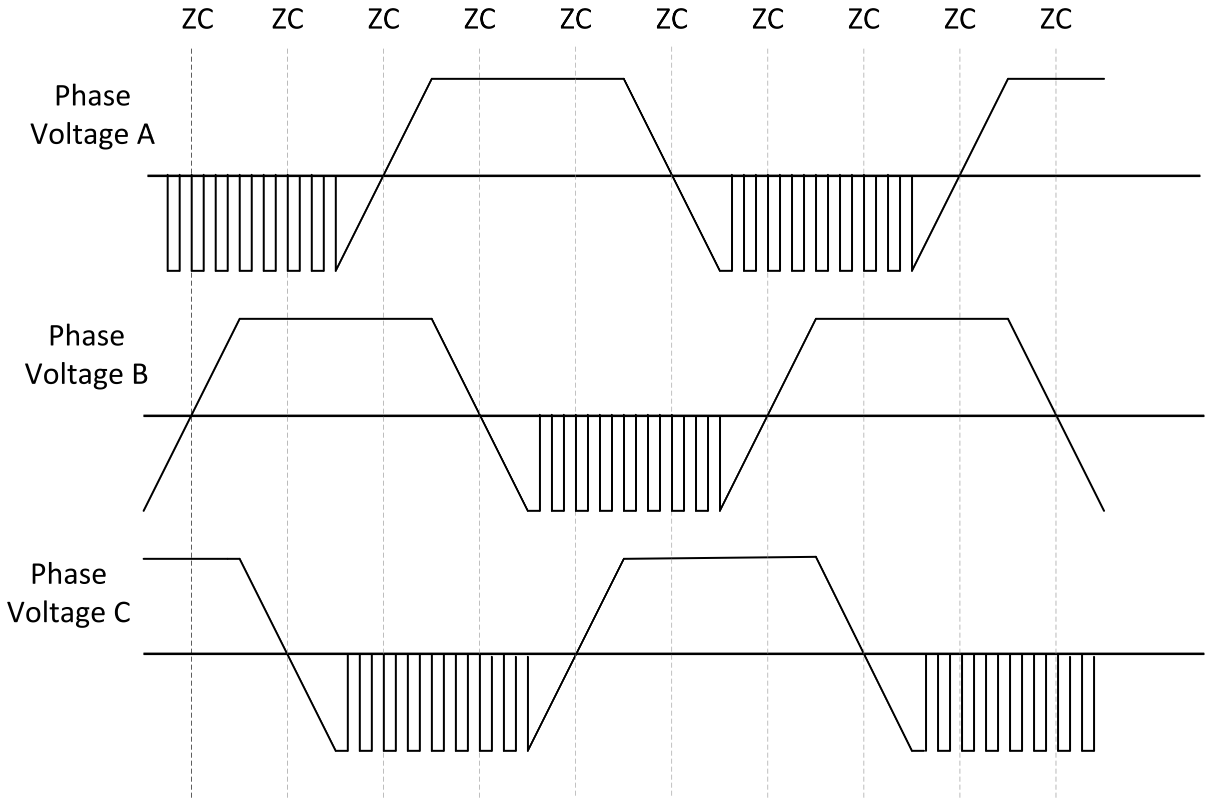

图 8-27. 120 º commutation in Low Side Modulation Mode

8.3.11.1.3 Mixed Modulation

Mixed modulation can be configured by setting PWM_MODUL to 10b. In mixed modulation, MCT8316A dynamically switches between high and low-side modulation (see 图 8-28). The switching losses are distributed evenly amongst the high and low-side MOSFETs in mixed modulation mode.

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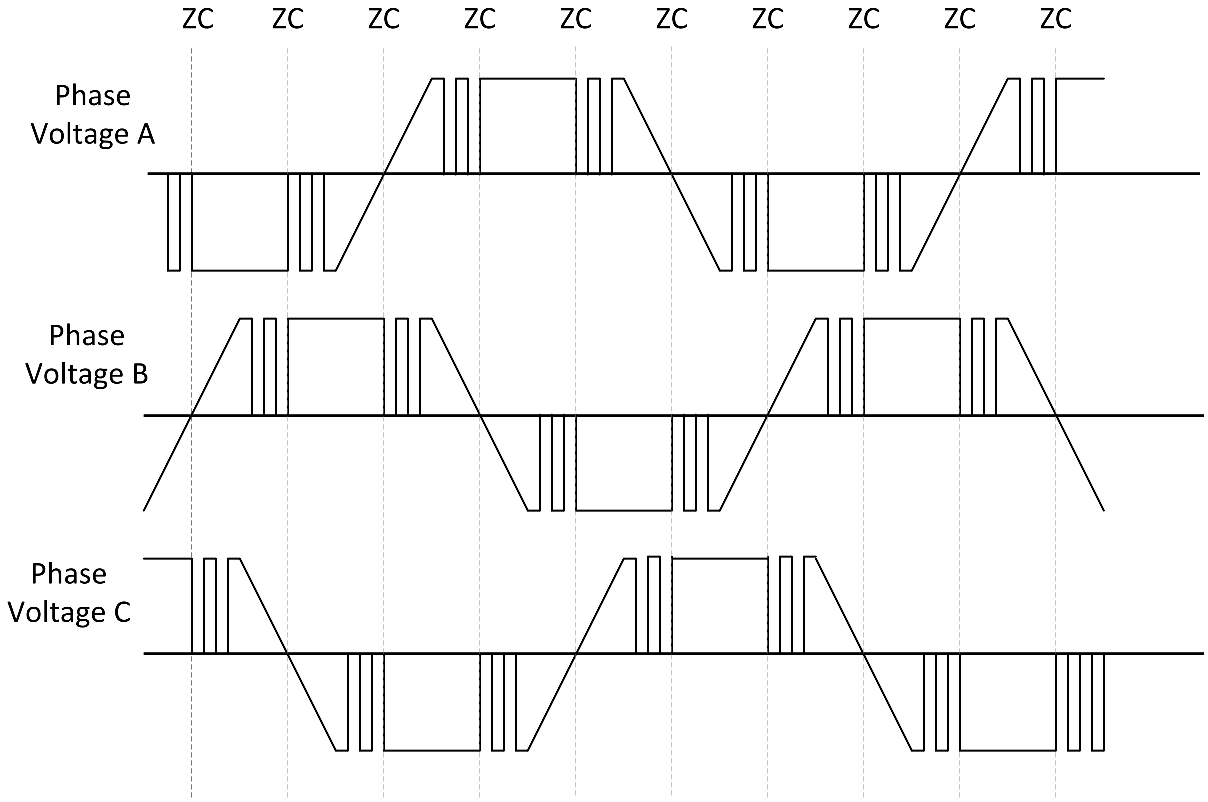

图 8-28. 120° commutation in Mixed Modulation Mode

8.3.11.2 Variable Commutation (Available only in MCT8316AV)

Variable commutation can be configured by setting COMM_CONTROL to 01b. 120° commutation may result in acoustic noise due to the long Hi-Z period causing some torque ripple in the motor. In order to reduce this torque ripple and acoustic noise, the MCT8316A uses variable commutation to reduce the phase current ripple at commutation by extending 120° driving time and gradually decreasing duty cycle prior to entering Hi-Z state. In this mode, the phase is Hi-Z between 30° and 60° and this window size is dynamically adjusted based on speed. A smaller window size will typically give better acoustic performance. 图 8-29 shows 150° commutation with 30° window size.

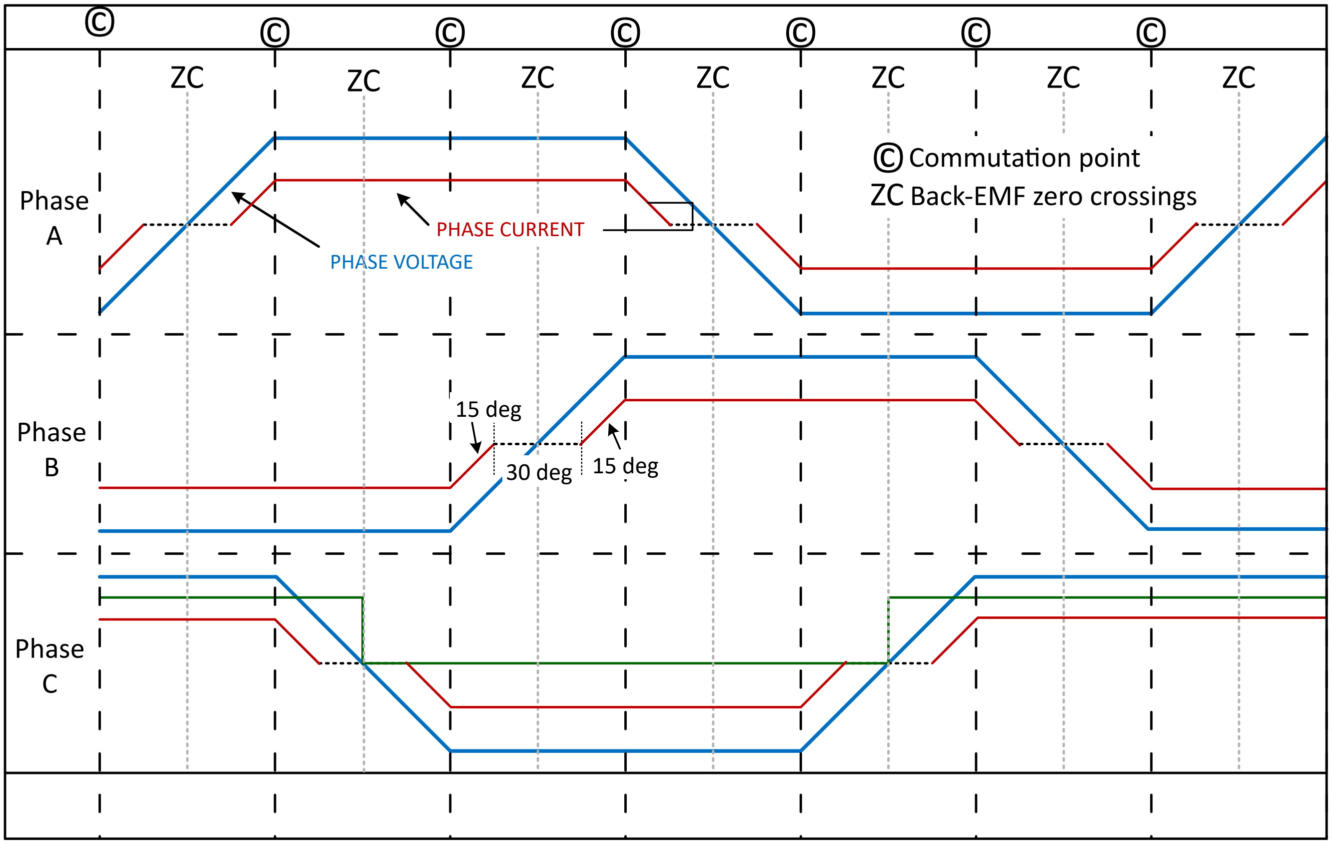

图 8-29. 150° commutation

备注

Different modulation modes are supported only with 120° commutation; variable commutation uses mixed modulation mode only.

8.3.11.3 Lead Angle Control

To achieve the best efficiency, it is often desirable to control the drive state of the motor so that the motor phase current is aligned with the motor BEMF voltage. MCT8316A provides the option to advance or delay the phase voltage from the commutation point by adjusting the lead angle. The lead angle can be adjusted to obtain optimal efficiency. This can be accomplished by operating the motor at constant speed and load conditions and adjusting the lead angle (LD_ANGLE) until the minimum current is achieved. The MCT8316A has the capability to apply both positive and negative lead angle (by configuring LD_ANGLE_POLARITY) as shown in 图 8-30

Lead angle can be calculated by {LD_ANGLE x 0.12}°; for example, if the LD_ANGLE is 0x1E and LD_ANGLE_POLARITY is 1b, then a lead angle of +3.6°(advance) is applied. If LD_ANGLE_POLARITY is 0b, then a lead angle of -3.6°(delay) is applied.

备注

For 120° commutation, the negative lead angle is limited to -20°; any lead angle lower than that will be clamped to -20°.

For variable commutation, negative lead angle is not supported and positive lead angle is limited to +15°. Anything configured higher than +15° or lower than 0^0 will be clamped to 15° and 0° respectively.

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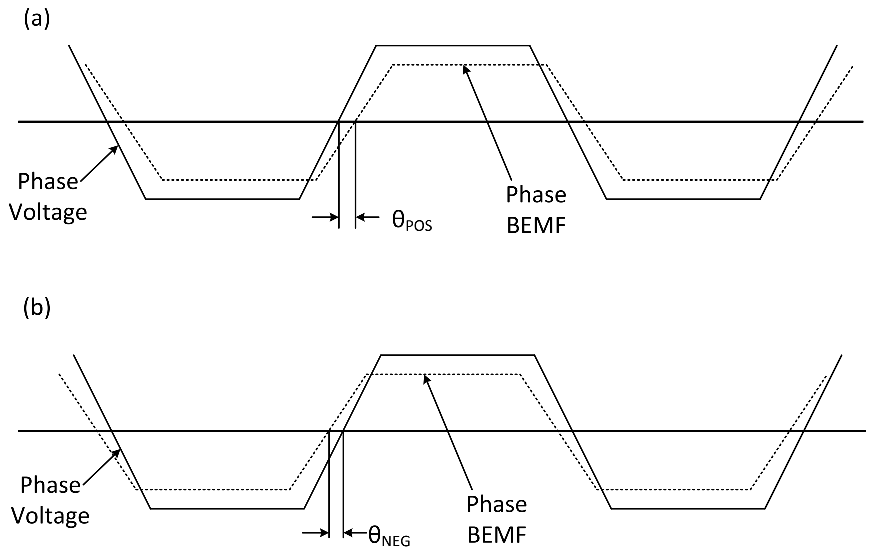

图 8-30. Positive and Negative Lead Angle Definition

8.3.11.4 Closed loop accelerate

To prevent sudden changes in the torque applied to the motor which could result in acoustic noise, the MCT8316A device provides the option of limiting the maximum rate at which the speed command can change. The closed loop acceleration rate parameter sets the maximum rate at which the speed command changes (shown in 图 8-31). In the MCT8316A, closed loop acceleration rate is configured through CL_ACC.

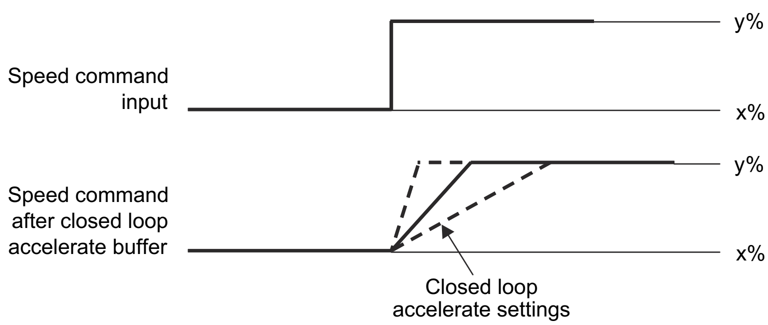

图 8-31. Closed loop accelerate

8.3.12 Speed Loop (Available only in MCT8316AV)

MCT8316A has a speed loop option which can be used to maintain constant speed under varying operating conditions. Speed loop is enabled by setting CLOSED_LOOP_MODE to 01b. K_p and K_i coefficients are configured through SPD_POWER_KP and SPD_POWER_KI. The output of speed loop (SPEED_PI_OUT) is used to generate the DUTY OUT (see 图 8-14). The PI controller output upper (V_{MAX}) and lower bound (V_{MIN}) saturation limits are configured through SPD_POWER_V_MAX and SPD_POWER_V_MIN respectively. When output of the speed loop saturates, the integrator is disabled to prevent integral wind-up. The speed loop PI controller is as in 图 8-32.

SPEED_REF is derived from duty command input and maximum motor speed (MAX_SPEED) configured by user (see 方程式 6). In speed loop mode, minimum SPEED_REF is set by MIN_DUTY * MAX_SPEED.

$$\text{SPEED\_REF} = \text{DUTY CMD} * \text{MAX\_SPEED} \tag{6}$$

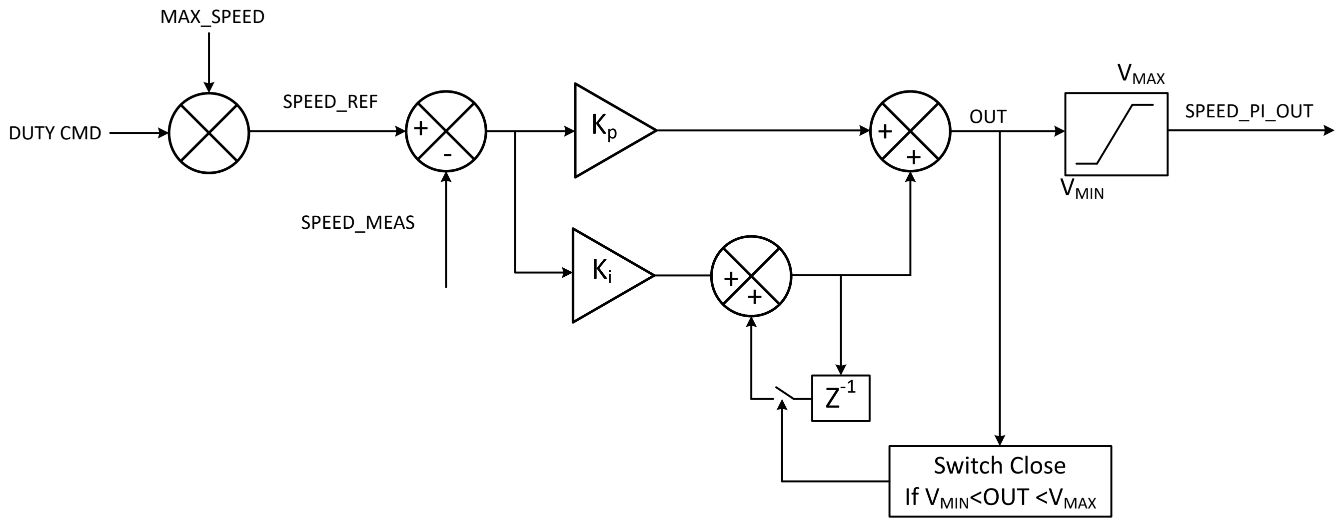

图 8-32. Speed Loop

8.3.13 Input Power Regulation (Available only in MCT8316AV)

MCT8316A provides an option of regulating the (input) power instead of motor speed - this input power regulation can be done in two modes, namely, closed loop power control and power limit control. Input power regulation (instead of motor speed) mode is selected by setting CLOSED_LOOP_MODE to 10b. This should be accompanied by setting CONST_POWER_MODE to 01b for closed loop power control or to 10b for power limit control. In either of the power regulation modes, the maximum power that MCT8316A can draw from the DC input supply is set by MAX_POWER - the power reference (POWER_REF in 图 8-33) varies as function of the duty command input (DUTY CMD) and MAX_POWER as given by 方程式 7. The hysteresis band for the power reference is set by CONST_POWER_LIMIT_HYST. In both the power regulation modes, the minimum power reference is set by MIN_DUTY x MAX_POWER.

$$\text{POWER\_REF} = \text{DUTY CMD} \times \text{MAX\_POWER} \tag{7}$$

In both the power regulation modes, MCT8316A uses the same PI controller parameters as in the speed loop mode. K_p and K_i coefficients are configured through SPD_POWER_KP and SPD_POWER_KI. The PI controller output upper (V_{MAX}) and lower bound (V_{MIN}) saturation limits are configured through SPD_POWER_V_MAX and SPD_POWER_V_MIN respectively. The key difference between closed loop power control and power limit control is in the when the PI controller decides the DUTY OUT (see 图 8-14) applied to FETs. In closed loop power control, DUTY OUT is always equal to POWER_PI_OUT from the PI controller output in 图 8-33. However, in power limit control, the PI controller decides the DUTY OUT only if POWER_MEAS > POWER_REF + CONST_POWER_LIMIT_HYST. If POWER_MEAS < POWER_REF + CONST_POWER_LIMIT_HYST, the PI controller is not used and DUTY OUT is equal to DUTY CMD. Essentially, in closed loop power control, input power is always actively regulated to POWER_REF whereas, in power limit control, input power is only limited to POWER_REF and not actively regulated to POWER_REF. When output of the power PI loop saturates, the integrator is disabled to prevent integral wind-up.

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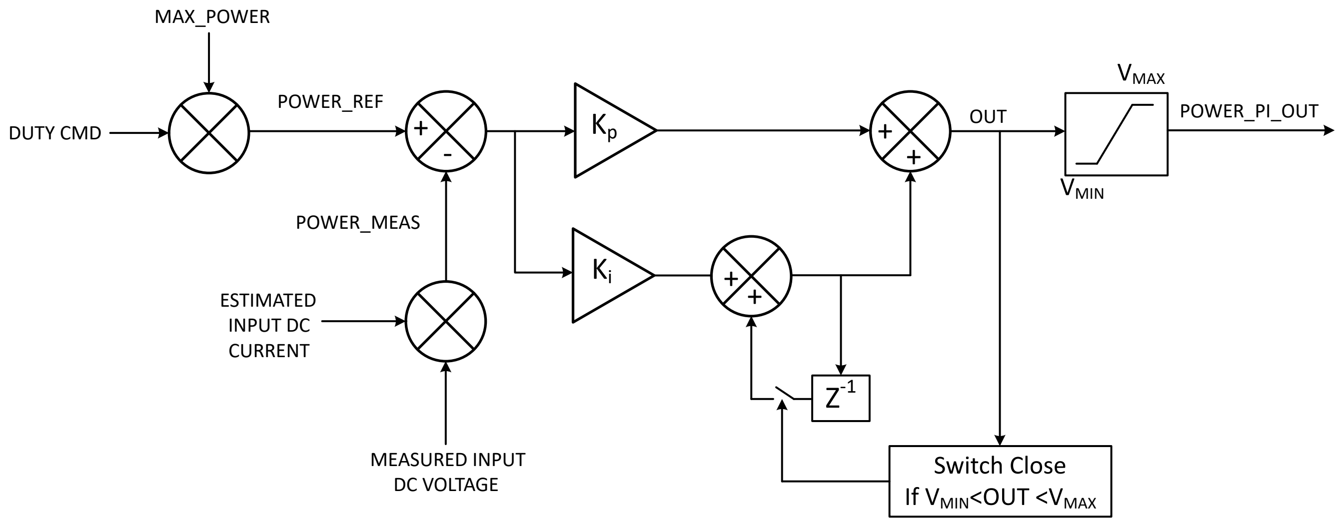

图 8-33. Power Regulation

8.3.14 Anti-Voltage Surge (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive and mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the V_M voltage surges. The AVS feature works to prevent this voltage surge on V_M and can be enabled by setting AVS_EN to 1b. AVS can be disabled by setting AVS_EN to 0b. When AVS is disabled, the deceleration rate is configured through CL_DEC_CONFIG

8.3.15 Output PWM Switching Frequency

MCT8316A provides the option to configure the output PWM switching frequency of the MOSFETs through PWM_FREQ_OUT. PWM_FREQ_OUT has range of 5-100 kHz. In order to select optimal output PWM switching frequency, user has to make tradeoff between the current ripple and the switching losses. Generally, motors having lower L/R ratio require higher PWM switching frequency to reduce current ripple.

8.3.16 Fast Start-up (< 50 ms)

MCT8316A has the capability to accelerate a motor from 0 to 100% speed within 50ms. This will only work on low inertia motors which are capable of this level of acceleration. In order to achieve fast start-up, the commutation instant detection needs to be configured to hybrid mode by setting INTEG_ZC_METHOD to 1b. In the hybrid mode, the commutation instant is determined by using back-EMF integration at low-medium speeds and by using built-in comparators (BEMF zero crossing) at higher speeds. MCT8316A automatically transitions between back-EMF integration and comparator based commutation depending on the motor speed as shown in 图 8-34. The duty cycles for commutation method transition at lower speeds are directly configured by INTEG_DUTY_THR_LOW and INTEG_DUTY_THR_HIGH and at higher speeds are indirectly configured by INTEG_CYC_THR_LOW and INTEG_CYC_THR_HIGH. These duty cycles should be configured to provide a sufficient hysteresis band to avoid repeated commutation method transitions near threshold duty cycles. The BEMF threshold values used to determine the commutation instant in the back-EMF integration method are configured by BEMF_THRESHOLD1 and BEMF_THRESHOLD2.

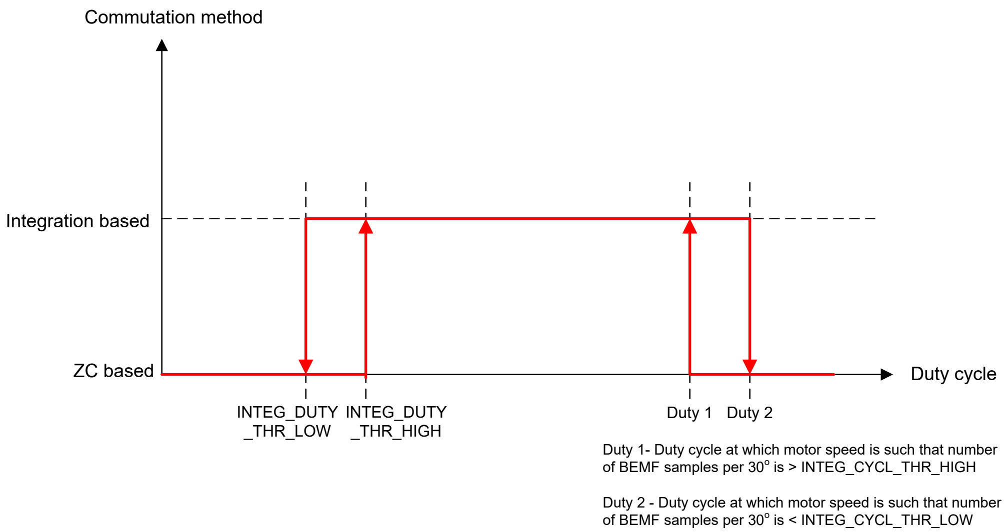

图 8-34. Commutation Method Transition

8.3.16.1 BEMF Threshold

图 8-35 shows the three-phase voltages during 120° trapezoidal operation. It is seen that one of the phases will always be floating within a 60° commuation interval and MCT8316A integrates this floating phase voltage (which denotes the motor back-EMF) in the back-EMF integration method to detect the next commutation instant. The floating phase voltage can either be increasing or decreasing and the algorithm starts the integration after the zero cross detection in order to eliminate integration errors due to variable degauss time. The floating phase voltage is periodically sampled (after zero cross) and added (discrete form of integration). BEMF threshold (BEMF_THRESHOLD1 and BEMF_THRESHOLD2) value is set such that the integral value of the floating phase voltage crosses the BEMF_THRESHOLD1 or BEMF_THRESHOLD2 value at (or very near) to the commutation instant. BEMF_THRESHOLD1 is the threshold for rising floating phase voltage and BEMF_THRESHOLD2 is the threshold for falling floating phase voltage. If BEMF_THRESHOLD2 is set to 0, then BEMF_THRESHOLD1 is used as the threshold for both rising and falling floating phase voltage.

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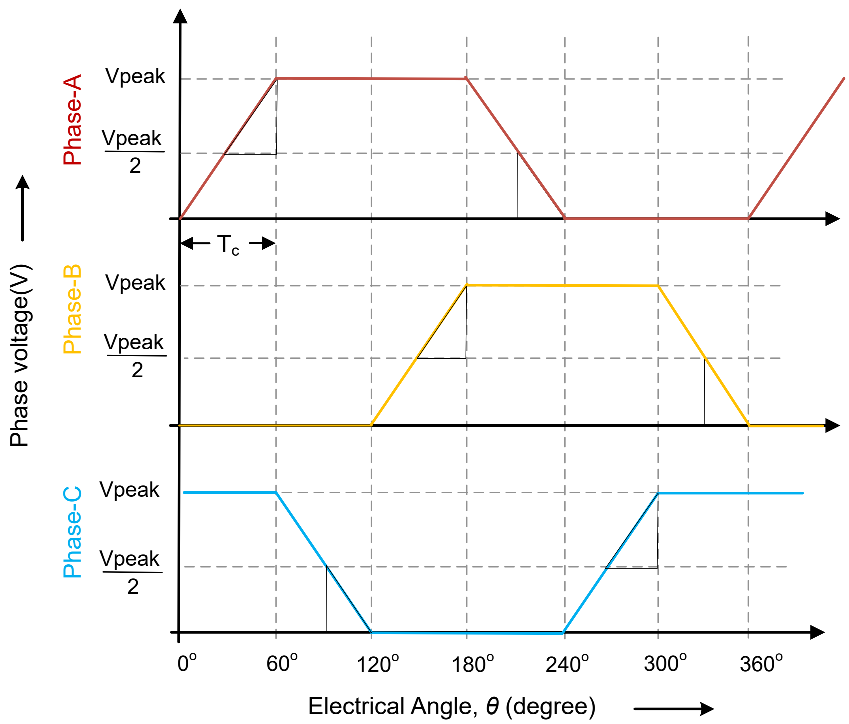


图 8-35. Back-EMF integration using floating phase voltage

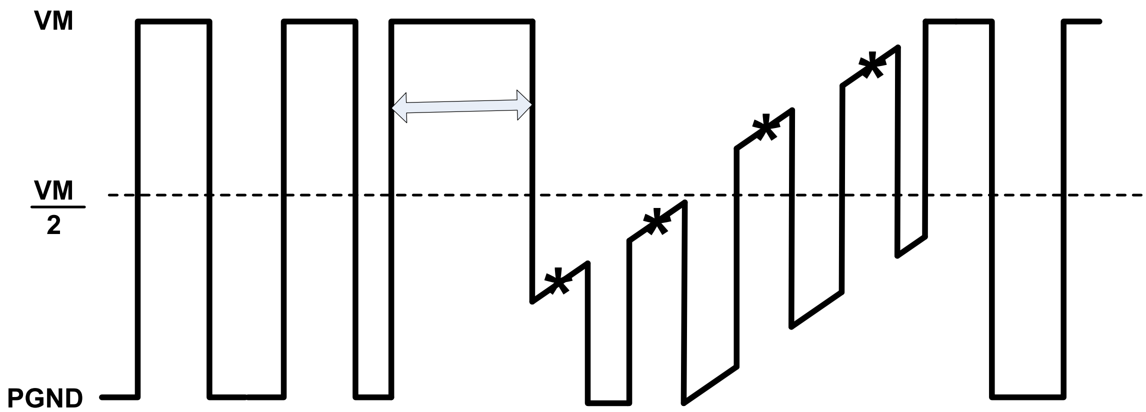
In 图 8-35 , Vpeak is the peak-peak value of the back-EMF , Vpeak/2 denotes the zero cross of the back-EMF and Tc is the commutation interval or time period of the 60° window. The highlighted triangle in each 60° window is the integral value of back-EMF used by the algorithm to determine the commutation instant. This integral value, which can be approximated as the area of the highlighted triangle, is given by 方程式 8.

$$(½)* (Vpeak/2) * Tc/2 \tag{8}$$

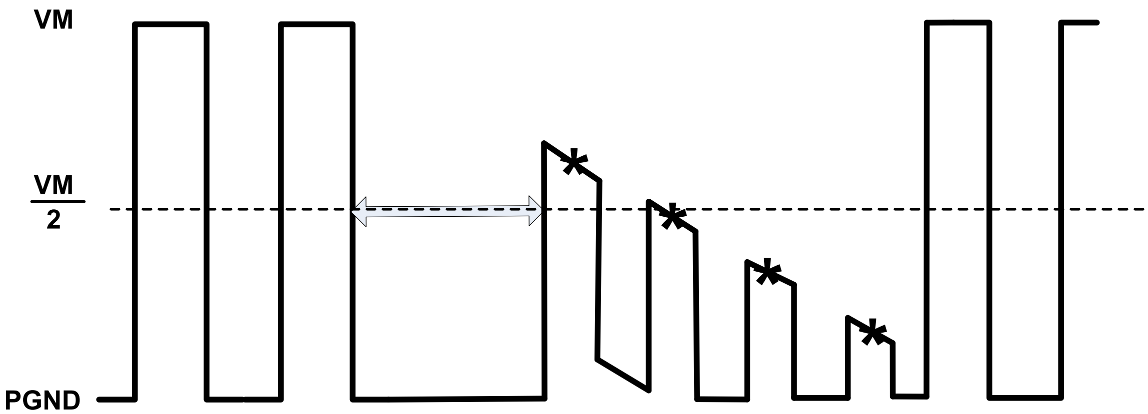
See for an example application on setting the BEMF threshold.

8.3.16.2 Dynamic Degauss

In MCT8316A, the degauss time can be dynamically computed after the commutation for a precise detection of the zero crossing instant. This is done by enabling the dynamic degauss feature (DYN_DEGAUSS_EN is set to 1b). This feature allows the motor control algorithm to capture the zero crossing instant after the outgoing (floating) phase voltage is completely settled; that is, when the outgoing phase current has decayed to zero and the outgoing (floating) phase voltage is not clamped (to either VM or PGND) and represents the true back-EMF. This accurate measurement of zero cross instant allows fast acceleration of the motors (< 50ms) using MCT8316A.



Degauss time(shown by double-sided arrow) after commutation during which the outgoing(floating) phase voltage is clamped to VM(by negative outgoing phase current) during increasing back-EMF; sampling of back-EMF(denoted by *) should start after degauss time is over for accurate zero cross instant detection



Degauss time(shown by double-sided arrow) after commutation during which the outgoing(floating) phase voltage is clamped to PGND(by positive outgoing phase current) during decreasing back-EMF; sampling of back-EMF(denoted by *) should start after degauss time is over for accurate zero cross instant detection

图 8-36. Degauss Time

8.3.17 Fast Deceleration

MCT8316A has the capability to decelerate a motor quickly (100% to 10% speed reduction within tens of ms) without pumping energy back into the input DC supply using the fast deceleration feature in conjunction with the AVS feature. The fast deceleration feature can be enabled by setting FAST_DECEL_EN to 1b; AVS_EN should be set to 1b to prevent energy pump-back into the input DC supply. This combination enables a linear braking effect resulting in a fast and smooth speed reduction without energy pump-back into the DC input supply. This feature combination can also be used during reverse drive (see Reverse Drive) or motor stop (see Active Spin-Down) to reduce the motor speed quickly without energy pump-back into the DC input supply.

The deceleration time can be controlled by appropriately configuring the current limit during deceleration, FAST_DECEL_CURR_LIM. A higher current limit results in a lower deceleration time and vice-versa. A higher than necessary current limit setting may result in motor stall faults, at low target speeds, due to excessive braking torque. This can also lead to higher losses in MCT8316A, especially in repeated acceleration-deceleration cycles. Therefore, the FAST_DECEL_CURR_LIM should be chosen appropriately, so as to decelerate within the required time without resulting in stall faults or overheating.

FAST_BRK_DELTA is used to configure the target speed hysteresis band to exit the fast deceleration mode and re-enter motoring mode when motor reaches the target speed. For example, if FAST_BRK_DELTA is set to 1%, the fast deceleration is deemed complete when motor speed reaches within 1% of target speed. Setting a higher

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value for FAST_BRK_DELTA may eliminate motor stall faults, especially when high FAST_DECEL_CURR_LIM values are used. Setting a higher value for FAST_BRK_DETLA will also result in higher speed error between target speed and motor speed at the end of deceleration mode - motor will eventually reach the target speed once motoring mode is resumed. FAST_DECEL_CURR_LIM and FAST_BRK_DELTA should be configured in tandem to optimize between lower deceleration time and reliable (no stall faults) deceleration profile.

FAST_DEC_DUTY_THR configures the speed below which fast deceleration will be implemented. For example, if FAST_DEC_DUTY_THR is set to 70%, any deceleration from speeds above 70% will not use fast deceleration until the speed goes below 70%. FAST_DEC_DUTY_WIN is used to set the minimum deceleration window (initial speed - target speed) below which fast deceleration will not be implemented. For example, if FAST_DEC_DUTY_WIN is set to 15% and 50%->40% deceleration command is received, fast deceleration is not used to reduce the speed from 50% to 40% since the deceleration window (10%) is smaller than FAST_DEC_DUTY_WIN.

MCT8316A provides a dynamic current limit option during fast deceleration to improve the stability of fast deceleration when braking to very low speeds; using this feature the current limit during fast deceleration can be reduced as the motor speed decreases. This feature can be enabled by setting DYNAMIC_BRK_CURR to 1b. The current limit at the start of fast deceleration (at FAST_DEC_DUTY_THR) is configured by FAST_DECEL_CURR_LIM and the current limit at zero speed is configured by DYN_BRK_CURR_LOW_LIM; the current limit during fast deceleration varies linearly with speed between these two operating points when dynamic current limit is enabled. If dynamic current limit is disabled, current limit during fast deceleration stays constant and is configured by FAST_DECEL_CURR_LIM.

8.3.18 Active Demagnetization

MCT8316A has smart rectification features (active demagnetization) which decreases power losses in the device by reducing diode conduction losses. When this feature is enabled, the device automatically turns ON the corresponding MOSFET whenever it detects diode conduction. This feature can be enabled by configuring EN_ASR.

备注
EN_ASR needs to be set to 1b to enable active demagnetization.

The MCT8316A device includes a high-side (AD_HS) and low-side (AD_LS) comparator which detects the negative flow of current in the device on each half-bridge. The AD_HS comparator compares the sense-FET output with the supply voltage (VM) threshold, whereas the AD_LS compatator compares with the ground (0-V) threshold. Depending upon the flow of current from OUTx to VM or PGND to OUTx, the AD_HS or the AD_LS comparator trips. These comparator outputs provide a reference point for the operation of active demagnetization feature.

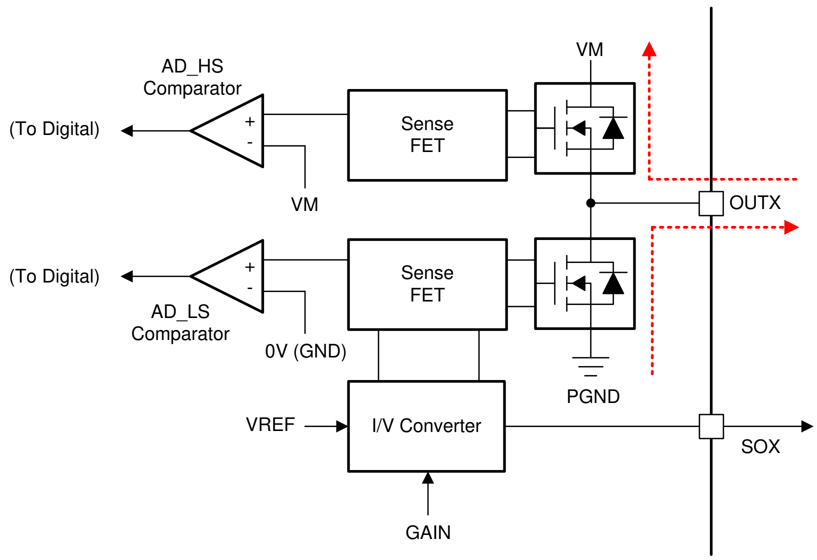

图 8-37. Active Demagnetization Operation

8.3.18.1 Active Demagnetization in action

图 8-38 shows the operation of active demagnetization during the BLDC motor commutation. As shown in 图 8-38 (a), the current is flowing from HA to LC in one commutation state. During the commutation change over as shown in 图 8-38 (b), the HB FET is turned ON (and HA FET is turned OFF), and the commutation current (due to motor inductance) in OUTA flows through the body diode of LA. This results in a higher diode loss depending on the commutation current. This commutation loss is reduced by turning on the LA FET for the commutation time as shown in 图 8-38 (c).

Similarly, the active demagnetization operation of a high-side FET is realized in 图 8-38 (d), (e) and (f).

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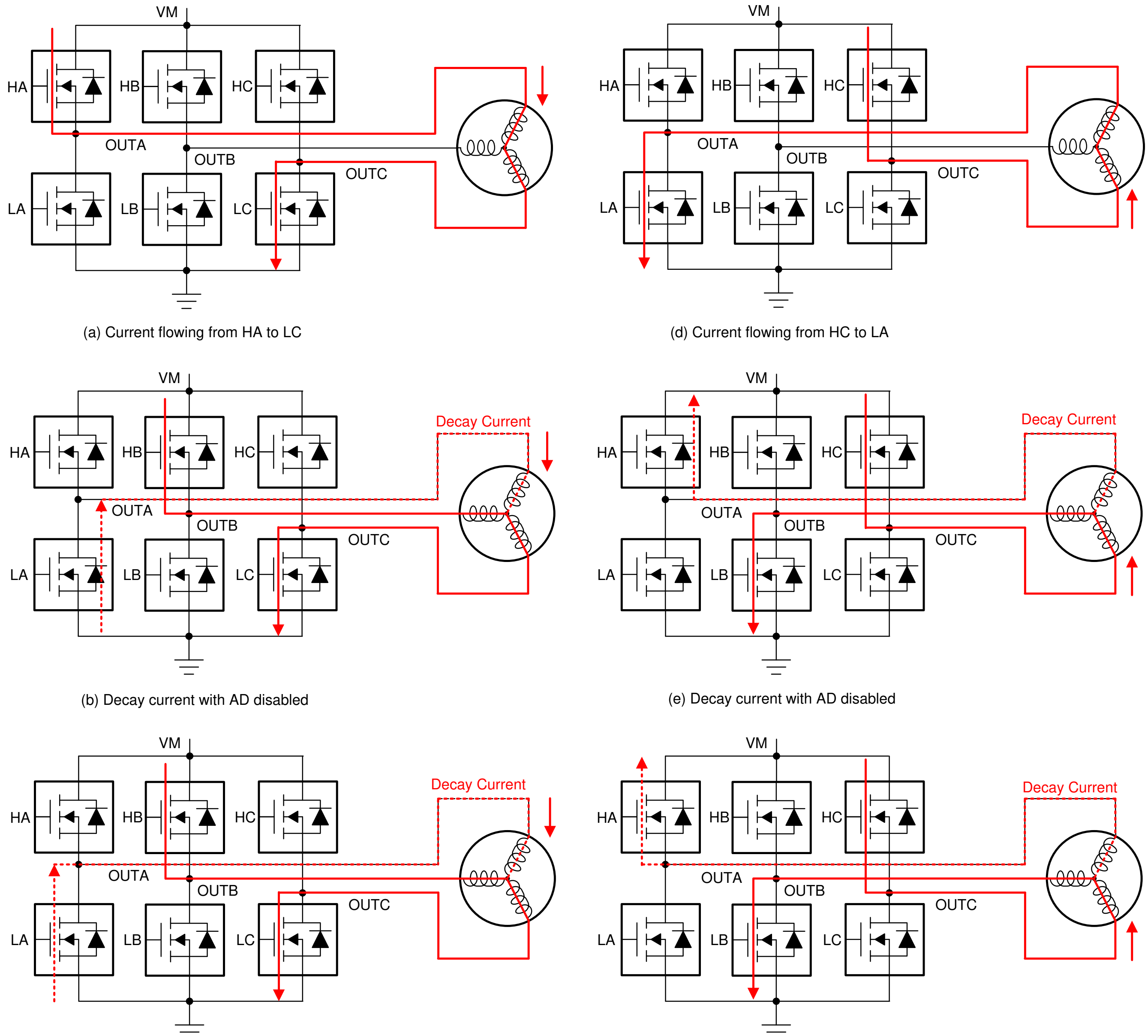


(a) Current flowing from HA to LC

(d) Current flowing from HC to LA

(b) Decay current with AD disabled

(e) Decay current with AD disabled

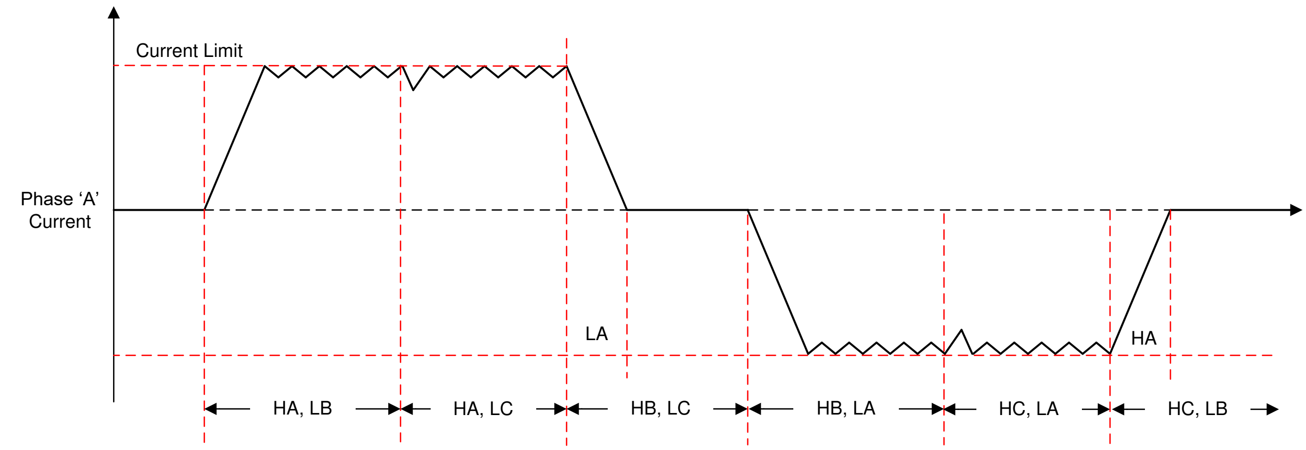
(c) Decay current with AD enabled

(f) Decay current with AD enabled

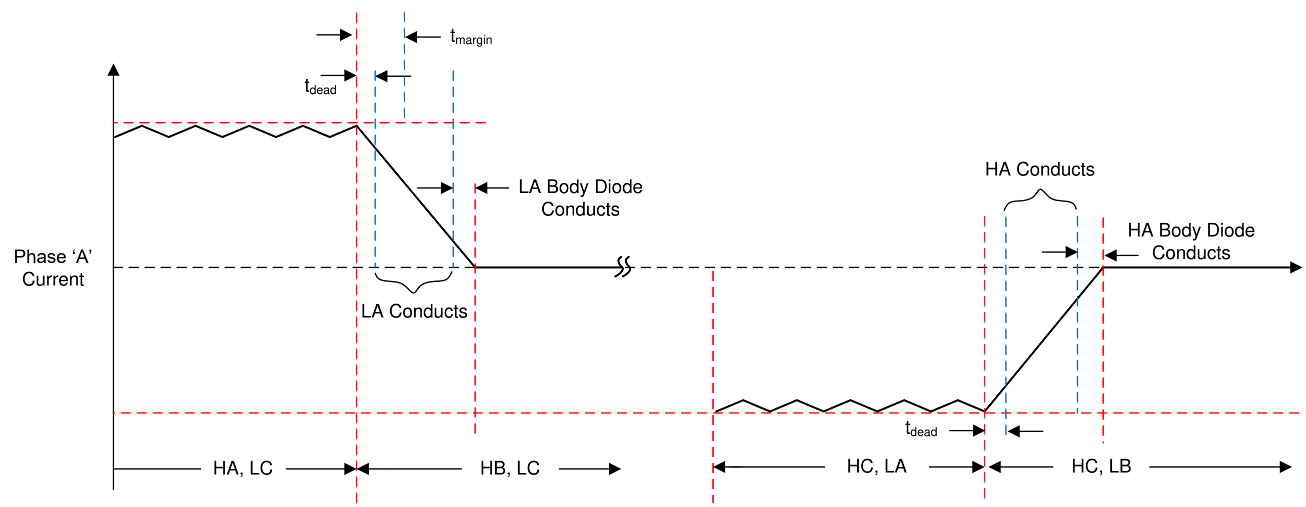
图 8-38. Active Demagnetization in BLDC Motor Commutation

图 8-39 (a) shows the BLDC motor phase current waveforms with Active Demagnetization with trapezoidal commutation. This figure shows the operation of various switches in a single commutation cycle.

图 8-39 (b) shows the zoomed waveform of commutation cycle.



(a) Commutation current of Phase "A"



(b) Zoomed waveform of Active Demagnetization

图 8-39. Current Waveforms with Active Demagnetization

8.3.19 Motor Stop Options

The MCT8316A provides different options for stopping the motor which can be configured by MTR_STOP.

8.3.19.1 Coast (Hi-Z) Mode

Coast (Hi-Z) mode is configured by setting MTR_STOP to 000b. When motor stop command is received, the MCT8316A will transition into a high impedance (Hi-Z) state by turning off all MOSFETs. When the MCT8316A transitions from driving the motor into a Hi-Z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the body diodes in the MOSFET output stage (see example 图 8-40).

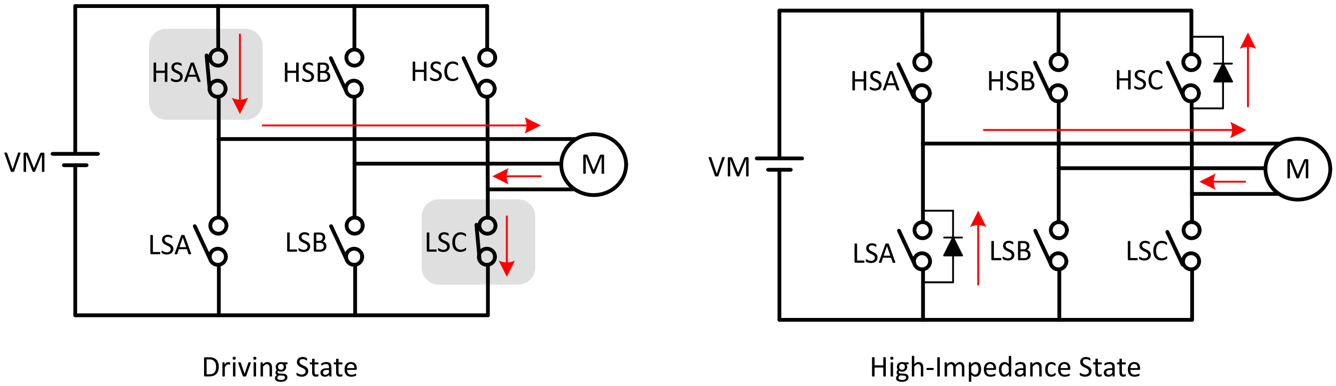


图 8-40. Coast (Hi-Z) Mode

In this example, current is applied to the motor through the high-side phase-A MOSFET (HSA) and returned through the low-side phase-C MOSFET (LSC). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs LSA and HSC.

8.3.19.2 Recirculation Mode

Recirculation mode is configured by setting MTR_STOP to 001b. In order to prevent the inductive energy from returning to DC input supply during motor stop, the MCT8316A allows current to circulate within the MOSFETs by selectively turning OFF some of the active (ON) MOSFETs for a certain time (auto calculated recirculation time to allow the inductive current to decay to zero) before transitioning into Hi-Z by turning OFF the remaining MOSFETs.

If high-side modulation was active, prior to motor stop command, then the high-side MOSFET is turned OFF on receiving motor stop command and the current recirculation takes place through low-side MOSFET (see example 图 8-41). Once the recirculation time lapses, the low-side MOSFET also turns OFF and all MOSFETs are in Hi-Z state.

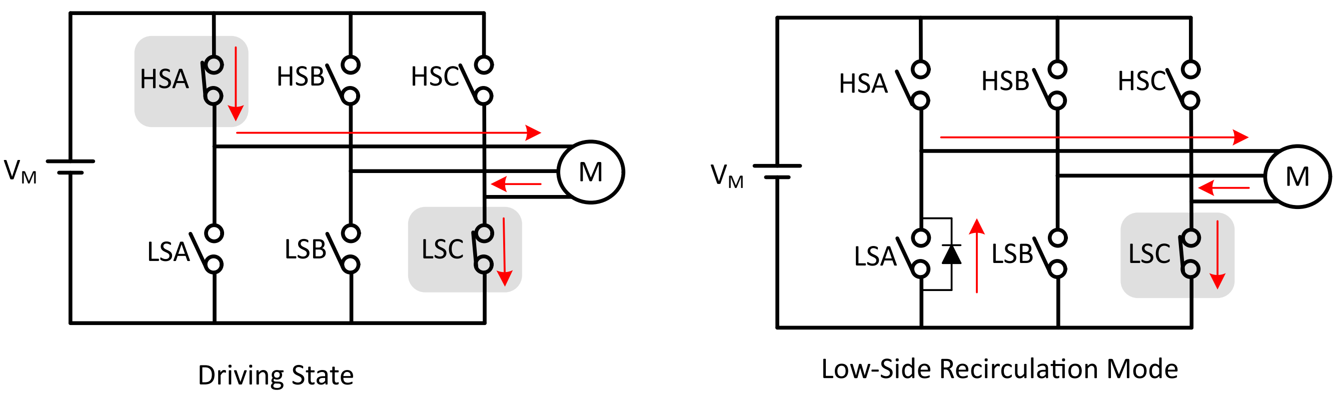


图 8-41. Low-Side Recirculation

If low-side modulation was active, prior to motor stop command, then the low-side MOSFET is turned OFF on receiving motor stop command and the current recirculation takes place through high-side MOSFET (see example 图 8-42). Once the recirculation time lapses, the high-side MOSFET also turns OFF and all MOSFETs are in Hi-Z state

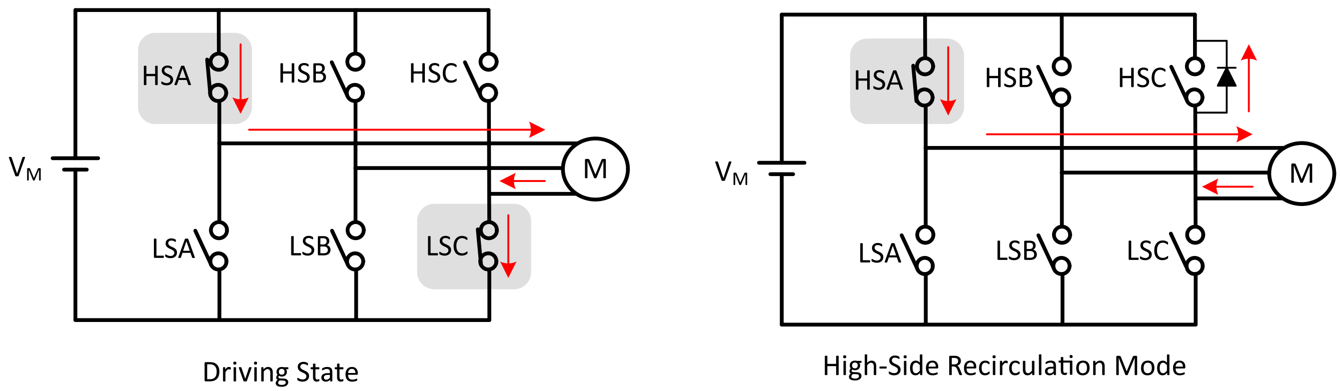


图 8-42. High-Side Recirculation

8.3.19.3 Low-Side Braking

Low-side braking mode is configured by setting MTR_STOP to 010b. When a motor stop command is received, the output speed is reduced to a value defined by ACT_SPIN_BRK_THR prior to turning all low-side MOSFETs ON (see example 图 8-43) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below ACT_SPIN_BRK_THR prior to receiving stop command, then the MCT8316A transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCT8316A transitions into the Hi-Z state by turning OFF all MOSFETs.

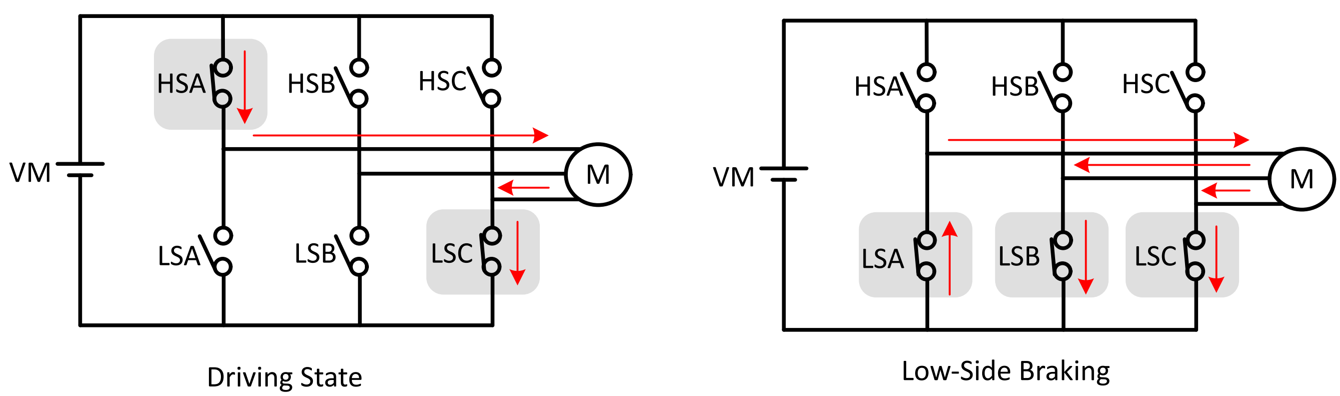


图 8-43. Low-Side Braking

The MCT8316A can also enter low-side braking through BRAKE pin input. When BRAKE pin is pulled to HIGH state, the output speed is reduced to a value defined by BRAKE_DUTY_THRESHOLD prior to turning all low-side MOSFETs ON. In this case, MCT8316A stays in low-side brake state till BRAKE pin changes to LOW state.

8.3.19.4 High-Side Braking

High-side braking mode is configured by setting MTR_STOP to 011b. When a motor stop command is received, the output speed is reduced to a value defined by ACT_SPIN_BRK_THR prior to turning all high-side MOSFETs ON (see example 图 8-44) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below ACT_SPIN_BRK_THR prior to receiving stop command, then the MCT8316A transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCT8316A transitions into Hi-Z state by turning OFF all MOSFETs.

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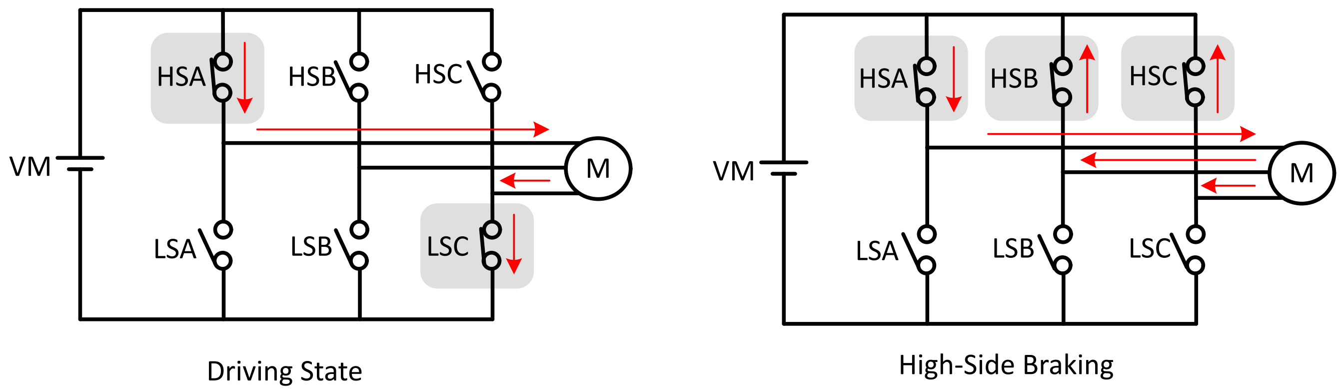

图 8-44. High-Side Braking

8.3.19.5 Active Spin-Down

Active spin down mode is configured by setting MTR_STOP to 100b. When motor stop command is received, MCT8316A reduces duty cycle to ACT_SPIN_BRK_THR and then transitions to Hi-Z state by turning all MOSFETs OFF. The advantage of this mode is that by reducing duty cycle, the motor is decelerated to a lower speed thereby reducing the phase currents before entering Hi-Z. Now, when motor transitions into Hi-Z state, the energy transfer to power supply is reduced. The threshold ACT_SPIN_BRK_THR needs to configured high enough for MCT8316A to not lose synchronization with the motor.

8.3.20 FG Configuration

The MCT8316A provides information about the motor speed through the Frequency Generate (FG) pin. In MCT8316A, the FG pin output is configured through FG_CONFIG. When FG_CONFIG is configured to 1b, the FG output is active as long as the MCT8316A is driving the motor. When FG_CONFIG is configured to 0b, the MCT8316A provides an FG output until the motor back-EMF falls below FG_BEMF_THR.

8.3.20.1 FG Output Frequency

The FG output frequency can be configured by FG_DIV_FACTOR. In MCT8316, FG toggles once every commutation cycle if FG_DIV_FACTOR is set to 0000b. Many applications require the FG output to provide a pulse for every mechanical rotation of the motor. Different FG_DIV_FACTOR configurations can accomplish this for 2-pole up to 30-pole motors.

图 8-45 shows the FG output when MCT8316A has been configured to provide FG pulses once every commutation cycle (electrical cycle/3), once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.

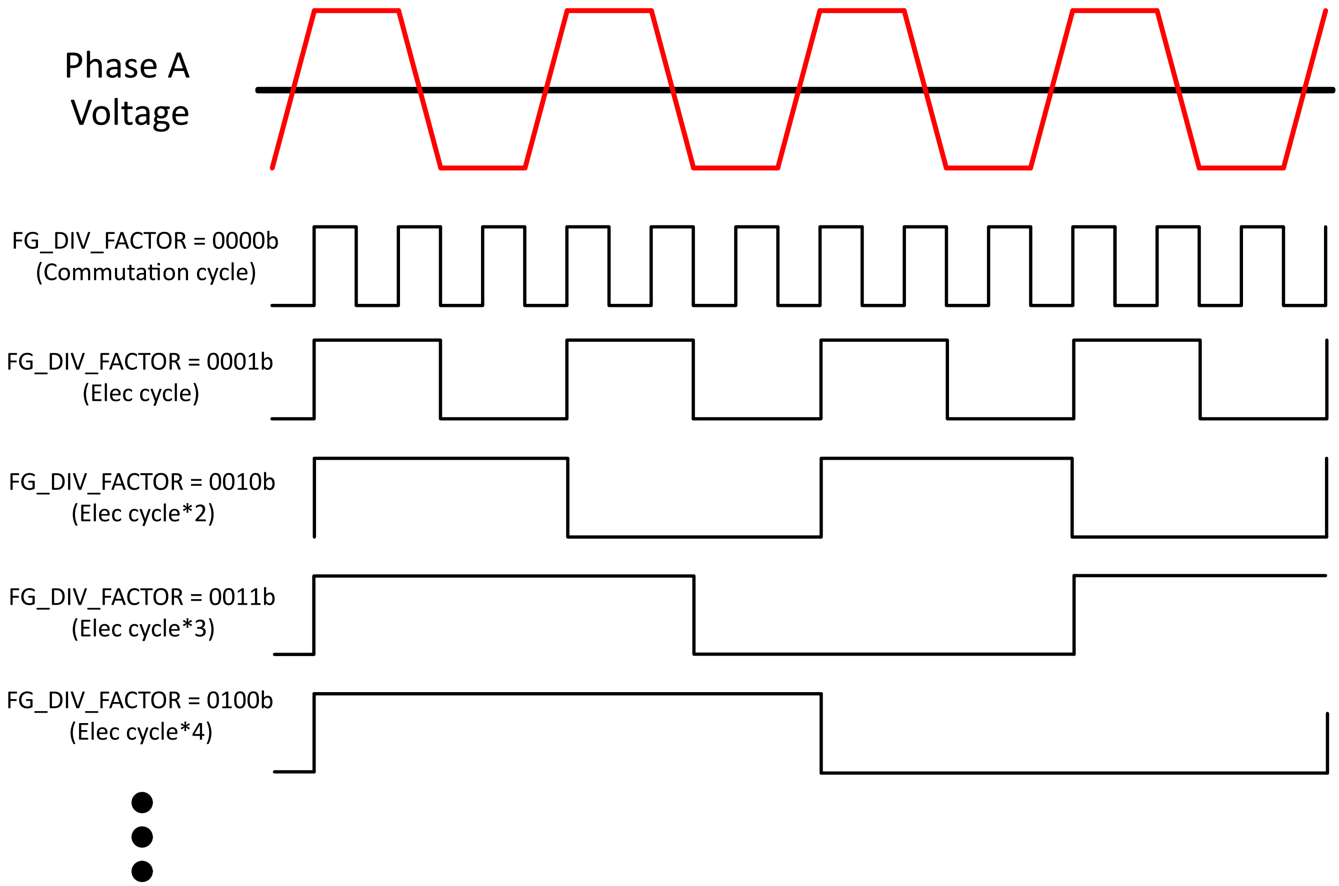

图 8-45. FG Frequency Divider

8.3.20.2 FG Open-Loop and Lock Behavior

During closed loop operation, the driving speed (FG output frequency) and the actual motor speed are synchronized. During open-loop operation, however, FG may not reflect the actual motor speed. During motor-lock condition, the FG output is driven high.

The MCT8316A provides three options for controlling the FG output during open loop, as shown in 图 8-46. The selection of these options is configured through FG_SEL.

If FG_SEL is set to,

- 00b: When in open loop, the FG output is based on the driving frequency.
- 01b: When in open loop, the FG output will be driven high.
- 10b: The FG output will reflect the driving frequency during open loop operation in the first motor start-up cycle after power-on, sleep/standby; FG will be held high during open loop operation in subsequent start-up cycles.

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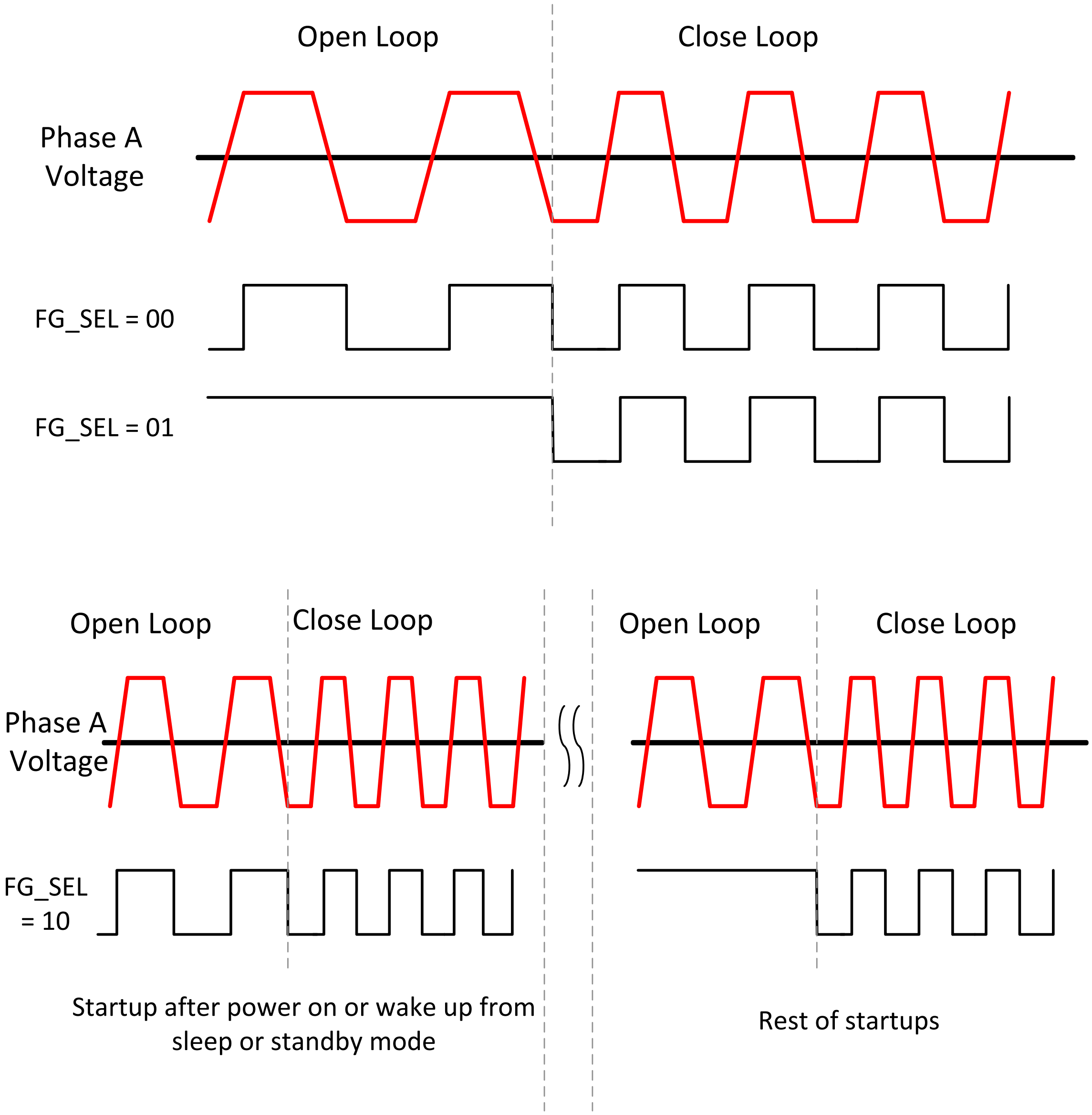

图 8-46. FG Behavior During Open Loop

8.3.21 Protections

The MCT8316A is protected from a host of fault events including motor lock, VM undervoltage, AVDD undervoltage, buck undervoltage, charge pump undervoltage, overtemperature and overcurrent events. 表 8-18 summarizes the response, recovery modes, power stage status, reporting mechanism for different faults.

表 8-18. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (NPOR)	$V_{VM} < V_{UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO}$
AVDD undervoltage (NPOR)	$V_{AVDD} < V_{AVDD\_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_UV}$
Buck undervoltage (BUCK_UV)	$V_{FB\_BK} < V_{BK\_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{FB\_BK} > V_{BK\_UV}$
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPUV}$	—	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$

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表 8-18. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
OverVoltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_EN = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_EN = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$
Overcurrent Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		OCP_MODE = 01b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	GATE_DRIVER_FAULT_STATUS register	Active	Active	No action
		OCP_MODE = 11b	None	Active	Active	No action
Buck Overcurrent Protection (BUCK_OCP)	$I_{BK} > I_{BK\_OCP}$	—	—	Hi-Z	Disabled	Retry: t_{RETRY}
Motor Lock (MTR_LCK)	Motor lock: Abnormal Speed; No Motor Lock; Loss of Sync	MTR_LCK_MODE = 0000b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0001b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	High side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0011b	nFAULT and CONTROLLER_FAULT_STATUS register	Low side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0100b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0101b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0110b	nFAULT and CONTROLLER_FAULT_STATUS register	High side brake	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0111b	nFAULT and CONTROLLER_FAULT_STATUS register	Low side brake	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 1000b	CONTROLLER_FAULT_STATUS register	Active	Active	No action
		MTR_LCK_MODE = 1xx1b	None	Active	Active	No action

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表 8-18. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
Cycle by Cycle Current Limit (CBC_ILIMIT)	V_{SOX} > CBC_ILIMIT	CBC_ILIMIT_MODE = 0000b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation	Active	Automatic: Next PWM cycle
		CBC_ILIMIT_MODE = 0001b	None	Recirculation	Active	Automatic: Next PWM cycle
		CBC_ILIMIT_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation	Active	Automatic: V_{SOX} < ILIMIT
		CBC_ILIMIT_MODE = 0011b	None	Recirculation	Active	Automatic: V_{SOX} < ILIMIT
		CBC_ILIMIT_MODE = 0100b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation	Active	Automatic: PWM cycle > CBC_RETRY_PWM_CYC
		CBC_ILIMIT_MODE = 0101b	None	Recirculation	Active	Automatic: PWM cycle > CBC_RETRY_PWM_CYC
		CBC_ILIMIT_MODE= 0110b	CONTROLLER_FAULT_STATUS register	Active	Active	No action
		CBC_ILIMIT_MODE = 0111b, 1xxxb	None	Active	Active	No action
Lock-Detection Current Limit (LOCK_ILIMIT)	V_{SOX} > LOCK_ILIMIT	LOCK_ILIMIT_MODE = 0000b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0001b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0011b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0100b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0101b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0110b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0111b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE= 1000b	CONTROLLER_FAULT_STATUS register	Active	Active	No action
		LOCK_ILIMIT_MODE = 1xx1b	None	Active	Active	No action
IPD Timeout Fault (IPD_T1_FAULT and IPD_T2_FAULT)	IPD TIME > 500ms (approx), during IPD current ramp up or ramp down	—	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
IP Frequency Fault (IPD_FREQ_FAULT)	IPD pulse before the current decay in previous IPD	—	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	None	Active	Active	No action
		OTW_REP = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	Automatic: $T_J < T_{OTW} - T_{OTW\_HYS}$ CLR_FLT

表 8-18. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
Thermal shutdown (TSD)	$T_J > T_{TSD}$	—	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Automatic: $T_J < T_{TSD} - T_{TSD\_HYS}$ CLR_FLT

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8.3.21.1 VM Supply Undervoltage Lockout

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all the integrated FETs, driver charge-pump and digital logic are disabled as shown in 图 8-47. MCT8316A goes into reset state whenever VM UVLO event occurs.

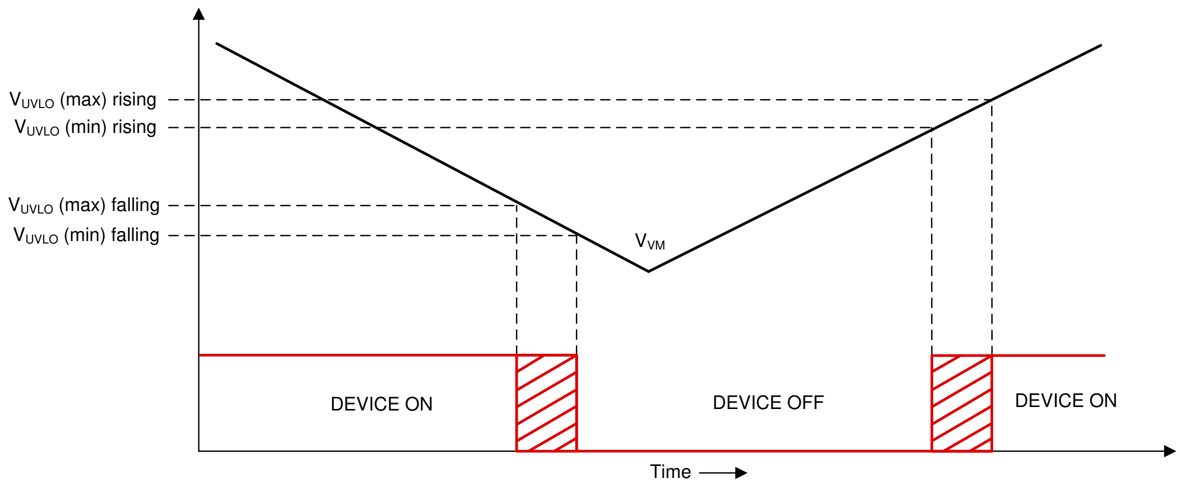

图 8-47. VM Supply Undervoltage Lockout

8.3.21.2 AVDD Undervoltage Lockout (AVDD_UV)

If at any time the voltage on the AVDD pin falls lower than the V_{AVDD_UV} threshold, all the integrated FETs, driver charge-pump and digital logic controller are disabled. Since internal circuitry in MCT8316A is powered through the AVDD regulator, MCT8316A goes into reset state whenever AVDD UV event occurs.

8.3.21.3 BUCK Undervoltage Lockout (BUCK_UV)

If at any time the input supply voltage on the FB_BK pin falls lower than the V_{BK_UVLO} threshold, both the high-side and low-side MOSFETs of the buck regulator are disabled . Since internal circuitry in MCT8316A is powered through the buck regulator,MCT8316A goes into reset state whenever buck UV event occurs.

8.3.21.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT and VCP_UV bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The VCP_UV bit stays set until cleared through the CLR_FLT bit.

8.3.21.5 Overvoltage Protection (OVP)

If at any time input supply voltage on the VM pins rises higher lower than the V_{OVP} threshold voltage, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT and OVP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR_FLT bit. Setting the OVP_EN to 1b enables this protection feature.

The OVP threshold can be set to 20-V or 32-V based on the OVP_SEL bit.

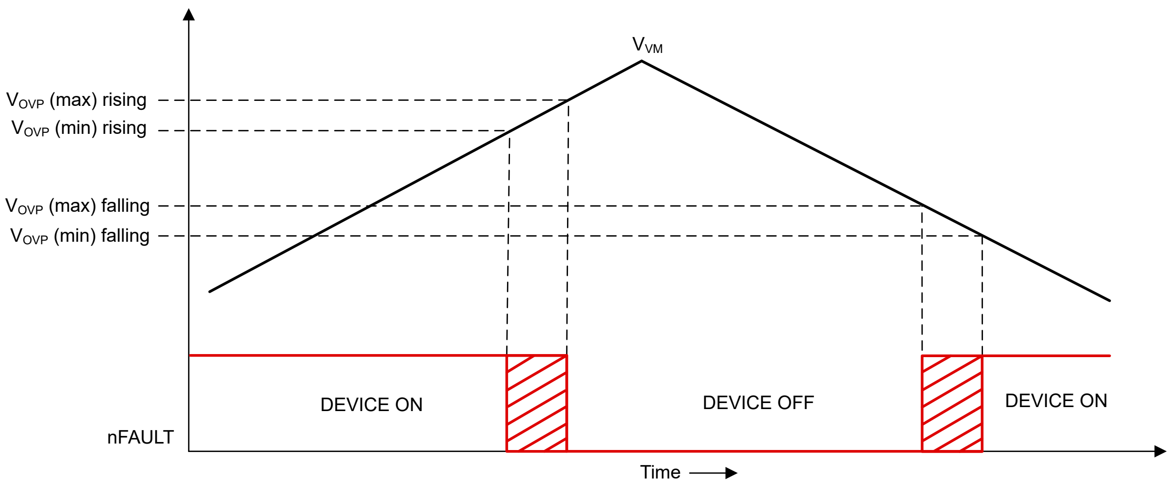

图 8-48. Over Voltage Protection

8.3.21.6 Overcurrent Protection (OCP)

MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and action is taken according to the OCP_MODE bit. The I_{OCP} threshold is set through the OCP_LVL, the t_{OCP_DEG} is set through the OCP_DEG and the OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only and OCP disabled.

8.3.21.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

When an OCP event happens in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear fault command is issued through the CLR_FLT bit.

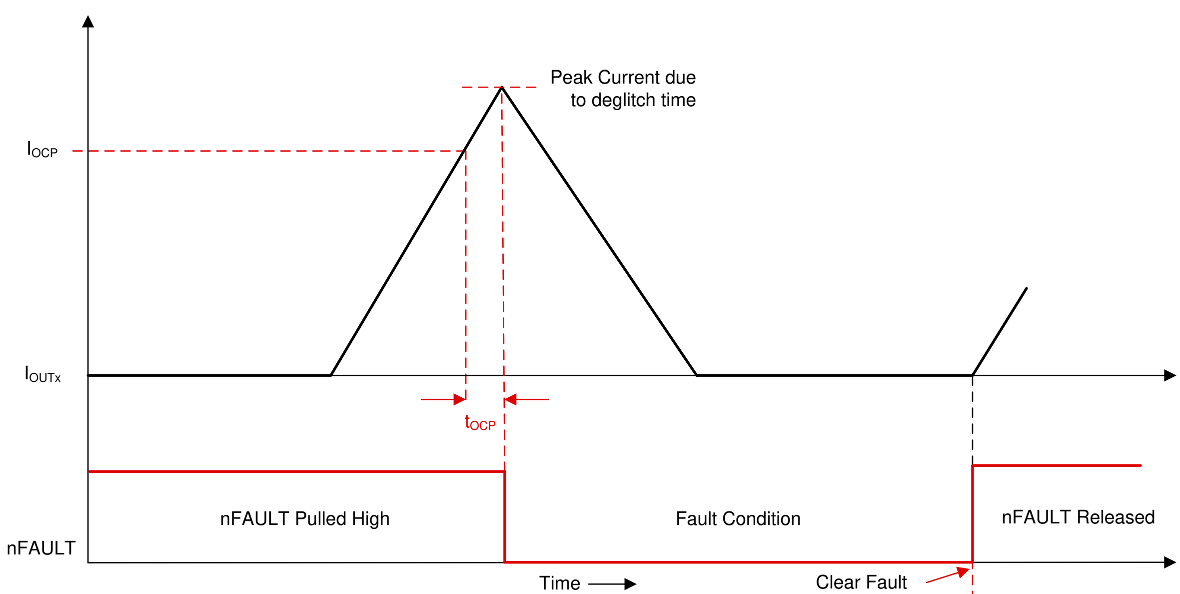

图 8-49. Overcurrent Protection - Latched Shutdown Mode

8.3.21.6.2 OCP Automatic Retry (OCP_MODE = 01b)

When an OCP event happens in this mode, all the FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the fault status registers. Normal

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operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} (OCP_RETRY) time elapses.The DRIVER_FAULT, OCP and corresponding FET's OCP bits are set to 1b until cleared through the CLR_FLT bit.

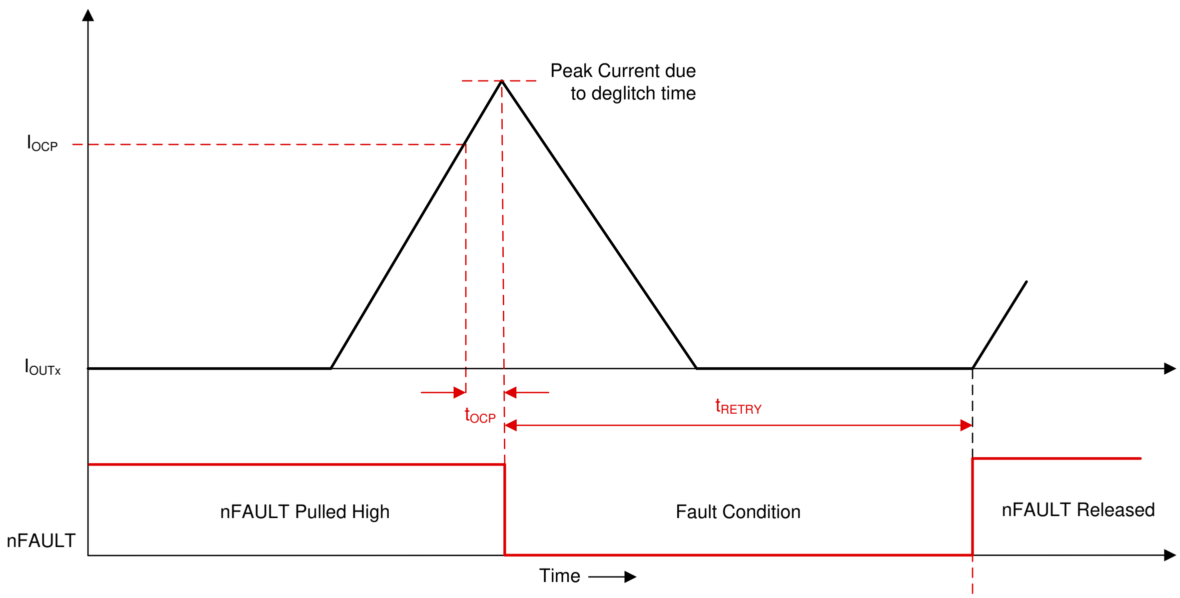

图 8-50. Overcurrent Protection - Automatic Retry Mode

8.3.21.6.3 OCP Report Only (OCP_MODE = 10b)

No protective action is taken when an OCP event happens in this mode. The overcurrent event is reported by setting the DRIVER_FAULT, OCP, and corresponding FET's OCP bits to 1b in the fault status registers. The device continues to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears when the OCP condition clears and a clear fault command is issued through the CLR_FLT bit.

8.3.21.6.4 OCP Disabled (OCP_MODE = 11b)

No action is taken when an OCP event happens in this mode.

8.3.21.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current through the high-side MOSFET exceeds the I_{BK_OCP} threshold for a time longer than the deglitch time (t_{OCP_DEG}), a buck OCP event is recognized. MCT8316A goes into reset state whenever buck OCP event occurs, since the internal circuitry in MCT8316A is powered from the buck regulator output.

8.3.21.8 Cycle-by-Cycle (CBC) Current Limit (CBC_ILIMIT)

Cycle-by-cycle (CBC) current limit provides a means of controlling the amount of current delivered to the motor. This is useful when the system must limit the amount of current pulled from the power supply during motor operation. The CBC current limit limits the current applied to the motor from exceeding the configured threshold. CBC current limit functionality is achieved by connecting the output of current sense amplifier V_{SOX} to a hardware comparator. If the voltage at output of current sense amplifier exceeds the CBC_ILIMIT threshold, a CBC_ILIMIT event is recognized and action is taken according to CBC_ILIMIT_MODE. Total delay in reaction to this event is dependent on the current sense amplifier gain and the comparator delay. CBC current limit in closed loop is set through CBC_ILIMIT while configuration of OL_ILIMIT_CONFIG sets the CBC current limit in open loop operation. Different modes can be configured through CBC_ILIMIT_MODE: CBC_ILIMIT automatic recovery next PWM cycle, CBC_ILIMIT automatic recovery threshold based, CBC_ILIMIT automatic recovery number of PWM cycles based, CBC_ILIMIT report only, CBC_ILIMIT disabled.

8.3.21.8.1 CBC_ILIMIT Automatic Recovery next PWM Cycle (CBC_ILIMIT_MODE = 000xb)

When a CBC_ILIMIT event happens in this mode, MCT8316A stops driving the FETs using recirculation mode to prevent the inductive energy from entering the DC input supply. The CBC_ILIMIT bit is set to 1b in the fault status registers. Normal operation resumes at the start of next PWM cycle and CBC_ILIMIT bit is reset to 0b. The status of CONTROLLER_FAULT bit and nFAULT pin will be determined by CBC_ILIMIT_MODE. When CBC_ILIMIT_MODE is 0000b, CONTROLLER_FAULT bit is set to 1b and nFAULT pin driven low until next PWM cycle. When CBC_ILIMIT_MODE is 0001b, CONTROLLER_FAULT bit is not set to 1b and nFAULT is not driven low.

8.3.21.8.2 CBC_ILIMIT Automatic Recovery Threshold Based (CBC_ILIMIT_MODE = 001xb)

When a CBC_ILIMIT event happens in this mode, MCT8316A stops driving the FETs using recirculation mode to prevent the inductive energy from entering the DC input supply. The CBC_ILIMIT bit is set to 1b in the status registers. Normal operation resumes after V_{SOX} falls below CBC_ILIMIT threshold and CBC_ILIMIT bit is set to 0b. The status of CONTROLLER_FAULT bit and nFAULT pin will be determined by CBC_ILIMIT_MODE. When CBC_ILIMIT_MODE is 0010b, CONTROLLER_FAULT bit is set to 1b and nFAULT pin driven low until V_{SOX} falls below CBC_ILIMIT threshold. When CBC_ILIMIT_MODE is 0011b, CONTROLLER_FAULT bit is not set to 1b and nFAULT is not driven low.

8.3.21.8.3 CBC_ILIMIT Automatic Recovery after 'n' PWM Cycles (CBC_ILIMIT_MODE = 010xb)

When a CBC_ILIMIT event happens in this mode, MCT8316A stops driving the FETs using recirculation mode to prevent the inductive energy from entering the DC input supply. The CBC_ILIMIT bit is set to 1b in the fault status registers. Normal operation resumes after (CBC_RETRY_PWM_CYC +1) PWM cycles and CBC_ILIMIT bit is set to 0b. The status of CONTROLLER_FAULT bit and nFAULT pin will be determined by CBC_ILIMIT_MODE. When CBC_ILIMIT_MODE is 0100b, CONTROLLER_FAULT bit is set to1b and nFAULT pin driven low until (CBC_RETRY_PWM_CYC +1) PWM cycles lapse. When CBC_ILIMIT_MODE is 0101b, CONTROLLER_FAULT bit is not set to 1b and nFAULT is not driven low.

8.3.21.8.4 CBC_ILIMIT Report Only (CBC_ILIMIT_MODE = 0110b)

No protective action is taken when a CBC_ILIMIT event happens in this mode. The CBC current limit event is reported by setting the CONTROLLER_FAULT and CBC_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages the overcurrent condition by acting appropriately. The reporting clears when the CBC_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

8.3.21.8.5 CBC_ILIMIT Disabled (CBC_ILIMIT_MODE = 0111b or 1xxxb)

No action is taken when a CBC_ILIMIT event happens in this mode.

8.3.21.9 Lock Detection Current Limit (LOCK_ILIMIT)

The lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The MCT8316A continuously monitors the output of the current sense amplifier (CSA) through the ADC. If at any time, the voltage on the output of CSA exceeds LOCK_ILIMIT for a time longer than t_{LCK_ILIMIT}, a LOCK_ILIMIT event is recognized and action is taken according to LOCK_ILIMIT_MODE. The threshold is set through LOCK_ILIMIT, the t_{LCK_ILIMIT} is set through LOCK_ILIMIT_DEG. LOCK_ILIMIT_MODE can be set to four different modes: LOCK_ILIMIT latched shutdown, LOCK_ILIMIT automatic retry, LOCK_ILIMIT report only and LOCK_ILIMIT disabled.

8.3.21.9.1 LOCK_ILIMIT Latched Shutdown (LOCK_ILIMIT_MODE = 00xxb)

When a LOCK_ILIMIT event happens in this mode, the status of MOSFETs will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFETs during LOCK_ILIMIT:

- LOCK_ILIMIT_MODE = 0000b: All MOSFETs are turned OFF.
- LOCK_ILIMIT_MODE = 0001b: MOSFET which was switching is turned OFF while the one which was conducting stays ON till inductive energy is completely recirculated.
- LOCK_ILIMIT_MODE = 0010b: All high-side MOSFETs are turned ON.
- LOCK_ILIMIT_MODE = 0011b: All low-side MOSFETs are turned ON.

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The CONTROLLER_FAULT and LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

8.3.21.9.2 LOCK_ILIMIT Automatic Recovery (LOCK_ILIMIT_MODE = 01xxb)

When a LOCK_ILIMIT event happens in this mode, the status of MOSFETs will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFETs during LOCK_ILIMIT:

- LOCK_ILIMIT_MODE = 0100b: All MOSFETs are turned OFF.
- LOCK_ILIMIT_MODE = 0101b: MOSFET which was switching is turned OFF while the one which was conducting stays ON till inductive energy is completely recirculated.
- LOCK_ILIMIT_MODE = 0110b: All high-side MOSFETs are turned ON
- LOCK_ILIMIT_MODE = 0111b: All low-side MOSFETs are turned ON

The CONTROLLER_FAULT and LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT and LOCK_ILIMIT bits are reset to 0b after the t_{LCK_RETRY} period expires.

8.3.21.9.3 LOCK_ILIMIT Report Only (LOCK_ILIMIT_MODE = 1000b)

No protective action is taken when a LOCK_ILIMIT event happens in this mode. The lock detection current limit event is reported by setting the CONTROLLER_FAULT and LOCK_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

8.3.21.9.4 LOCK_ILIMIT Disabled (LOCK_ILIMIT_MODE = 1xx1b)

No action is taken when a LOCK_ILIMIT event happens in this mode.

8.3.21.10 Thermal Warning (OTW)

If the die temperature exceeds the thermal warning limit (T_{OTW}), the OT and OTW bits in the status register are set to 1b. The reporting of OTW on the nFAULT pin can be enabled by setting OTW_REP to 1b. The device performs no additional action and continues to function. In this case, the nFAULT pin is released when the die temperature decreases below the hysteresis point of the thermal warning limit (T_{OTW} - T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit and the die temperature is lower than thermal warning limit. (T_{OTW}).

备注

Over-temperature warning (OTW) is not reported on nFAULT pin by default.

8.3.21.11 Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown limit (T_{TSD}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the DRIVER_FAULT, OT and TSD bit in the status register are set to 1b. Normal operation resumes (driver operation and the nFAULT pin is released) when the die temperature decreases below the hysteresis point of the thermal shutdown limit (T_{TSD} - T_{TSD_HYS}). The TSD bit stays latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

8.3.21.12 Motor Lock (MTR_LCK)

The MCT8316A continuously checks for different motor lock conditions (see Motor Lock Detection) during motor operation. When one of the enabled lock condition happens, a MTR_LCK event is recognized and action is taken according to the MTR_LCK_MODE.

In MCT8316AT, all motor lock condition detections are enabled and motor lock mode is configured to automatic retry after 5 seconds.

In MCT8316AV, all locks can be enabled or disabled individually and retry times can be configured through LCK_RETRY . MTR_LCK_MODE bit can operate in four different modes: MTR_LCK latched shutdown, MTR_LCK automatic retry, MTR_LCK report only and MTR_LCK disabled.

8.3.21.12.1 MTR_LCK Latched Shutdown (MTR_LCK_MODE = 00xxb)

When a MTR_LCK event happens in this mode, the status of MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 0000b: All MOSFETs are turned OFF.
- MTR_LCK_MODE = 0001b: MOSFET which was switching is turned OFF while the one which was conducting stays ON till inductive energy is completely recirculated.
- MTR_LCK_MODE = 0010b: All high-side MOSFETs are turned ON.
- MTR_LCK_MODE = 0011b: All low-side MOSFETs are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

8.3.21.12.2 MTR_LCK Automatic Recovery (MTR_LCK_MODE= 01xxb)

When a MTR_LCK event happens in this mode, the status of MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 0100b: All MOSFETs are turned OFF.
- MTR_LCK_MODE = 0101b: MOSFET which was switching is turned OFF while the one which was conducting stays ON till inductive energy is completely recirculated.
- MTR_LCK_MODE = 0110b: All high-side MOSFETs are turned ON.
- MTR_LCK_MODE = 0111b: All low-side MOSFETs are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are reset to 0b after the t_{LCK_RETRY} period expires.

8.3.21.12.3 MTR_LCK Report Only (MTR_LCK_MODE = 1000b)

No protective action is taken when a MTR_LCK event happens in this mode. The motor lock event is reported by setting the CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

8.3.21.12.4 MTR_LCK Disabled (MTR_LCK_MODE = 1xx1b)

No action is taken when a MTR_LCK event happens in this mode.

8.3.21.13 Motor Lock Detection

The MCT8316A provides different lock detect mechanisms to determine if the motor is in a locked state. Multiple detection mechanisms work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCT8316A can also identify and take action if there is no motor connected to the system. Each of the lock detect mechanisms and the no-motor detection can be disabled by their respective register bits (LOCK1/2/3_EN).

8.3.21.13.1 Lock 1: Abnormal Speed (ABN_SPEED)

MCT8316A monitors the speed continuously and at any time the speed exceeds LOCK_ABN_SPEED, an ABN_SPEED lock event is recognized and action is taken according to the MTR_LCK_MODE.

threshold is set through the LOCK_ABN_SPEED register. ABN_SPEED lock can be enabled/disabled by LOCK1_EN.

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8.3.21.13.2 Lock 2: Loss of Sync (LOSS_OF_SYNC)

The motor is commutated by detecting the zero crossing on the phase which is in Hi-Z state. If the motor is locked, the back-EMF will disappear and MCT8316A will be not able to detect the zero crossing. If MCT8316A is not able to detect zero crossing for LOSS_SYNC_TIMES number of times, LOSS_OF_SYNC event is recognized and action is taken according to the MTR_LCK_MODE. LOSS_OF_SYNC lock can be enabled/ disabled by LOCK2_EN.

8.3.21.13.3 Lock3: No-Motor Fault (NO_MTR)

The MCT8316A continuously monitors the relevant phase current (low-side phase in the present phase pattern); if the relevant phase current stays below NO_MTR_THR for a time longer than NO_MTR_DEG_TIME, a NO_MTR event is recognized. The response to the NO_MTR event is configured through MTR_LCK_MODE . NO_MTR lock can be enabled/disabled by LOCK3_EN.

8.3.21.14 IPD Faults

The MCT8316A uses 12-bit timers to estimate the time during the current ramp up and ramp down during IPD, when the motor start-up is configured as IPD (MTR_STARTUP is set to 10b). During IPD, the algorithm checks for a successful current ramp-up to IPD_CURR_THR, starting with an IPD clock of 10MHz; if unsuccessful (timer overflow before current reaches IPD_CURR_THR), IPD is repeated with lower frequency clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD_CURR_THR) with all the four clock frequencies, then the IPD_T1_FAULT gets triggered. Similarly the algorithm check sfor a successful current decay to zero during IPD current ramp down using all the mentioned IPD clock frequencies. If the IPD timer overflows (current does not ramp down to zero) in all the four attempts, then the IPD_T2_FAULT gets triggered.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCT8316A can generate a fault called IPD_FREQ_FAULT during such a scenario . The IPD_FREQ_FAULT maybe triggerd if the IPD frequency is too high for the IPD current limit and the IPD release mode or if the motor inductance is too high for the IPD frequency, IPD current limit and IPD release mode.

8.4 Device Functional Modes

8.4.1 Functional Modes

8.4.1.1 Sleep Mode

In sleep mode, the MOSFETs, sense amplifiers, buck regulator, charge pump, AVDD LDO regulator and the I^2C bus are disabled. The device can be configured to enter sleep (instead of standby) mode by configuring DEV_MODE to 1b. SPEED pin determines entry and exit from sleep state as described in 表 8-19.

备注

During power-up and power-down of the device, the nFAULT pin is held low as the internal regulators are disabled. After the regulators have been enabled, the nFAULT pin is automatically released.

8.4.1.2 Standby Mode

In standby mode the charge pump, AVDD LDO, buck regulator and I^2C bus are active. The device can be configured to enter standby mode by configuring DEV_MODE to 0b. SPEED pin determines entry and exit from standby state as described in 表 8-19

8.4.1.3 Fault Reset (CLR_FLT)

In the case of latched faults, the device goes into a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR_FLT to 1b.

表 8-19. Conditions to Enter or Exit Sleep or Standby Modes

SPEED COMMAND MODE	ENTER STANDBY CONDITION	ENTER SLEEP CONDITION	EXIT FROM STANDBY CONDITION	EXIT FROM SLEEP CONDITION
Analog	SPEED pin voltage < V_{EN_SB} for $t_{DET\_SB\_ANA}$	SPEED pin voltage < V_{EN_SL} for $t_{DET\_SL\_ANA}$	SPEED pin voltage > V_{EX_SB} for t_{DET_ANA}	SPEED pin voltage > V_{EX_SL} for t_{DET_ANA}
PWM/ Frequency	SPEED pin low ($V < V_{DIG\_IL}$) for $t_{EN\_SB\_PWM}$/ $t_{EN\_SB\_FREQ}$	SPEED pin low ($V < V_{DIG\_IL}$) for $t_{DET\_SL\_PWM}$/ $t_{DET\_SL\_FREQ}$	SPEED pin high ($V > V_{DIG\_IH}$) for t_{DET_PWM}	SPEED pin high ($V > V_{DIG\_IH}$) for t_{DET_PWM}
I^2C	SPEED_CTRL is programmed as 0.	SPEED pin voltage < V_{EN_SL} for t > SLEEP_TIME	SPEED_CTRL is programmed as non-zero.	SPEED pin voltage > V_{EX_SL} for t_{DET_ANA}

8.5 External Interface

8.5.1 DRVOFF Functionality

When DRVOFF pin is driven high, all six MOSFETs are disabled. In this mode, if SPEED pin is high, the charge pump, AVDD regulator, buck regulator and I^2C bus are active; driver faults like OCP will be inactive.

8.5.2 DAC outputs

MCT8316A has two 12-bit DACs which output analog voltage equivalent of digital variables on DACOUT1 and DACOUT2 pins with resolution of 12 bits and maximum voltage is 3-V. Signals available on DACOUT pins is useful in tracking algorithm variables in real-time and can be used for tuning speed controller or motor acceleration time. The address for variables for DACOUT1 and DACOUT2 are configured using DACOUT1_VAR_ADDR and DACOUT2_VAR_ADDR. DACOUT1 is available on pin 37 and DACOUT2 can be configured on pin 36 by setting DAC_SOX_CONFIG to 00b. DACOUT2 is also available on pin 38.

8.5.3 SOX Output

MCT8316A can provide the built-in current sense amplifiers' output on the SOX pin. SOX output is available on pin 36 and can be configured by DAC_SOX_CONFIG.

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8.5.4 Oscillator Source

MCT8316A has a built-in oscillator that is used as the clock source for all digital peripherals and timing measurements. Default configuration for MCT8316A is to use the internal oscillator and it is sufficient to drive the motor without need for any external crystal or clock sources.

In case MCT8316A does not meet accuracy requirements of timing measurement or speed loop, then MCT8316AV has an option to support an external clock reference.

In order to improve EMI performance, MCT8316AV provides the option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SSM_CONFIG

.

8.5.4.1 External Clock Source (Available for MCT8316AV)

Speed loop accuracy of MCT8316A over wide operating temperature range can be improved by providing more accurate optional clock reference on EXT_CLK pin as shown in 图 8-51. EXT_CLK will be used to calibrate internal clock oscillator and match the accuracy of the external clock. External clock source can be selected by configuring CLK_SEL to 11b and setting EXT_CLK_EN to 1b. The external clock source frequency can be configured through EXT_CLK_CONFIG.

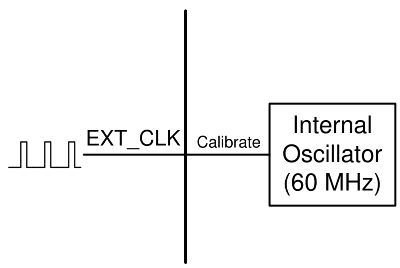

图 8-51. External Clock Reference

备注

External clock is optional and can be used when higher clock accuracy is needed. MCT8316A will always power up using the internal oscillator in all modes.

8.5.5 External Watchdog (Available only in MCT836AV)

MCT8316A provides an external watchdog feature - EXT_WD_EN bit should be set to 1b to enable the external watchdog. When this feature is enabled, the device waits for a tickle (low to high transition in GPIO mode, EXT_WD_STATUS_SET set to 1b in I^2C mode) from the external watchdog input for a configured time interval; if the time interval between two consecutive tickles is higher than the configured time, a watchdog fault is triggered. This fault can be configured using EXT_WD_FAULT either as a report only fault or as a latched fault with outputs in Hi-Z state. The latched fault can be cleared by writing 1b to CLR_FLT. In case, the next tickle arrives before the configured time interval elapses, the watchdog timer is reset and it begins to wait for the next tickle. This can be used to continuously monitor the health of an external MCU (which is the external watchdog input) and put the MCT8316A outputs in Hi-Z in case the external MCU is in an erroneous state.

The external watchdog input is selected using EXT_WD_INPUT and can either be the EXT_WD pin or the I^2C interface . The time interval between two tickles to trigger a watchdog fault is configured by EXT_WD_FREQ; there are 4 time (frequency) settings - 100 (10Hz), 200 (5Hz), 500 (2Hz) and 1000ms (1Hz).

8.6 EEPROM access and I2C interface

8.6.1 EEPROM Access

MCT8316A has 1024 bits (16 rows of 64 bits each) of EEPROM, which are used to store the motor configuration parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit write and read operations are supported. EEPROM can be written and read using the I2C serial interface but erase cannot be performed using I2C serial interface. The shadow registers corresponding to the EEPROM are located at addresses 0x000080-0x0000AE.

备注

MCT8316A allows EEPROM write and read operations only when the motor is not spinning.

8.6.1.1 EEPROM Write

In MCT8316A, EEPROM write procedure is as follows,

1. Write register 0x000080 (ISD_CONFIG) with ISD configuration like resync enable, reverse drive enable, stationary detect threshold etc.,
2. Write register 0x000082 (MOTOR_STARTUP1) with motor start-up configuration like start-up method, first cycle frequency, IPD parameters, align parameters etc.,
3. Write register 0x000084 (MOTOR_STARTUP2) with motor start-up configuration like open loop acceleration, minimum duty cycle etc.,
4. Write register 0x000086 (CLOSED_LOOP1) with motor control configuration like closed loop acceleration, PWM frequency, PWM modulation etc.,
5. Write register 0x000088 (CLOSED_LOOP2) with motor control configuration like FG signal parameters, motor stop options etc.,
6. Write register 0x00008A (CLOSED_LOOP3) with motor control configuration like fast start-up and dynamic degauss parameters including BEMF thresholds, duty cycle thresholds etc.,
7. Write register 0x00008C (CLOSED_LOOP4) with motor control configuration like fast deceleration parameters including fast deceleration duty threshold, window, current limits etc.,
8. Write register 0x00008E (CONST_SPEED) with motor control configuration like speed loop parameters including closed loop mode, saturation limits, K_p, K_i etc.,
9. Write register 0x000090 (CONST_PWR) with motor control configuration like input power regulation parameters including maximum power, constant power mode, power level hysteresis, maximum speed etc.,
10. Write register 0x000092 (FAULT_CONFIG1) with fault control configuration like CBC, lock current limits and actions, retry times etc.,
11. Write register 0x000094 (FAULT_CONFIG2) with fault control configuration like OV, UV limits and actions, abnormal speed level, motor lock setting etc.,
12. Write registers 0x000096 and 0x000098 (150_DEG_TWO_PH_PROFILE, 150_DEG_THREE_PH_PROFILE) with PWM duty cycle configurations for 150º modulation.
13. Write registers 0x00009A and 0x00009C (TRAP_CONFIG1 and TRAP_CONFIG2) with algorithm parameters like ISD BEMF threshold, blanking time, AVS current limits etc.,
14. Write registers 0x0000A4 and 0x0000A6 (PIN_CONFIG1 and PIN_CONFIG2) with pin configuration for DIR, BRAKE, DACOUT1 and DACOUT2, SOX, external watchdog etc.,
15. Write register 0x0000A8 (DEVICE_CONFIG) with device configuration like device mode, external clock enable, clock source, speed input PWM frequency range etc.,
16. Write registers 0x0000AC and 0x0000AE (GD_CONFIG1 and GD_CONFIG2) with gate driver configuration like slew rate, CSA gain, OCP level, mode, OVP enable etc.,
17. Write 0x80000000 into register 0x0000E6 to write the shadow register (0x000080-0x0000AE) values into the EEPROM.
18. Wait for 100ms for the EEPROM write operation to complete

Steps 1-16 can be selectively executed based on registers/parameters that need to be modified. After all shadow registers have been updated with the required values, step 17 should be executed to copy the contents of the shadow registers into the EEPROM.

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8.6.1.2 EEPROM Read

In MCT8316A, EEPROM read procedure is as follows,

1. Write 0x40000000 into register 0x0000E6 to read the EEPROM data into the shadow registers (0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow register values, 1 or 2 registers at a time, using the I^{2}C read command as explained in 节 8.6.2. Shadow register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation (since each address is a 16-bit location).

8.6.2 I^{2}C Serial Interface (Available only in MCT8316AV)

MCT8316A interfaces with an external MCU over an I^{2}C serial interface. MCT8316A is an I^{2}C target to be interfaced with a controller. External MCU can use this interface to read/write from/to any non-reserved register in MCT8316A

备注

For reliable communication, a 100-µs delay should be used between every byte transferred over the I^{2}C bus.

8.6.2.1 I^{2}C Data Word

The I^{2}C data word format is shown in 表 8-20.

表 8-20. I^{2}C Data Word Format

TARGET_ID	R/W	CONTROL WORD	DATA	CRC-8
A6 - A0	W0	CW23 - CW0	D15 / D31/ D63 - D0	C7 - C0

Target ID and R/W Bit: The first byte includes the 7-bit I^{2}C target ID (0x00), followed by the read/write command bit. Every packet in MCT8316A the communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

24-bit Control Word: The Target Address is followed by a 24-bit control bit. The control word format is shown in 表 8-21.

表 8-21. 24-bit Control Word Format

OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR
CW23	CW22	CW21- CW20	CW19 - CW16	CW15 - CW12	CW11 - CW0

Each field in the control word is explained in detail below.

OP_R/W – Read/Write: R/W bit gives information on whether this is a read operation or write operation. Bit value 0 indicates it is a write operation. Bit value 1 indicates it is a read operation. For write operation, MCT8316A will expect data bytes to be sent after the 24-bit control word. For read operation, MCT8316A will expect an I^{2}C read request with repeated start or normal start after the 24-bit control word.

CRC_EN – Cyclic Redundancy Check(CRC) Enable: MCT8316A supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

DLEN – Data Length: DLEN field determines the length of the data that will be sent by external MCU to MCT8316A. MCT8316A protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

表 8-22. Data Length Configuration

DLEN Value	Data Length
00b	16-bit
01b	32-bit
10b	64-bit

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表 8-22. Data Length Configuration (continued)

DLEN Value	Data Length
11b	Reserved

MEM_SEC – Memory Section: Each memory location in MCT8316A is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

MEM_PAGE – Memory Page: Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

MEM_ADDR – Memory Address: Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCT8316A using all three fields – Memory Section, Memory Page, Memory Address. For memory locations 0x000000-0x000800, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x800 for 0x000800)

Data Bytes: For a write operation to MCT8316A, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section.

CRC Byte: If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Procedure to calculate CRC is explained in CRC Byte Calculation below.

8.6.2.2 I²C Write Operation

MCT8316A write operation over I²C involves the following sequence.

1. I²C start condition.
2. The sequence starts with I²C target start byte, made up of 7-bit target ID (0x00) to identify the MCT8316A along with the R/W bit set to 0.
3. The start byte is followed by 24-bit control word. Bit 23 in the control word has to be 0 as it is a write operation.
4. The 24-bit control word is then followed by the data bytes. The length of the data byte depends on the DLEN field.
   a. While sending data bytes, the LSB byte is sent first. Refer below examples for more details.
   b. 16-bit/32-bit write – The data sent is written to the address mentioned in Control Word.
   c. 64-bit Write – 64-bit is treated as two 32-bit writes. The address mentioned in Control word is taken as Addr 0. Addr 1 is calculating internally by MCT8316A by incrementing Addr 0 by 2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first way) are written to Addr 0 and the next 4 bytes are written to Addr 1.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes).
6. I²C stop condition.

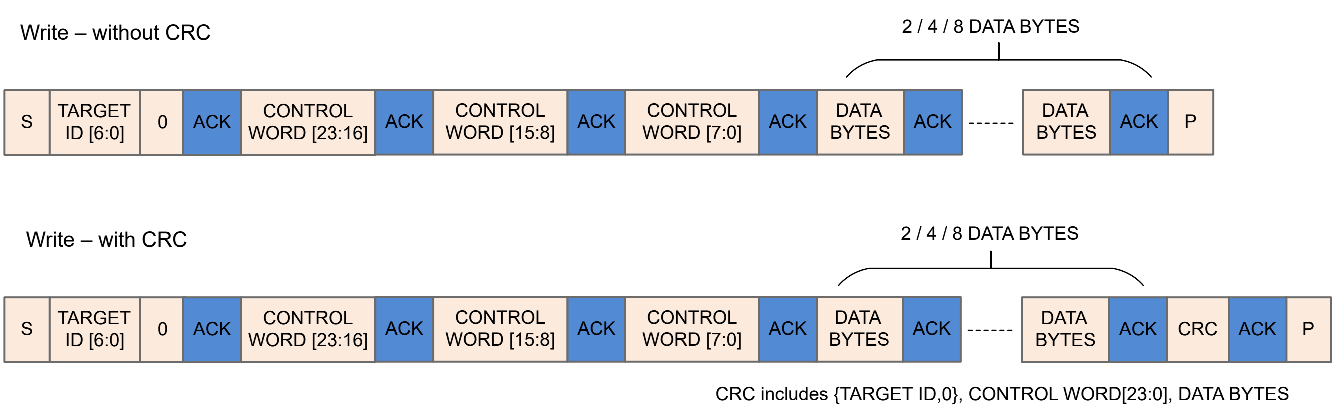

图 8-52. I²C Write Operation Sequence

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8.6.2.3 I²C Read Operation

MCT8316A read operation over I²C involves the following sequence.

1. I²C start condition.
2. The sequence starts with I²C target Start Byte.
3. The Start Byte is followed by 24-bit Control Word. Bit 23 in the control word has to be 1 as it is a read operation.
4. The control word is followed by a repeated start or normal start.
5. MCT8316A sends the data bytes on SDA. The number of bytes sent by MCT8316A depends on the DLEN field value in the control word.
   a. While sending data bytes, the LSB byte is sent first. Refer the examples below for more details.
   b. 16-bit/32-bit Read – The data from the address mentioned in Control Word is sent back.
   c. 64-bit Read – 64-bit is treated as two 32-bit read. The address mentioned in Control Word is taken as Addr 0. Addr 1 is calculating internally by MCT8316A by incrementing Addr 0 by 2. A total of 8 data bytes are sent by MCT8316A. The first 4 bytes (sent in LSB first way) are read from Addr 0 and the next 4 bytes are read from Addr 1.
   d. MCT8316A takes some time to process the control word and read data from the given address. This involves some delay. It is quite possible that the repeated start with Target ID will be NACK'd. If the I²C read request has been NACK'd by MCT8316A, retry after few cycles. During this retry, it is not necessary to send the entire packet along with the control word. It is sufficient to send only the start condition with target ID and read bit.
6. If CRC is enabled, then MCT8316A sends an additional CRC byte at the end. If CRC is enabled, external MCU I²C controller has to read this additional byte before sending the stop bit. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).
7. I²C stop condition.

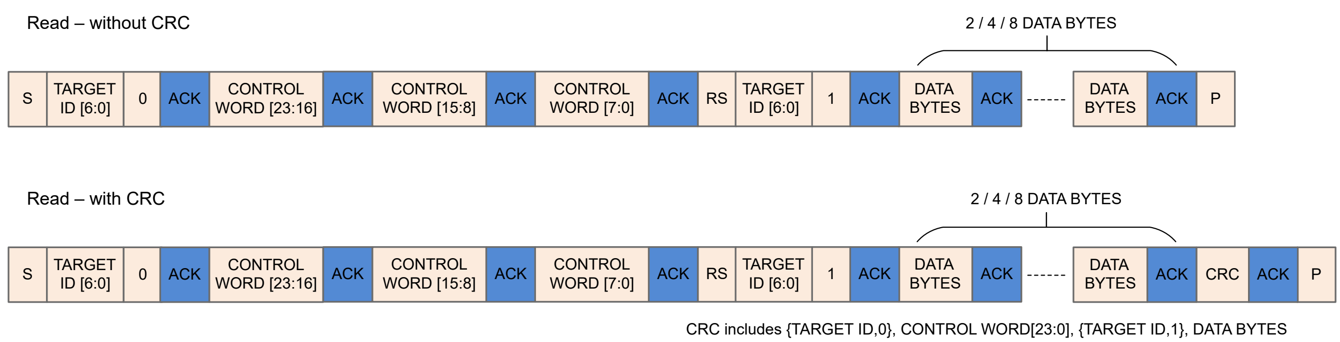

图 8-53. I²C Read Operation Sequence

8.6.2.4 Examples of MCT8316A I²C Communication Protocol Packets

All values used in this example section are in hex format. I²C target ID used in the examples is 0x00.

Example for 32-bit Write Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

表 8-23. Example for 32-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes				CRC
Target ID	I²C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x00	0x0	0x0	0x1	0x1	0x0	0x0	0x0	0x80	0xCD	0xAB	0x34	0x12	0x45
0x00		0x50				0x00		0x80	0xCD	0xAB	0x34	0x12	0x45

Example for 64-bit Write Operation: Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

表 8-24. Example for 64-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes	CRC
Target ID	I^2C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0 - DB7	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	[D7-D0] x 8	C7-C0
0x00	0x0	0x0	0x1	0x2	0x0	0x0	0x0	0x80	0x67452301EFCDAB89	0x45
0x00		0x60				0x00		0x80	0x67452301EFCDAB89	0x45

Example for 32-bit Read Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

表 8-25. Example for 32-bit Read Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Start Byte		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Target ID	I^2C Write	R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	Target ID	I^2C Read	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	A6-A0	W0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x00	0x0	0x1	0x1	0x1	0x0	0x0	0x0	0x80	0x00	0x1	0xCD	0xAB	0x34	0x12	0x56
0x00		0xD0				0x00		0x80	0x01		0xCD	0xAB	0x34	0x12	0x56

8.6.2.5 Internal Buffers

MCT8316A uses buffers internally to store the data received on I^2C. Highest priority is given to collecting data on the I^2C Bus. There are 2 buffers (ping-pong) for I^2C Rx Data and 2 buffers (ping-pong) for I^2C Tx Data.

A write request from external MCU is stored in Rx Buffer 1 and then the parsing block is triggered to work on this data in Rx Buffer 1. While MCT8316A is processing a write packet from Rx Buffer 1, if there is another new read/write request, the entire data from the I^2C bus is stored in Rx Buffer 2 and it will be processed after the current request.

MCT8316A can accommodate a maximum of two consecutive read/write requests. If MCT8316A is busy due to high priority interrupts, the data sent will be stored in internal buffers (Rx Buffer 1 and Rx Buffer 2). At this point, if there is a third read/write request, the Target ID will be NACK’d as the buffers are already full.

During read operations, the read request is processed and the read data from the register is stored in the Tx Buffer along with the CRC byte, if enabled. Now if the external MCU initiates an I^2C Read (Target ID + R bit), the data from this Tx Buffer is sent over I^2C. Since there are two Tx Buffers, register data from 2 MCT8316A reads can be buffered. Given this scenario, if there is a third read request, the control word will be stored in the Rx Buffer 1, but it will not be processed by MCT8316A as the Tx Buffers are full.

Once a data is read from Tx Buffer, the data is no longer stored in the Tx buffer. The buffer is cleared and it becomes available for the next data to be stored. If the read transaction was interrupted in between and if the MCU had not read all the bytes, external MCU can initiate another I^2C read (only I^2C read, without any control word information) to read all the data bytes from first.

8.6.2.6 CRC Byte Calculation

An 8-bit CCIT polynomial ($x^8 + x^2 + x + 1$) is used for CRC computation.

CRC Calculation in Write Operation: When the external MCU writes to MCT8316A, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCT8316A will

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compute CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

CRC Calculation in Read Operation: When the external MCU reads from MCT8316A, if the CRC is enabled, MCT8316A sends the CRC byte at the end of the data. The CRC computation in read operation involves the start byte, control words sent by external MCU along with data bytes sent by MCT8316A. Input data for CRC calculation by external MCU to verify the data sent by MCT8316A are listed below :

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

8.7 EEPROM (Non-Volatile) Register Map

8.7.1 Algorithm_Configuration Registers

ALGORITHM_CONFIGURATION Registers lists the memory-mapped registers for the Algorithm_Configuration registers. All register offset addresses not listed in ALGORITHM_CONFIGURATION Registers should be considered as reserved locations and the register contents should not be modified.

表 8-26. ALGORITHM_CONFIGURATION Registers

Address	Acronym	Register Name	Section
80h	ISD_CONFIG	ISD configuration	节 8.7.1.1
82h	MOTOR_STARTUP1	Motor start-up configuration 1	节 8.7.1.2
84h	MOTOR_STARTUP2	Motor start-up configuration 2	节 8.7.1.3
86h	CLOSED_LOOP1	Closed loop configuration 1	节 8.7.1.4
88h	CLOSED_LOOP2	Closed loop configuration 2	节 8.7.1.5
8Ah	CLOSED_LOOP3	Closed loop configuration 3	节 8.7.1.6
8Ch	CLOSED_LOOP4	Closed loop configuration 4	节 8.7.1.7
8Eh	CONST_SPEED	Constant speed configuration	节 8.7.1.8
90h	CONST_PWR	Constant power configuration	节 8.7.1.9
96h	150_DEG_TWO_PH_PROFILE	150° Two-ph profile	节 8.7.1.10
98h	150_DEG_THREE_PH_PROFILE	150° Three-ph profile	节 8.7.1.11
9Ah	TRAP_CONFIG1	Trap configuration 1	节 8.7.1.12
9Ch	TRAP_CONFIG2	Trap configuration 2	节 8.7.1.13

Complex bit access types are encoded to fit into small table cells. Algorithm_Configuration Access Type Codes shows the codes that are used for access types in this section.

表 8-27. Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.7.1.1 ISD_CONFIG Register (Address = 80h) [Reset = 00000000h]

ISD_CONFIG is shown in ISD_CONFIG Register and described in ISD_CONFIG Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure initial speed detect settings

图 8-54. ISD_CONFIG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PARITY</td><td>ISD_EN</td><td>BRAKE_EN</td><td>HIZ_EN</td><td>RVS_DR_EN</td><td>RESYNC_EN</td><td>STAT_BRK_EN</td><td>STAT_DETECT_THR</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">STAT_DETECT_THR</td><td>BRK_MODE</td><td>BRK_CONFIG</td><td colspan="3">BRK_CURR_THR</td><td>BRK_TIME</td></tr>
<tr><td colspan="2">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td colspan="3">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">BRK_TIME</td><td colspan="4">HIZ_TIME</td><td>STARTUP_BRK_TIME</td></tr>
<tr><td colspan="3">R/W-0h</td><td colspan="4">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">STARTUP_BRK_TIME</td><td colspan="3">RESYNC_MIN_THRESHOLD</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="2">R/W-0h</td><td colspan="3">R/W-0h</td><td colspan="3">R/W-0h</td></tr>
</table>

表 8-28. ISD_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	ISD_EN	R/W	0h	ISD enable 0h = Disable 1h = Enable
29	BRAKE_EN	R/W	0h	Brake enable 0h = Disable 1h = Enable
28	HIZ_EN	R/W	0h	Hi-Z enable 0h = Disable 1h = Enable
27	RVS_DR_EN	R/W	0h	Reverse drive enable 0h = Disable 1h = Enable
26	RESYNC_EN	R/W	0h	Resynchronization enable 0h = Disable 1h = Enable
25	STAT_BRK_EN	R/W	0h	Enable or disable brake during stationary 0h = Disable 1h = Enable

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表 8-28. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	STAT_DETECT_THR	R/W	0h	Stationary BEMF detect threshold 0h = 5 mV 1h = 10 mV 2h = 15 mV 3h = 20 mV 4h = 25 mV 5h = 30 mV 6h = 50 mV 7h = 100 mV
21	BRK_MODE	R/W	0h	Brake mode 0h = All three low-side FETs turned ON 1h = All three high-side FETs turned ON
20	BRK_CONFIG	R/W	0h	Brake configuration 0h = Brake time is used to come out of Brake state 1h = Brake current threshold is used to come out of Brake state
19-17	BRK_CURR_THR	R/W	0h	Brake current threshold 0h = 5 mV 1h = 10 mV 2h = 15 mV 3h = 20 mV 4h = 25 mV 5h = 30 mV 6h = 50 mV 7h = 100 mV
16-13	BRK_TIME	R/W	0h	Brake time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s

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表 8-28. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-9	HIZ_TIME	R/W	0h	Hi-Z time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
8-6	STARTUP_BRK_TIME	R/W	0h	Brake time when motor is stationary 0h = 1 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms
5-3	RESYNC_MIN_THRESHOLD	R/W	0h	Minimum phase BEMF below which the motor is coasted instead of resync 0h = computed based on MIN_DUTY 1h = 300 mV 2h = 400 mV 3h = 500 mV 4h = 600 mV 5h = 800 mV 6h = 1000 mV 7h = 1250 mV
2-0	RESERVED	R/W	0h	Reserved

8.7.1.2 MOTOR_STARTUP1 Register (Address = 82h) [Reset = 00000000h]

MOTOR_STARTUP1 is shown in MOTOR_STARTUP1 Register and described in MOTOR_STARTUP1 Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure motor startup settings1

图 8-55. MOTOR_STARTUP1 Register

31	30	29	28	27	26	25	24
PARITY	MTR_STARTUP		ALIGN_RAMP_RATE				ALIGN_TIME
R/W-0h	R/W-0h		R/W-0h				R/W-0h
23	22	21	20	19	18	17	16
ALIGN_TIME			ALIGN_CURR_THR				IPD_CLK_FREQ
R/W-0h			R/W-0h				R/W-0h
15	14	13	12	11	10	9	8
IPD_CLK_FREQ		IPD_CURR_THR				IPD_RLS_MODE	
R/W-0h		R/W-0h				R/W-0h	
7	6	5	4	3	2	1	0
IPD_ADV_ANGLE		IPD_REPEAT		SLOW_FIRST_CYC_FREQ			
R/W-0h		R/W-0h		R/W-0h			

表 8-29. MOTOR_STARTUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	MTR_STARTUP	R/W	0h	Motor start-up method 0h = Align 1h = Double Align 2h = IPD 3h = Slow first cycle
28-25	ALIGN_RAMP_RATE	R/W	0h	Align voltage ramp rate 0h = 0.1 V/s 1h = 0.2 V/s 2h = 0.5 V/s 3h = 1 V/s 4h = 2.5 V/s 5h = 5 V/s 6h = 7.5 V/s 7h = 10 V/s 8h = 25 V/s 9h = 50 V/s Ah = 75 V/s Bh = 100 V/s Ch = 250 V/s Dh = 500 V/s Eh = 750 V/s Fh = 1000 V/s

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表 8-29. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-21	ALIGN_TIME	R/W	0h	Align time 0h = 5 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 75 ms 5h = 100 ms 6h = 200 ms 7h = 400 ms 8h = 600 ms 9h = 800 ms Ah = 1 s Bh = 2 s Ch = 4 s Dh = 6 s Eh = 8 s Fh = 10 s
20-17	ALIGN_CURR_THR	R/W	0h	Align current threshold (Align current threshold (A) = ALIGN_CURR_THR / CSA_GAIN) 0h = N/A 1h = 0.1V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V
16-14	IPD_CLK_FREQ	R/W	0h	IPD clock frequency 0h = 50 Hz 1h = 100 Hz 2h = 250 Hz 3h = 500 Hz 4h = 1000 Hz 5h = 2000 Hz 6h = 5000 Hz 7h = 10000 Hz

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表 8-29. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-10	IPD_CURR_THR	R/W	0h	IPD current threshold (IPD current threshold (A) = IPD_CURR_THR / CSA_GAIN) 0h = N/A 1h = N/A 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V
9-8	IPD_RLS_MODE	R/W	0h	IPD release mode 0h = Brake 1h = Tristate 2h = N/A 3h = N/A
7-6	IPD_ADV_ANGLE	R/W	0h	IPD advance angle 0h = 0° 1h = 30° 2h = 60° 3h = 90°
5-4	IPD_REPEAT	R/W	0h	Number of times IPD is executed 0h = one 1h = average of 2 times 2h = average of 3 times 3h = average of 4 times
3-0	SLOW_FIRST_CYC_FREQ	R/W	0h	Frequency of first cycle 0h = 0.05 Hz 1h = 0.1 Hz 2h = 0.25 Hz 3h = 0.5 Hz 4h = 1 Hz 5h = 2 Hz 6h = 3 Hz 7h = 5 Hz 8h = 10 Hz 9h = 15 Hz Bh = 25 Hz Ch = 50 Hz Dh = 100 Hz Eh = 150 Hz Fh = 200 Hz

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8.7.1.3 MOTOR_STARTUP2 Register (Address = 84h) [Reset = X]

MOTOR_STARTUP2 is shown in MOTOR_STARTUP2 Register and described in MOTOR_STARTUP2 Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure motor startup settings2

图 8-56. MOTOR_STARTUP2 Register

31	30	29	28	27	26	25	24
PARITY	OL_ILIMIT_CONFIG	OL_DUTY			OL_ILIMIT		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OL_ILIMIT	OL_ACC_A1					OL_ACC_A2	
R/W-0h	R/W-0h					R/W-0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OL_ACC_A2			OPN_CL_HANDOFF_THR				
R/W-0h			R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AUTO_HANDOFF	FIRST_CYCLE_FREQ_SEL	MIN_DUTY				RESERVED	
R/W-0h	R/W-0h	R/W-0h				R-X	

表 8-30. MOTOR_STARTUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	OL_ILIMIT_CONFIG	R/W	0h	Open loop current limit configuration 0h = Open loop current limit defined by OL_ILIMIT 1h = Open loop current limit defined by ILIMIT
29-27	OL_DUTY	R/W	0h	Duty cycle limit during open loop 0h = 10% 1h = 15% 2h = 20% 3h = 25% 4h = 30% 5h = 40% 6h = 50% 7h = 100%

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表 8-30. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	OL_ILIMIT	R/W	0h	Open loop current limit (OL current threshold (A) = OL_CURR_THR / CSA_GAIN) 0h = N/A 1h = 0.1V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V
22-18	OL_ACC_A1	R/W	0h	Open loop acceleration A1 0h = 0.005 Hz/s 1h = 0.01 Hz/s 2h = 0.025 Hz/s 3h = 0.05 Hz/s 4h = 0.1 Hz/s 5h = 0.25 Hz/s 6h = 0.5 Hz/s 7h = 1 Hz/s 8h = 2.5 Hz/s 9h = 5 Hz/s Ah = 7.5 Hz/s Bh = 10 Hz/s Ch = 12.5 Hz/s Dh = 15 Hz/s Eh = 20 Hz/s Fh = 30 Hz/s 10h = 40 Hz/s 11h = 50 Hz/s 12h = 60 Hz/s 13h = 75 Hz/s 14h = 100 Hz/s 15h = 125 Hz/s 16h = 150 Hz/s 17h = 175 Hz/s 18h = 200 Hz/s 19h = 250 Hz/s 1Ah = 300 Hz/s 1Bh = 400 Hz/s 1Ch = 500 Hz/s 1Dh = 750 Hz/s 1Eh = 1000 Hz/s 1Fh = No Limit (32767) Hz/s

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表 8-30. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-13	OL_ACC_A2	R/W	0h	Open loop acceleration A2 0h = 0.005 Hz/s2 1h = 0.01 Hz/s2 2h = 0.025 Hz/s2 3h = 0.05 Hz/s2 4h = 0.1 Hz/s2 5h = 0.25 Hz/s2 6h = 0.5 Hz/s2 7h = 1 Hz/s2 8h = 2.5 Hz/s2 9h = 5 Hz/s2 Ah = 7.5 Hz/s2 Bh = 10 Hz/s2 Ch = 12.5 Hz/s2 Dh = 15 Hz/s2 Eh = 20 Hz/s2 Fh = 30 Hz/s2 10h = 40 Hz/s2 11h = 50 Hz/s2 12h = 60 Hz/s2 13h = 75 Hz/s2 14h = 100 Hz/s2 15h = 125 Hz/s2 16h = 150 Hz/s2 17h = 175 Hz/s2 18h = 200 Hz/s2 19h = 250 Hz/s2 1Ah = 300 Hz/s2 1Bh = 400 Hz/s2 1Ch = 500 Hz/s2 1Dh = 750 Hz/s2 1Eh = 1000 Hz/s2 1Fh = No Limit (32767) Hz/s2

表 8-30. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	OPN_CL_HANDOFF_THR	R/W	0h	Open to closed loop handoff threshold 0h = 1 Hz 1h = 4 Hz 2h = 8 Hz 3h = 12 Hz 4h = 16 Hz 5h = 20 Hz 6h = 24 Hz 7h = 28 Hz 8h = 32 Hz 9h = 36 Hz Ah = 40 Hz Bh = 45 Hz Ch = 50 Hz Dh = 55 Hz Eh = 60 Hz Fh = 65 Hz 10h = 70 Hz 11h = 75 Hz 12h = 80 Hz 13h = 85 Hz 14h = 90 Hz 15h = 100 Hz 16h = 150 Hz 17h = 200 Hz 18h = 250 Hz 19h = 300 Hz 1Ah = 350 Hz 1Bh = 400 Hz 1Ch = 450 Hz 1Dh = 500 Hz 1Eh = 550 Hz 1Fh = 600 Hz
7	AUTO_HANDOFF	R/W	0h	Auto handoff enable 0h = Disable Auto Handoff (and use OPN_CL_HANDOFF_THR) 1h = Enable Auto Handoff
6	FIRST_CYCLE_FREQ_SEL	R/W	0h	First cycle frequency select 0h = Defined by SLOW_FIRST_CYC_FREQ 1h = 0 Hz

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表 8-30. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-2	MIN_DUTY	R/W	0h	Min operational duty cycle 0h = 1.5 % 1h = 2 % 2h = 3 % 3h = 4 % 4h = 5 % 5h = 6 % 6h = 7 % 7h = 8 % 8h = 9 % 9h = 10 % Ah = 12 % Bh = 15 % Ch = 17.5 % Dh = 20 % Eh = 25 % Fh = 30 %
1-0	RESERVED	R	X	Reserved

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8.7.1.4 CLOSED_LOOP1 Register (Address = 86h) [Reset = 00000000h]

CLOSED_LOOP1 is shown in CLOSED_LOOP1 Register and described in CLOSED_LOOP1 Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure close loop settings1

图 8-57. CLOSED_LOOP1 Register

31	30	29	28	27	26	25	24
PARITY	COMM_CONTROL		CL_ACC				
R/W-0h	R/W-0h		R/W-0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CL_DEC_CONFIG	CL_DEC					PWM_FREQ_OUT	
R/W-0h	R/W-0h					R/W-0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWM_FREQ_OUT			PWM_MODUL		PWM_MODE	LD_ANGLE_POLARITY	LD_ANGLE
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LD_ANGLE							RESERVED
R/W-0h							R/W-0h

表 8-31. CLOSED_LOOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	COMM_CONTROL	R/W	0h	Trapezoidal commutation mode 0h = 120° Commutation 1h = Variable commutation between 120° and 150° 2h = N/A 3h = N/A

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表 8-31. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	CL_ACC	R/W	0h	Closed loop acceleration rate 0h = 0.005 V/s 1h = 0.01 V/s 2h = 0.025 V/s 3h = 0.05 V/s 4h = 0.1 V/s 5h = 0.25 V/s 6h = 0.5 V/s 7h = 1 V/s 8h = 2.5 V/s 9h = 5 V/s Ah = 7.5 V/s Bh = 10 V/s Ch = 12.5 V/s Dh = 15 V/s Eh = 20 V/s Fh = 30 V/s 10h = 40 V/s 11h = 50 V/s 12h = 60 V/s 13h = 75 V/s 14h = 100 V/s 15h = 125 V/s 16h = 150 V/s 17h = 175 V/s 18h = 200 V/s 19h = 250 V/s 1Ah = 300 V/s 1Bh = 400 V/s 1Ch = 500 V/s 1Dh = 750 V/s 1Eh = 1000 V/s 1Fh = 32767 V/s
23	CL_DEC_CONFIG	R/W	0h	Closed loop decel configuration 0h = Close loop deceleration defined by CL_DEC 1h = Close loop deceleration defined by CL_ACC

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表 8-31. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-18	CL_DEC	R/W	0h	Closed loop deceleration rate 0h = 0.005 V/s 1h = 0.01 V/s 2h = 0.025 V/s 3h = 0.05 V/s 4h = 0.1 V/s 5h = 0.25 V/s 6h = 0.5 V/s 7h = 1 V/s 8h = 2.5 V/s 9h = 5 V/s Ah = 7.5 V/s Bh = 10 V/s Ch = 12.5 V/s Dh = 15 V/s Eh = 20 V/s Fh = 30 V/s 10h = 40 V/s 11h = 50 V/s 12h = 60 V/s 13h = 75 V/s 14h = 100 V/s 15h = 125 V/s 16h = 150 V/s 17h = 175 V/s 18h = 200 V/s 19h = 250 V/s 1Ah = 300 V/s 1Bh = 400 V/s 1Ch = 500 V/s 1Dh = 750 V/s 1Eh = 1000 V/s 1Fh = 32767 V/s

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表 8-31. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-13	PWM_FREQ_OUT	R/W	0h	Output PWM switching frequency 0h = 5 kHz 1h = 6 kHz 2h = 7 kHz 3h = 8 kHz 4h = 9 kHz 5h = 10 kHz 6h = 11 kHz 7h = 12 kHz 8h = 13 kHz 9h = 14 kHz Ah = 15 kHz Bh = 16 kHz Ch = 17 kHz Dh = 18 kHz Eh = 19 kHz Fh = 20 kHz 10h = 25 kHz 11h = 30 kHz 12h = 35 kHz 13h = 40 kHz 14h = 45 kHz 15h = 50 kHz 16h = 55 kHz 17h = 60 kHz 18h = 65 kHz 19h = 70 kHz 1Ah = 75 kHz 1Bh = 80 kHz 1Ch = 85 kHz 1Dh = 90 kHz 1Eh = 95 kHz 1Fh = 100 kHz
12-11	PWM_MODUL	R/W	0h	PWM modulation. 0h = High-Side Modulation 1h = Low-Side Modulation 2h = Mixed Modulation 3h = N/A
10	PWM_MODE	R/W	0h	PWM mode 0h = Single Ended Mode 1h = Complementary Mode
9	LD_ANGLE_POLARITY	R/W	0h	Polarity of applied lead angle 0h = Negative 1h = Positive
8-1	LD_ANGLE	R/W	0h	Lead Angle {Lead Angle (deg) = LD_ANGLE * 0.12}
0	RESERVED	R/W	0h	Reserved

8.7.1.5 CLOSED_LOOP2 Register (Address = 88h) [Reset = 00000000h]

CLOSED_LOOP2 is shown in CLOSED_LOOP2 Register and described in CLOSED_LOOP2 Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure close loop settings2

图 8-58. CLOSED_LOOP2 Register

31	30	29	28	27	26	25	24
PARITY	FG_SEL		FG_DIV_FACTOR				FG_CONFIG
R/W-0h	R/W-0h		R/W-0h				R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FG_BEMF_THR			MTR_STOP			MTR_STOP_BRK_TIME	
R/W-0h			R/W-0h			R/W-0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MTR_STOP_BRK_TIME		ACT_SPIN_BRK_THR			BRAKE_DUTY_THRESHOLD		
R/W-0h		R/W-0h			R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AVS_EN	CBC_ILIMIT				RESERVED		
R/W-0h	R/W-0h				R/W-0h		

表 8-32. CLOSED_LOOP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	FG_SEL	R/W	0h	FG mode select 0h = Output FG in open loop and closed loop 1h = Output FG in only closed loop 2h = Output FG in open loop for the first try. 3h = N/A
28-25	FG_DIV_FACTOR	R/W	0h	FG division factor 0h = Divide by 3 (2-pole motor mechanical speed/3) 1h = Divide by 1 (2-pole motor mechanical speed) 2h = Divide by 2 (4-pole motor mechanical speed) 3h = Divide by 3 (6-pole motor mechanical speed) 4h = Divide by 4 (8-pole motor mechanical speed) 5h = Divide by 5 (10-pole motor mechanical speed) 6h = Divide by 6 (12-pole motor mechanical speed) 7h = Divide by 7 (14-pole motor mechanical speed) 8h = Divide by 8 (16-pole motor mechanical speed) 9h = Divide by 9 (18-pole motor mechanical speed) Ah = Divide by 10 (20-pole motor mechanical speed) Bh = Divide by 11 (22-pole motor mechanical speed) Ch = Divide by 12 (24-pole motor mechanical speed) Dh = Divide by 13 (26-pole motor mechanical speed) Eh = Divide by 14 (28-pole motor mechanical speed) Fh = Divide by 15 (30-pole motor mechanical speed)
24	FG_CONFIG	R/W	0h	FG output configuration 0h = FG active till speed drops below BEMF threshold defined by FG_BEMF_THR 1h = FG active as long as motor is driven

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表 8-32. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-21	FG_BEMF_THR	R/W	0h	FG output BEMF threshold 0h = +/- 1mV 1h = +/- 2mV 2h = +/- 5mV 3h = +/- 10mV 4h = +/- 20mV 5h = +/- 30mV 6h = N/A 7h = N/A
20-18	MTR_STOP	R/W	0h	Motor stop method 0h = Hi-z 1h = Recirculation 2h = Low-side braking 3h = High-side braking 4h = Active spin down 5h = N/A 6h = N/A 7h = N/A
17-14	MTR_STOP_BRK_TIME	R/W	0h	Brake time during motor stop 0h = 1 ms 1h = 2 ms 2h = 5 ms 3h = 10 ms 4h = 15 ms 5h = 25 ms 6h = 50 ms 7h = 75 ms 8h = 100 ms 9h = 250 ms Ah = 500 ms Bh = 1000 ms Ch = 2500 ms Dh = 5000 ms Eh = 10000 ms Fh = 15000 ms
13-11	ACT_SPIN_BRK_THR	R/W	0h	Duty cycle threshold for motor stop using active spin down, low- and high-side braking 0h = Immediate 1h = 50 % 2h = 25 % 3h = 15 % 4h = 10 % 5h = 7.5 % 6h = 5 % 7h = 2.5 %

表 8-32. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	BRAKE_DUTY_THRESHOLD	R/W	0h	Duty cycle threshold for BRAKE pin based low-side braking 0h = Immediate 1h = 50 % 2h = 25 % 3h = 15 % 4h = 10 % 5h = 7.5 % 6h = 5 % 7h = 2.5 %
7	AVS_EN	R/W	0h	AVS enable 0h = Disable 1h = Enable
6-3	CBC_ILIMIT	R/W	0h	Cycle by Cycle (CBC) current limit (CBC current limit (A) = CBC_ILIMIT / CSA_GAIN) 0h = N/A 1h = 0.1 V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V
2-0	RESERVED	R/W	0h	Reserved

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8.7.1.6 CLOSED_LOOP3 Register (Address = 8Ah) [Reset = 14000000h]

CLOSED_LOOP3 is shown in CLOSED_LOOP3 Register and described in CLOSED_LOOP3 Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure close loop settings3

图 8-59. CLOSED_LOOP3 Register

31	30	29	28	27	26	25	24
PARITY	DYN_DGS_FILT_COUNT		DYN_DGS_UPPER_LIM		DYN_DGS_LOWER_LIM		INTEG_CYCL_THR_LOW
R/W-0h	R/W-0h		R/W-2h		R/W-2h		R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTEG_CYCL_THR_LOW	INTEG_CYCL_THR_HIGH		INTEG_DUTY_THR_LOW		INTEG_DUTY_THR_HIGH		BEMF_THRESHOLD2
R/W-0h	R/W-0h		R/W-0h		R/W-0h		R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BEMF_THRESHOLD2					BEMF_THRESHOLD1		
R/W-0h					R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BEMF_THRESHOLD1			INTEG_ZC_METHOD	DEGAUSS_MAX_WIN			DYN_DEGAUSS_EN
R/W-0h			R/W-0h	R/W-0h			R/W-0h

表 8-33. CLOSED_LOOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	DYN_DGS_FILT_COUNT	R/W	0h	Number of samples needed for dynamic degauss check 0h = 2 1h = 3 2h = 4 3h = 5
28-27	DYN_DGS_UPPER_LIM	R/W	2h	Dynamic degauss voltage upper bound 0h = (VM - 0.09) V 1h = (VM - 0.12) V 2h = (VM - 0.15) V 3h = (VM - 0.18) V
26-25	DYN_DGS_LOWER_LIM	R/W	2h	Dynamic degauss voltage lower bound 0h = 0.03 V 1h = 0.06 V 2h = 0.09 V 3h = 0.12 V
24-23	INTEG_CYCL_THR_LOW	R/W	0h	Number of BEMF samples per 30° below which commutation method switches from integration to ZC 0h = 3 1h = 4 2h = 6 3h = 8

表 8-33. CLOSED_LOOP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-21	INTEG_CYCL_THR_HIGH	R/W	0h	Number of BEMF samples per 30° above which commutation method switches from ZC to integration 0h = 4 1h = 6 2h = 8 3h = 10
20-19	INTEG_DUTY_THR_LOW	R/W	0h	Duty cycle below which commutation method switches from integration to ZC 0h = 12 % 1h = 15 % 2h = 18 % 3h = 20 %
18-17	INTEG_DUTY_THR_HIGH	R/W	0h	Duty cycle above which commutation method switches from ZC to integration 0h = 12 % 1h = 15 % 2h = 18 % 3h = 20 %

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表 8-33. CLOSED_LOOP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-11	BEMF_THRESHOLD2	R/W	0h	BEMF threshold for integration based commutation during falling floating phase voltage 0h = 0 1h = 25 2h = 50 3h = 75 4h = 100 5h = 125 6h = 150 7h = 175 8h = 200 9h = 225 Ah = 250 Bh = 275 Ch = 300 Dh = 325 Eh = 350 Fh = 375 10h = 400 11h = 425 12h = 450 13h = 475 14h = 500 15h = 525 16h = 550 17h = 575 18h = 600 19h = 625 1Ah = 650 1Bh = 675 1Ch = 700 1Dh = 725 1Eh = 750 1Fh = 775 20h = 800 21h = 850 22h = 900 23h = 950 24h = 1000 25h = 1050 26h = 1100 27h = 1150 28h = 1200 29h = 1250 2Ah = 1300 2Bh = 1350 2Ch = 1400 2Dh = 1450 2Eh = 1500 2Fh = 1550 30h = 1600 31h = 1700 32h = 1800

表 8-33. CLOSED_LOOP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				33h = 1900 34h = 2000 35h = 2100 36h = 2200 37h = 2300 38h = 2400 39h = 2600 3Ah = 2800 3Bh = 3000 3Ch = 3200 3Dh = 3400 3Eh = 3600 3Fh = 3800

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表 8-33. CLOSED_LOOP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-5	BEMF_THRESHOLD1	R/W	0h	BEMF threshold for integration based commutation during rising floating phase voltage 0h = 0 1h = 25 2h = 50 3h = 75 4h = 100 5h = 125 6h = 150 7h = 175 8h = 200 9h = 225 Ah = 250 Bh = 275 Ch = 300 Dh = 325 Eh = 350 Fh = 375 10h = 400 11h = 425 12h = 450 13h = 475 14h = 500 15h = 525 16h = 550 17h = 575 18h = 600 19h = 625 1Ah = 650 1Bh = 675 1Ch = 700 1Dh = 725 1Eh = 750 1Fh = 775 20h = 800 21h = 850 22h = 900 23h = 950 24h = 1000 25h = 1050 26h = 1100 27h = 1150 28h = 1200 29h = 1250 2Ah = 1300 2Bh = 1350 2Ch = 1400 2Dh = 1450 2Eh = 1500 2Fh = 1550 30h = 1600 31h = 1700 32h = 1800

表 8-33. CLOSED_LOOP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				33h = 1900 34h = 2000 35h = 2100 36h = 2200 37h = 2300 38h = 2400 39h = 2600 3Ah = 2800 3Bh = 3000 3Ch = 3200 3Dh = 3400 3Eh = 3600 3Fh = 3800
4	INTEG_ZC_METHOD	R/W	0h	Commutation method select 0h = ZC based 1h = Integration based
3-1	DEGAUSS_MAX_WIN	R/W	0h	Maximum degauss window 0h = 22.5° 1h = 10° 2h = 15° 3h = 18° 4h = 30° 5h = 37.5° 6h = 45° 7h = 60°
0	DYN_DEGAUSS_EN	R/W	0h	Dynamic degauss detection 0h = Disable 1h = Enable

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8.7.1.7 CLOSED_LOOP4 Register (Address = 8Ch) [Reset = 00000000h]

CLOSED_LOOP4 is shown in CLOSED_LOOP4 Register and described in CLOSED_LOOP4 Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure close loop settings4

图 8-60. CLOSED_LOOP4 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED				WCOMP_BLANK_EN	FAST_DEC_DUTY_WIN		
R/W-0h				R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
FAST_DEC_DUTY_THR			DYN_BRK_CURR_LOW_LIM				DYNAMIC_BRK_CURR
R/W-0h			R/W-0h				R/W-0h
7	6	5	4	3	2	1	0
FAST_DECEL_EN	FAST_DECEL_CURR_LIM				FAST_BRK_DELTA		
R/W-0h	R/W-0h				R/W-0h		

表 8-34. CLOSED_LOOP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-20	RESERVED	R/W	0h	Reserved
19	WCOMP_BLANK_EN	R/W	0h	Enable WCOMP blanking during fast deceleration 0h = Disable 1h = Enable
18-16	FAST_DEC_DUTY_WIN	R/W	0h	Fast deceleration duty window 0h = 0 % 1h = 2.5 % 2h = 5 % 3h = 7.5 % 4h = 10 % 5h = 15 % 6h = 20 % 7h = 25 %
15-13	FAST_DEC_DUTY_THR	R/W	0h	Fast deceleration duty threshold 0h = 100 % 1h = 95 % 2h = 90 % 3h = 85 % 4h = 80 % 5h = 75 % 6h = 70% 7h = 65 %

表 8-34. CLOSED_LOOP4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-9	DYN_BRK_CURR_LOW_LIM	R/W	0h	Fast deceleration dynamic current limit lower threshold (Deceleration current lower threshold (A) = DYN_BRK_CURR_LOW_LIM / CSA_GAIN) 0h = N/A 1h = 0.1V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V
8	DYNAMIC_BRK_CURR	R/W	0h	Enable dynamic decrease in current limit during fast deceleration 0h = Disable 1h = Enable
7	FAST_DECEL_EN	R/W	0h	Fast deceleration enable 0h = Disable 1h = Enable
6-3	FAST_DECEL_CURR_LIM	R/W	0h	Deceleration current threshold (Fast Deceleration current limit upper threshold (A) = FAST_DECEL_CURR_LIM / CSA_GAIN) 0h = N/A 1h = 0.1V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V
2-0	FAST_BRK_DELTA	R/W	0h	Fast deceleration exit speed delta 0h = 0.5 % 1h = 1 % 2h = 1.5 % 3h = 2 % 4h = 2.5 % 5h = 3 % 6h = 4 % 7h = 5 %

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8.7.1.8 CONST_SPEED Register (Address = 8Eh) [Reset = 00000000h]

CONST_SPEED is shown in CONST_SPEED Register and described in CONST_SPEED Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure Constant speed mode settings

图 8-61. CONST_SPEED Register

31	30	29	28	27	26	25	24
PARITY	RESERVED	SPD_POWER_KP					
R/W-0h	R/W-0h	R/W-0h					

23	22	21	20	19	18	17	16
SPD_POWER_KP				SPD_POWER_KI			
R/W-0h				R/W-0h			

15	14	13	12	11	10	9	8
SPD_POWER_KI							
R/W-0h							

7	6	5	4	3	2	1	0
SPD_POWER_V_MAX			SPD_POWER_V_MIN			CLOSED_LOOP_MODE	
R/W-0h			R/W-0h			R/W-0h	

表 8-35. CONST_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	RESERVED	R/W	0h	Reserved
29-20	SPD_POWER_KP	R/W	0h	Speed/ Power loop Kp (Kp = SPD_LOOP_KP / 10000)
19-8	SPD_POWER_KI	R/W	0h	Speed/ Power loop Ki (Ki = SPD_LOOP_KI / 1000000)
7-5	SPD_POWER_V_MAX	R/W	0h	Upper saturation limit for speed/ power loop 0h = 100 % 1h = 95 % 2h = 90 % 3h = 85 % 4h = 80 % 5h = 75 % 6h = 70% 7h = 65 %
4-2	SPD_POWER_V_MIN	R/W	0h	Lower saturation limit for speed/power loop 0h = 0 % 1h = 2.5 % 2h = 5 % 3h = 7.5 % 4h = 10 % 5h = 15 % 6h = 20 % 7h = 25 %
1-0	CLOSED_LOOP_MODE	R/W	0h	Closed loop mode 0h = Disabled 1h = Speed Loop 2h = Power Loop 3h = Reserved

8.7.1.9 CONST_PWR Register (Address = 90h) [Reset = 00000000h]

CONST_PWR is shown in CONST_PWR Register and described in CONST_PWR Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure Constant power mode settings

图 8-62. CONST_PWR Register

31	30	29	28	27	26	25	24
PARITY	MAX_SPEED						
R/W-0h	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAX_SPEED							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX_SPEED	DEADTIME_COMP_EN	MAX_POWER					
R/W-0h	R/W-0h	R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX_POWER				CONST_POWER_LIMIT_HYST		CONST_POWER_MODE	
R/W-0h				R/W-0h		R/W-0h	

表 8-36. CONST_PWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-15	MAX_SPEED	R/W	0h	Maximum Speed (Maximum Speed (Hz) = MAX_SPEED / 16)
14	DEADTIME_COMP_EN	R/W	0h	Enable dead time compensation 0h = Disable 1h = Enable
13-4	MAX_POWER	R/W	0h	Maximum power (Maximum power (W) = MAX_POWER / 4)
3-2	CONST_POWER_LIMIT_HYST	R/W	0h	Hysteresis for input power regulation 0h = 5 % 1h = 7.5 % 2h = 10 % 3h = 12.5 %
1-0	CONST_POWER_MODE	R/W	0h	Input power regulation mode 0h = Disabled 1h = Closed Loop Power Control 2h = Power Limit Control 3h = Reserved

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8.7.1.10 150_DEG_TWO_PH_PROFILE Register (Address = 96h) [Reset = 00000000h]

150_DEG_TWO_PH_PROFILE is shown in 150_DEG_TWO_PH_PROFILE Register and described in 150_DEG_TWO_PH_PROFILE Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure 150 degree modulation TWO phase duty

图 8-63. 150_DEG_TWO_PH_PROFILE Register

31	30	29	28	27	26	25	24
PARITY	TWOPH_STEP0			TWOPH_STEP1			TWOPH_STEP 2
R/W-0h	R/W-0h			R/W-0h			R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TWOPH_STEP2		TWOPH_STEP3			TWOPH_STEP4		
R/W-0h		R/W-0h			R/W-0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TWOPH_STEP5			TWOPH_STEP6			TWOPH_STEP7	
R/W-0h			R/W-0h			R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TWOPH_STEP 7	RESERVED						
R/W-0h	R/W-0h						

表 8-37. 150_DEG_TWO_PH_PROFILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	TWOPH_STEP0	R/W	0h	150° modulation , Two ph. - step duty - 0 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
27-25	TWOPH_STEP1	R/W	0h	150° modulation , Two ph. - step duty - 1 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %

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表 8-37. 150_DEG_TWO_PH_PROFILE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	TWOPH_STEP2	R/W	0h	150° modulation, Two ph. - step duty - 2 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
21-19	TWOPH_STEP3	R/W	0h	150° modulation, Two ph. - step duty - 3 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
18-16	TWOPH_STEP4	R/W	0h	150° modulation, Two ph. - step duty - 4 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
15-13	TWOPH_STEP5	R/W	0h	150° modulation, Two ph. - step duty - 5 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
12-10	TWOPH_STEP6	R/W	0h	150° modulation, Two ph. - step duty - 6 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %

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表 8-37. 150_DEG_TWO_PH_PROFILE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-7	TWOPH_STEP7	R/W	0h	150° modulation, Two ph. - step duty - 7 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
6-0	RESERVED	R/W	0h	reserved bits for algo parameter update

8.7.1.11 150_DEG_THREE_PH_PROFILE Register (Address = 98h) [Reset = 00000000h]

150_DEG_THREE_PH_PROFILE is shown in 150_DEG_THREE_PH_PROFILE Register and described in 150_DEG_THREE_PH_PROFILE Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure 150 degree modulation Three phase duty

图 8-64. 150_DEG_THREE_PH_PROFILE Register

31	30	29	28	27	26	25	24
PARITY	THREEPH_STEP0			THREEPH_STEP1			THREEPH_STEP2
R/W-0h	R/W-0h			R/W-0h			R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
THREEPH_STEP2		THREEPH_STEP3			THREEPH_STEP4		
R/W-0h		R/W-0h			R/W-0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
THREEPH_STEP5			THREEPH_STEP6			THREEPH_STEP7	
R/W-0h			R/W-0h			R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
THREEPH_STEP7	LEAD_ANGLE_150DEG_ADV		RESERVED				
R/W-0h	R/W-0h		R/W-0h				

表 8-38. 150_DEG_THREE_PH_PROFILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	THREEPH_STEP0	R/W	0h	150° modulation, Three ph. - step duty - 0 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
27-25	THREEPH_STEP1	R/W	0h	150° modulation, Three ph. - step duty - 1 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %

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表 8-38. 150_DEG_THREE_PH_PROFILE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	THREEPH_STEP2	R/W	0h	150° modulation, Three ph. - step duty - 2 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
21-19	THREEPH_STEP3	R/W	0h	150° modulation, Three ph. - step duty - 3 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
18-16	THREEPH_STEP4	R/W	0h	150° modulation, Three ph. - step duty - 4 0h = 0.0 % 1h = 0.5 % 2h = 0.75 % 3h = 0.8375 % 4h = 0.875 % 5h = 0.9375 % 6h = 0.975 % 7h = 0.99 %
15-13	THREEPH_STEP5	R/W	0h	150° modulation, Three ph. - step duty - 5 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
12-10	THREEPH_STEP6	R/W	0h	150° modulation, Three ph. - step duty - 6 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %

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表 8-38. 150_DEG_THREE_PH_PROFILE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-7	THREEPH_STEP7	R/W	0h	150° modulation, Three ph. - step duty - 7 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
6-5	LEAD_ANGLE_150DEG_ADV	R/W	0h	Angle advance for 150° modulation 0h = 0° 1h = 5° 2h = 10° 3h = 15°
4-0	RESERVED	R/W	0h	Reserved

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8.7.1.12 TRAP_CONFIG1 Register (Address = 9Ah) [Reset = 00000000h]

TRAP_CONFIG1 is shown in TRAP_CONFIG1 Register and described in TRAP_CONFIG1 Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure internal Algorithm Variables

图 8-65. TRAP_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED		RESERVED			RESERVED	
R/W-0h	R/W-0h		R/W-0h			R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OL_HANDOFF_CYCLES		RESERVED			AVS_NEG_CURR_LIMIT		
R/W-0h		R/W-0h			R/W-0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AVS_LIMIT_HYST	ISD_BEMF_THR					ISD_CYCLE_THR	
R/W-0h	R/W-0h					R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ISD_CYCLE_THR	RESERVED	RESERVED		ZC_ANGLE_OL_THR		FAST_STARTUP_DIV_FACTOR	
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	

表 8-39. TRAP_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	RESERVED	R/W	0h	Reserved
28-26	RESERVED	R/W	0h	Reserved
25-24	RESERVED	R/W	0h	Reserved
23-22	OL_HANDOFF_CYCLES	R/W	0h	Open loop handoff cycles 0h = 3 1h = 6 2h = 12 3h = 24
21-19	RESERVED	R/W	0h	Reserved
18-16	AVS_NEG_CURR_LIMIT	R/W	0h	AVS negative current limit (AVS negative current limit (A) = (AVS_NEG_CURRENT_LIMIT * 3 /4095) / CSA_GAIN) 0h = 0 1h = -40 2h = -30 3h = -20 4h = -10 5h = 10 6h = 20 7h = 30
15	AVS_LIMIT_HYST	R/W	0h	AVS current hysteresis (AVS positive current limit (A) = ((AVS_LIMIT_HYST + AVS_NEG_CURR_LIMIT) * 3 /4095) / CSA_GAIN) 0h = 20 1h = 10

表 8-39. TRAP_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-10	ISD_BEMF_THR	R/W	0h	ISD BEMF threshold (ISD BEMF threshold = 200 * ISD_BEMF_THR) 0h = 0 1h = 200 2h = 400 3h = 600 4h = 800 5h = 1000 6h = 1200 7h = 1400 8h = 1600 9h = 1800 Ah = 2000 Bh = 2200 Ch = 2400 Dh = 2600 Eh = 2800 Fh = 3000 10h = 3200 11h = 3400 12h = 3600 13h = 3800 14h = 4000 15h = 4200 16h = 4400 17h = 4600 18h = 4800 19h = 5000 1Ah = 5200 1Bh = 5400 1Ch = 5600 1Dh = 5800 1Eh = 6000 1Fh = 6200
9-7	ISD_CYCLE_THR	R/W	0h	ISD cycle threshold 0h = 2, 1h = 5, 2h = 8, 3h = 11, 4h = 14, 5h = 17, 6h = 20, 7h = 23
6	RESERVED	R/W	0h	Reserved
5-4	RESERVED	R/W	0h	Reserved
3-2	ZC_ANGLE_OL_THR	R/W	0h	Angle above which the ZC detection is done during OL 0h = 5° 1h = 8° 2h = 12° 3h = 15°

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表 8-39. TRAP_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	FAST_STARTUP_DIV_FACTOR	R/W	0h	Dynamic A1, A2 change rate 0h = 1 1h = 2 2h = 4 3h = 8

8.7.1.13 TRAP_CONFIG2 Register (Address = 9Ch) [Reset = 00200000h]

TRAP_CONFIG2 is shown in TRAP_CONFIG2 Register and described in TRAP_CONFIG2 Register Field Descriptions.

Return to the ALGORITHM_CONFIGURATION Registers.

Register to configure internal Algorithm Variables

图 8-66. TRAP_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	TBLANK				TPWDTH		
R/W-0h	R/W-0h				R/W-0h		

23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	ALIGN_DUTY			RESERVED	
R/W-0h	R/W-0h	R/W-1h	R/W-0h			R/W-0h	

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

表 8-40. TRAP_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	TBLANK	R/W	0h	Blanking time after PWM edge 0h = 0 µs 1h = 1 µs 2h = 2 µs 3h = 3 µs 4h = 4 µs 5h = 5 µs 6h = 6 µs 7h = 7 µs 8h = 8 µs 9h = 9 µs Ah = 10 µs Bh = 11 µs Ch = 12 µs Dh = 13 µs Eh = 14 µs Fh = 15 µs
26-24	TPWDTH	R/W	0h	Comparator deglitch time 0h = 0 µs 1h = 1 µs 2h = 2 µs 3h = 3 µs 4h = 4 µs 5h = 5 µs 6h = 6 µs 7h = 7 µs
23	RESERVED	R/W	0h	Reserved

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表 8-40. TRAP_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	1h	Reserved
20-18	ALIGN_DUTY	R/W	0h	Duty cycle limit during align 0h = 10 % 1h = 15 % 2h = 20 % 3h = 25 % 4h = 30 % 5h = 40 % 6h = 50 % 7h = 100 %
17-0	RESERVED	R/W	0h	Reserved

8.7.2 Fault_Configuration Registers

FAULT_CONFIGURATION Registers lists the memory-mapped registers for the Fault_Configuration registers. All register offset addresses not listed in FAULT_CONFIGURATION Registers should be considered as reserved locations and the register contents should not be modified.

表 8-41. FAULT_CONFIGURATION Registers

Address	Acronym	Register Name	Section
92h	FAULT_CONFIG1	Fault configuration 1	节 8.7.2.1
94h	FAULT_CONFIG2	Fault configuration 2	节 8.7.2.2

Complex bit access types are encoded to fit into small table cells. Fault_Configuration Access Type Codes shows the codes that are used for access types in this section.

表 8-42. Fault_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

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8.7.2.1 FAULT_CONFIG1 Register (Address = 92h) [Reset = 00000000h]

FAULT_CONFIG1 is shown in FAULT_CONFIG1 Register and described in FAULT_CONFIG1 Register Field Descriptions.

Return to the FAULT_CONFIGURATION Registers.

Register to configure fault settings1

图 8-67. FAULT_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED	NO_MTR_DEG_TIME			CBC_ILIMIT_MODE		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CBC_ILIMIT_MODE	LOCK_ILIMIT				LOCK_ILIMIT_MODE		
R/W-0h	R/W-0h				R/W-0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK_ILIMIT_MODE	LOCK_ILIMIT_DEG				CBC_RETRY_PWM_CYC		
R/W-0h	R/W-0h				R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	MTR_LCK_MODE				LCK_RETRY		
R/W-0h	R/W-0h				R/W-0h		

表 8-43. FAULT_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	RESERVED	R/W	0h	Reserved
29-27	NO_MTR_DEG_TIME	R/W	0h	No motor detect deglitch time 0h = 1 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms

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表 8-43. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	CBC_ILIMIT_MODE	R/W	0h	Cycle by cycle current limit 0h = Automatic recovery next PWM cycle; nFAULT active; driver is in recirculation mode 1h = Automatic recovery next PWM cycle; nFAULT inactive; driver is in recirculation mode 2h = Automatic recovery if VSOX < ILIMIT; nFAULT active; driver is in recirculation mode (Only available with high-side modulation) 3h = Automatic recovery if VSOX < ILIMIT; nFAULT inactive; driver is in recirculation mode (Only available with high-side modulation) 4h = Automatic recovery after CBC_RETRY_PWM_CYC; nFAULT active; driver is in recirculation mode 5h = Automatic recovery after CBC_RETRY_PWM_CYC; nFAULT inactive; driver is in recirculation mode 6h = VSOX > ILIMIT is report only but no action is taken 7h = Cycle by Cycle limit is disabled 8h = Cycle by Cycle limit is disabled 9h = Cycle by Cycle limit is disabled Ah = Cycle by Cycle limit is disabled Bh = Cycle by Cycle limit is disabled Ch = Cycle by Cycle limit is disabled Dh = Cycle by Cycle limit is disabled Eh = Cycle by Cycle limit is disabled Fh = Cycle by Cycle limit is disabled
22-19	LOCK_ILIMIT	R/W	0h	Lock detection current limit (Lock detection current limit (A) = LOCK_ILIMIT / CSA_GAIN) 0h = N/A 1h = 0.1 V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V

表 8-43. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	LOCK_ILIMIT_MODE	R/W	0h	Lock detection current limit mode 0h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode 2h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high-side brake mode (All high-side FETs are turned ON) 3h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low-side brake mode (All low-side FETs are turned ON) 4h = Automatic recovery after tLCK_RETRY; Gate driver is tristated 5h = Automatic recovery after tLCK_RETRY; Gate driver is in recirculation mode 6h = Automatic recovery after tLCK_RETRY; Gate driver is in high-side brake mode (All high-side FETs are turned ON) 7h = Automatic recovery after tLCK_RETRY; Gate driver is in low-side brake mode (All low-side FETs are turned ON) 8h = Ilimit lock detection is in report only but no action is taken 9h = Ilimit lock detection is disabled Ah = Ilimit lock detection is disabled Bh = Ilimit lock detection is disabled Ch = Ilimit lock detection is disabled Dh = Ilimit lock detection is disabled Eh = Ilimit lock detection is disabled Fh = Ilimit lock detection is disabled
14-11	LOCK_ILIMIT_DEG	R/W	0h	Lock detection current limit deglitch time 0h = 1 ms 1h = 2 ms 2h = 5 ms 3h = 10 ms 4h = 25 ms 5h = 50 ms 6h = 75 ms 7h = 100 ms 8h = 250 ms 9h = 500 ms Ah = 1 s Bh = 2.5 s Ch = 5 s Dh = 10 s Eh = 25 s Fh = 50 s
10-8	CBC_RETRY_PWM_CYC	R/W	0h	Number of PWM cycles for CBC current limit to retry 0h = 0 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7
7	RESERVED	R/W	0h	Reserved

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表 8-43. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-3	MTR_LCK_MODE	R/W	0h	Motor lock mode 0h = Motor lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode 2h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in high-side brake mode (All high-side FETs are turned ON) 3h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in low-side brake mode (All low-side FETs are turned ON) 4h = Automatic recovery after tLCK_RETRY; Gate driver is tristated 5h = Automatic recovery after tLCK_RETRY; Gate driver is in recirculation mode 6h = Automatic recovery after tLCK_RETRY; Gate driver is in high-side brake mode (All high-side FETs are turned ON) 7h = Automatic recovery after tLCK_RETRY; Gate driver is in low-side brake mode (All low-side FETs are turned ON) 8h = Motor lock detection is in report only but no action is taken 9h = Motor lock detection is disabled Bh = Motor lock detection is disabled Ch = Motor lock detection is disabled Dh = Motor lock detection is disabled Eh = Motor lock detection is disabled Fh = Motor lock detection is disabled
2-0	LCK_RETRY	R/W	0h	Lock retry time 0h = 100 ms 1h = 500 ms 2h = 1000 ms 3h = 2000 ms 4h = 3000 ms 5h = 5000 ms 6h = 7500 ms 7h = 10000 ms

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8.7.2.2 FAULT_CONFIG2 Register (Address = 94h) [Reset = 00000000h]

FAULT_CONFIG2 is shown in FAULT_CONFIG2 Register and described in FAULT_CONFIG2 Register Field Descriptions.

Return to the FAULT_CONFIGURATION Registers.

Register to configure fault settings2

图 8-68. FAULT_CONFIG2 Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>PARITY</td><td>LOCK1_EN</td><td>LOCK2_EN</td><td>LOCK3_EN</td><td colspan="4">LOCK_ABN_SPEED</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td colspan="4">R/W-0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="3">LOSS_SYNC_TIMES</td><td colspan="3">NO_MTR_THR</td><td>MAX_VM_MODE</td><td>MAX_VM_MOTOR</td></tr>
<tr><td colspan="3">R/W-0h</td><td colspan="3">R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">MAX_VM_MOTOR</td><td>MIN_VM_MODE</td><td colspan="3">MIN_VM_MOTOR</td><td colspan="2">AUTO_RETRY_TIMES</td></tr>
<tr><td colspan="2">R/W-0h</td><td>R/W-0h</td><td colspan="3">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>AUTO_RETRY_TIMES</td><td colspan="3">LOCK_MIN_SPEED</td><td colspan="2">ABN_LOCK_SPD_RATIO</td><td colspan="2">ZERO_DUTY_THR</td></tr>
<tr><td>R/W-0h</td><td colspan="3">R/W-0h</td><td colspan="2">R/W-0h</td><td colspan="2">R/W-0h</td></tr>
</table>

表 8-44. FAULT_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	LOCK1_EN	R/W	0h	Lock 1 (Abnormal Speed) Enable 0h = Disable 1h = Enable
29	LOCK2_EN	R/W	0h	Lock 2 (Loss of Sync) Enable 0h = Disable 1h = Enable
28	LOCK3_EN	R/W	0h	Lock 3 (No Motor) Enable 0h = Disable 1h = Enable

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表 8-44. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-24	LOCK_ABN_SPEED	R/W	0h	Abnormal speed lock threshold 0h = 250 Hz 1h = 500 Hz 2h = 750 Hz 3h = 1000 Hz 4h = 1250 Hz 5h = 1500 Hz 6h = 1750 Hz 7h = 2000 Hz 8h = 2250 Hz 9h = 2500 Hz Ah = 2750 Hz Bh = 3000 Hz Ch = 3250 Hz Dh = 3500 Hz Eh = 3750 Hz Fh = 4000 Hz
23-21	LOSS_SYNC_TIMES	R/W	0h	Number of times sync lost for loss of sync lock fault 0h = Trigger after losing sync 2 times 1h = Trigger after losing sync 3 times 2h = Trigger after losing sync 4 times 3h = Trigger after losing sync 5 times 4h = Trigger after losing sync 6 times 5h = Trigger after losing sync 7 times 6h = Trigger after losing sync 8 times 7h = Trigger after losing sync 9 times
20-18	NO_MTR_THR	R/W	0h	No motor lock current threshold (No motor lock current threshold (A) = NO_MTR_THR / CSA_GAIN) 0h = 0.005 V 1h = 0.0075 V 2h = 0.010 V 3h = 0.0125 V 4h = 0.020 V 5h = 0.025 V 6h = 0.030 V 7h = 0.04 V
17	MAX_VM_MODE	R/W	0h	0h = Latch on Overvoltage 1h = Automatic clear if voltage in bounds
16-14	MAX_VM_MOTOR	R/W	0h	Maximum voltage for running motor 0h = No Limit 1h = 20.0 V 2h = 25.0 V 3h = 30.0 V 4h = 35.0 V 5h = 40.0 V 6h = 50.0 V 7h = 60.0 V
13	MIN_VM_MODE	R/W	0h	0h = Latch on Undervoltage 1h = Automatic clear if voltage in bounds

表 8-44. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	MIN_VM_MOTOR	R/W	0h	Minimum voltage for running motor 0h = No Limit 1h = 6.0 V 2h = 7.0 V 3h = 8.0 V 4h = 9.0 V 5h = 10.0 V 6h = 12.0 V 7h = 15.0 V
9-7	AUTO_RETRY_TIMES	R/W	0h	Number of automatic retry attempts 0h = No Limit 1h = 2 2h = 3 3h = 5 4h = 7 5h = 10 6h = 15 7h = 20
6-4	LOCK_MIN_SPEED	R/W	0h	Speed below which lock fault is triggered 0h = 0.5 Hz 1h = 1 Hz 2h = 2 Hz 3h = 3 Hz 4h = 5 Hz 5h = 10 Hz 6h = 15 Hz 7h = 25 Hz
3-2	ABN_LOCK_SPD_RATIO	R/W	0h	Ratio of electrical speed between two consecutive cycles above which abnormal speed lock fault is triggered 0h = 2 1h = 4 2h = 6 3h = 8
1-0	ZERO_DUTY_THR	R/W	0h	Duty cycle below which target speed is zero 0h = 1% 1h = 1.5% 2h = 2.0% 3h = 2.5%

8.7.3 Hardware_Configuration Registers

HARDWARE_CONFIGURATION Registers lists the memory-mapped registers for the Hardware_Configuration registers. All register offset addresses not listed in HARDWARE_CONFIGURATION Registers should be considered as reserved locations and the register contents should not be modified.

表 8-45. HARDWARE_CONFIGURATION Registers

Address	Acronym	Register Name	Section
A4h	PIN_CONFIG1	Hardware pin configuration	节 8.7.3.1
A6h	PIN_CONFIG2	Hardware pin configuration	节 8.7.3.2
A8h	DEVICE_CONFIG	Device configuration	节 8.7.3.3

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Complex bit access types are encoded to fit into small table cells. Hardware_Configuration Access Type Codes shows the codes that are used for access types in this section.

表 8-46. Hardware_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

8.7.3.1 PIN_CONFIG1 Register (Address = A4h) [Reset = 00000000h]

PIN_CONFIG1 is shown in PIN_CONFIG1 Register and described in PIN_CONFIG1 Register Field Descriptions.

Return to the HARDWARE_CONFIGURATION Registers.

Register to configure hardware pins

图 8-69. PIN_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	DACOUT1_VAR_ADDR						
R/W-0h	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DACOUT1_VAR_ADDR					DACOUT2_VAR_ADDR		
R/W-0h					R/W-0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DACOUT2_VAR_ADDR							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACOUT2_VAR_ADDR	BRAKE_INPUT		DIR_INPUT		SPD_CTRL_MODE		RESERVED
R/W-0h	R/W-0h		R/W-0h		R/W-0h		R/W-0h

表 8-47. PIN_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-19	DACOUT1_VAR_ADDR	R/W	0h	12-bit address of variable to be monitored
18-7	DACOUT2_VAR_ADDR	R/W	0h	12-bit address of variable to be monitored
6-5	BRAKE_INPUT	R/W	0h	Brake input configuration 0h = Hardware Pin BRAKE 1h = Overwrite Hardware pin with Active Brake 2h = Overwrite Hardware pin with brake functionality disabled 3h = N/A
4-3	DIR_INPUT	R/W	0h	Direction input configuration 0h = Hardware Pin DIR 1h = Overwrite Hardware pin with clockwise rotation OUTA-OUTB-OUTC 3h = N/A
2-1	SPD_CTRL_MODE	R/W	0h	Speed input configuration 0h = Analog mode speed Input 1h = PWM Mode Speed Input 2h = I2C Speed Input mode 3h = Frequency based speed Input mode
0	RESERVED	R/W	0h	Reserved

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8.7.3.2 PIN_CONFIG2 Register (Address = A6h) [Reset = 00000000h]

PIN_CONFIG2 is shown in PIN_CONFIG2 Register and described in PIN_CONFIG2 Register Field Descriptions.

Return to the HARDWARE_CONFIGURATION Registers.

Register to configure hardware pins

图 8-70. PIN_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	DAC_SOX_CONFIG		RESERVED	DAC_XTAL_CONFIG	RESERVED		
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				SLEEP_TIME		EXT_WD_EN	EXT_WD_INPUT
R/W-0h				R/W-0h		R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXT_WD_FAULT	EXT_WD_FREQ		RESERVED				
R/W-0h	R/W-0h		R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

表 8-48. PIN_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	DAC_SOX_CONFIG	R/W	0h	Pin 36 configuration 0h = DACOUT2 1h = SOA 2h = SOB 3h = SOC
28	RESERVED	R/W	0h	Reserved
27	DAC_XTAL_CONFIG	R/W	0h	Pin 37 and pin 38 configuration 0h = N/A 1h = Pin 37 as DACOUT1 and pin 38 as DACOUT2
26-20	RESERVED	R/W	0h	Reserved
19-18	SLEEP_TIME	R/W	0h	Sleep Time 0h = Check low for 50 µs 1h = Check low for 200 µs 2h = Check low for 20 ms 3h = Check low for 200 ms
17	EXT_WD_EN	R/W	0h	Enable external watchdog 0h = Disable 1h = Enable
16	EXT_WD_INPUT	R/W	0h	External watchdog source 0h = I2C 1h = GPIO
15	EXT_WD_FAULT	R/W	0h	External watchdog fault mode 0h = Report only 1h = Latched fault with Hi-Z outputs

表 8-48. PIN_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-13	EXT_WD_FREQ	R/W	0h	External watchdog frequency 0h = 10Hz 1h = 5Hz 2h = 2Hz 3h = 1Hz
12-0	RESERVED	R/W	0h	Reserved

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8.7.3.3 DEVICE_CONFIG Register (Address = A8h) [Reset = 00000000h]

DEVICE_CONFIG is shown in DEVICE_CONFIG Register and described in DEVICE_CONFIG Register Field Descriptions.

Return to the HARDWARE_CONFIGURATION Registers.

Register to configure device

图 8-71. DEVICE_CONFIG Register

31	30	29	28	27	26	25	24
PARITY	INPUT_MAX_FREQUENCY						
R/W-0h	R/W-0h						

23	22	21	20	19	18	17	16
INPUT_MAX_FREQUENCY							
R/W-0h							

15	14	13	12	11	10	9	8
STL_ENABLE	SSM_CONFIG	RESERVED		DEV_MODE	SPD_PWM_RANGE_SELECT	CLK_SEL	
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	

7	6	5	4	3	2	1	0
RESERVED	EXT_CLK_EN	EXT_CLK_CONFIG			RESERVED		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

表 8-49. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-16	INPUT_MAX_FREQUENCY	R/W	0h	Maximum frequency (in Hz) for frequency based speed input
15	STL_ENABLE	R/W	0h	STL enable 0h = Disable 1h = Enable
14	SSM_CONFIG	R/W	0h	SSM enable 0h = Enable 1h = Disable
13-12	RESERVED	R/W	0h	Reserved
11	DEV_MODE	R/W	0h	Device mode select 0h = Standby mode 1h = Sleep mode
10	SPD_PWM_RANGE_SELECT	R/W	0h	PWM frequency range select 0h = 325 Hz to 95 kHz speed PWM input 1h = 10 Hz to 325 Hz speed PWM input
9-8	CLK_SEL	R/W	0h	Clock source 0h = Internal Oscillator 1h = N/A 2h = N/A 3h = External Clock input
7	RESERVED	R/W	0h	Reserved
6	EXT_CLK_EN	R/W	0h	External clock enable 0h = Disable 1h = Enable

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表 8-49. DEVICE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	EXT_CLK_CONFIG	R/W	0h	External clock frequency 0h = 8 kHz 1h = 16 kHz 2h = 32 kHz 3h = 64 kHz 4h = 128 kHz 5h = 256 kHz 6h = 512 kHz 7h = 1024 kHz
2-0	RESERVED	R/W	0h	Reserved

8.7.4 Gate_Driver_Configuration Registers

GATE_DRIVER_CONFIGURATION Registers lists the memory-mapped registers for the Gate_Driver_Configuration registers. All register offset addresses not listed in GATE_DRIVER_CONFIGURATION Registers should be considered as reserved locations and the register contents should not be modified.

表 8-50. GATE_DRIVER_CONFIGURATION Registers

Address	Acronym	Register Name	Section
ACh	GD_CONFIG1	Gate driver configuration 1	节 8.7.4.1
AEh	GD_CONFIG2	Gate driver configuration 2	节 8.7.4.2

Complex bit access types are encoded to fit into small table cells. Gate_Driver_Configuration Access Type Codes shows the codes that are used for access types in this section.

表 8-51. Gate_Driver_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.7.4.1 GD_CONFIG1 Register (Address = ACh) [Reset = 00228000h]

GD_CONFIG1 is shown in GD_CONFIG1 Register and described in GD_CONFIG1 Register Field Descriptions.

Return to the GATE_DRIVER_CONFIGURATION Registers.

Register to configure gated driver settings1

图 8-72. GD_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED		RESERVED	SLEW_RATE		RESERVED	
R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h	

23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	OVP_SEL	OVP_EN	RESERVED	OTW_REP
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

15	14	13	12	11	10	9	8
RESERVED	RESERVED	OCP_DEG		OCP_RETRY	OCP_LVL	OCP_MODE	
R/W-1h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	

7	6	5	4	3	2	1	0
RESERVED	RESERVED	ADCOMP_TH_LS	ADCOMP_TH_HS	EN_ASR	EN_AAR	CSA_GAIN	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

表 8-52. GD_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	RESERVED	R/W	0h	Reserved
28	RESERVED	R/W	0h	Reserved
27-26	SLEW_RATE	R/W	0h	Slew rate 0h = 25 V/µs 1h = 50 V/µs 2h = 125 V/µs 3h = 200 V/µs
25-24	RESERVED	R/W	0h	Reserved
23	RESERVED	R/W	0h	Reserved
22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	1h	Reserved
20	RESERVED	R/W	0h	Reserved
19	OVP_SEL	R/W	0h	Overvoltage protection level 0h = VM overvoltage level is 32-V 1h = VM overvoltage level is 20-V
18	OVP_EN	R/W	0h	Overvoltage protection enable 0h = Disable 1h = Enable
17	RESERVED	R/W	1h	Reserved
16	OTW_REP	R/W	0h	Overtemperature warning reporting on nFAULT 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled
15	RESERVED	R/W	1h	Reserved
14	RESERVED	R/W	0h	Reserved

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表 8-52. GD_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	OCP_DEG	R/W	0h	OCP deglitch time 0h = 0.2 μs 1h = 0.6 μs 2h = 1.1 μs 3h = 1.6 μs
11	OCP_RETRY	R/W	0h	OCP retry time 0h = 5 ms 1h = 500 ms
10	OCP_LVL	R/W	0h	OCP level 0h = 16 A (Typical) 1h = 24 A (Typical)
9-8	OCP_MODE	R/W	0h	OCP fault mode 0h = Overcurrent causes a latched fault 1h = Overcurrent causes an automatic retrying fault 2h = Overcurrent is report only but no action is taken 3h = Overcurrent is not reported and no action is taken
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	ADCOMP_TH_LS	R/W	0h	Active demag comparator threshold for low-side 0h = 100 mA 1h = 150 mA
4	ADCOMP_TH_HS	R/W	0h	Active demag comparator threshold for high-side 0h = 100 mA 1h = 150 mA
3	EN_ASR	R/W	0h	Active synchronous rectification enable 0h = Disable 1h = Enable
2	EN_AAR	R/W	0h	Active asynchronous rectification enable 0h = Disable 1h = Enable
1-0	CSA_GAIN	R/W	0h	Current Sense Amplifier (CSA) Gain 0h = 0.15 V/A 1h = 0.3 V/A 2h = 0.6 V/A 3h = 1.2 V/A

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8.7.4.2 GD_CONFIG2 Register (Address = AEh) [Reset = 01200000h]

GD_CONFIG2 is shown in GD_CONFIG2 Register and described in GD_CONFIG2 Register Field Descriptions.

Return to the GATE_DRIVER_CONFIGURATION Registers.

Register to configure gated driver settings2

图 8-73. GD_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	DELAY_COMP_EN	TARGET_DELAY				BUCK_SR	BUCK_PS_DIS
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BUCK_CL	BUCK_SEL		BUCK_DIS	RESERVED			
R/W-0h	R/W-1h		R/W-0h	R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

表 8-53. GD_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	DELAY_COMP_EN	R/W	0h	Driver delay compensation enable 0h = Disable 1h = Enable
29-26	TARGET_DELAY	R/W	0h	Target delay 0h = Automatic based on slew rate 1h = 0.4 μs 2h = 0.6 μs 3h = 0.8 μs 4h = 1 μs 5h = 1.2 μs 6h = 1.4 μs 7h = 1.6 μs 8h = 1.8 μs 9h = 2 μs Ah = 2.2 μs Bh = 2.4 μs Ch = 2.6 μs Dh = 2.8 μs Eh = 3 μs Fh = 3.2 μs
25	BUCK_SR	R/W	0h	Buck slew rate 0h = Buck's FET slew rate is 1000V/μs 1h = Buck's FET slew rate is 200V/μs
24	BUCK_PS_DIS	R/W	1h	Buck power sequencing disable 0h = Buck power sequencing is enabled 1h = Buck power sequencing is disabled

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表 8-53. GD_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	BUCK_CL	R/W	0h	Buck current limit 0h = 600 mA 1h = 150 mA
22-21	BUCK_SEL	R/W	1h	Buck voltage selection 0h = Buck voltage is 3.3 V 1h = Buck voltage is 5.0 V 2h = Buck voltage is 4.0 V 3h = Buck voltage is 5.7 V
20	BUCK_DIS	R/W	0h	Buck disable 0h = Buck regulator is enabled 1h = Buck regulator is disabled
19-0	RESERVED	R/W	0h	Reserved

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8.8 RAM (Volatile) Register Map

8.8.1 Fault_Status Registers

FAULT_STATUS Registers lists the memory-mapped registers for the Fault_Status registers. All register offset addresses not listed in FAULT_STATUS Registers should be considered as reserved locations and the register contents should not be modified.

表 8-54. FAULT_STATUS Registers

Address	Acronym	Register Name	Section
E0h	GATE_DRIVER_FAULT_STATUS	Fault Status Register	节 8.8.1.1
E2h	CONTROLLER_FAULT_STATUS	Fault Status Register	节 8.8.1.2

Complex bit access types are encoded to fit into small table cells. Fault_Status Access Type Codes shows the codes that are used for access types in this section.

表 8-55. Fault_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.8.1.1 GATE_DRIVER_FAULT_STATUS Register (Address = E0h) [Reset = 00000000h]

GATE_DRIVER_FAULT_STATUS is shown in GATE_DRIVER_FAULT_STATUS Register and described in GATE_DRIVER_FAULT_STATUS Register Field Descriptions.

Return to the FAULT_STATUS Registers.

Status of various faults

图 8-74. GATE_DRIVER_FAULT_STATUS Register

31	30	29	28	27	26	25	24
DRIVER_FAULT	BK_FLT	RESERVED	OCP	NPOR	OVP	OT	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
OTW	TSD	OCP_HC	OCP_LC	OCP_HB	OCP_LB	OCP_HA	OCP_LA
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED	OTP_ERR	BUCK_OCP	BUCK_UV	VCP_UV	RESERVED		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

表 8-56. GATE_DRIVER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRIVER_FAULT	R	0h	Logic OR of driver fault registers 0h = No Gate Driver fault condition is detected 1h = Gate Driver fault condition is detected
30	BK_FLT	R	0h	Buck fault 0h = No buck regulator fault condition is detected 1h = Buck regulator fault condition is detected
29	RESERVED	R	0h	Reserved
28	OCP	R	0h	Overcurrent protection status 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
27	NPOR	R	0h	Supply power on reset 0h = Power on reset condition is detected on VM 1h = No power-on-reset condition is detected on VM
26	OVP	R	0h	Supply overvoltage protection status 0h = No overvoltage condition is detected on VM 1h = Overvoltage condition is detected on VM
25	OT	R	0h	Overtemperature fault status 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
24	RESERVED	R	0h	Reserved
23	OTW	R	0h	Overtemperature warning status 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
22	TSD	R	0h	Overtemperature shutdown status 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected
21	OCP_HC	R	0h	Overcurrent status on high-side switch of OUTC 0h = No overcurrent detected on high-side switch of OUTC 1h = Overcurrent detected on high-side switch of OUTC
20	OCP_LC	R	0h	Overcurrent status on low-side switch of OUTC 0h = No overcurrent detected on low-side switch of OUTC 1h = Overcurrent detected on low-side switch of OUTC
19	OCP_HB	R	0h	Overcurrent status on high-side switch of OUTB 0h = No overcurrent detected on high-side switch of OUTB 1h = Overcurrent detected on high-side switch of OUTB
18	OCP_LB	R	0h	Overcurrent status on low-side switch of OUTB 0h = No overcurrent detected on low-side switch of OUTB 1h = Overcurrent detected on low-side switch of OUTB
17	OCP_HA	R	0h	Overcurrent status on high-side switch of OUTA 0h = No overcurrent detected on high-side switch of OUTA 1h = Overcurrent detected on high-side switch of OUTA
16	OCP_LA	R	0h	Overcurrent status on low-side switch of OUTA 0h = No overcurrent detected on low-side switch of OUTA 1h = Overcurrent detected on low-side switch of OUTA
15	RESERVED	R	0h	Reserved
14	OTP_ERR	R	0h	One-time programmable (OTP) error 0h = No OTP error is detected 1h = OTP Error is detected

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表 8-56. GATE_DRIVER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	BUCK_OCP	R	0h	Buck regulator overcurrent status 0h = No buck regulator overcurrent is detected 1h = Buck regulator overcurrent is detected
12	BUCK_UV	R	0h	Buck regulator undervoltage status 0h = No buck regulator undervoltage is detected 1h = Buck regulator undervoltage is detected
11	VCP_UV	R	0h	Charge pump undervoltage status 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
10-0	RESERVED	R	0h	Reserved

8.8.1.2 CONTROLLER_FAULT_STATUS Register (Address = E2h) [Reset = 00000000h]

CONTROLLER_FAULT_STATUS is shown in CONTROLLER_FAULT_STATUS Register and described in CONTROLLER_FAULT_STATUS Register Field Descriptions.

Return to the FAULT_STATUS Registers.

Status of various faults

图 8-75. CONTROLLER_FAULT_STATUS Register

31	30	29	28	27	26	25	24
CONTROLLER_FAULT	RESERVED	IPD_FREQ_FAULT	IPD_T1_FAULT	IPD_T2_FAULT	RESERVED		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ABN_SPEED	LOSS_OF_SYNC	NO_MTR	MTR_LCK	CBC_ILIMIT	LOCK_ILIMIT	MTR_UNDER_VOLTAGE	MTR_OVER_VOLTAGE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXT_WD_TIMEOUT	RESERVED						
R-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					STL_EN	STL_STATUS	APP_RESET
R-0h					R-0h	R-0h	R-0h

表 8-57. CONTROLLER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CONTROLLER_FAULT	R	0h	Logic OR of controller fault registers 0h = No controller fault condition is detected 1h = Controller fault condition is detected
30	RESERVED	R	0h	Reserved
29	IPD_FREQ_FAULT	R	0h	Indicates IPD frequency fault 0h = No IPD frequency fault detected 1h = IPD frequency fault detected
28	IPD_T1_FAULT	R	0h	Indicates IPD T1 fault 0h = No IPD T1 fault detected 1h = IPD T1 fault detected

表 8-57. CONTROLLER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	IPD_T2_FAULT	R	0h	Indicates IPD T2 fault 0h = No IPD T2 fault detected 1h = IPD T2 fault detected
26-24	RESERVED	R	0h	Reserved
23	ABN_SPEED	R	0h	Indicates abnormal speed motor lock condition 0h = No abnormal speed fault detected 1h = Abnormal speed fault detected
22	LOSS_OF_SYNC	R	0h	Indicates sync lost motor lock condition 0h = No sync lost fault detected 1h = Sync lost fault detected
21	NO_MTR	R	0h	Indicates no motor fault 0h = No motor fault not detected 1h = No motor fault detected
20	MTR_LCK	R	0h	Indicates when one of the motor lock is triggered 0h = Motor lock fault not detected 1h = Motor lock fault detected
19	CBC_ILIMIT	R	0h	Indicates CBC current limit fault 0h = No CBC fault detected 1h = CBC fault detected
18	LOCK_ILIMIT	R	0h	Indicates lock detection current limit fault 0h = No lock current limit fault detected 1h = Lock current limit fault detected
17	MTR_UNDER_VOLTAGE	R	0h	Indicates motor undervoltage fault 0h = No motor undervoltage detected 1h = Motor undervoltage detected
16	MTR_OVER_VOLTAGE	R	0h	Indicates motor overvoltage fault 0h = No motor overvoltage detected 1h = Motor overvoltage detected
15	EXT_WD_TIMEOUT	R	0h	Indicates external watchdog timeout fault 0h = No external watchdog timeout fault detected 1h = External watchdog timeout fault detected
14-3	RESERVED	R	0h	Reserved
2	STL_EN	R	0h	Indicates STL is enabled in EEPROM 0h = STL Disable 1h = STL Enable
1	STL_STATUS	R	0h	Indicates STL success criteria Pass = 1b; Fail = 0b 0h = STL Fail 1h = STL Pass
0	APP_RESET	R	0h	App reset 0h = App Reset Fail 1h = App Reset Successful

8.8.2 System_Status Registers

SYSTEM_STATUS Registers lists the memory-mapped registers for the System_Status registers. All register offset addresses not listed in SYSTEM_STATUS Registers should be considered as reserved locations and the register contents should not be modified.

表 8-58. SYSTEM_STATUS Registers

Address	Acronym	Register Name	Section
E4h	SYS_STATUS1	System Status Register1	节 8.8.2.1

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表 8-58. SYSTEM_STATUS Registers (continued)

Address	Acronym	Register Name	Section
EAh	SYS_STATUS2	System Status Register2	节 8.8.2.2
ECh	SYS_STATUS3	System Status Register3	节 8.8.2.3

Complex bit access types are encoded to fit into small table cells. System_Status Access Type Codes shows the codes that are used for access types in this section.

表 8-59. System_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.8.2.1 SYS_STATUS1 Register (Address = E4h) [Reset = 00000000h]

SYS_STATUS1 is shown in SYS_STATUS1 Register and described in SYS_STATUS1 Register Field Descriptions.

Return to the SYSTEM_STATUS Registers.

Status of various system and motor parameters

图 8-76. SYS_STATUS1 Register

31	30	29	28	27	26	25	24
VOLT_MAG							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VOLT_MAG							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPEED_CMD							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEED_CMD							I2C_ENTRY_STATUS
R-0h							R-0h

表 8-60. SYS_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VOLT_MAG	R	0h	Applied DC input voltage (/10 to get DC input voltage in V)
15-1	SPEED_CMD	R	0h	Decoded speed command in PWM/Analog/Freq. mode (SPEED_CMD (%) = SPEED_CMD/32767 * 100%)
0	I2C_ENTRY_STATUS	R	0h	Indicates if I2C entry has happened 0h = I2C mode not entered through pin sequence 1h = I2C mode entered through pin sequence

8.8.2.2 SYS_STATUS2 Register (Address = EAh) [Reset = 00000000h]

SYS_STATUS2 is shown in SYS_STATUS2 Register and described in SYS_STATUS2 Register Field Descriptions.

Return to the SYSTEM_STATUS Registers.

Status of various system and motor parameters

图 8-77. SYS_STATUS2 Register

31	30	29	28	27	26	25	24
STATE				RESERVED			
R-0h				R-0h			
23	22	21	20	19	18	17	16
RESERVED						STL_FAULT	RESERVED
R-0h						R-0h	R-0h
15	14	13	12	11	10	9	8
MOTOR_SPEED							
R-0h							
7	6	5	4	3	2	1	0
MOTOR_SPEED							
R-0h							

表 8-61. SYS_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	STATE	R	0h	Current status of state machine; 4-bit value indicating status of state machine 0h = SYSTEM_IDLE 1h = MOTOR_START 2h = MOTOR_RUN 3h = SYSTEM_INIT 4h = MOTOR_IPD 5h = MOTOR_ALIGN 6h = MOTOR_IDLE 7h = MOTOR_STOP 8h = FAULT 9h = MOTOR_DIRECTION Ah = HALL_ALIGN Ch = MOTOR_FREEWHEEL Dh = MOTOR_DESCEL Eh = MOTOR_BRAKE Fh = N/A
27-18	RESERVED	R	0h	Reserved
17	STL_FAULT	R	0h	STL fault status 0h = Pass 1h = Fail
16	RESERVED	R	0h	Reserved
15-0	MOTOR_SPEED	R	0h	Speed output (/10 to get motor electrical speed in Hz)

8.8.2.3 SYS_STATUS3 Register (Address = ECh) [Reset = 00000000h]

SYS_STATUS3 is shown in SYS_STATUS3 Register and described in SYS_STATUS3 Register Field Descriptions.

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Return to the SYSTEM_STATUS Registers.

Status of various system and motor parameters

图 8-78. SYS_STATUS3 Register

31–16	15–0
DC_BUS_CURR	DC_BATT_POW
R-0h	R-0h

表 8-62. SYS_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DC_BUS_CURR	R	0h	DC bus current (/256 to get DC bus current in A)
15-0	DC_BATT_POW	R	0h	Battery (input) power (/64 to get battery power in W)

8.8.3 Algo_Control Registers

ALGO_CONTROL Registers lists the memory-mapped registers for the Algo_Control registers. All register offset addresses not listed in ALGO_CONTROL Registers should be considered as reserved locations and the register contents should not be modified.

表 8-63. ALGO_CONTROL Registers

Address	Acronym	Register Name	Section
E6h	ALGO_CTRL1	Algorithm Control Parameters	节 8.8.3.1

Complex bit access types are encoded to fit into small table cells. Algo_Control Access Type Codes shows the codes that are used for access types in this section.

表 8-64. Algo_Control Access Type Codes

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.8.3.1 ALGO_CTRL1 Register (Address = E6h) [Reset = 00000000h]

ALGO_CTRL1 is shown in ALGO_CTRL1 Register and described in ALGO_CTRL1 Register Field Descriptions.

Return to the ALGO_CONTROL Registers.

Algorithm Control Parameters

图 8-79. ALGO_CTRL1 Register

31	30	29	28	27–24
EEPROM_WRT	EEPROM_READ	CLR_FLT	CLR_FLT_RETRY_COUNT	EEPROM_WRITE_ACCESS_KEY
W-0h	W-0h	W-0h	W-0h	W-0h

23–20	19–16
EEPROM_WRITE_ACCESS_KEY	RESERVED
W-0h	W-0h

15–8
RESERVED
W-0h

图 8-79. ALGO_CTRL1 Register (continued)

7	6	5	4	3	2	1	0
RESERVED							EXT_WD_STATUS_SET
W-0h							W-0h

表 8-65. ALGO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EEPROM_WRT	W	0h	Write the configuration to EEPROM 1h = Write to the EEPROM registers from shadow registers
30	EEPROM_READ	W	0h	Read the default configuration from EEPROM 1h = Read the EEPROM registers to shadow registers
29	CLR_FLT	W	0h	Clears all faults 1h = Clear all the driver and controller faults
28	CLR_FLT_RETRY_COUNT	W	0h	Clears fault retry count 1h = clear the lock fault retry counts
27-20	EEPROM_WRITE_ACCESS_KEY	W	0h	EEPROM write access key; 8-bit key to unlock the EEPROM write command
19-1	RESERVED	W	0h	Reserved
0	EXT_WD_STATUS_SET	W	0h	Watchdog status to be set by external MCU in I2C watchdog mode 0h = Reset automatically by the MCC 1h = To set the EXT_WD_STATUS_SET

8.8.4 Device_Control Registers

DEVICE_CONTROL Registers lists the memory-mapped registers for the Device_Control registers. All register offset addresses not listed in DEVICE_CONTROL Registers should be considered as reserved locations and the register contents should not be modified.

表 8-66. DEVICE_CONTROL Registers

Address	Acronym	Register Name	Section
E8h	DEVICE_CTRL	Device Control Parameters	节 8.8.4.1

Complex bit access types are encoded to fit into small table cells. Device_Control Access Type Codes shows the codes that are used for access types in this section.

表 8-67. Device_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

8.8.4.1 DEVICE_CTRL Register (Address = E8h) [Reset = 00000000h]

DEVICE_CTRL is shown in DEVICE_CTRL Register and described in DEVICE_CTRL Register Field Descriptions.

Return to the DEVICE_CONTROL Registers.

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Device Control Parameters

图 8-80. DEVICE_CTRL Register

31	30	29	28	27	26	25	24
RESERVED	SPEED_CTRL						
W-0h	W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPEED_CTRL							
W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OVERRIDE	RESERVED						
W-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

表 8-68. DEVICE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	W	0h	Reserved
30-16	SPEED_CTRL	W	0h	Digital speed command (SPEED_CTRL (%) = SPEED_CTRL/32767 * 100%)
15	OVERRIDE	W	0h	Speed input select for I2C vs speed pin 0h = SPEED_CMD using Analog/Freq/PWM mode 1h = SPEED_CMD using SPD_CTRL[14:0]
14-0	RESERVED	R	0h	Reserved

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MCT8316A device is used in sensorless 3-phase BLDC motor control. The driver provides a high performance, high-reliability, flexible solution for robotic vacuum, fuel pumps, automotive fans and blowers, medical CPAP blowers etc., The following section shows a common application of the MCT8316A device.

9.2 Typical Applications

图 9-1 shows the typical schematic of MCT8316AV.

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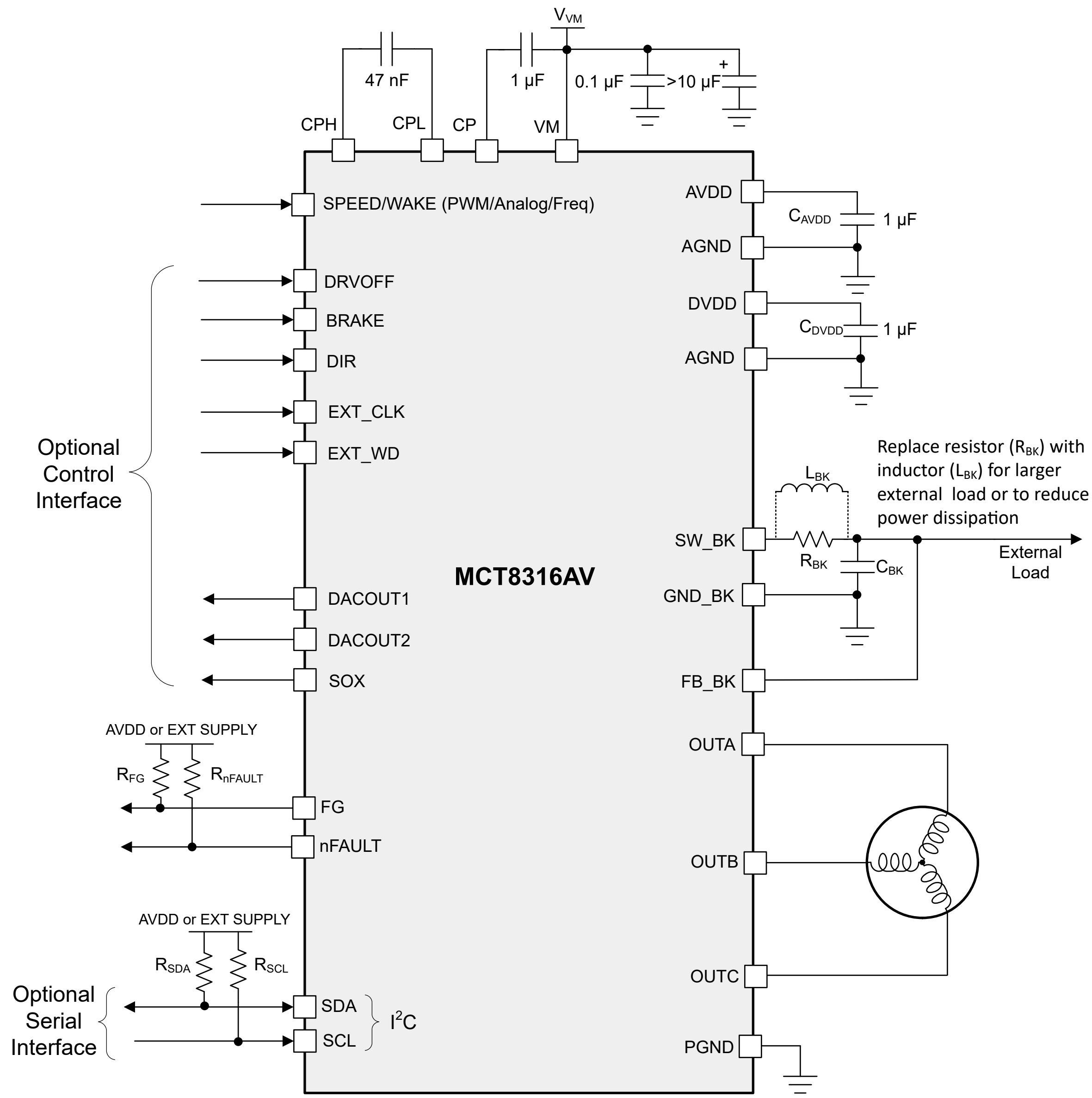

图 9-1. Primary Application Schematic

表 9-1 lists the recommended values of the external components for MCT8316A.

表 9-1. MCT8316A External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{VM2}	VM	PGND	⩾ 10-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{CP}	CP	VM	X5R or X7R, 16-V, 1-µF capacitor
C_{FLY}	CPH	CPL	X5R or X7R, 47-nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin

表 9-1. MCT8316A External Components (continued)

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{AVDD}	AVDD	AGND	X5R or X7R, 1-μF, ≥ 6.3-V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-μF to 1.3-μF at 3.3-V across operating temperature.
C_{DVDD}	AVDD	AGND	X5R or X7R, 1-μF, ≥ 4-V. In order for DVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.6-μF to 1.3-μF at 1.5-V across operating temperature.
C_{BK}	SW_BK	GND_BK	X5R or X7R, buck-output rated capacitor
L_{BK}	SW_BK	FB_BK	Buck-output inductor
R_{FG}	1.8 to 5-V Supply	FG	5.1-kΩ, Pull-up resistor
R_{nFAULT}	1.8 to 5-V Supply	nFAULT	5.1-kΩ, Pull-up resistor
R_{SDA}	1.8 to 3.3-V Supply	SDA	5.1-kΩ, Pull-up resistor
R_{SCL}	1.8 to 3.3-V Supply	SCL	5.1-kΩ, Pull-up resistor

Recommended application range for MCT8316A is shown in 表 9-2.

表 9-2. Recommended Application Range

Parameter	Min	Max	Unit
Motor voltage	4.5	35	V
Motor electrical speed	-	3000	Hz
Peak motor phase current	-	8	A

Default EEPROM configuration for MCT8316A is listed in 表 9-3. Default values are chosen for reliable motor startup and closed loop operation. Refer to MCT8316A tuning guide which provides step by step procedure to tune a 3-phase BLDC motor in closed loop, conform to use-case and explore features in the device.

表 9-3. Recommended Default Values

Address Name	Address	Recommended Value
ISD_CONFIG	0x00000080	0x6EC4C100
MOTOR_STARTUP1	0x00000082	0x2EA610E4
MOTOR_STARTUP2	0x00000084	0x1221109C
CLOSED_LOOP1	0x00000086	0x0C321200
CLOSED_LOOP2	0x00000088	0x024224B0
CLOSED_LOOP3	0x0000008A	0x4CCC03E0
CLOSED_LOOP4	0x0000008C	0x000CE944
CONST_SPEED	0x0000008E	0x00A00510
CONST_PWR	0x00000090	0x5DC04C84
FAULT_CONFIG1	0x00000092	0x60F43025
FAULT_CONFIG2	0x00000094	0x7F87A009
TRAP_CONFIG1	0x0000009A	0x0548A186
TRAP_CONFIG2	0x0000009C	0x3A840000
150_DEG_TWO_PH_PROFILE	0x00000096	0x6ADB44A6
150_DEG_THREE_PH_PROFILE	0x00000098	0x392DFF80
PIN_CONFIG1	0x000000A4	0x2D720600
PIN_CONFIG2	0x000000A6	0x08000000
DEVICE_CONFIG	0x000000A8	0x7FFF0000
PERIPH_CONFIG	0x000000AA	0x00000000
GD_CONFIG1	0x000000AC	0x1C440000

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表 9-3. Recommended Default Values (continued)

GD_CONFIG2	0x000000AE	0x00000000

Once the device EEPROM is programmed with the desired configuration, device can be operated stand-alone and I^2C serial interface is not required anymore. Speed can be commanded using SPEED pin.

Below are the two essential parameters that are required to spin the motor in closed loop.

1. Maximum motor speed.
2. Cycle by cycle (CBC) current limit.

9.2.1 Application curves

9.2.1.1 Motor startup

图 9-2 shows the phase current waveforms of various startup methods in MCT8316A such as align, double align, IPD and slow first cycle.

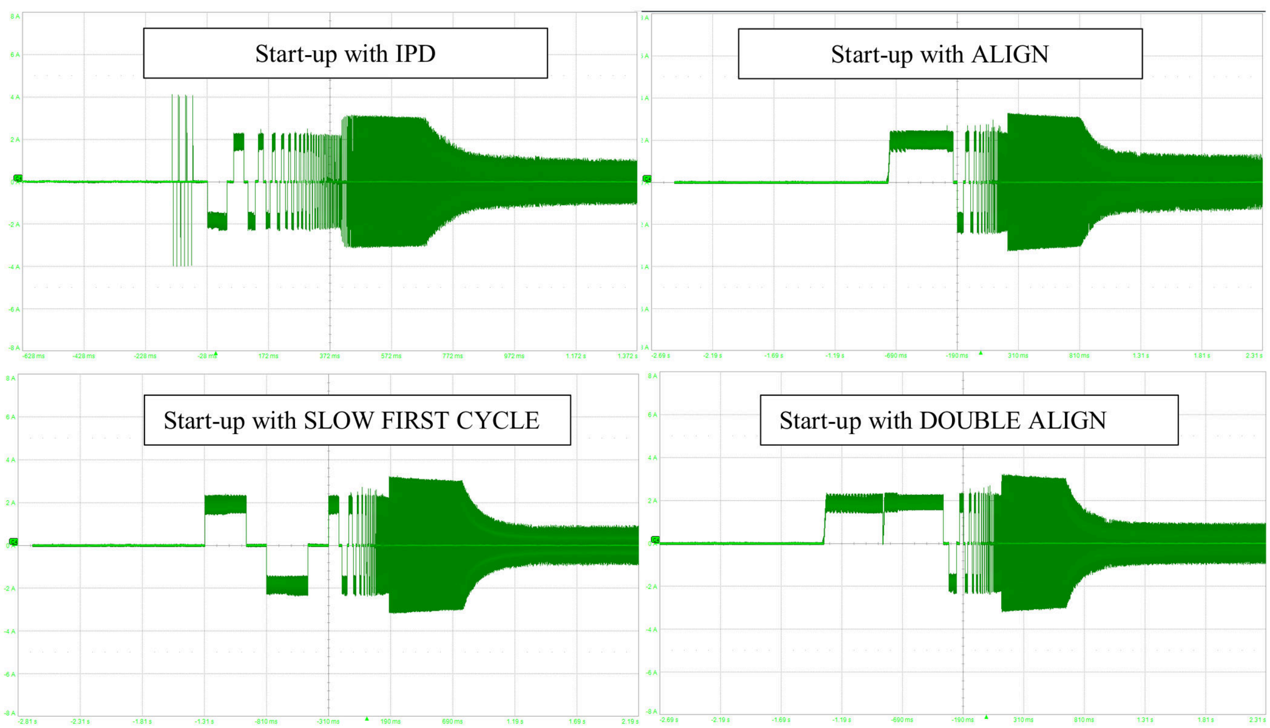

图 9-2. Motor phase current waveforms of all startup methods

9.2.1.2 120º and variable commutation

In 120° commutation scheme, each motor phase is driven for 120° and Hi-Z for 60° within each half electrical cycle, resulting in six different commutation states for a motor. 图 9-3 shows the phase current and current waveform FFT in 120° commutation mode. In variable commutation scheme, MCT8316A device switches dynamically between 120° and 150° trapezoidal commutation depending on motor speed. The device operates

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in 150° mode at lower speeds and moves to 120° mode at higher speeds. 图 9-4 shows the phase current and current waveform FFT in 150° commutation.

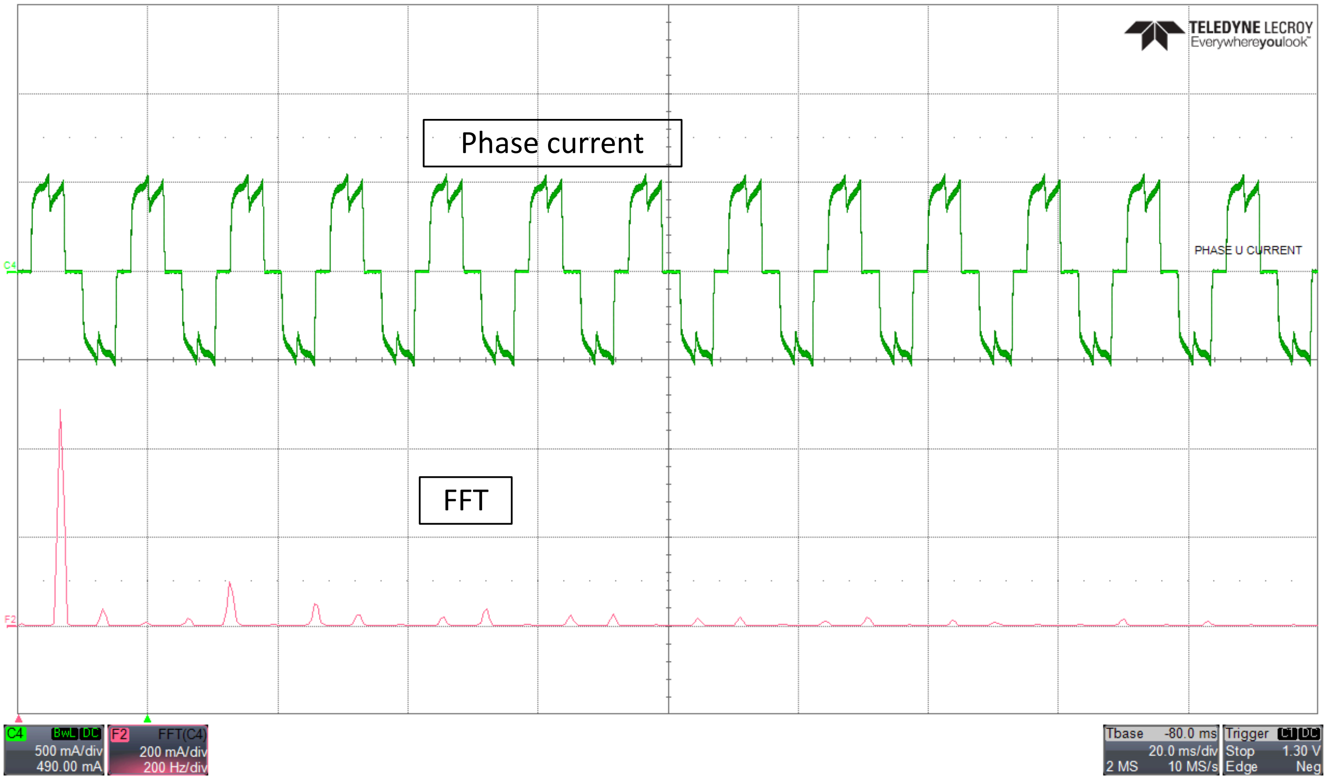

图 9-3. Phase current and FFT - 120 °commutation

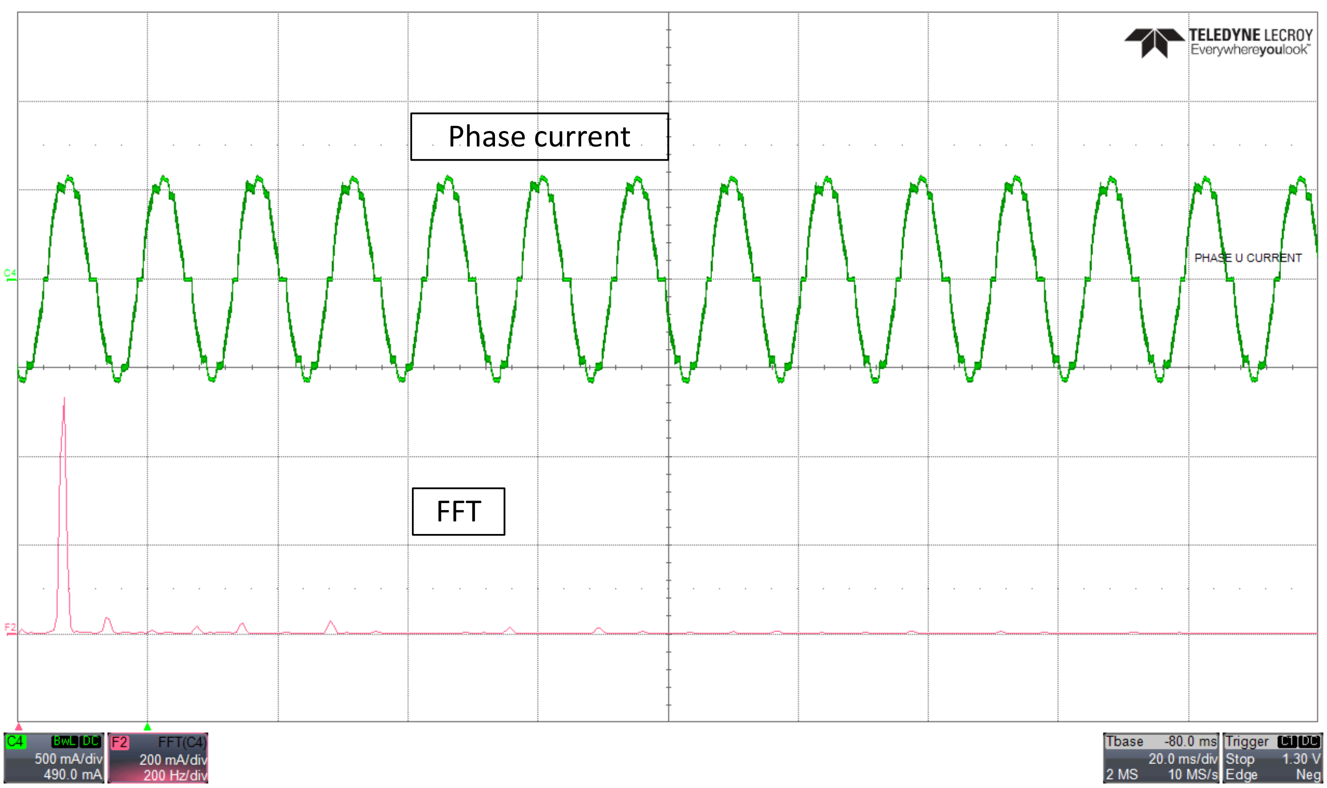

图 9-4. Phase current and FFT - 150°commutation

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9.2.1.3 Faster startup time

Startup time is the time taken for the motor to reach the target speed from zero speed. Faster startup time can be achieved in MCT8316A by tuning motor startup, open loop and closed loop settings. 图 9-5 shows FG, phase current and motor electrical speed waveform. Motor takes 50 ms to reach target speed from zero speed.

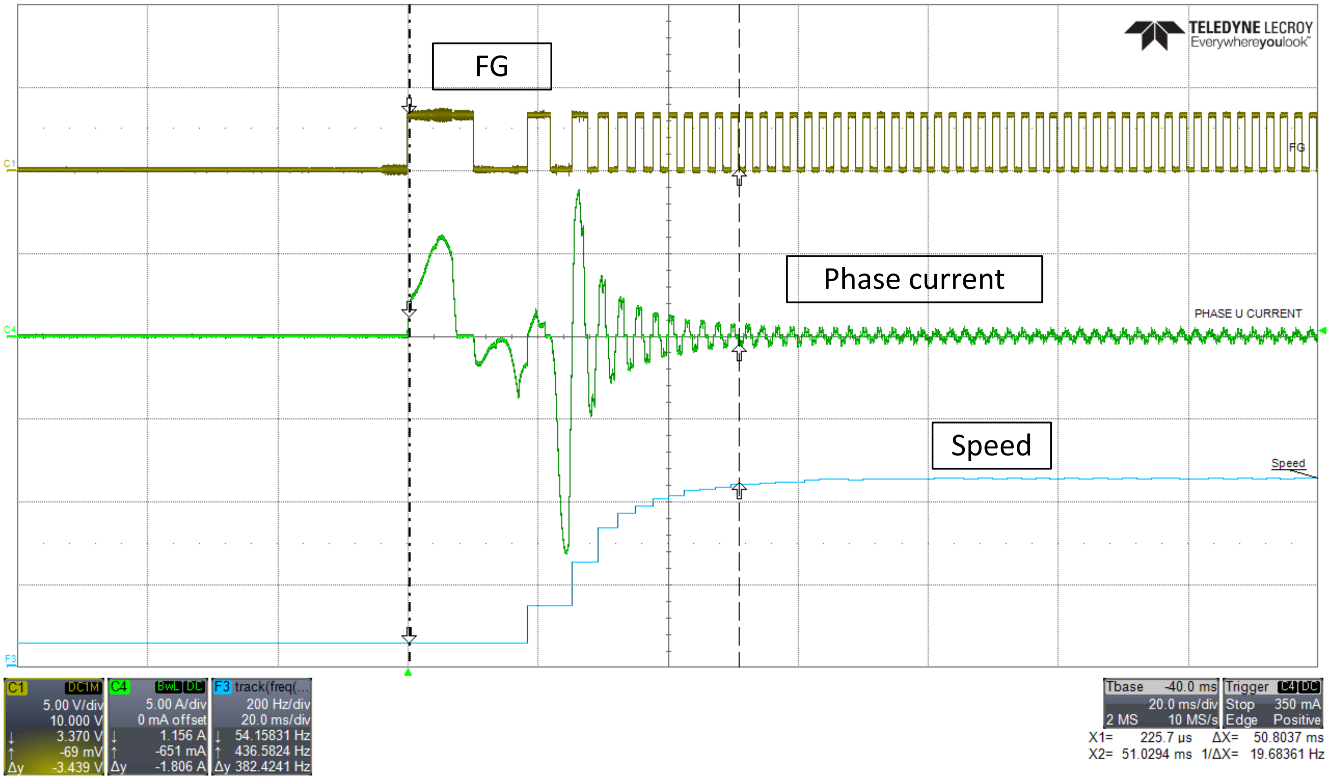

图 9-5. Phase current, FG and motor speed - Faster startup time

9.2.1.4 Setting the BEMF threshold

The BEMF_THRESHOLD1 and BEMF_THRESHOLD2 values used for commutation instant detection in MCT8316A can be computed from the motor phase voltage waveforms during coasting. For example, consider the three-phase voltage waveforms of a BLDC motor while coasting as in 图 9-6. The motor phase voltage during coasting is the motor back-EMF.

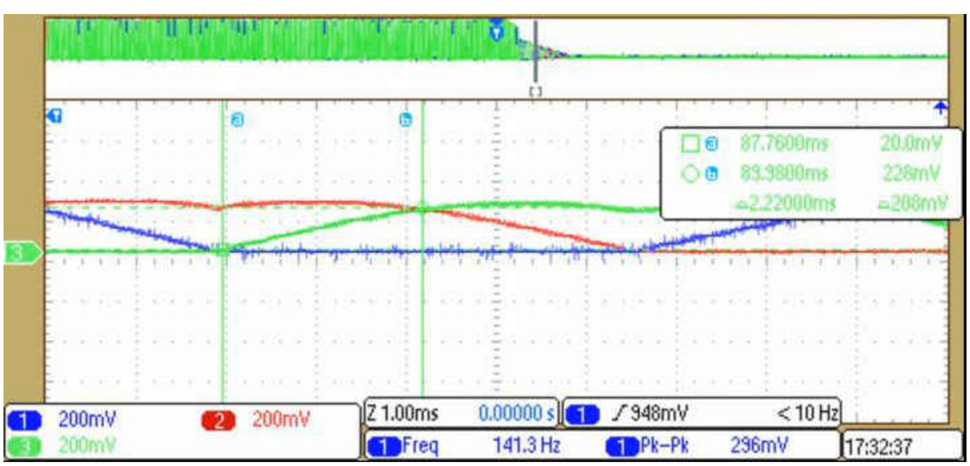

图 9-6. Motor phase voltage during coasting

In 图 9-6, one floating phase voltage interval is denoted by the vertical markers on channel 3. The Vpeak (peak-peak back-EMF) on channel 3 is 208-mV and Tc (commutation interval) is 2.22-ms as denoted by the horizontal and vertical markers on channel 3. The digital equivalent counts for Vpeak and Tc are calculated as follows.

In MCT8316A, a 3-V analog input corresponds to 4095 counts(12-bit) and phase voltage is scaled down by 10x factor before ADC input; therfore, Vpeak of 208-mV corresponds to an ADC input of 20.8mV, which in turn equals 29 ADC counts. Assuming the PWM switching frequency is 25-kHz, one back-EMF sample is available every 40-μs. So, in a time interval of 2.22-ms, a total of 55 back-EMF samples are integrated. Therefore, the BEMF_THRESHOLD1 or BEMF_THRESHOLD2 value calculated as per 方程式 8 is (½) * (29/2) * (55/2) = 199. Hence, in this example, BEMF_THRESHOLD1 and BEMF_THRESHOLD2 are set to 8h (corresponding to 200 which is the closest value to 199) for commutation instant detection using back-EMF integration method during fast start-up. The exact speed at which the Vpeak and Tc values are measured to calculate the BEMF_THRESHOLD1 and BEMF_THRESHOLD2 values is not critical (as long as there is sufficient resolution in digital counts) since the product (Vpeak * Tc) is, largely, a constant for a given BLDC motor.

9.2.1.5 Maximum speed

图 9-7 shows phase current, phase voltage and FG of a motor that spins at maximum electrical speed of 3 kHz.

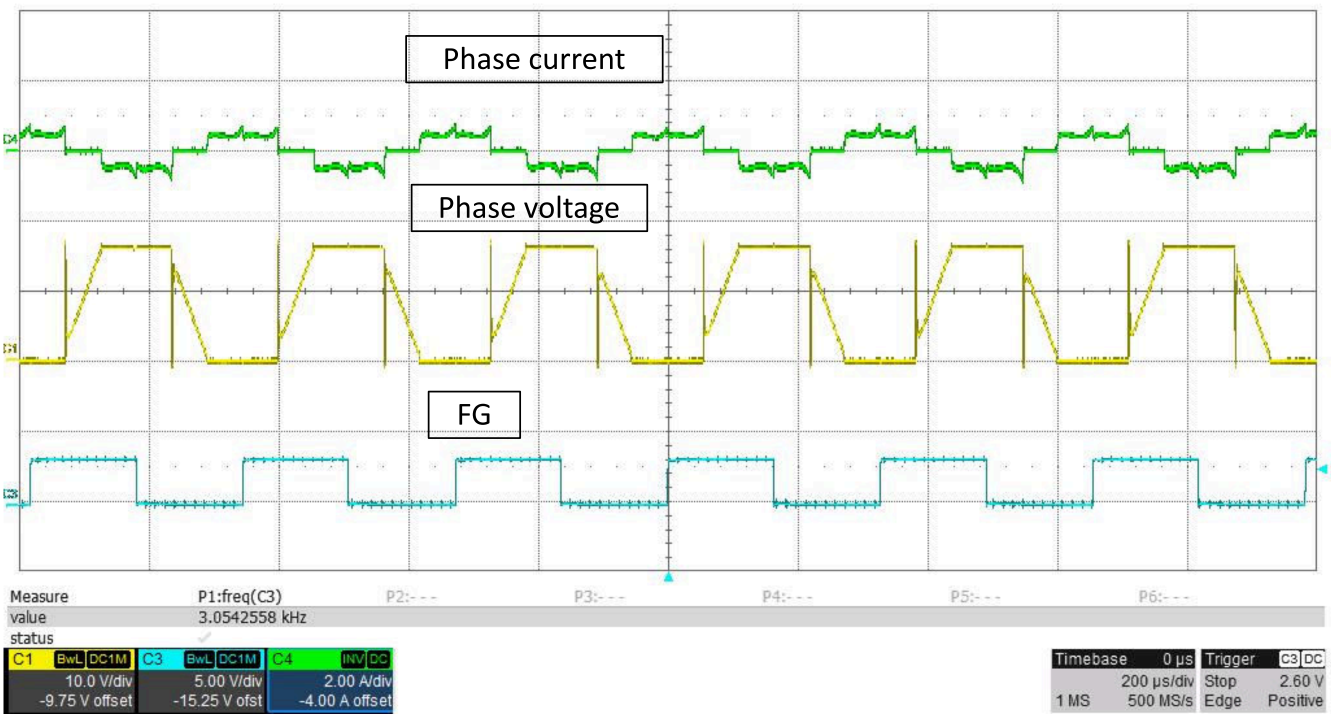

图 9-7. Phase current, Phase voltage and FG at Maximum speed

9.2.1.6 Faster deceleration

MCT8316A has features to decelerate the motor quickly. 图 9-8 shows phase current and motor electrical speed waveform when the motor decelerates from 100% duty cycle to 10% duty cycle. Time taken for the motor to decelerate from 100% duty cycle to 10% duty cycle when fast deceleration is disabled is around 10 seconds. 图 9-9 shows phase current and motor electrical speed waveform when the motor decelerates from 100% duty cycle to 10% duty cycle. Time taken for the motor to decelerate from 100% duty cycle to 10% duty cycle when fast deceleration is enabled is around 1.5 seconds.

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备注

Please note that when fast deceleration is enabled and anti-voltage surge (AVS) is disabled, there might be voltage spikes seen in supply voltage. Enable AVS to protect the power supply from voltage overshoots during motor deceleration.

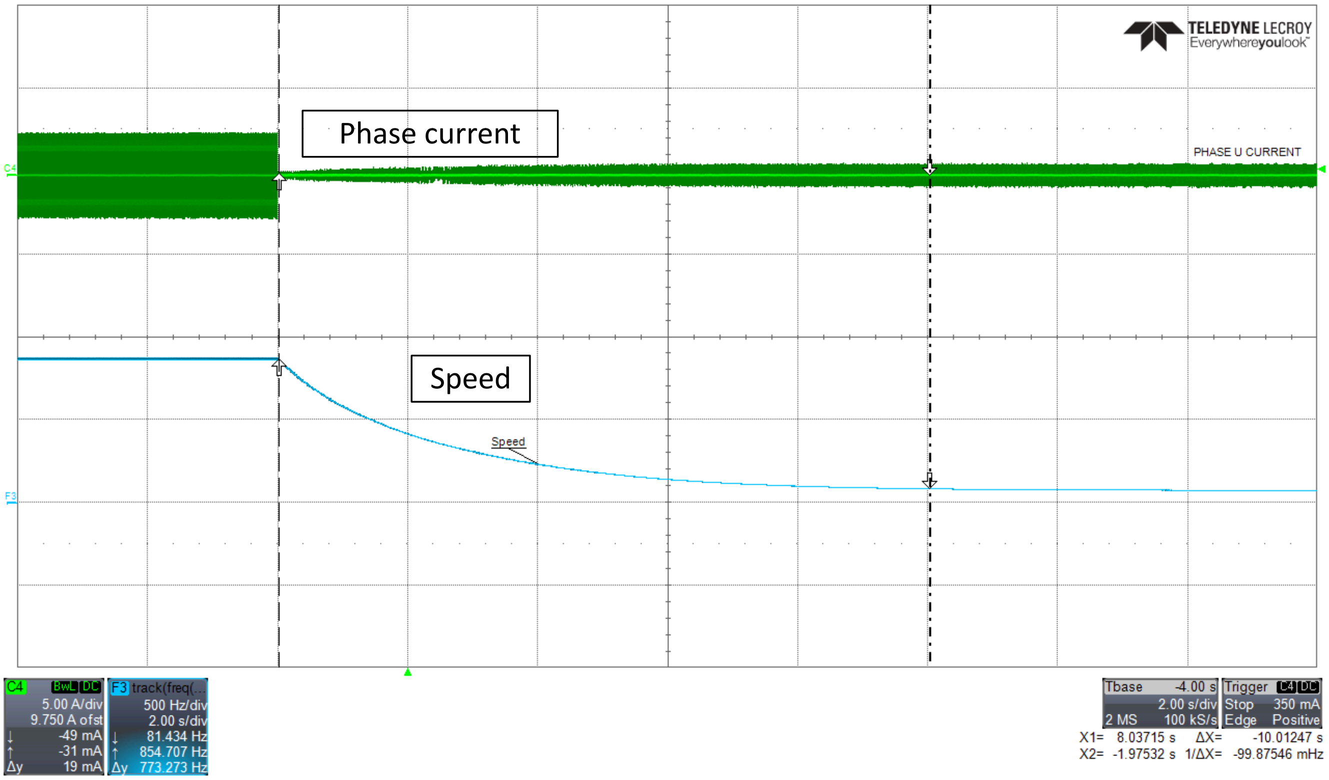

图 9-8. Phase current and motor speed - Faster deceleration disabled

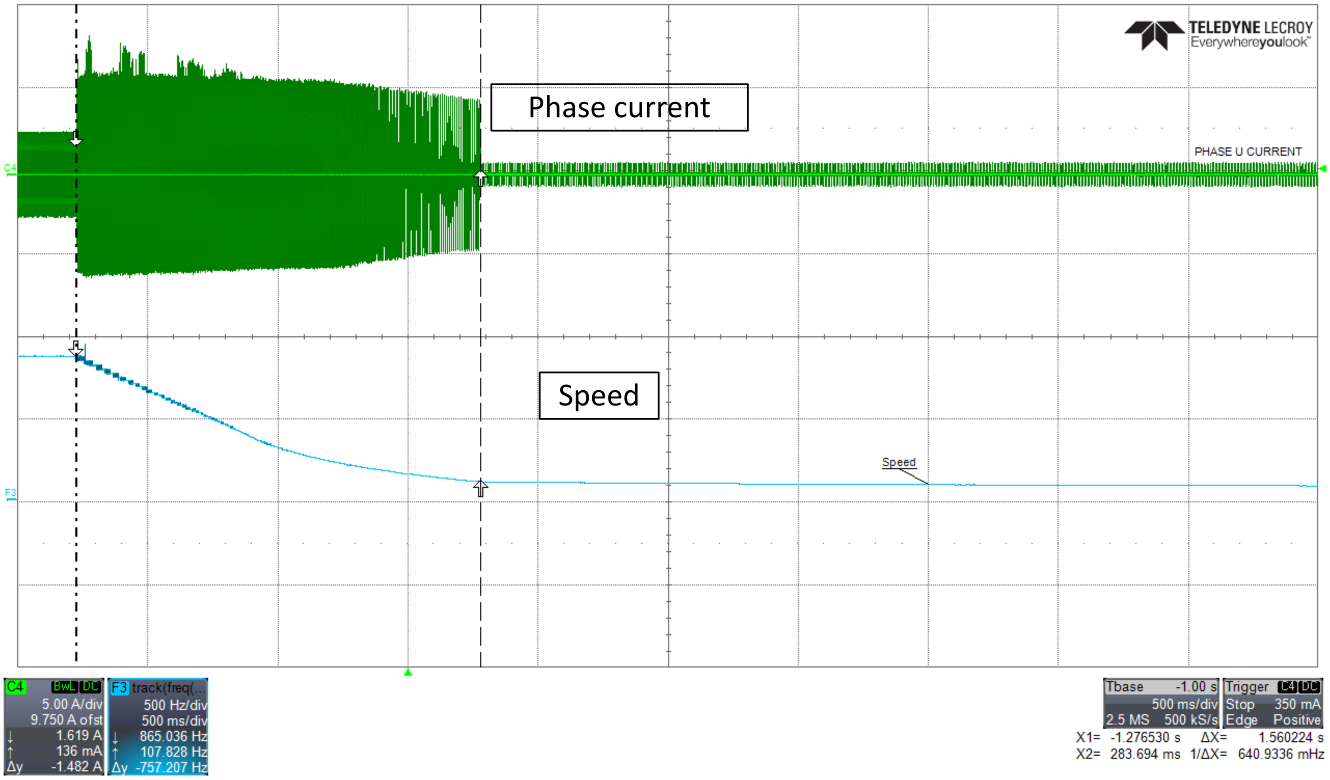

图 9-9. Phase current and motor speed -Faster deceleration enabled

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10 Power Supply Recommendations

10.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in VM voltage. When adequate bulk capacitance is used, the VM voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate bulk capacitor.

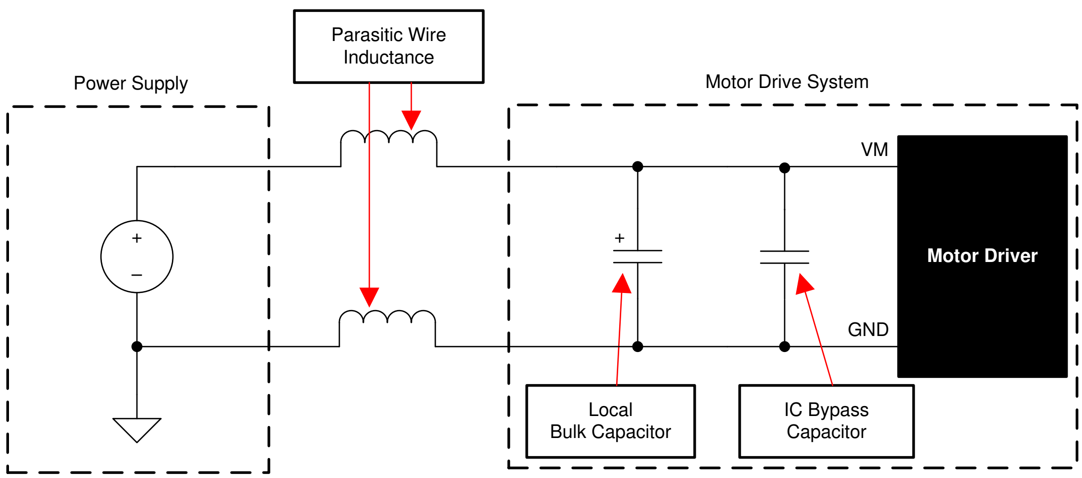

图 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize parasitic inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND_BK can be split. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW_BK and FB_BK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB_BK trace as much as possible to allow for faster load switching.

图 11-1 shows a layout example for the MCT8316A. Also, for layout example, refer to MCT8316A EVM.

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11.2 Layout Example

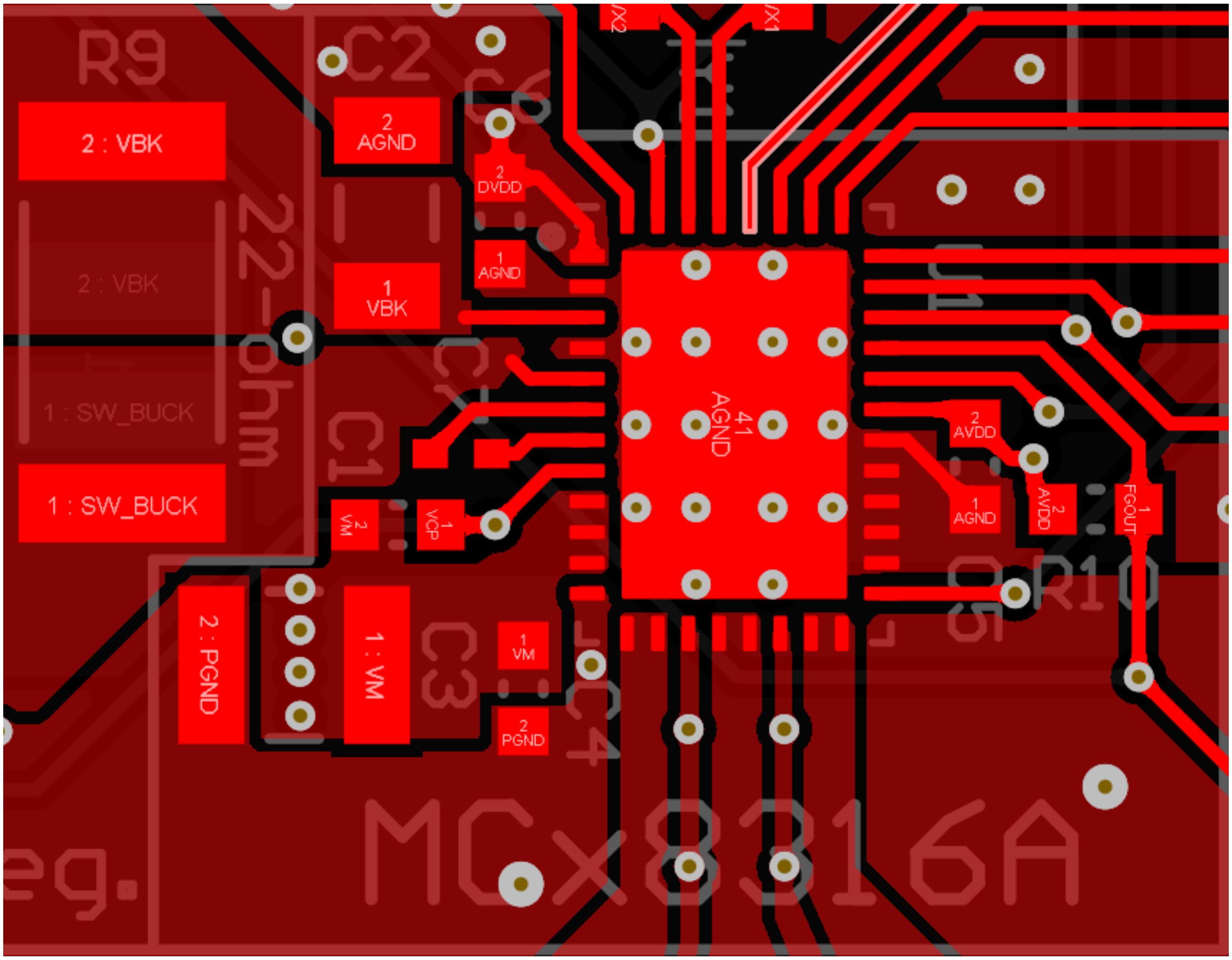

图 11-1. Recommended Layout Example

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11.3 Thermal Considerations

The MCT8316A has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11.3.1 Power Dissipation

The power dissipated in the output FET resistance ($R_{DS(on)}$) dominates power dissipation in MCT8316A.

At start-up and fault conditions, the FET current is much higher than normal operating FET current; remember to take these peak currents and their duration into consideration.

The total device power dissipation is the power dissipated in each of the three half-bridges added together along with standby power, LDO and buck regulator losses.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

A summary of equations for calculating each loss is shown below in 表 11-1.

表 11-1. Power Losses for MCT8316A

Loss type	MCT8316A
Standby power	$P_{standby}$ = VM x I_{VM_TA}
LDO	P_{LDO} = (VM-V_{AVDD}) x I_{AVDD}, if BUCK_PS_DIS = 1b P_{LDO} = (V_{BK}-V_{AVDD}) x I_{AVDD}, if BUCK_PS_DIS = 0b
FET conduction	P_{CON} = 2 x $(I_{RMS(trap)})^2$ x $R_{ds,on(TA)}$
FET switching	P_{SW} = $I_{PK(trap)}$ x $V_{PK(trap)}$ x $t_{rise/fall}$ x f_{PWM}
Diode	P_{diode} = $I_{PK(trap)}$ x V_{diode} x t_{dead} x f_{PWM}
Demagnetization	Without Active Demag: 3 x $I_{PK(trap)}$ x V_{diode} x $t_{commutation}$ x f_{motor_elec} With Active Demag: 3 x $(I_{RMS(trap)})^2$ x $R_{ds,on(TA)}$ x $t_{commutation}$ x f_{motor_elec}
Buck	P_{BK} = 0.11 x V_{BK} x I_{BK} (η_{BK} = 90%)

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12 Device and Documentation Support

12.1 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.2 Trademarks

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12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 术语表

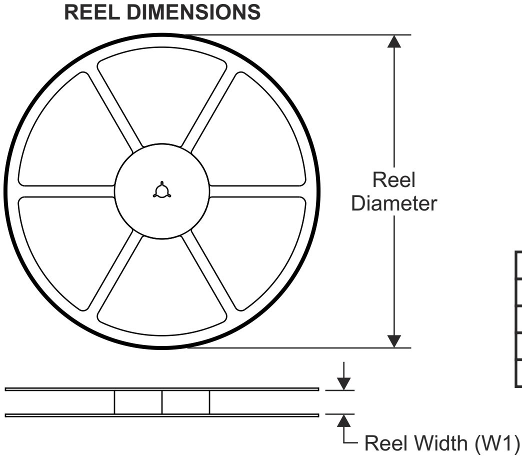
TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

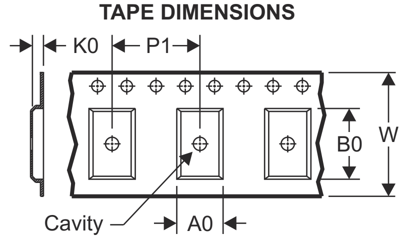
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

13.1 Tape and Reel Information

REEL DIMENSIONS

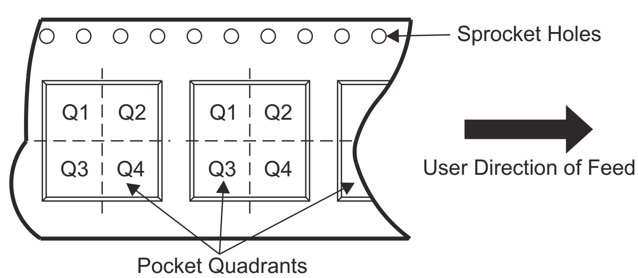


TAPE DIMENSIONS



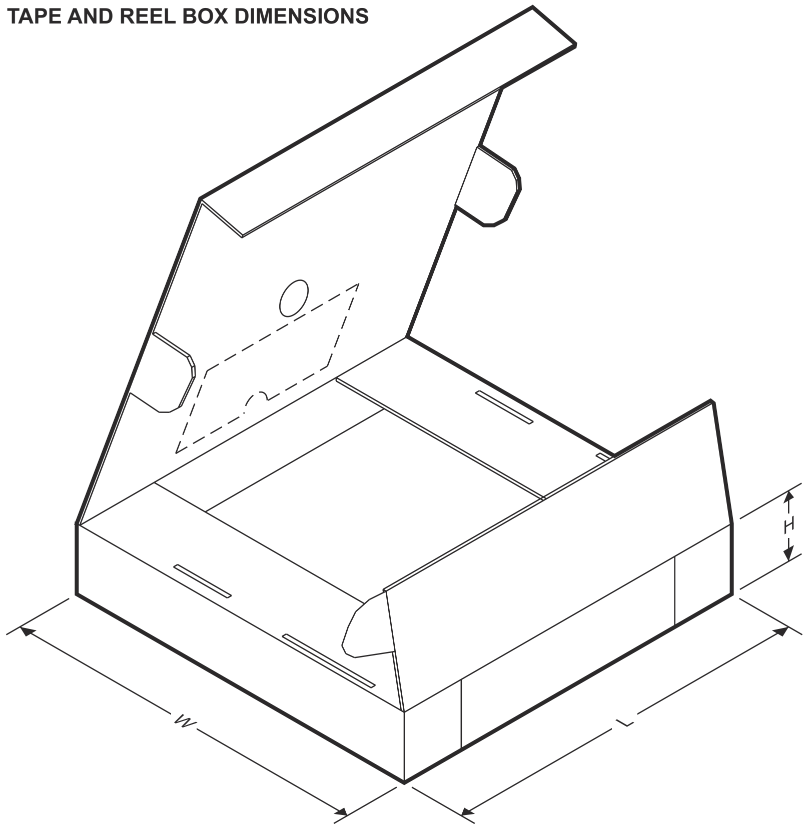
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCT8316A1TRGFR	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCT8316A1TRGFR	VQFN	RGF	40	3000	367.0	367.0	38.0

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MCT8316A1VRGFR	ACTIVE	VQFN	RGF	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MCT83 16A1V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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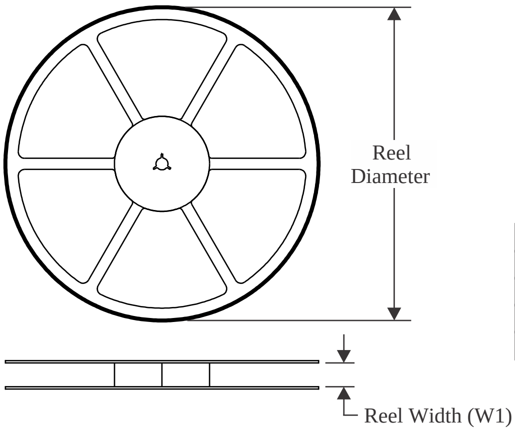
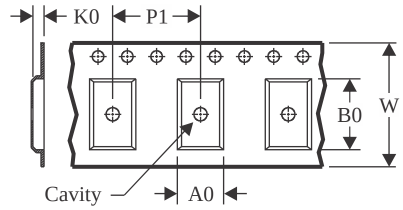
TAPE AND REEL INFORMATION

REEL DIMENSIONS

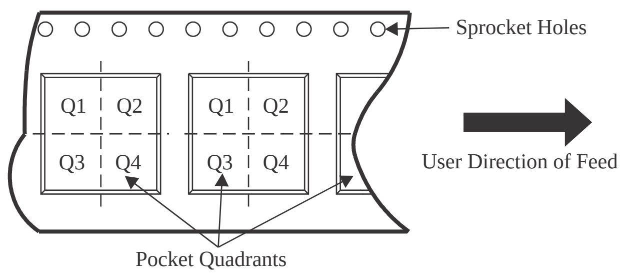


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

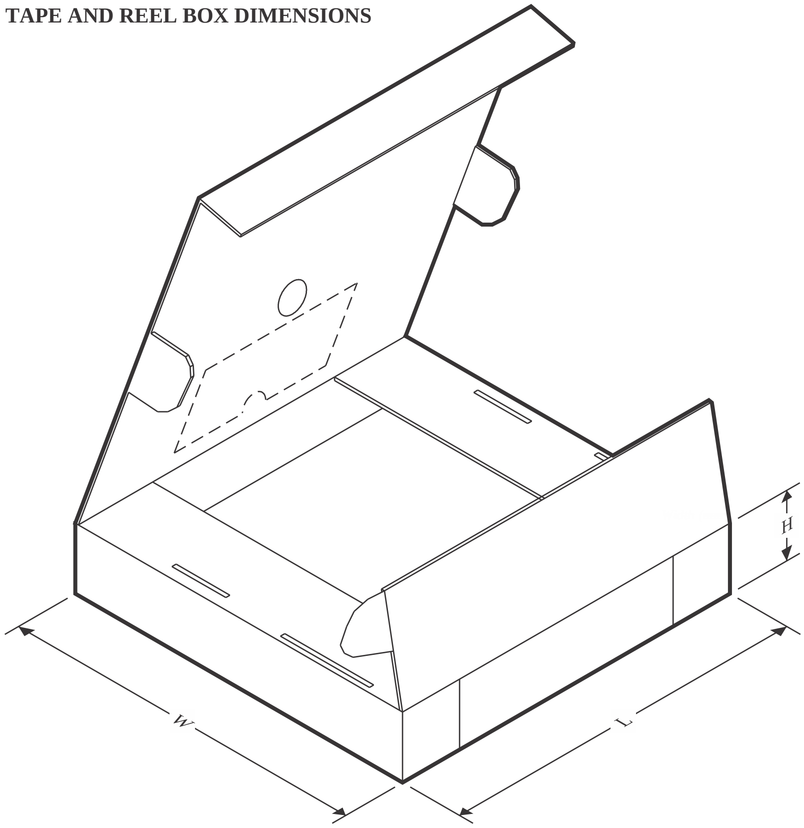
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCT8316A1VRGFR	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCT8316A1VRGFR	VQFN	RGF	40	3000	367.0	367.0	35.0

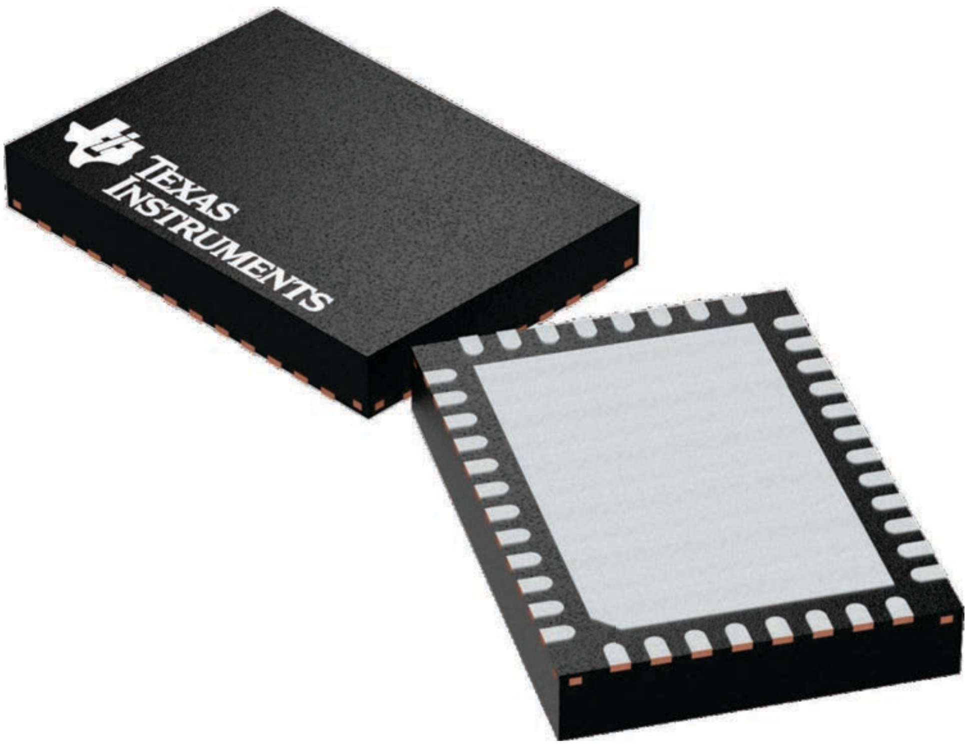
RGF 40

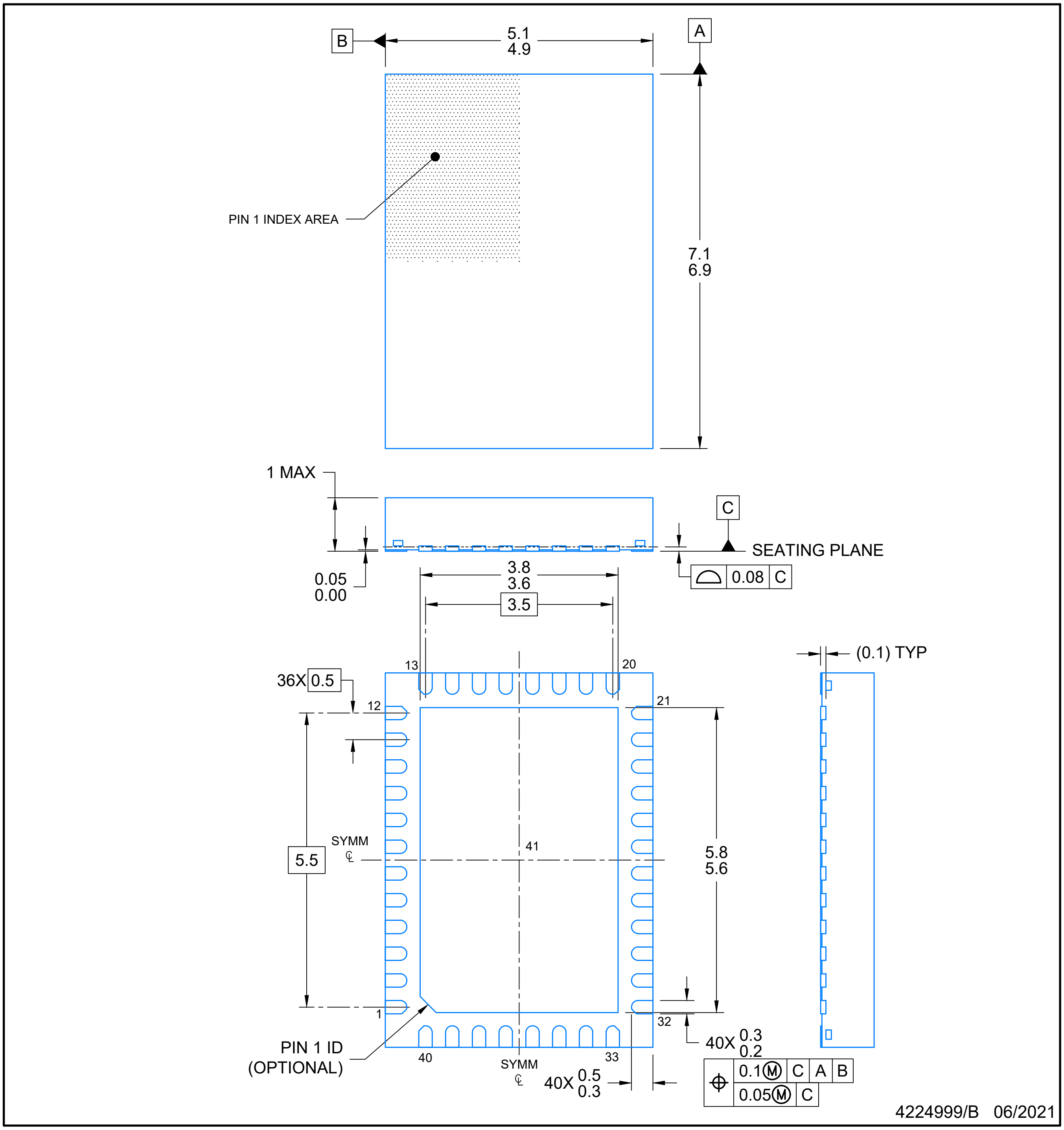
VQFN - 1 mm max height

5 x 7, 0.5 mm pitch

PLASTIC QUAD FLAT PACK- NO LEAD

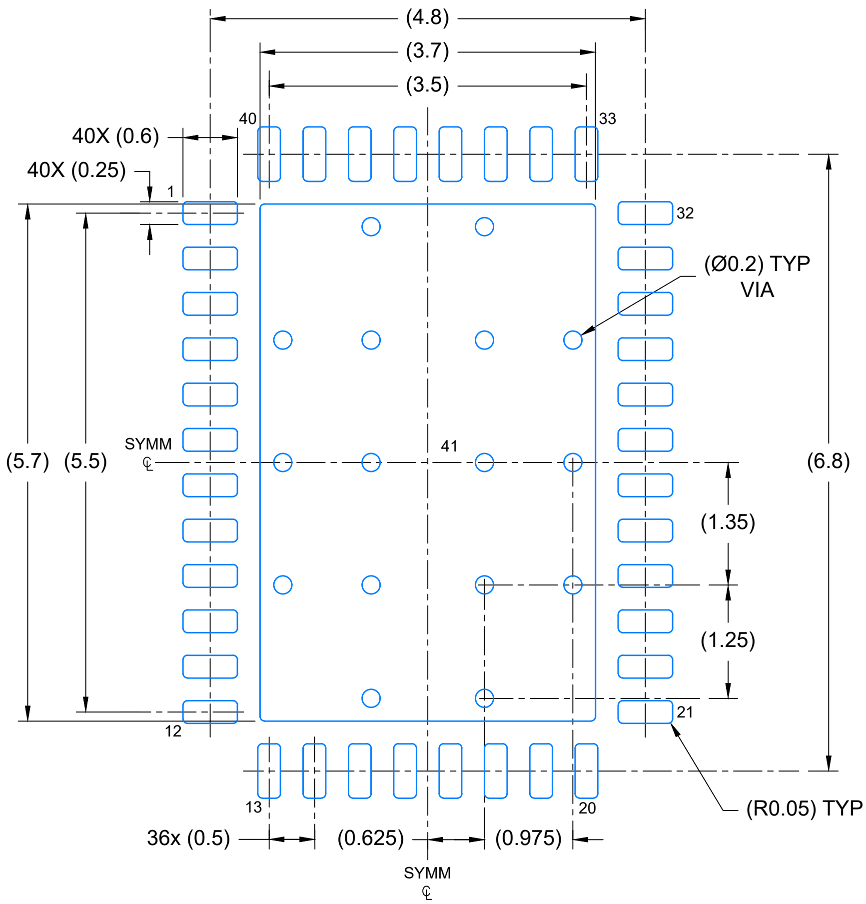
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



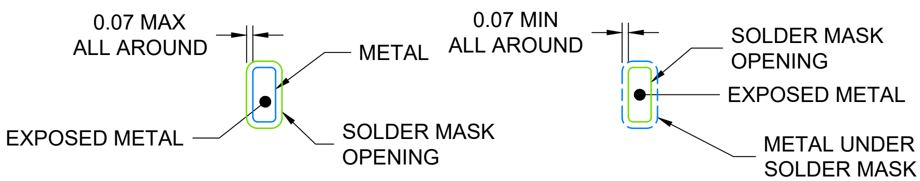


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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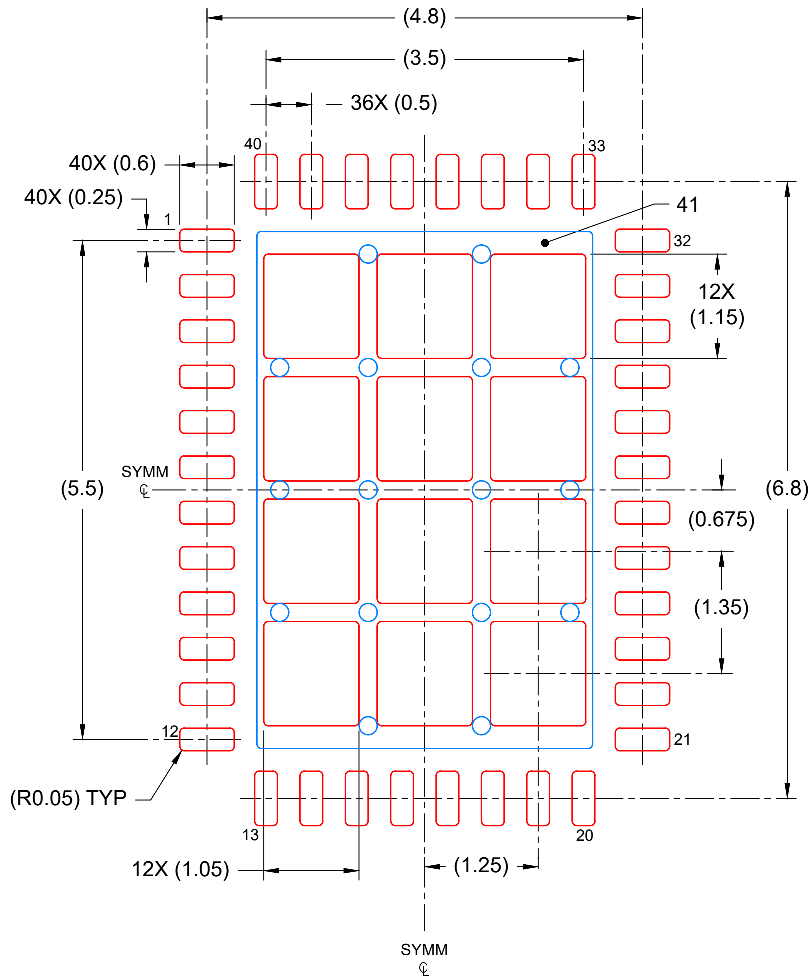
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

4224999/B 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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