OPAx170-Q1 36V 单电源、低功耗、汽车级运算放大器

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度等级 1：环境工作温度范围为 –40°C 至 +125°C
  - 器件 HBM ESD 分类等级 3A
  - 带电器件模型 (CDM) ESD 分类等级 C5
- 电源电压范围：2.7V 至 36V，±1.35V 至 ±18V
- 低噪声：19 nV/√Hz
- 已过滤的射频干扰 (RFI) 输入
- 输入范围包括负电源
- 输入范围运行至正电源
- 轨到轨输出
- 增益带宽：1.2MHz
- 低静态电流：每个放大器 110μA
- 高共模抑制：120dB
- 低偏置电流：15pA（最大值）
- 通道数量：
  - OPA170-Q1 - 1 条
  - OPA2170-Q1 - 2 条
  - OPA4170-Q1 - 4 条
- 行业标准封装

2 应用

- 汽车
- 混合动力汽车 (HEV) 和电动车 (EV) 动力传动
- 高级驾驶员辅助系统 (ADAS)
- 自动恒温控制
- 温度测量
- 应力计放大器
- 精密积分器

3 说明

OPA170-Q1、OPA2170-Q1 和 OPA4170-Q1 器件 (OPAx170-Q1) 属于 36V、单电源、低噪声运算放大器系列。该器件系列采用微型封装，可由电压介于 2.7V (±1.35V) 至 36V (±18V) 之间的电源供电运行。此类器件在确保静态电流较低的情况下提供良好的偏移、漂移和带宽。

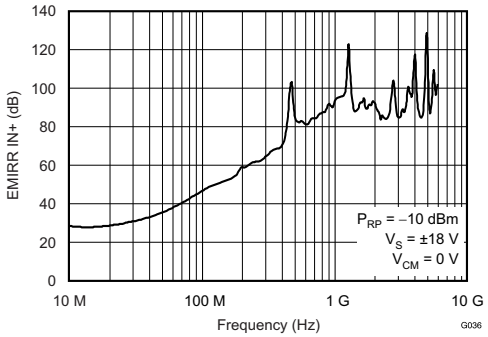
多数运算放大器仅有一个指定的电源电压，OPAx170-Q1 系列运算放大器则有所不同，其可在 2.7V 至 36V 电压范围内额定运行。超过电源轨的输入信号不会导致反相。OPAx170-Q1 系列在容性负载高达 300pF 时可保持稳定。输入可在负电源轨以下 100mV 以及正电源轨 2V 之内正常运行。请注意，这些器件可在正电源轨之上 100mV 的满轨到轨输入上运行，但是在正电源轨 2V 内运行时，性能会受到影响。OPAx170-Q1 运算放大器的额定工作温度范围为 -40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA170-Q1	SOT-23 (5)	2.90mm × 1.60mm
OPA2170-Q1	VSSOP (8)	3.00mm × 3.00mm
OPA4170-Q1	TSSOP封装(14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

EMIRR IN+ 与频率间的关系



目录

4 修订历史记录

Changes from Revision A (March 2017) to Revision B **Page**

- 已删除 从*器件信息* 表中删除了 8 引脚 SOIC、5 引脚 SOT、8 引脚 VSSOP 和 14 引脚 SOIC 封装 ... 1
- 已更改 首页图 ... 1
- Deleted OPA170-Q1 D (SOIC) and DRL (SOT) pinout drawings and pinout table information ... 3
- Deleted OPA2170-Q1 D (SOIC) and DCU (VSSOP *Micro* size packages ... 4
- Deleted OPA170-Q1 D (SOIC) pinout drawing ... 5
- Deleted D (SOIC) and DRL (SOT) thermal information from OPA170-Q1 *Thermal Information* table ... 7
- Deleted D (SOIC) and DCU (VSSOP) thermal information from OPA2170-Q1 *Thermal Information* table ... 7
- Deleted D (SOIC) thermal information from OPA4170-Q1 *Thermal Information* table ... 7
- 已更改 values in 图 38 from 250 Ω to 2.5 kΩ ... 21

Changes from Original (December 2016) to Revision A **Page**

- 已删除 说明中第一段的*最后一句* ... 1
- Deleted static literature number in *Thermal Information: OPA170-Q1* table note ... 7
- Separated the IB and IOS test conditions for the OPA4170 in *Electrical Characteristics* table ... 8
- 已添加 additional text to Figure 8 title ... 12
- 已更改 "many specifications apply from –40°C to +125°C" to "many specifications apply from –40°C to +85°C" to correct typo ... 26

5 Pin Configuration and Functions

OPA170-Q1 DBV Package
5-Pin SOT-23
Top View

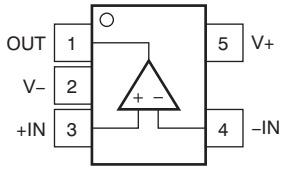


Table 1. Pin Functions: OPA170-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN– (–IN)	4	I	Negative (inverting) input
IN+ (+IN)	3	I	Positive (noninverting) input
OUT	1	O	Output
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

OPA2170-Q1 DGK Package
8-Pin VSSOP
Top View

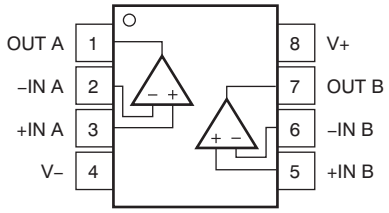


Table 2. Pin Functions: OPA2170-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

OPA4170-Q1 PW Package
14-Pin TSSOP
Top View

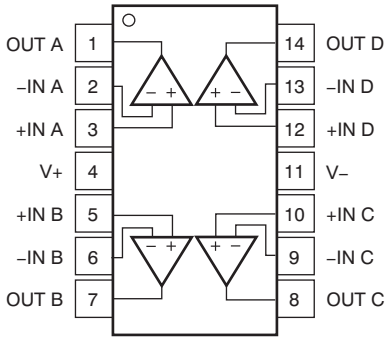


Table 3. Pin Functions: OPA4170-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage	–20	20	V
Single supply voltage		40	V
Signal input pin voltage	(V–) – 0.5	(V+) + 0.5	V
Signal input pin current	–10	10	mA
Output short-circuit current(2)	Continuous		
Operating ambient temperature, T_A	–55	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V+ – V–)	2.7	36	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information: OPA170-Q1

THERMAL METRIC(1)		OPA170-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	245.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	133.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2170-Q1

THERMAL METRIC(1)		OPA2170-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4170-Q1

THERMAL METRIC(1)		OPA4170-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C		0.25	±1.8	mV
		T_A = –40°C to 125°C			±2	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		±0.3	±2	µV/°C
PSRR	Input offset voltage vs power supply	V_S = 4 V to 36 V T_A = –40°C to 125°C		1	±5	µV/V
	Channel separation, dc			5		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		±8	±15	pA
		T_A = –40°C to 125°C (OPA170-Q1 and OPA2170-Q1)			±3.5	nA
		T_A = –40°C to 125°C (OPA4170-Q1)			±16	
I_{OS}	Input offset current	T_A = 25°C		±4	±15	pA
		T_A = –40°C to 125°C (OPA170-Q1 and OPA2170-Q1)			±3.5	nA
		T_A = –40°C to 125°C (OPA4170-Q1)			±16	
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		22		$nV/\sqrt{Hz}$
		f = 1 kHz		19		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range (1)		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = ±2 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V T_A = –40°C to 125°C	90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V T_A = –40°C to 125°C	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 4 V to 36 V (V–) + 0.35 V < V_O < (V+) – 0.35 V T_A = –40°C to 125°C	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			1.2		MHz
SR	Slew rate	G = 1		0.4		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = 1 10-V step		20		µs
		To 0.01% (12-bit), V_S = ±18 V, G = 1 10-V step		28		µs
	Overload recovery time	V_{IN} × Gain > V_S		2		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}		0.0002%		

(1) The input range can be extended beyond (V+) – 2 V up to V+. For additional information, see *Typical Characteristics* and *Application and Implementation*.

Electrical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from positive rail	I_L = 0 mA V_S = 4 V to 36 V	10			mV
		I_L sourcing 1 mA V_S = 4 V to 36 V	115			mV
V_O	Voltage output swing from negative rail	I_L = 0 mA V_S = 4 V to 36 V			8	mV
		I_L sinking 1 mA V_S = 4 V to 36 V			70	mV
V_O	Voltage output swing from rail	V_S = 5 V R_L = 10 kΩ T_A = –40°C to 125°C	(V–) + 0.03		(V+) – 0.05	V
		R_L = 10 kΩ A_{OL} ≥ 110 dB T_A = –40°C to 125°C	(V–) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current		–20		17	mA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			pF
R_O	Open-loop output resistance	f = 1 MHz I_O = 0 A		900		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A T_A = 25°C		110	145	µA
		I_O = 0 A T_A = –40°C to 125°C			155	µA
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–55		150	°C

6.8 Typical Characteristics: Table of Graphs

表 4. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature	图 3
Offset Voltage vs Common-Mode Voltage	图 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	图 5
Offset Voltage vs Power Supply	图 6
I_B and I_{OS} vs Common-Mode Voltage	图 7
Input Bias Current vs Temperature	图 8
Output Voltage Swing vs Output Current (Maximum Supply)	图 9
CMRR and PSRR vs Frequency (Referred-to-Input)	图 10
CMRR vs Temperature	图 11
PSRR vs Temperature	图 12
0.1-Hz to 10-Hz Noise	图 13
Input Voltage Noise Spectral Density vs Frequency	图 14
THD+N Ratio vs Frequency	图 15
THD+N vs Output Amplitude	图 16
Quiescent Current vs Temperature	图 17
Quiescent Current vs Supply Voltage	图 18
Open-Loop Gain and Phase vs Frequency	图 19
Closed-Loop Gain vs Frequency	图 20
Open-Loop Gain vs Temperature	图 21
Open-Loop Output Impedance vs Frequency	图 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	图 23, 图 24
No Phase Reversal	图 25
Positive Overload Recovery	图 26
Negative Overload Recovery	图 27
Small-Signal Step Response (100 mV)	图 28, 图 29
Large-Signal Step Response	图 30, 图 31
Large-Signal Settling Time (10-V Positive Step)	图 32
Large-Signal Settling Time (10-V Negative Step)	图 33
Short-Circuit Current vs Temperature	图 34
Maximum Output Voltage vs Frequency	图 35
EMIRR IN+ vs Frequency	图 36

6.9 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

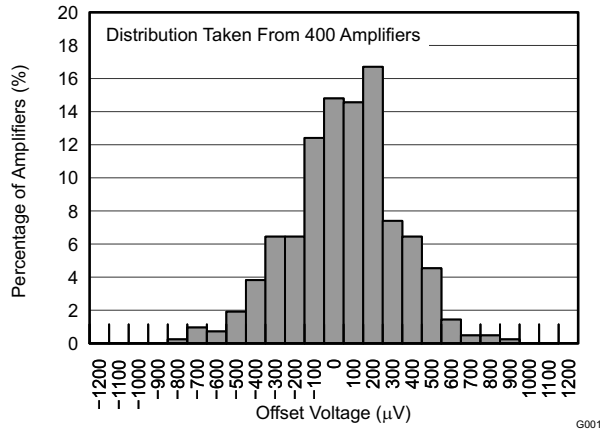


图 1. Offset Voltage Production Distribution

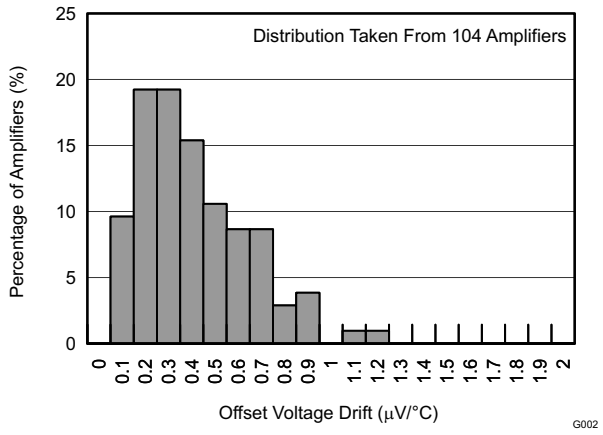


图 2. Offset Voltage Drift Distribution

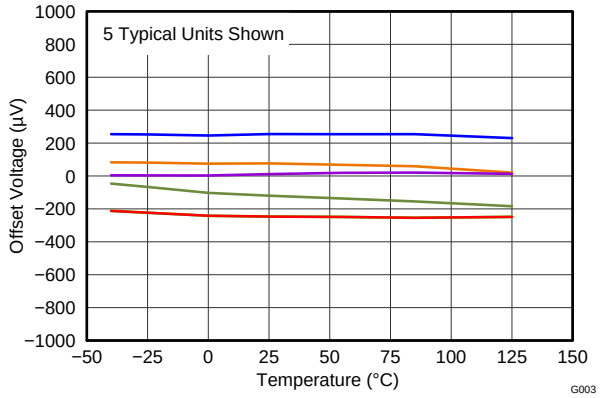


图 3. Offset Voltage vs Temperature

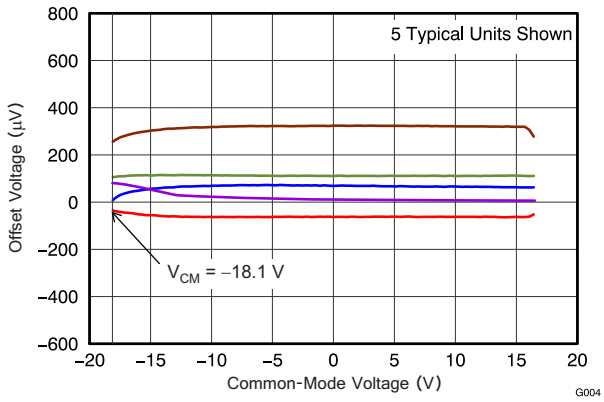


图 4. Offset Voltage vs Common-Mode Voltage

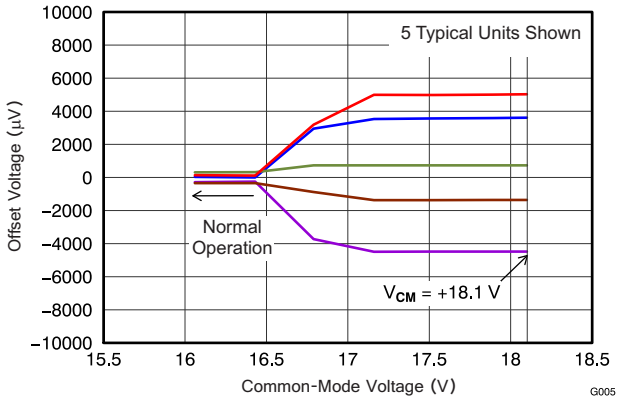


图 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

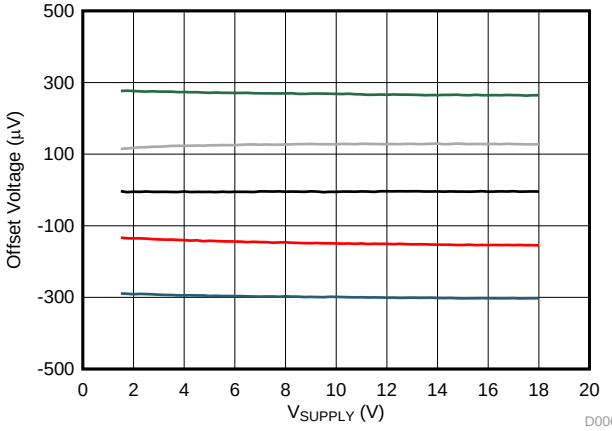


图 6. Offset Voltage vs Power Supply

Typical Characteristics (接下页)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

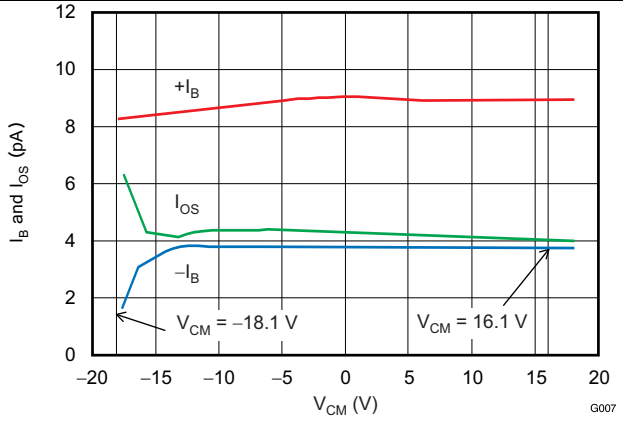


图 7. I_B and I_{OS} vs Common-Mode Voltage

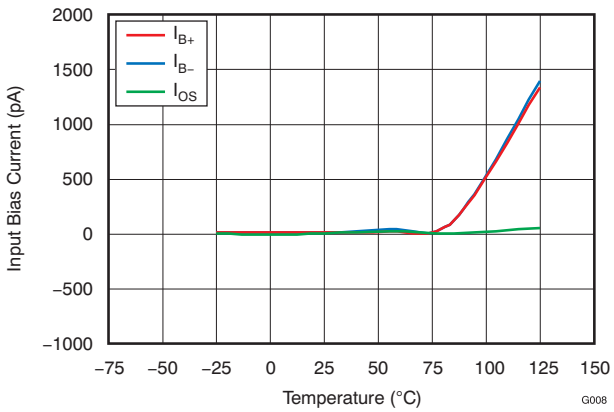


图 8. Input Bias Current vs Temperature for Single and Dual Versions

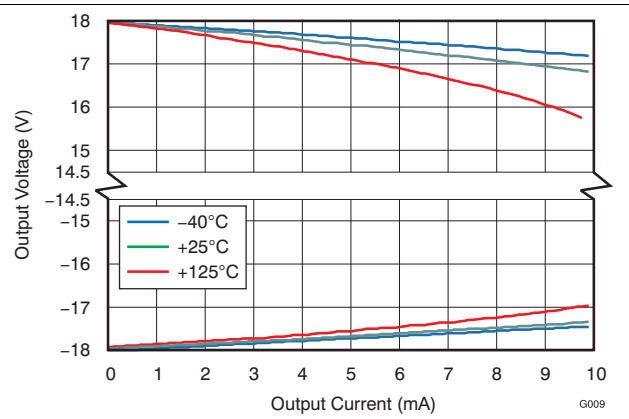


图 9. Output Voltage Swing vs Output Current (Maximum Supply)

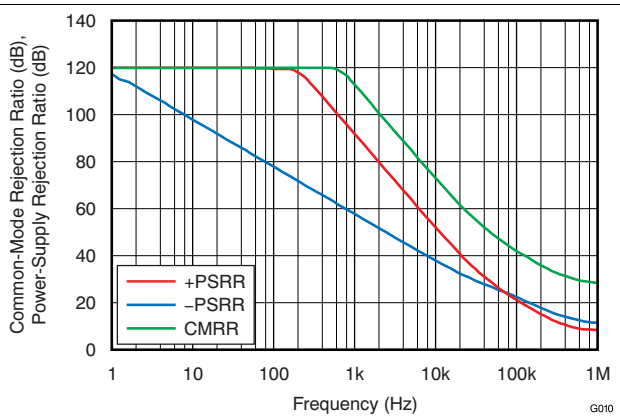


图 10. CMRR and PSRR vs Frequency (Referred to Input)

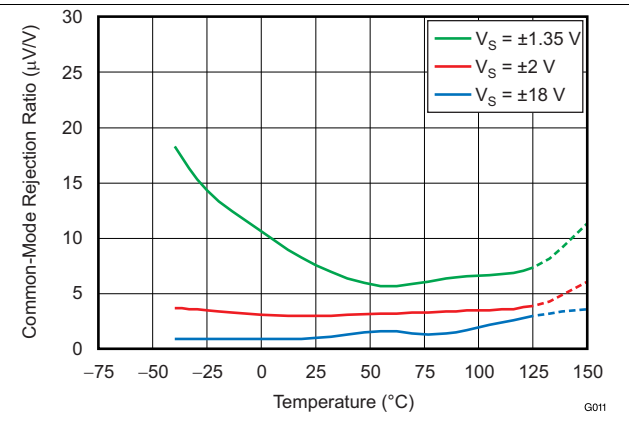


图 11. CMRR vs Temperature

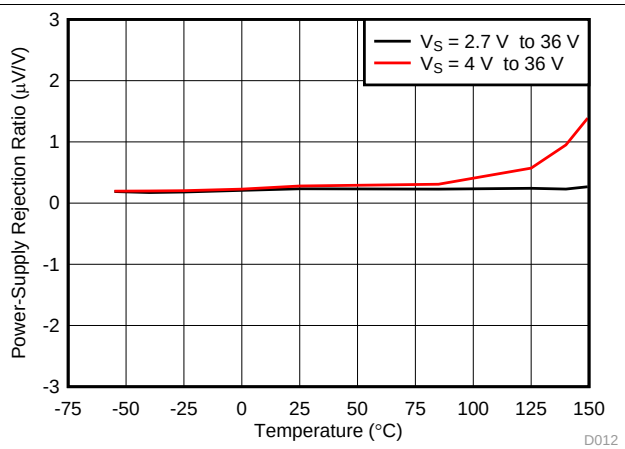


图 12. PSRR vs Temperature

Typical Characteristics (接下页)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

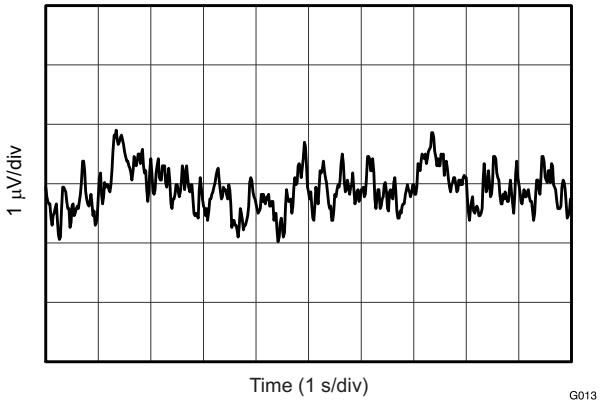


图 13. 0.1-Hz to 10-Hz Noise

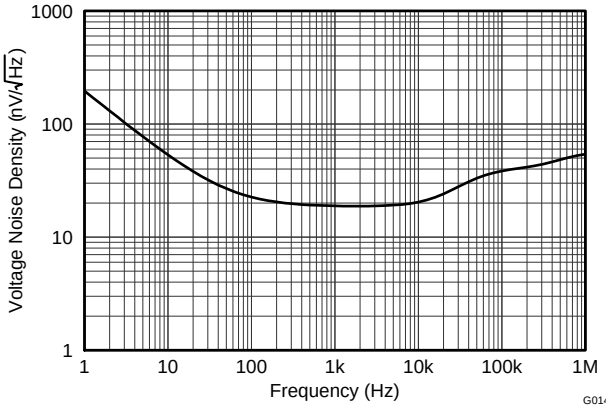


图 14. Input Voltage Noise Spectral Density vs Frequency

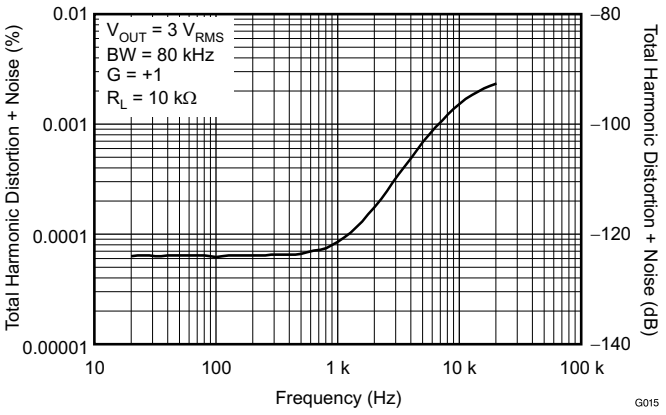


图 15. THD + N Ratio vs Frequency

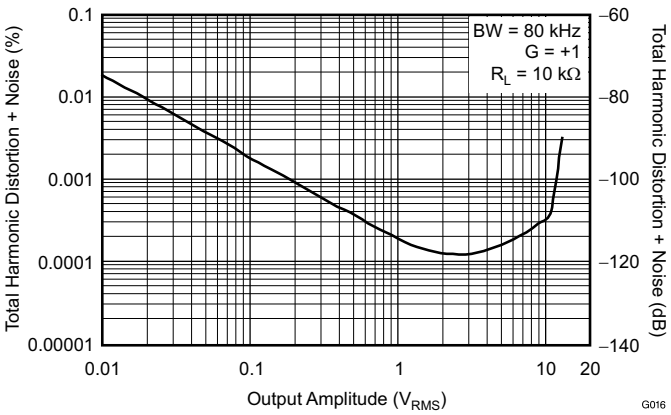


图 16. THD + N vs Output Amplitude

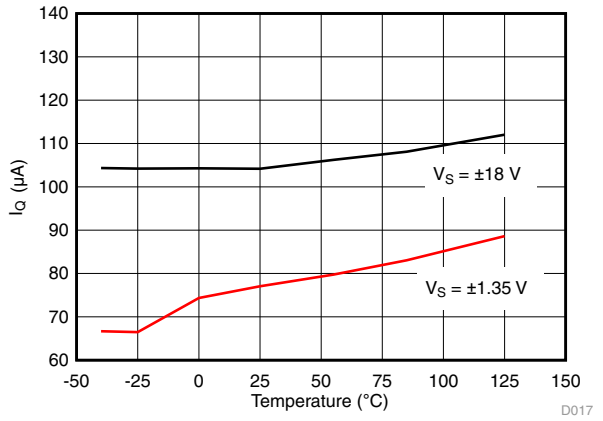


图 17. Quiescent Current vs Temperature

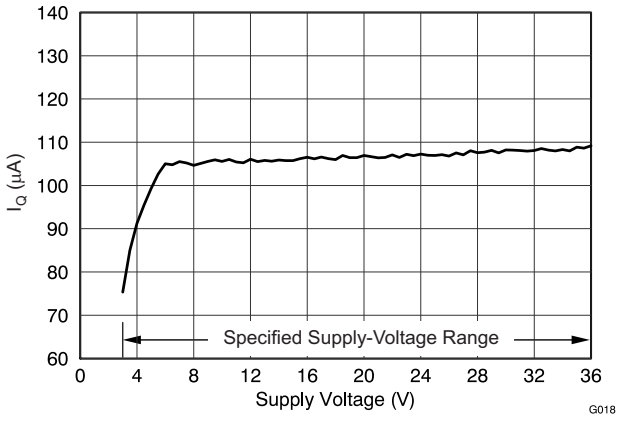


图 18. Quiescent Current vs Supply Voltage

Typical Characteristics (接下页)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

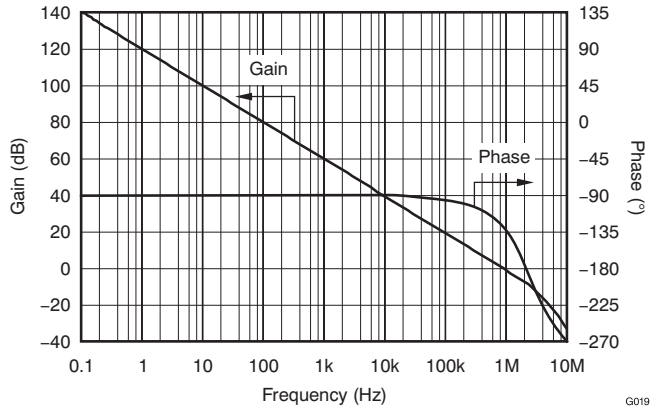


图 19. Open-Loop Gain and Phase vs Frequency

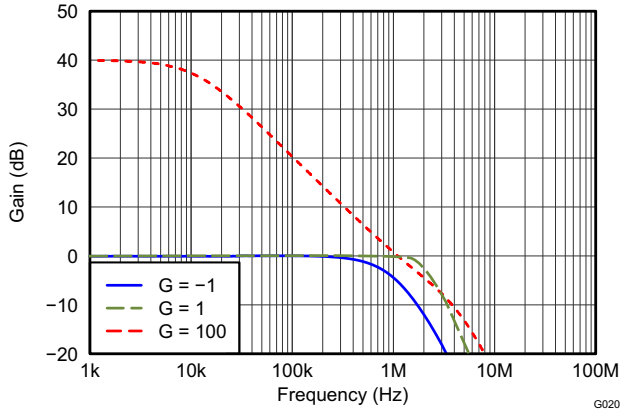


图 20. Closed-Loop Gain vs Frequency

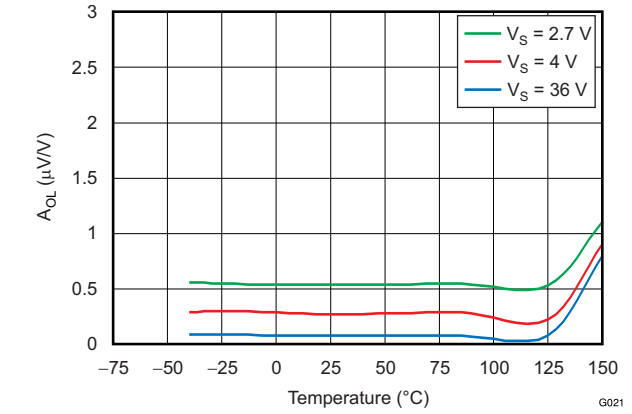


图 21. Open-Loop Gain vs Temperature

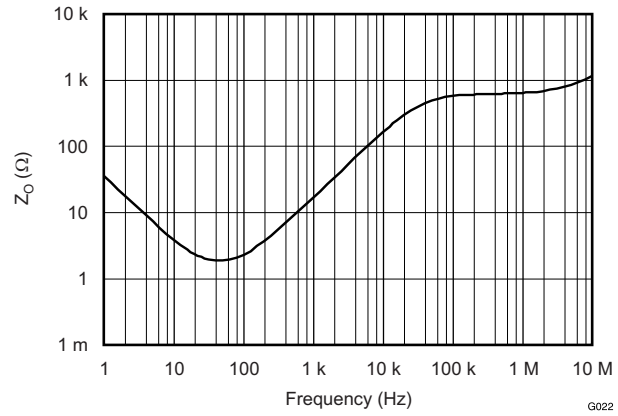


图 22. Open-Loop Output Impedance vs Frequency

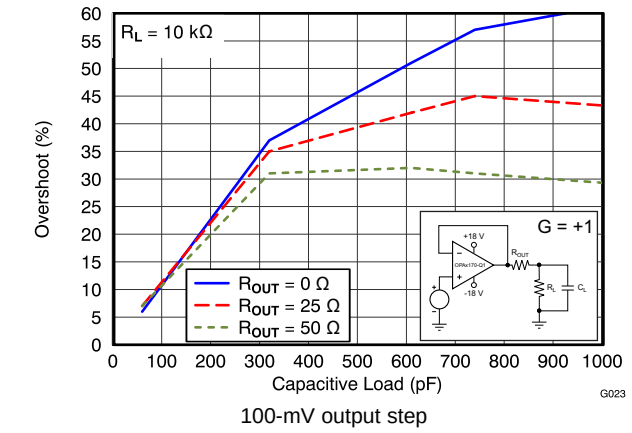


图 23. Small-Signal Overshoot vs Capacitive Load

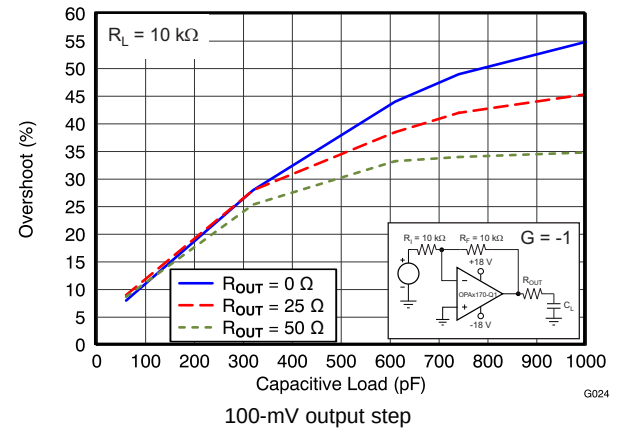


图 24. Small-Signal Overshoot vs Capacitive Load

Typical Characteristics (接下页)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

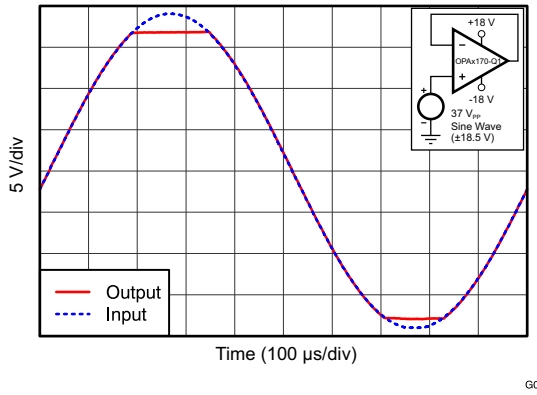


图 25. No Phase Reversal

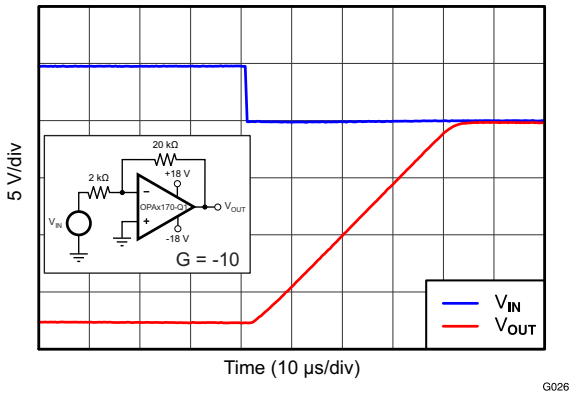


图 26. Positive Overload Recovery

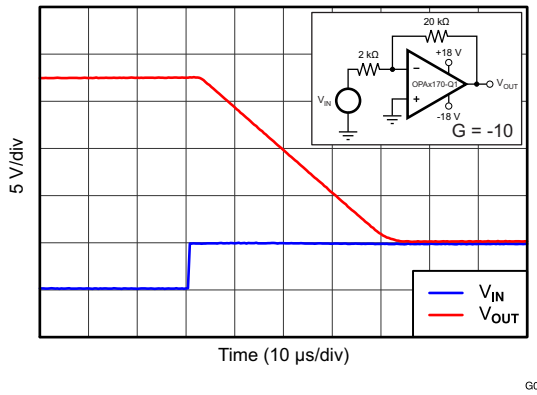


图 27. Negative Overload Recovery

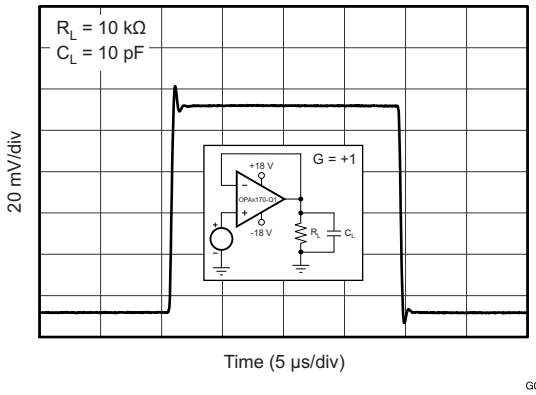


图 28. Small-Signal Step Response (100-mV)

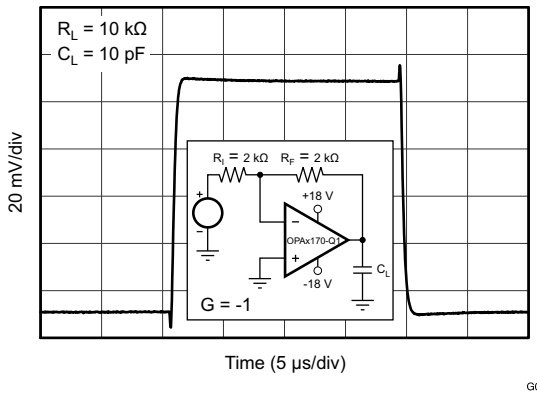


图 29. Small-Signal Step Response (100-mV)

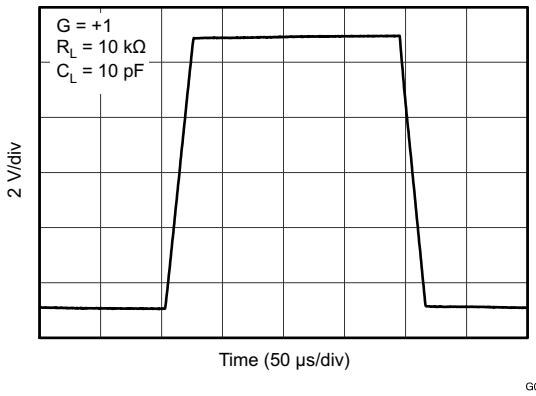


图 30. Large-Signal Step Response

Typical Characteristics (接下页)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

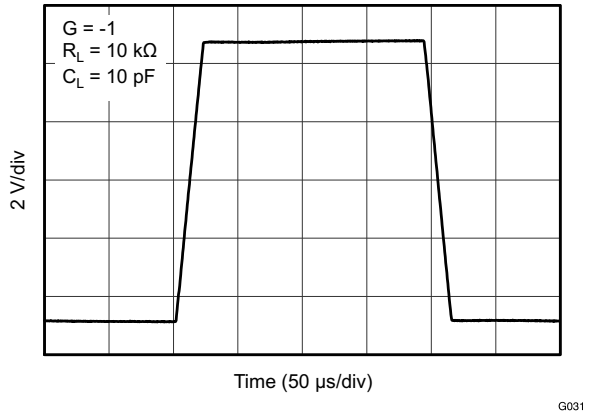
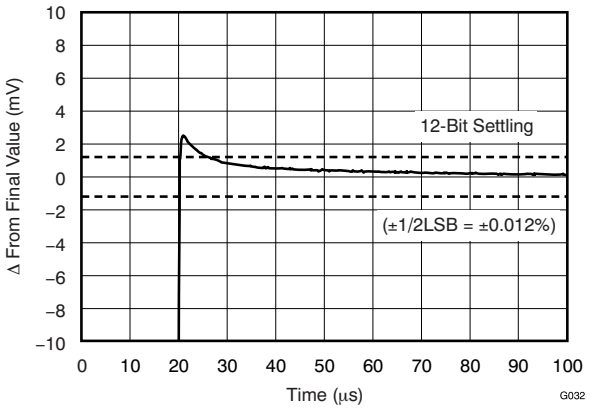
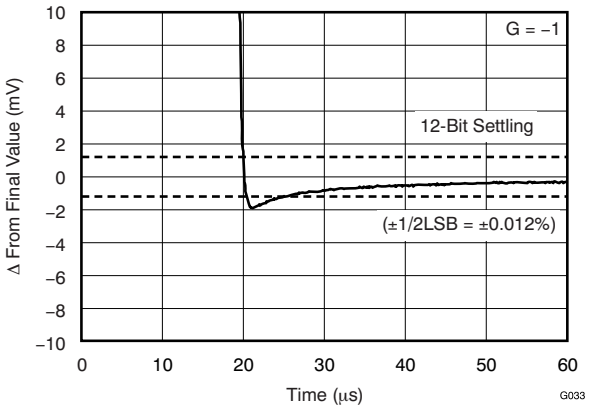


图 31. Large-Signal Step Response



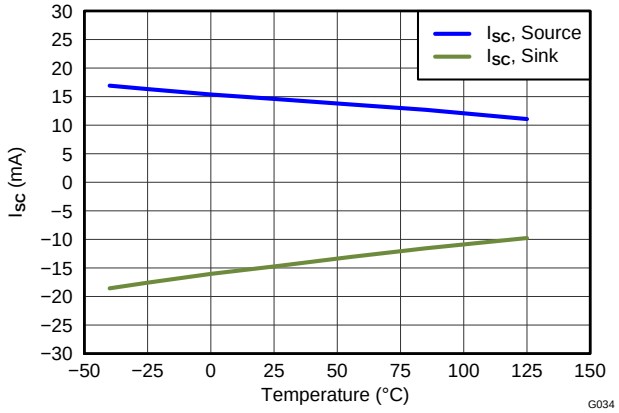
10-V positive step

图 32. Large-Signal Settling Time



10-V negative step

图 33. Large-Signal Settling Time



10-V negative step

图 34. Short-Circuit Current vs Temperature

Typical Characteristics (接下页)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

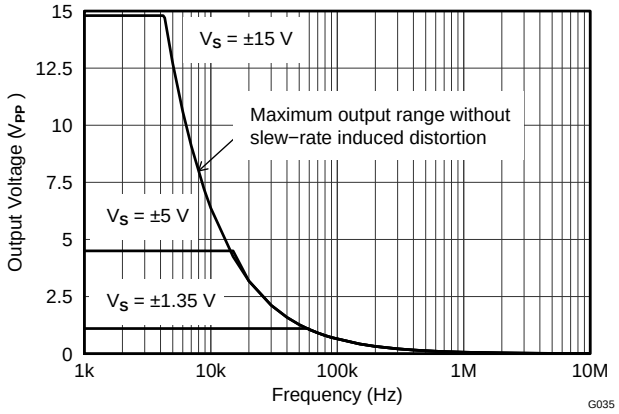


图 35. Maximum Output Voltage vs Frequency

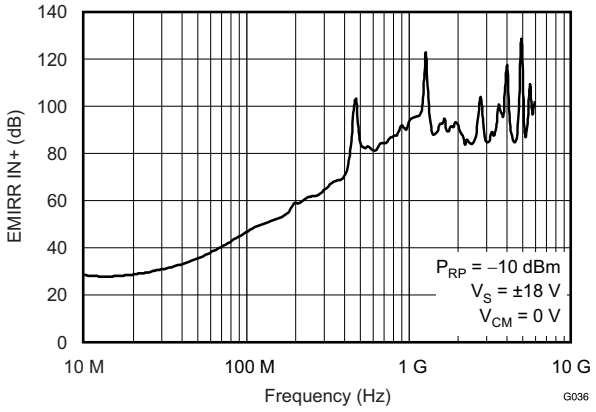


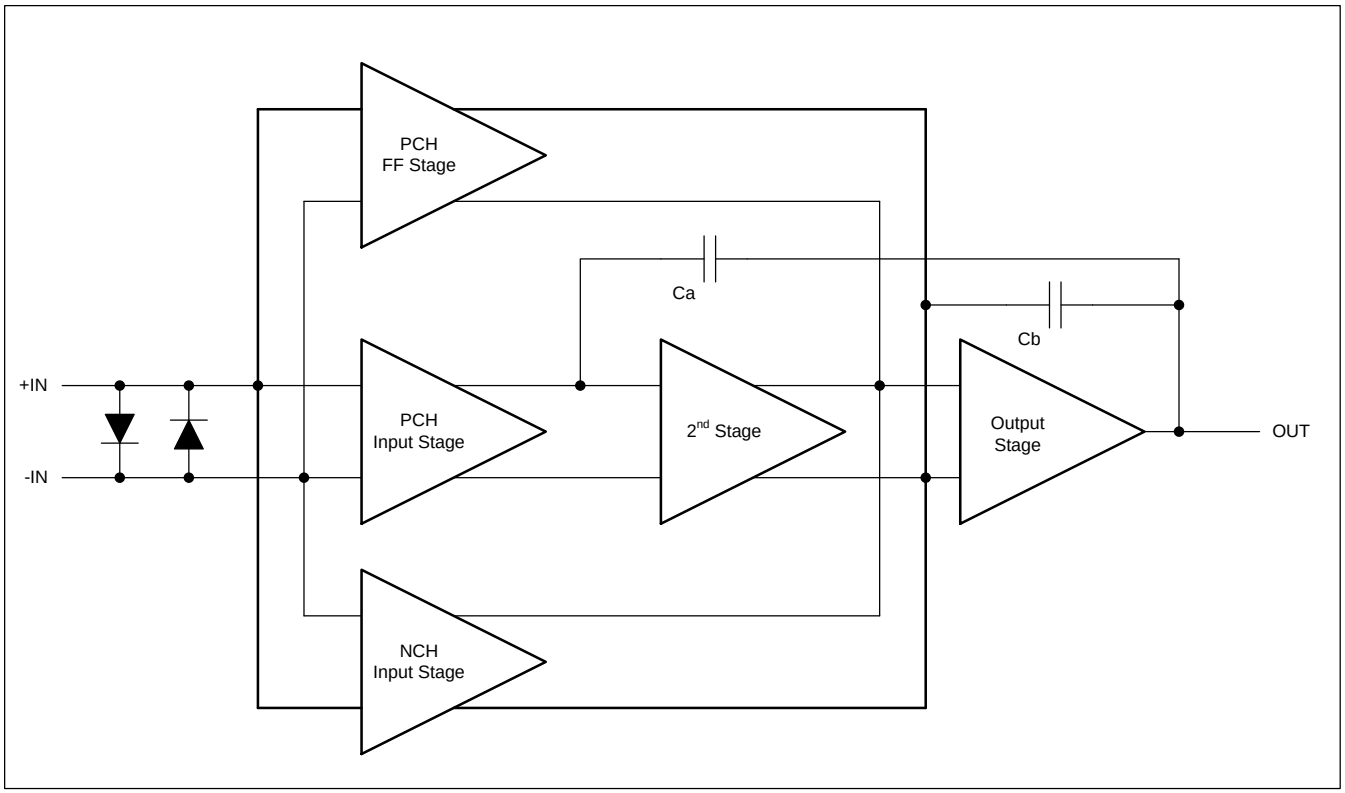
图 36. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The OPAx170-Q1 family of operational amplifiers provides high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 2 μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx170-Q1 family of amplifiers is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are listed in *表 4*.

Feature Description (接下页)

7.3.2 Phase-Reversal Protection

The OPAx170-Q1 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx170-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. 图 37 shows this performance.

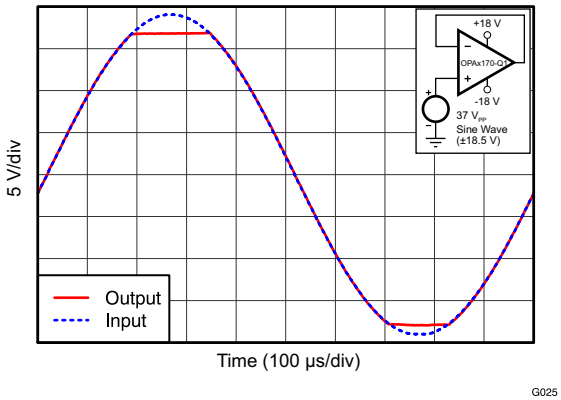


图 37. No Phase Reversal

7.3.3 Electrical Overstress

Designers typically ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions typically focus on the device inputs, but may involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of basic ESD circuitry and the relevance of the circuitry to an electrical overstress event is helpful. 图 38 shows the ESD circuits (indicated by the dashed line area) in the OPAx170-Q1. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (接下页)

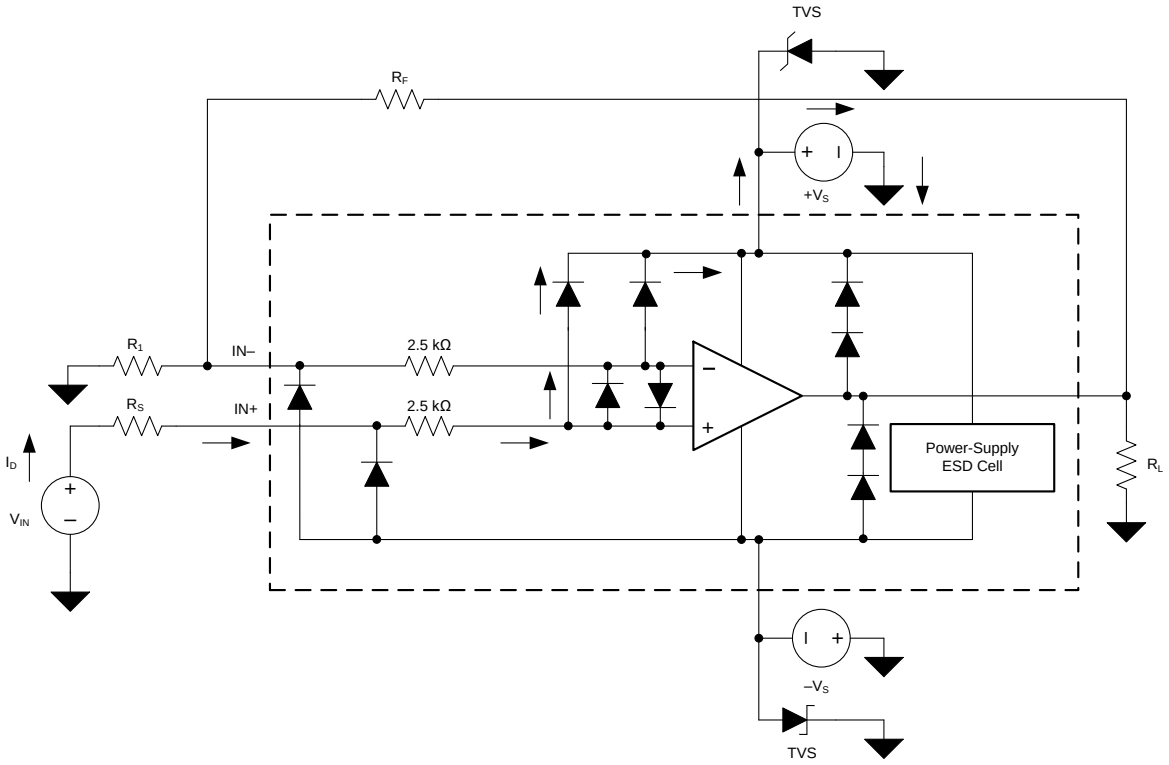


图 38. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. The absorption device can activate depending on the path of the current. The absorption device has a trigger (or threshold voltage) that is above the normal operating voltage of the OPAx170-Q1, but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (see 图 38), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 38 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Feature Description (接下页)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 图 38. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPAx170-Q1 input pins are protected from excessive differential voltage with back-to-back diodes, as shown in 图 38. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx170-Q1. 图 38 is an example configuration that implements a current-limiting feedback resistor.

7.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx170-Q1 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 图 39 and 图 40 are graphs showing small-signal overshoot versus capacitive load for several values of R_{OUT}. See *Feedback Plots Define Op Amp AC Performance* for details of analysis techniques and application circuits.

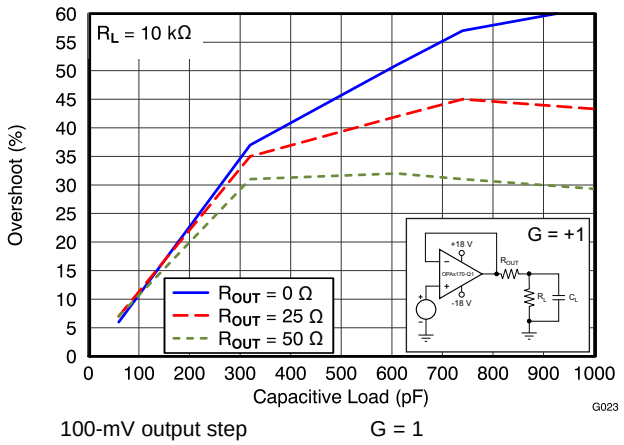


图 39. Small-Signal Overshoot vs Capacitive Load

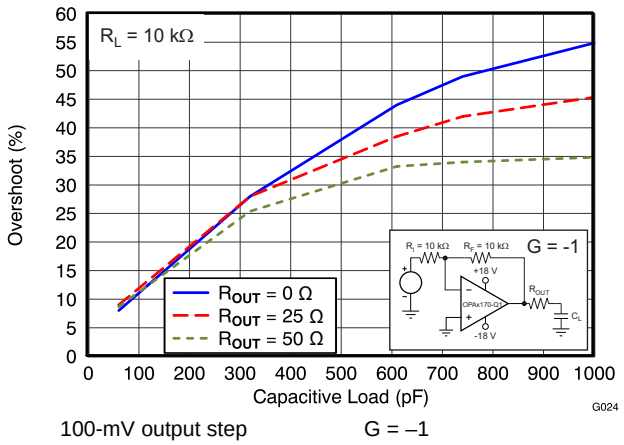


图 40. Small-Signal Overshoot vs Capacitive Load

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx170-Q1 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in 表 5.

表 5. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER		MIN	TYP	MAX	UNIT
Input common-mode voltage		(V+) – 2		(V+) + 0.1	V
Offset voltage			7		mV
	vs temperature		12		µV/°C
Common-mode rejection			65		dB
Open-loop gain			60		dB
Gain-bandwidth product			0.3		MHz
Slew rate			0.3		V/µs

7.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx170-Q1 is approximately 2 µs.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx170-Q1 family of operational amplifiers provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, capacitors with a value of 0.1 µF are adequate. Follow the additional recommendations in the *Layout Guidelines* section to achieve the maximum performance from this device. Many applications may introduce capacitive loading to the output of the amplifier that may cause instability. Adding an isolation resistor between the amplifier output and the capacitive load stabilizes the amplifier. The design process for selecting this resistor is shown in the *Typical Application* section.

8.2 Typical Application

This circuit can drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an operational amplifier. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.

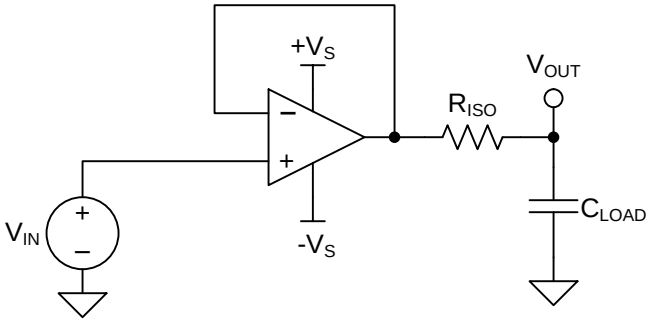


图 41. Unity-Gain Buffer With R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100-pF, 1000-pF, 0.01-µF, 0.1-µF, and 1-µF
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

图 41 shows a unity-gain buffer driving a capacitive load. 公式 1 shows the transfer function for the circuit in 图 41. Not shown in 图 41 is the open-loop output resistance of the operational amplifier, R_O.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in 公式 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_O + R_{ISO}) and C_{LOAD}. R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO}, so the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB / decade. 图 42 depicts the concept. The 1/β curve for a unity-gain buffer is 0 dB.

Typical Application (接下页)

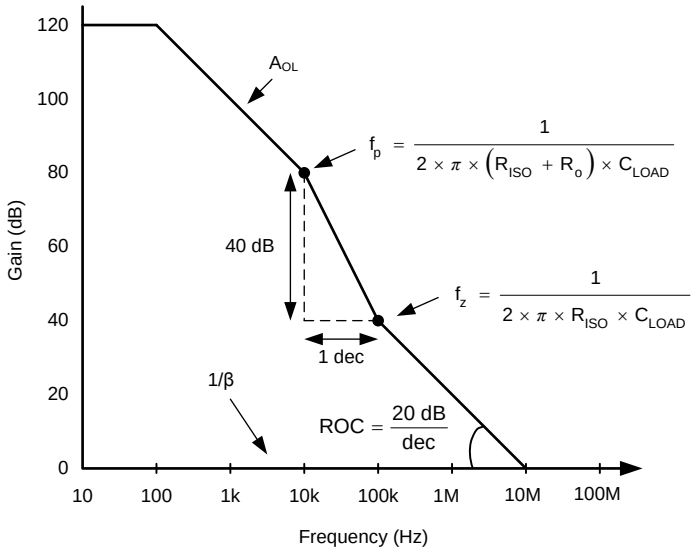


图 42. Unity-Gain Amplifier With R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_O. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 6 shows the overshoot percentage and ac gain peaking that correspond to 45° and 60° phase margins. For more details on this design and other alternative devices that can be used in place of the OPAx170-Q1 family, see *Capacitive Load Drive Solution Using an Isolation Resistor*.

表 6. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.3 Application Curve

Using the described methodology, the values of R_{ISO} that yield phase margins of 45º and 60º for various capacitive loads were determined. 图 43 shows the results.

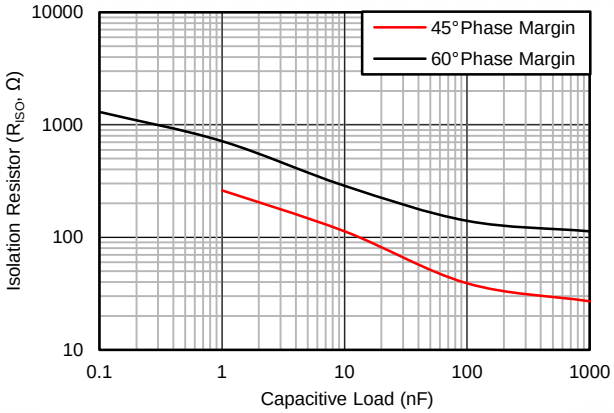


图 43. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

9 Power Supply Recommendations

The OPAx170-Q1 family is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *表 4*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in 图 45, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

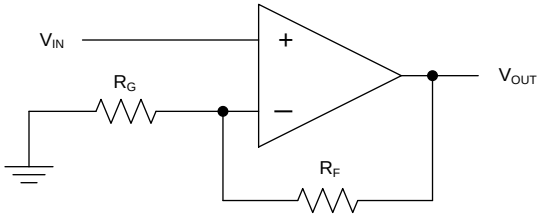


图 44. Schematic Representation of a Noninverting Configuration

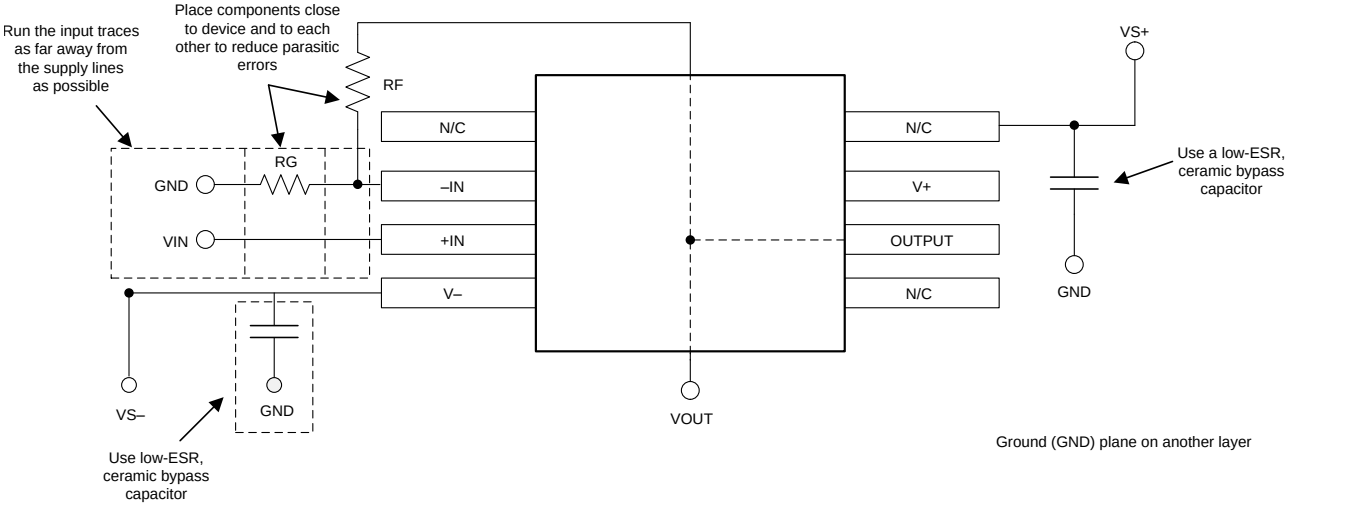


图 45. Operational Amplifier Board Layout for a Noninverting Configuration

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 WEBENCH® 设计中心免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 DIP 适配器 EVM

DIP 适配器 EVM 工具提供了一种针对小型表面贴装器件进行原型设计的简易低成本方法。评估工具适用于以下 TI 封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (MSOP-8)、DBV（SOT-23-6、SOT-23-5 和 SOT-23-3）、DCK（SC70-6 和 SC70-5）以及 DRL (SOT563-6)。DIP 适配器 EVM 也可搭配引脚排使用或直接与现有电路相连。

11.1.1.3 通用运算放大器评估模块 (EVM)

通用运放 EVM 是一系列通用空白电路板，可简化采用各种器件封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、MSOP、TSSOP 和 SOT-23 封装。

注

这些电路板均为空白电路板，用户必须自行提供相关器件。TI 建议您在订购通用运算放大器 EVM 时申请几个运算放大器器件样品。

11.1.1.4 TI 高精度设计

TI 高精度设计的模拟设计方案是由 TI 公司高精度模拟实验室设计 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

器件支持 (接下页)

11.1.1.5 WEBENCH® 滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。WEBENCH® Filter Designer 允许用户通过选择 TI 运算放大器以及 TI 供应商合作伙伴的无源组件构建优化滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

相关文档如下（下载网站 www.ti.com.cn）：

- *《反馈曲线图定义运算放大器交流性能》*
- *《采用隔离电阻的电容式负载驱动器解决方案》*

11.3 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **7.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
OPA170-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2170-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA4170-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA170AQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	170Q
OPA170AQDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	170Q
OPA2170AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2170
OPA2170AQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2170
OPA4170AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4170Q1
OPA4170AQPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4170Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA170-Q1, OPA2170-Q1, OPA4170-Q1 :

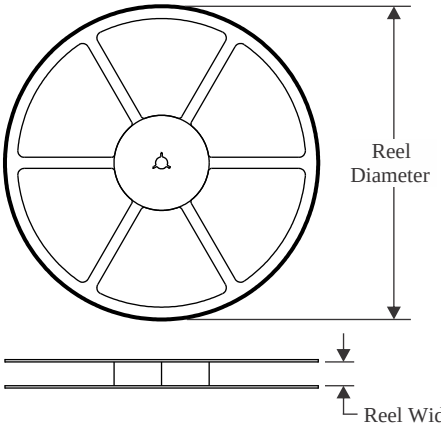
- Catalog : OPA170, OPA2170, OPA4170
- Enhanced Product : OPA170-EP

NOTE: Qualified Version Definitions:

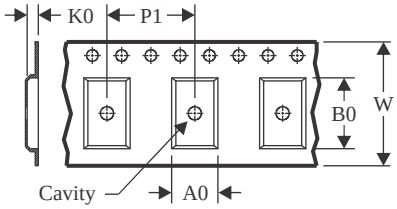
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

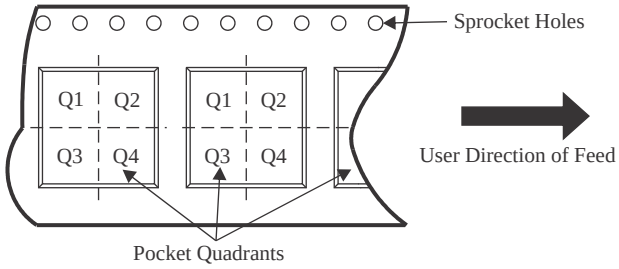


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

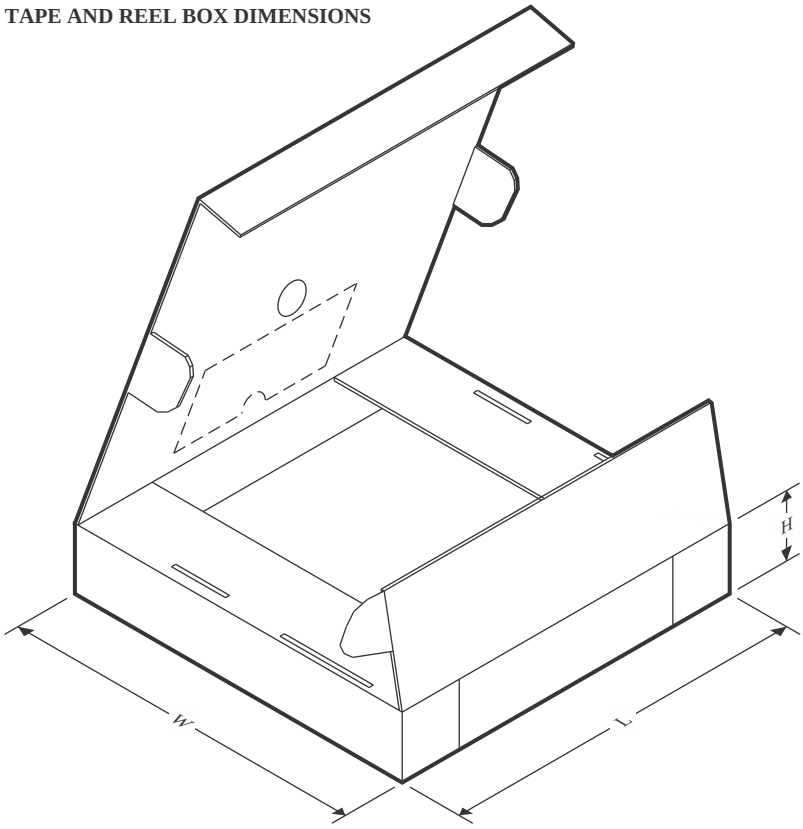
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA170AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2170AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA4170AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

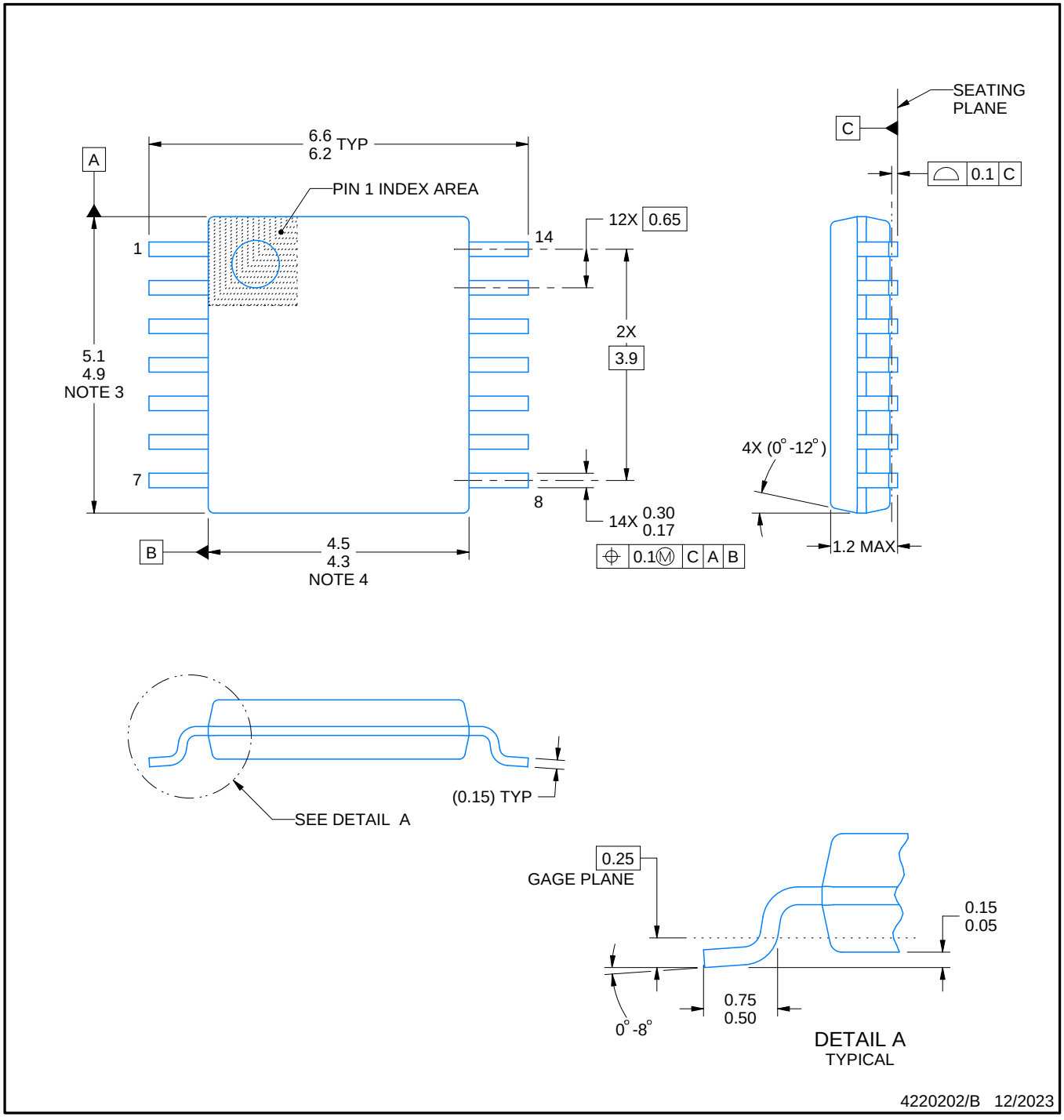
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA170AQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA2170AQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA4170AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0014A

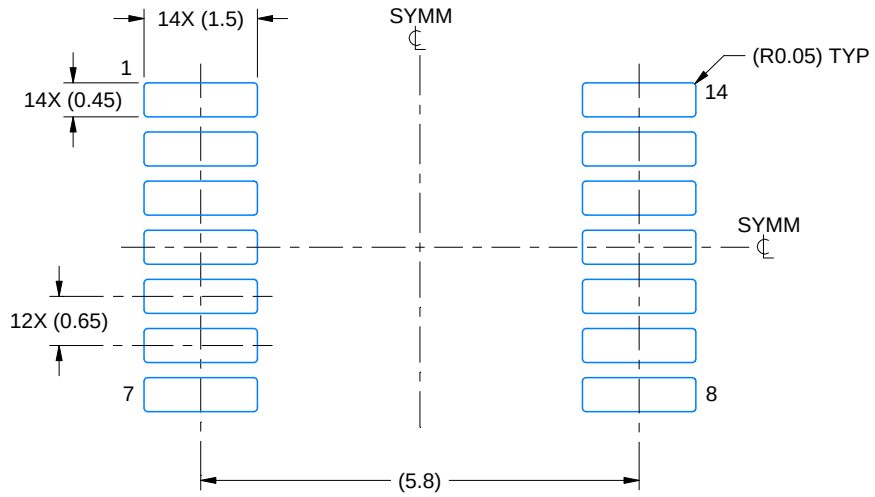
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

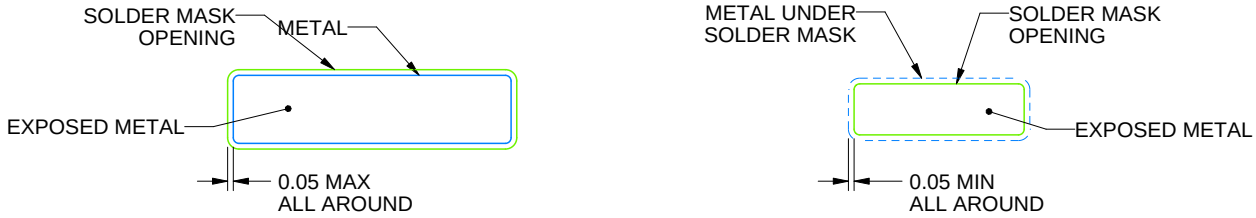


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

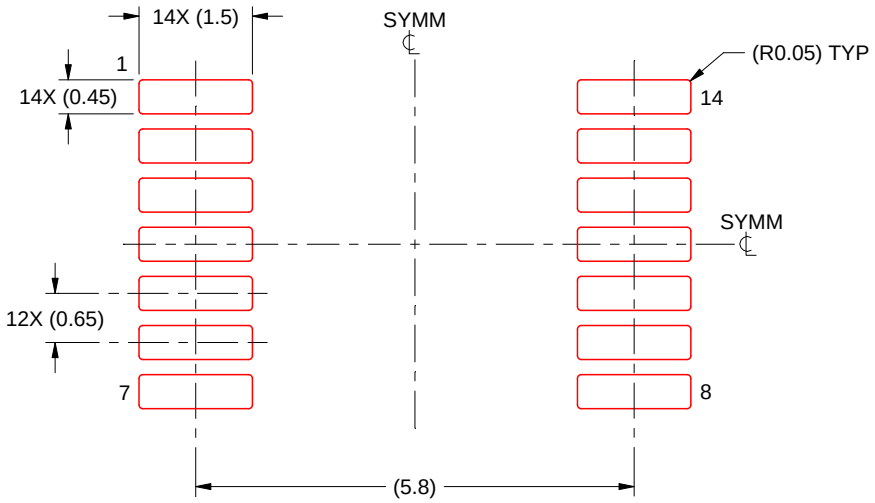


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

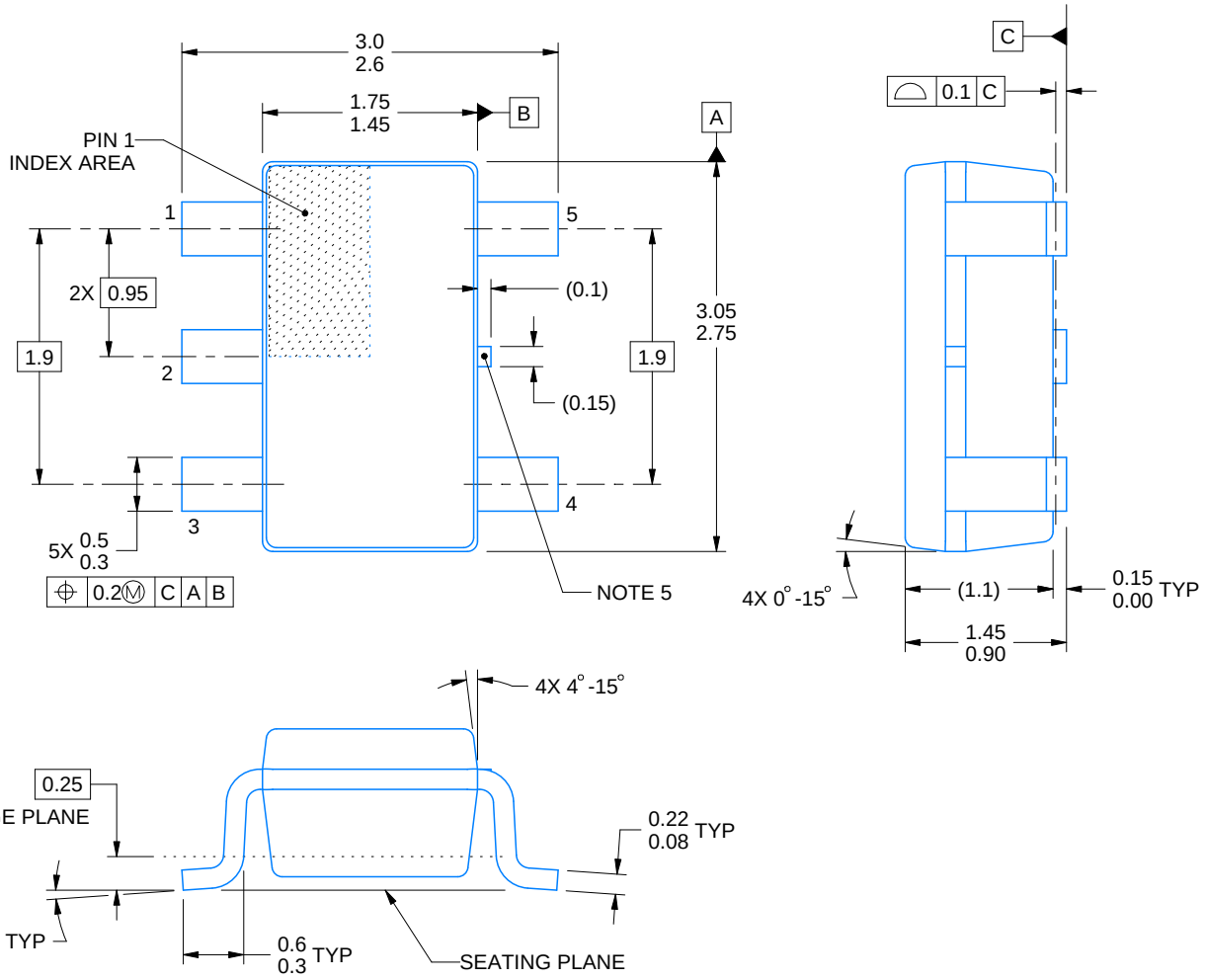
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

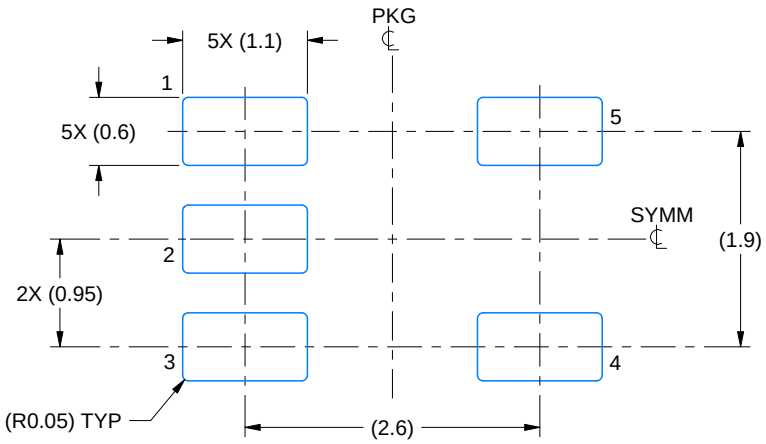
SMALL OUTLINE TRANSISTOR



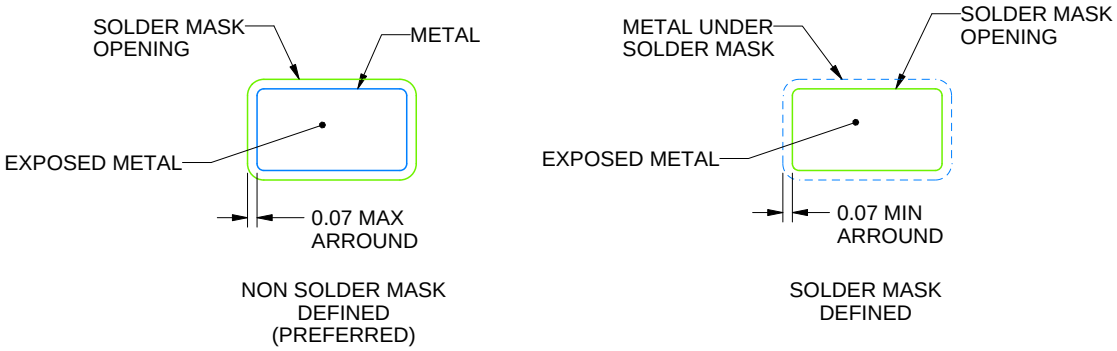
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

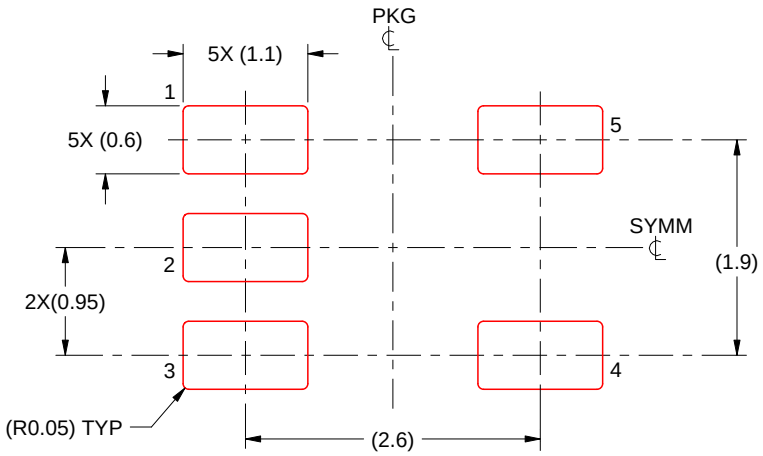


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

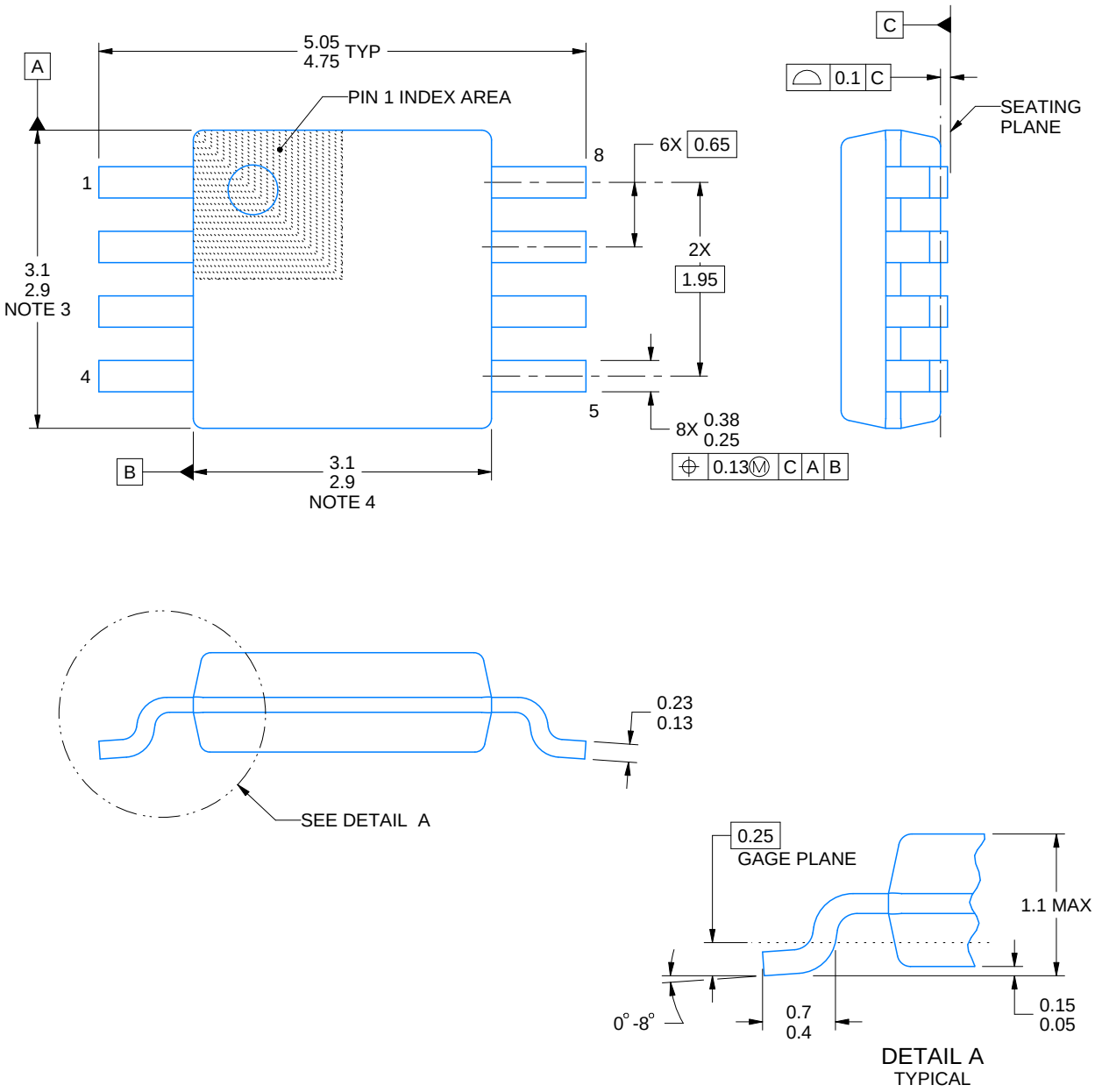
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

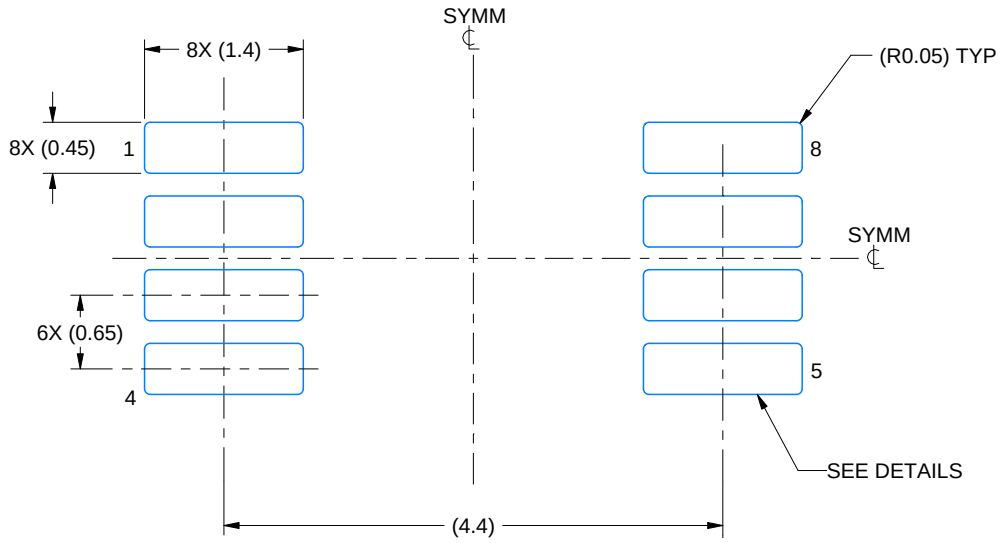
SMALL OUTLINE PACKAGE



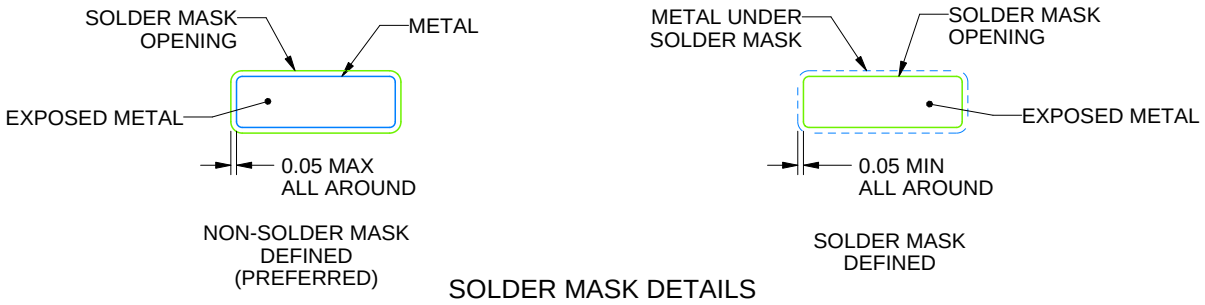
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

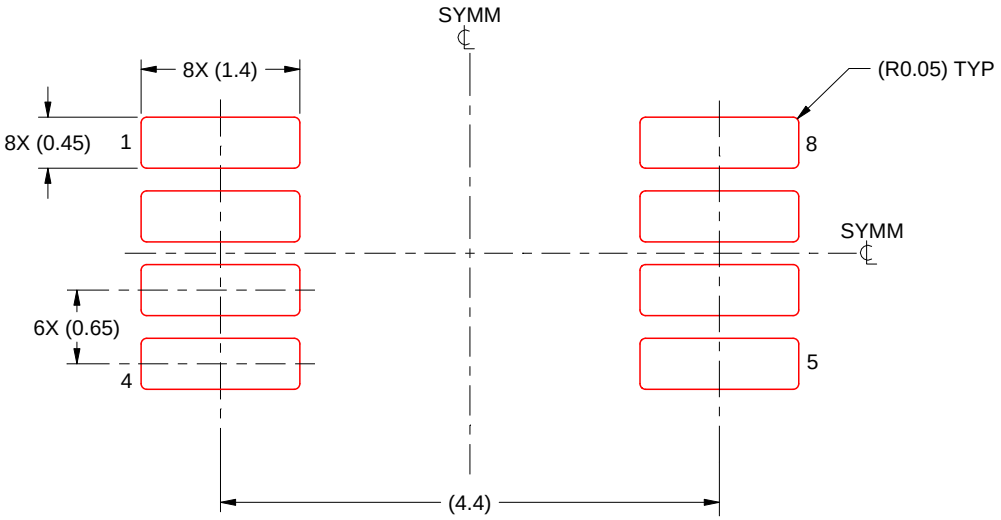


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月