OPA2211-EP 1.1nV/√Hz 噪声、低功耗精密运算放大器

1 特性

- 低电压噪声：1kHz 时为 1.1nV/√Hz
- 输入电压噪声: 80 nV_{PP}（0.1Hz 至 10Hz）
- 总谐波失真+噪声 (THD+N)：–136dB（G = 1，*f* = 1kHz）
- 偏移电压：180μV（最大值）
- 偏移电压漂移：0.35μV/°C（典型值）
- 低电源电流：3.6mA/通道（典型值）
- 单位增益稳定
- 增益带宽产品：
  80MHz (G= 100)
  45MHz (G= 1)
- 转换速率：27V/μs
- 16 位稳定时间：700ns
- 宽电源范围：
  ±2.25V 至 ±18V、+4.5V 至 +36V
- 轨到轨输出
- 输出电流：30mA
- 支持国防、航天和医疗应用
  - 受控基线
  - 同一组装和测试场所
  - 同一制造场所
  - 支持军用温度范围（-55°C 至 125°C） (1)
  - 延长的产品生命周期
  - 延长产品的变更通知周期
  - 产品可追溯性

2 应用范围

- 锁相环 (PLL) 环路滤波器
- 低噪声、低功耗信号处理
- 16 位模数转换器 (ADC) 驱动器
- 数模转换器 (DAC) 输出放大器
- 有源滤波器
- 低噪声仪表放大器
- 超声波放大器
- 专业音频前置放大器
- 低噪声频率合成器
- 红外检测器放大器
- 水下听音器放大器
- 地震检波器放大器
- 医疗

(1) 可提供额外温度范围--请与厂家联系

3 说明

OPA2211-EP 系列精密运算放大器通过仅 3.6mA 的电源电流即可实现 1.1nV/√Hz 极低噪声密度。 该系列器件同时提供轨到轨输出摆幅，最大限度地扩大了动态范围。

凭借极低电压和低电流噪声、高速以及宽输出摆幅等特性，OPA2211-EP 系列器件可作为性能优异的环路滤波器放大器而广泛应用于各类 PLL 应用。

在精密数据采集应用中，OPA2211-EP 系列运算放大器可在 10V 输出摆幅下为 16 位数据精度提供 700ns 的稳定时间。 该交流性能与仅为 125μV 的偏移电压以及 0.35μV/°C 的温度漂移相结合，使 OPA2211-EP 成为驱动高精度 16 位模数转换器 (ADC) 或缓冲高分辨率数模转换器 (DAC) 输出的理想选择。

OPA2211-EP 可在 ±2.25V 至 ±18V 的双电源宽电压范围或 4.5V 至 36V 的单电源宽电压范围内额定运行。

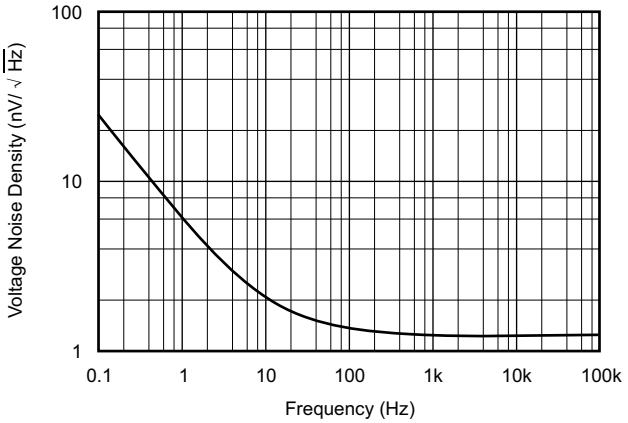
OPA2211-EP 采用小型双边扁平无引线 (DFN)-8 (3mm × 3mm) 封装。 此类运算放大器的额定工作结温范围 T_J = –55°C 至 125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA2211-EP	WSON (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

电压噪声密度与频率间的关系



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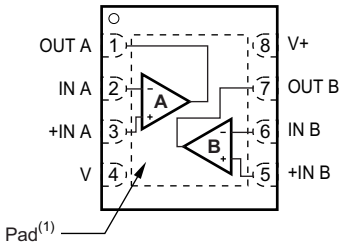
4 修订历史记录

日期	修订版本	注释
2015 年 11 月	*	最初发布。

5 Pin Configuration and Functions

DRG Package
8-Pin WSON
Top View



(1) Exposed thermal die pad on underside; connect thermal die pad to V–. Soldering the thermal pad improves heat dissipation and provides specified performance

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input for channel A
–IN A	2	I	Inverting input for channel A
+IN B	5	I	Noninverting input for channel B
–IN B	6	I	Inverting input for channel B
OUT A	1	O	Output terminal for channel A
OUT B	7	O	Output terminal for channel B
V+	8	—	Positive supply voltage
V–	4	—	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)		40	V
Input voltage		(V–) – 0.5	(V+) + 0.5	V
Input current (any pin except power-supply pins)		–10	10	mA
Output short-circuit(2)		Continuous		
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2 (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Operating temperature, T_J	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA2211-EP DRG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_S = ±2.25 to ±18 V

at T_J = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}	V_S = ±15 V		±50	±175	µV
Over temperature		T_J = –55°C to 125°C			±350	µV
Drift	dV_{OS}/dT	T_J = –55°C to 125°C		0.35		µV/°C
vs power supply	PSRR	V_S = ±2.25 V to ±18 V		0.1	1	µV/V
Over temperature					3	µV/V
INPUT BIAS CURRENT						
Input bias current	I_B	V_{CM} = 0 V, T_J = –55°C to 125°C		±50	±350	nA
Offset current	I_{OS}	V_{CM} = 0 V, T_J = –55°C to 125°C		±20	±200	nA
NOISE						
Input voltage noise	e_n	f = 0.1 Hz to 10 Hz		80		nV_{PP}
Input voltage noise density		f = 10 Hz		2		$nV/\sqrt{Hz}$
		f = 100 Hz		1.4		$nV/\sqrt{Hz}$
		f = 1 kHz		1.1		$nV/\sqrt{Hz}$
Input current noise density	I_n	f = 10 Hz		3.2		$pA/\sqrt{Hz}$
		f = 1 kHz		1.7		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-mode voltage range	V_{CM}	V_S ≥ ±5 V	(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5 V	(V–) + 2		(V+) – 1.4	V
Common-mode rejection ratio	CMRR	V_S ≥ ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V, T_J = –55°C to 125°C	114	120		dB
		V_S < ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V, T_J = –55°C to 125°C	106	120		dB
INPUT IMPEDANCE						
Differential				20k || 8		Ω || pF
Common-mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{OL}	(V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2V, R_L = 10 kΩ, T_J = –55°C to 125°C	114	130		dB
		(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 600 Ω	110	114		dB
Over temperature	A_{OL}	(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6V, I_O ≤ 15 mA, T_J = –55°C to 125°C	100			dB
FREQUENCY RESPONSE						
Gain-bandwidth product	GBW	G = 100		80		MHz
		G = 1		45		MHz
Slew rate	SR			27		V/µs
Settling time, 0.01%	t_S	V_S = ±15 V, G = –1, 10-V step, C_L = 100 pF		400		ns
0.0015% (16-bit)		V_S = ±15 V, G = –1, 10-V step, C_L = 100 pF		700		ns
Overload recovery time		G = –10		500		ns
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$, R_L = 600 Ω		0.000015 %		
				–136		dB

Electrical Characteristics: V_S = ±2.25 to ±18 V (continued)

at T_J = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
Voltage output	V_{OUT}	R_L = 10 kΩ, A_{OL} ≥ 114 dB, T_J = –55°C to 125°C	(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} ≥ 110 dB	(V–) + 0.6		(V+) – 0.6	V
		I_O < 15 mA, A_{OL} ≥ 100 dB, T_J = –55°C to 125°C	(V–) + 0.6		(V+) – 0.6	V
Short-circuit current	I_{SC}			+30/–45		mA
Capacitive load drive	C_{LOAD}			See *Typical Characteristics*		pF
Open-loop output impedance	Z_O	f = 1MHz		5		Ω
POWER SUPPLY						
Specified voltage	V_S		±2.25		±18	V
Quiescent current (per channel)	I_Q	I_{OUT} = 0 A		3.6	4.5	mA
Over temperature		T_J = –55°C to 125°C			6	mA
TEMPERATURE RANGE						
Operating range		T_J	–55		125	°C

6.6 Typical Characteristics

At T_J = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

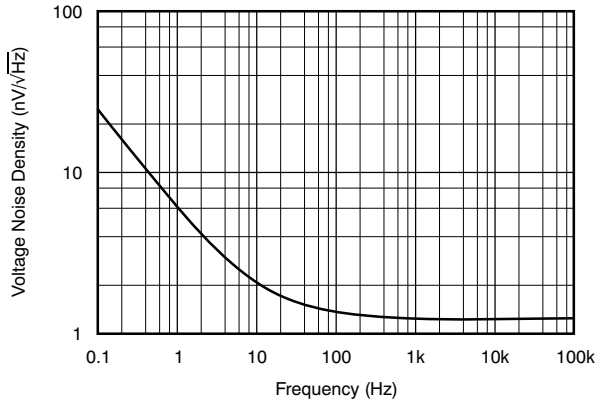


Figure 1. Input Voltage Noise Density vs Frequency

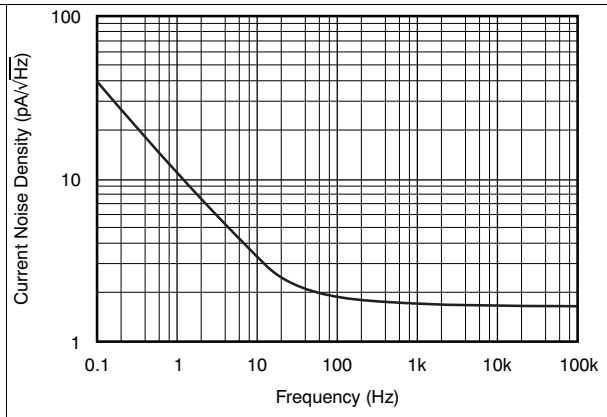


Figure 2. Input Current Noise Density vs Frequency

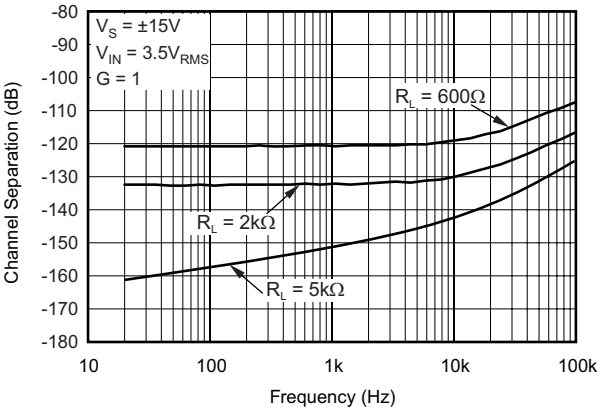


Figure 3. Channel Separation vs Frequency

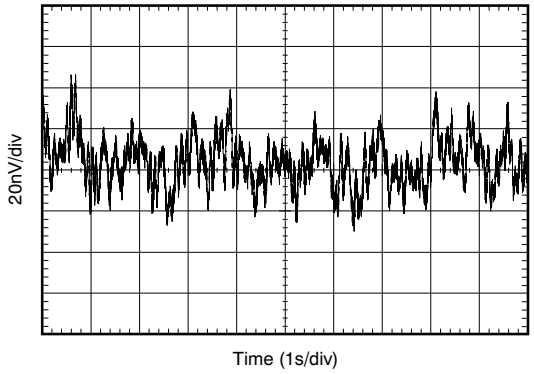


Figure 4. 0.1-Hz to 10-Hz Noise

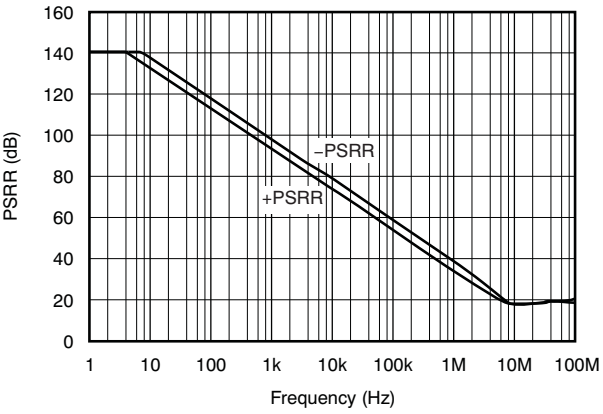


Figure 5. Power-Supply Rejection Ratio vs Frequency (Referred to Input)

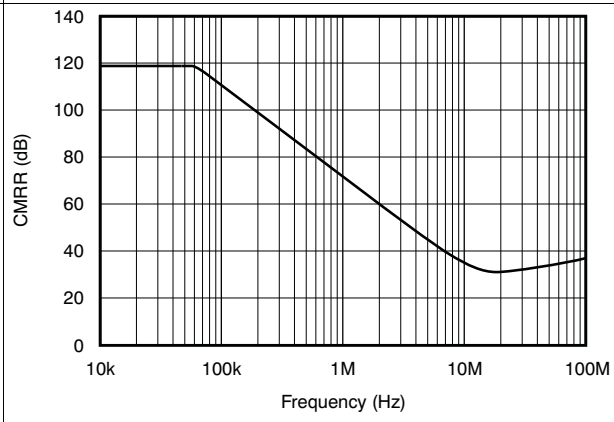


Figure 6. Common-Mode Rejection Ratio vs Frequency

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

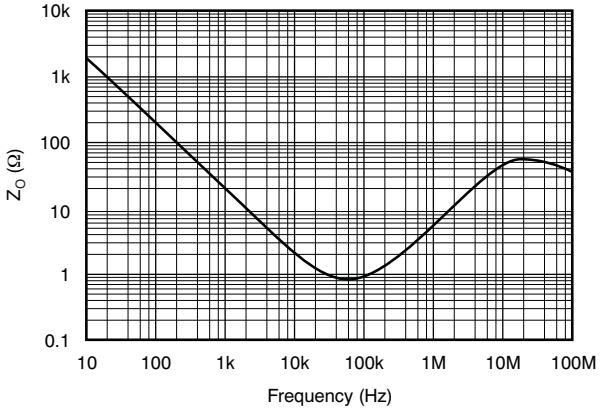


Figure 7. Open-Loop Output Impedance vs Frequency

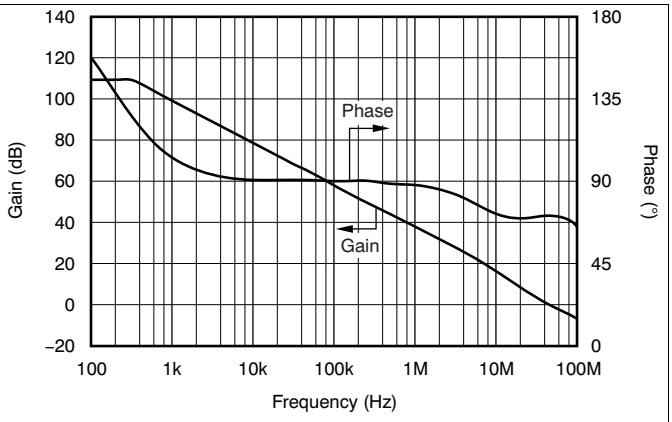


Figure 8. Gain and Phase vs Frequency

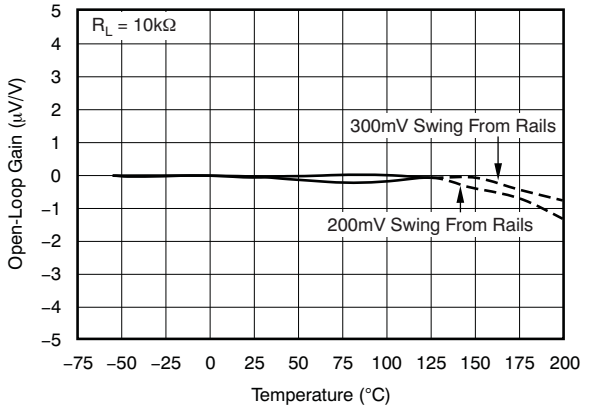


Figure 9. Normalized Open-Loop Gain vs Temperature

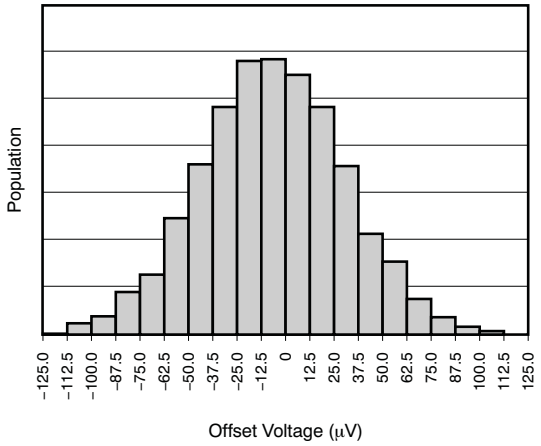


Figure 10. Offset Voltage Production Distribution

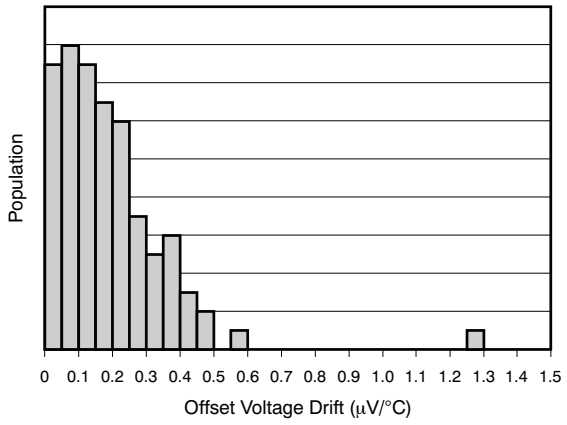


Figure 11. Offset Voltage Drift Production Distribution

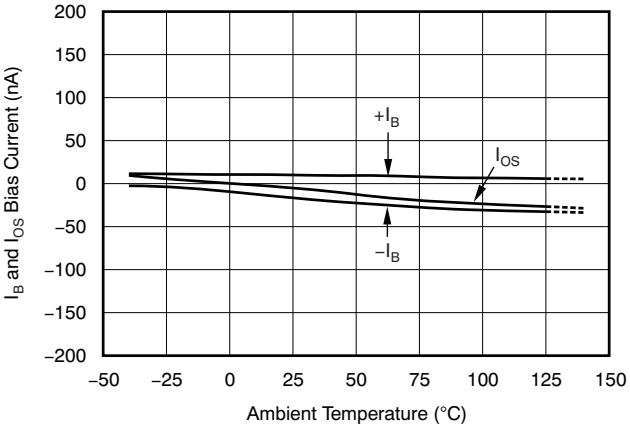


Figure 12. I_B and I_{OS} Current vs Temperature

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

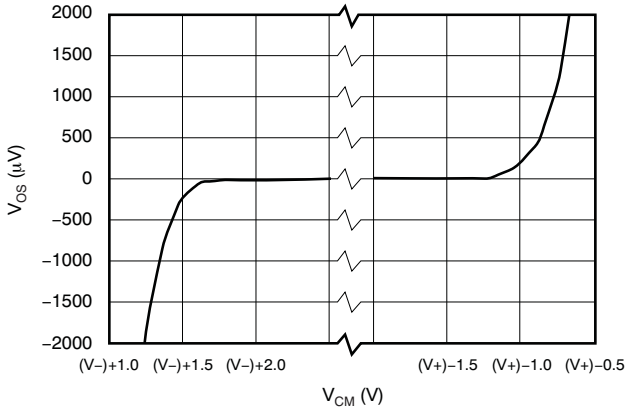


Figure 13. Offset Voltage vs Common-Mode Voltage

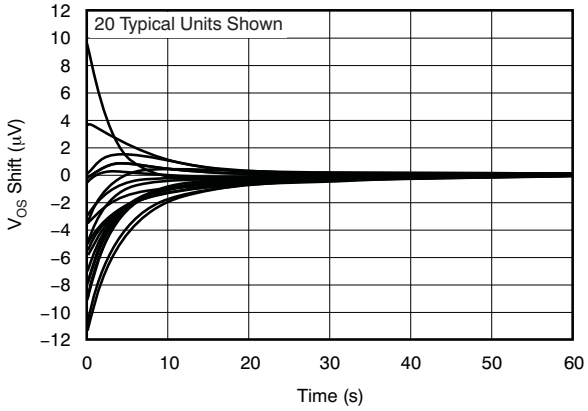


Figure 14. V_{OS} Warmup

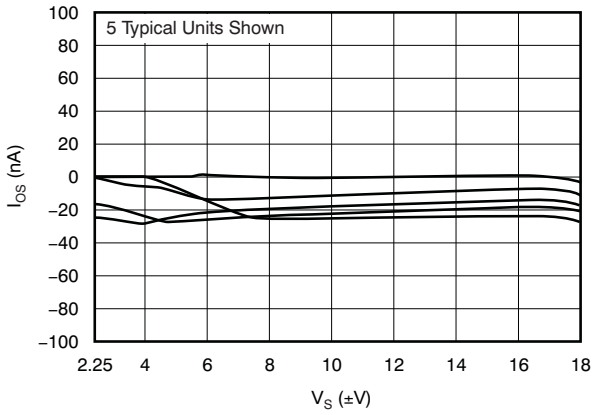


Figure 15. Input Offset Current vs Supply Voltage

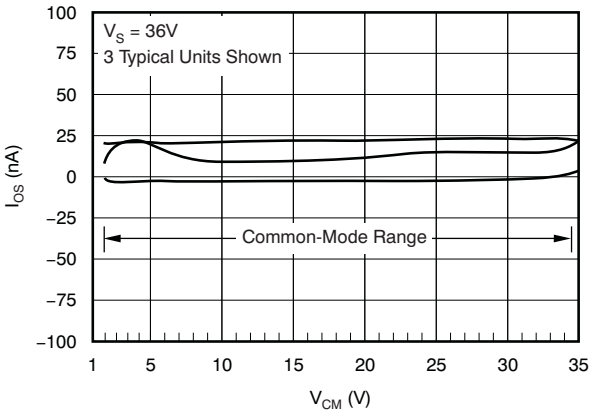


Figure 16. Input Offset Current vs Common-Mode Voltage

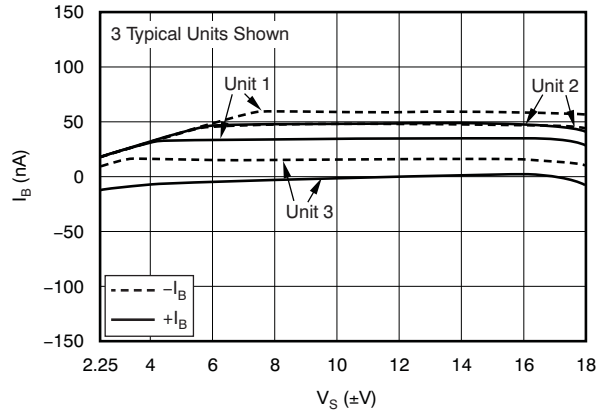


Figure 17. Input Bias Current vs Supply Voltage

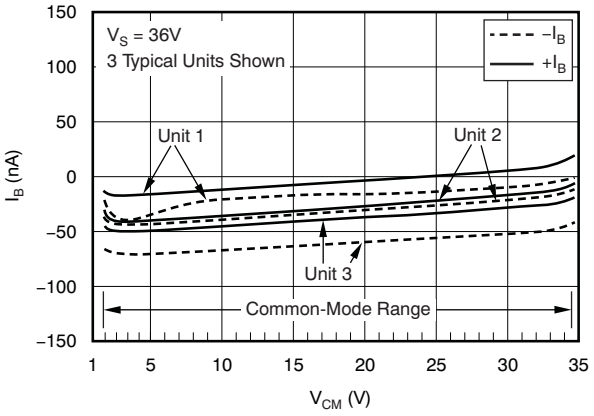


Figure 18. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

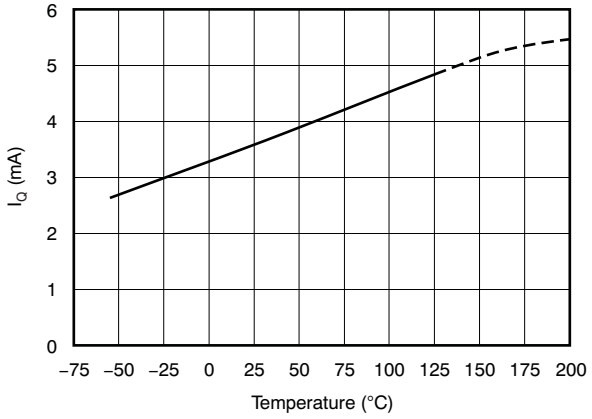


Figure 19. Quiescent Current vs Temperature

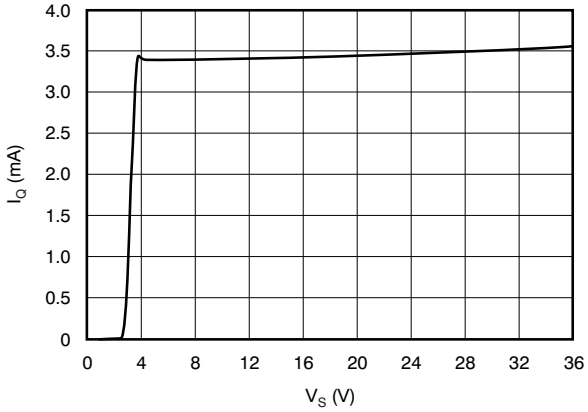


Figure 20. Quiescent Current vs Supply Voltage

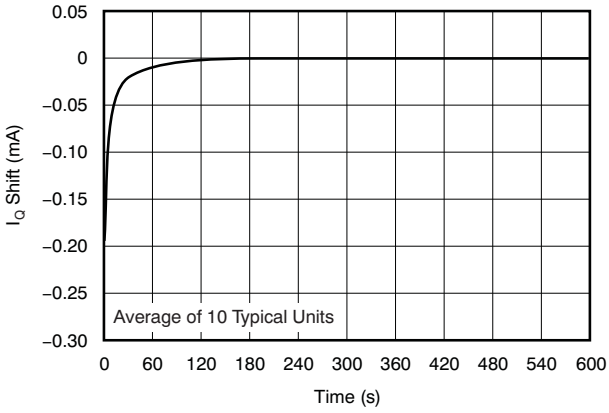


Figure 21. Normalized Quiescent Current vs Time

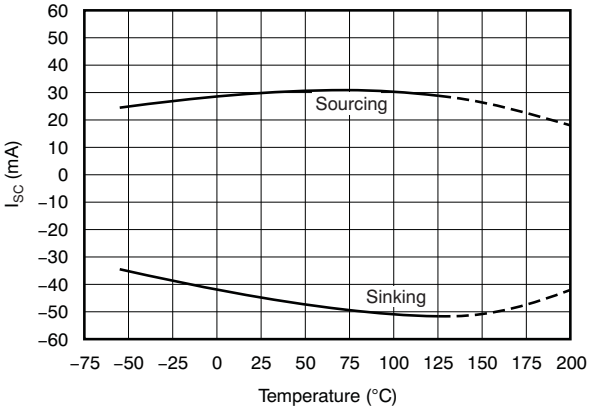


Figure 22. Short-Circuit Current vs Temperature

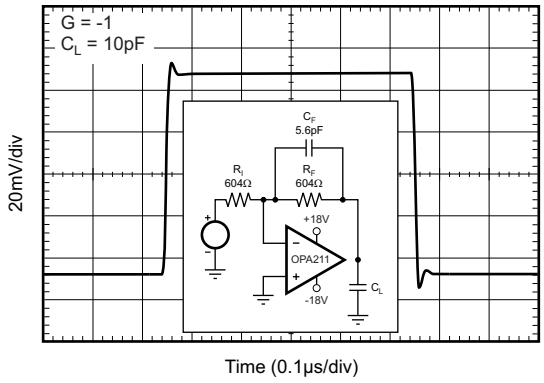


Figure 23. Small-Signal Step Response (100 mV)

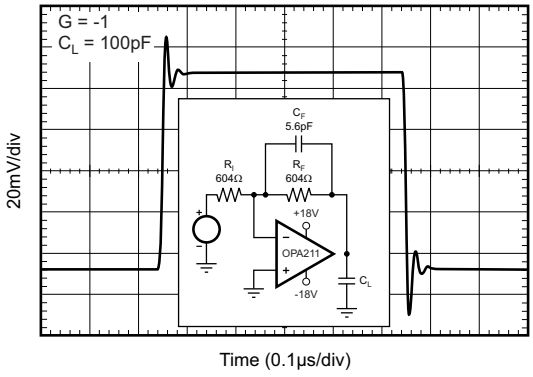


Figure 24. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

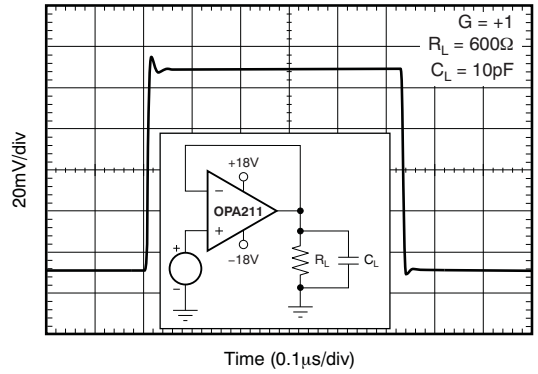


Figure 25. Small-Signal Step Response (100 mV)

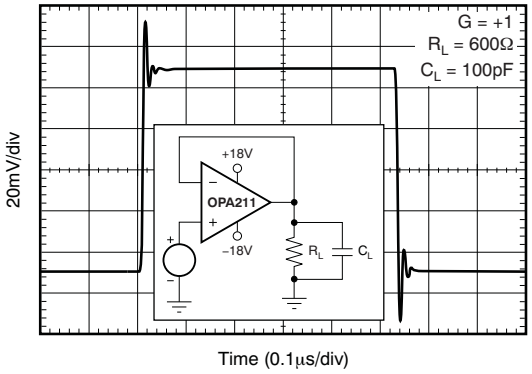


Figure 26. Small-Signal Step Response (100 mV)

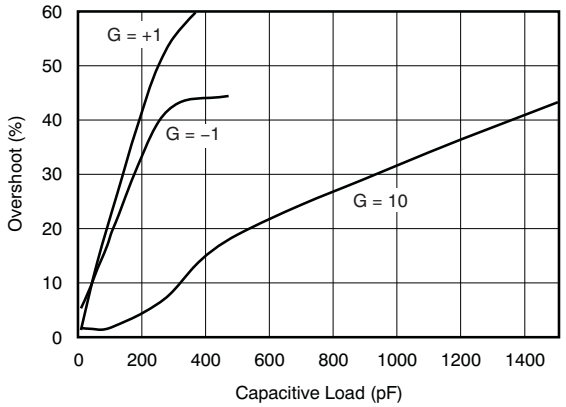


Figure 27. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

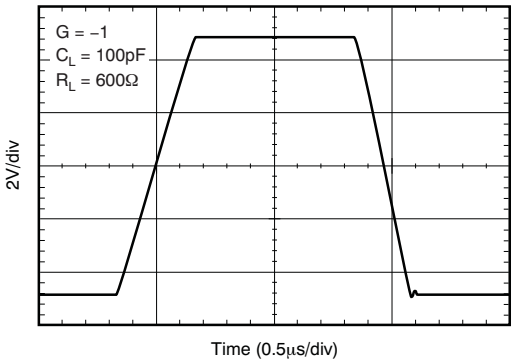


Figure 28. Large-Signal Step Response

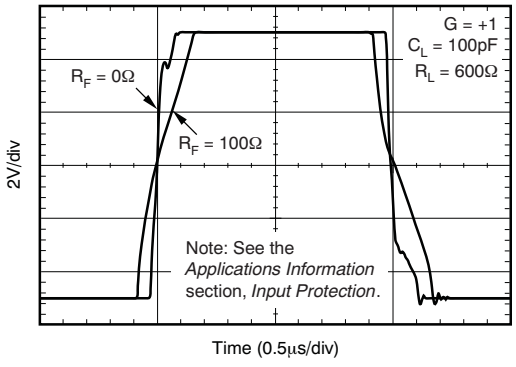


Figure 29. Large-Signal Step Response

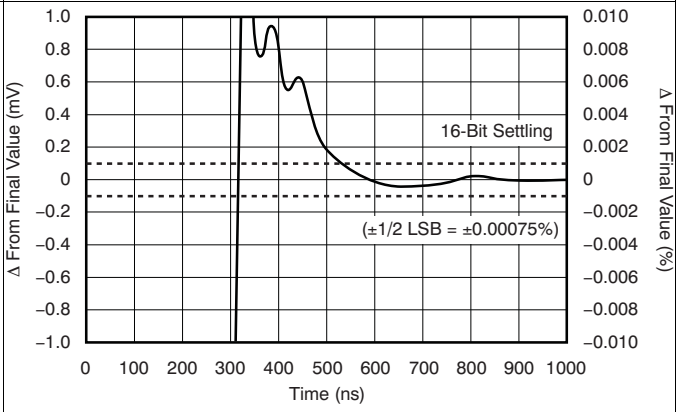


Figure 30. Large-Signal Positive Settling Time ($10\ V_{PP}$, C_L = 100 pF)

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

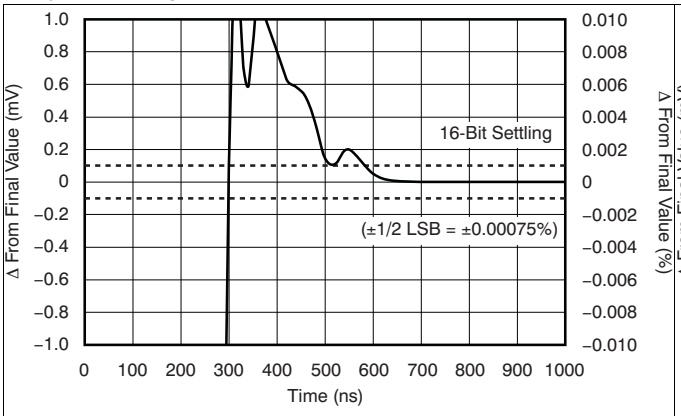


Figure 31. Large-Signal Positive Settling Time (10 V_{PP}, C_L = 10 pF)

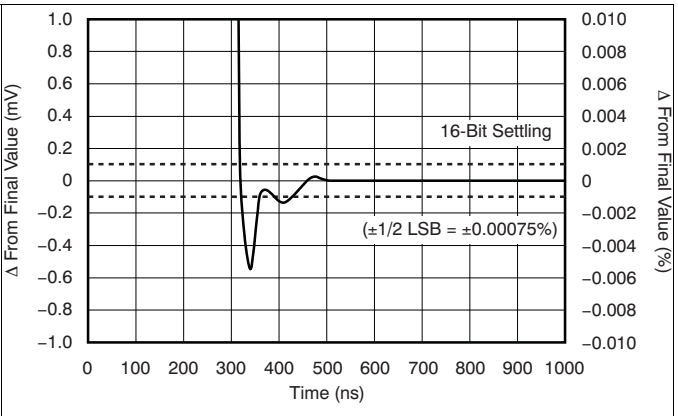


Figure 32. Large-Signal Negative Settling Time (10 V_{PP}, C_L = 100 pF)

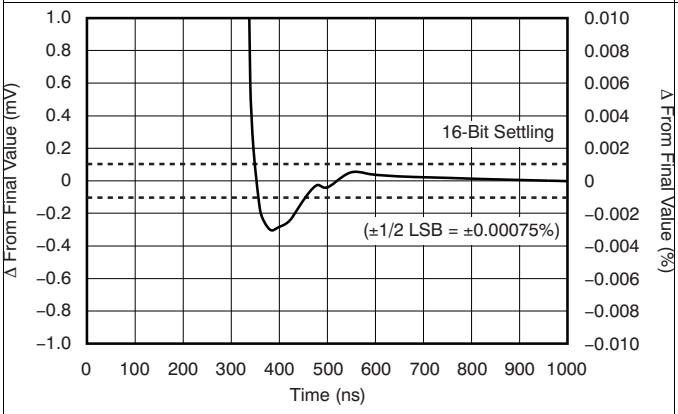


Figure 33. Large-Signal Negative Settling Time (10 V_{PP}, C_L = 10 pF)

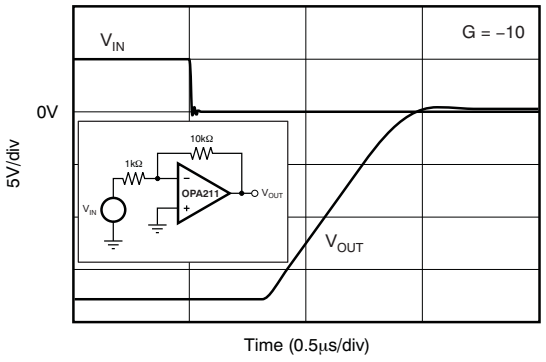


Figure 34. Negative Overload Recovery

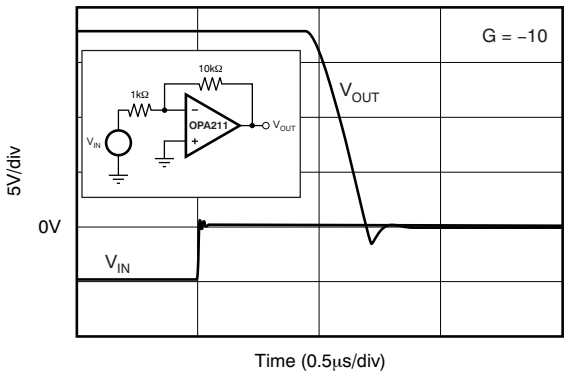


Figure 35. Positive Overload Recovery

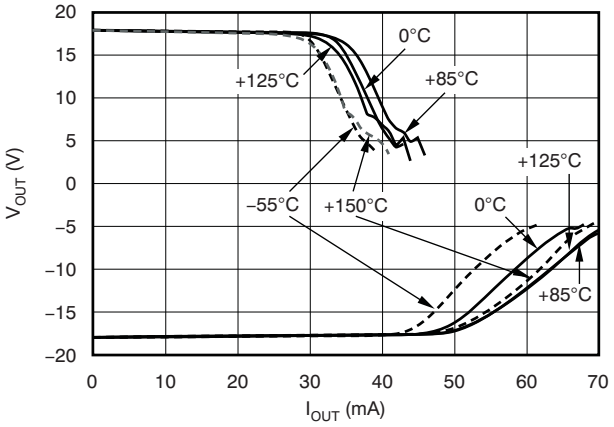


Figure 36. Output Voltage vs Output Current

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

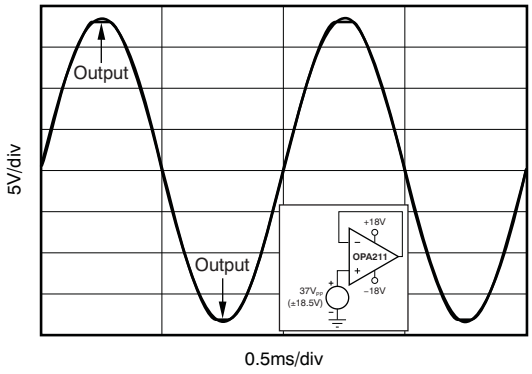


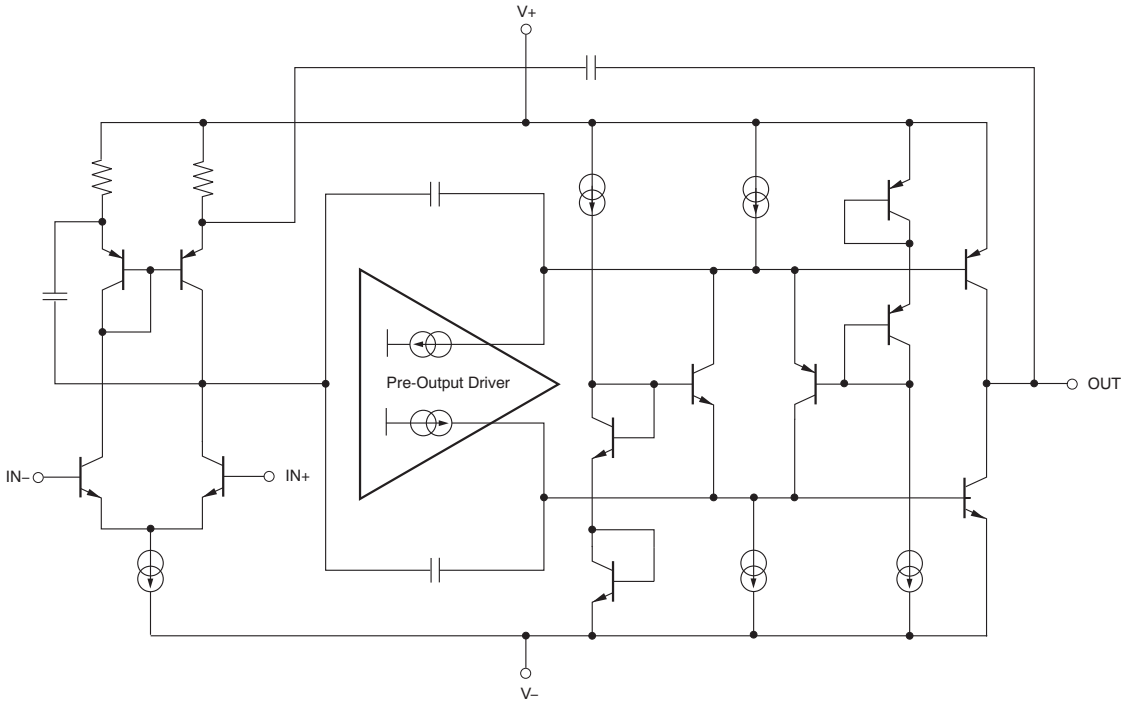
Figure 37. No Phase Reversal

7 Detailed Description

7.1 Overview

The OPA2211-EP is a unity-gain stable, precision operational amplifier with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. *Functional Block Diagram* shows a simplified schematic of the OPA2211-EP. This die uses a SiGe bipolar process and contains 180 transistors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection

The input terminals of the OPA2211-EPFigure 38 are protected from excessive differential voltage with back-to-back diodes, as shown in . In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 29 in the *Typical Characteristics*. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA2211-EP, and is discussed in *Noise Performance*. Figure 38 shows an example implementing a current-limiting feedback resistor.

Feature Description (continued)

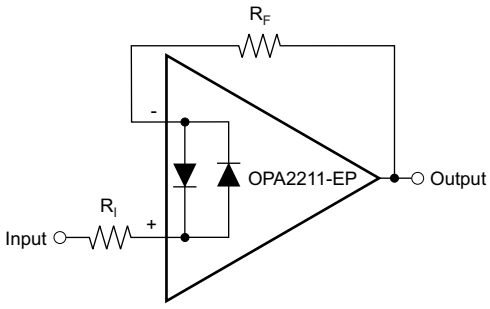


Figure 38. Pulsed Operation

7.3.2 Noise Performance

Figure 39 shows total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPA2211-EP has very low voltage noise, making it ideal for low source impedances (<2 kΩ). A similar precision operational amplifier, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 kΩ to 100 kΩ). Above 100 kΩ, a FET-input operational amplifier such as the OPA132 (very-low current noise) may provide improved performance. The equation in Figure 39 is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, I_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38 × 10^{-23} J/K, and T is temperature in K.

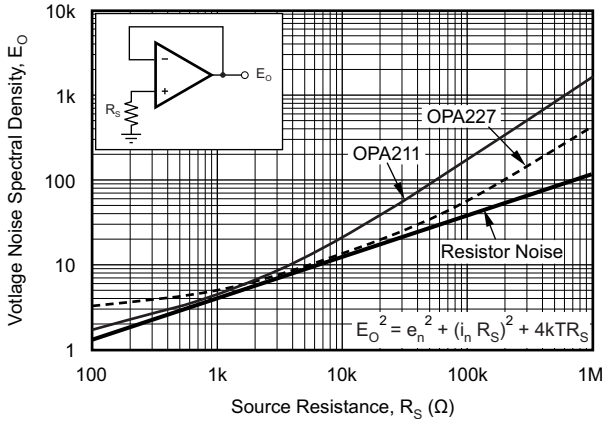


Figure 39. Noise Performance of the OPA2211-EP and OPA227 in Unity-Gain Buffer Configuration

7.3.3 Basic Noise Calculations

Design of low-noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 39. The source impedance is usually fixed; consequently, select the operational amplifier and the feedback resistors to minimize the respective contributions to the total noise.

Feature Description (continued)

Figure 39 depicts total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 41 shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

7.3.4 Total Harmonic Distortion Measurements

OPA2211-EP series operational amplifiers have excellent distortion characteristics. THD + Noise is below 0.0002% (G = +1, V_{OUT} = 3 V_{RMS}) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600-Ω load.

The distortion produced by OPA2211-EP series operational amplifiers is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in Figure 42 can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. Figure 42 shows a circuit that causes the operational amplifier distortion to be 101 times greater than that normally produced by the operational amplifier. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the operational amplifier are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

7.4 Device Functional Modes

The OPAx211 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx211 is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

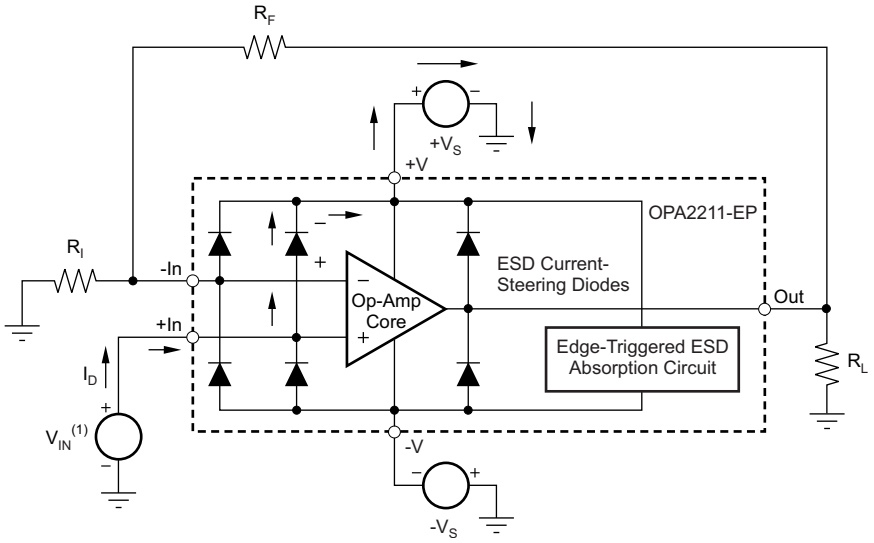
It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 40 illustrates the ESD circuits contained in the OPA2211-EP (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2211-EP but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 40, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Application Information (continued)



(1) $V_{IN} = +V_S + 500$ mV

Figure 40. Equivalent Internal ESD Circuitry and its Relation to a Typical Circuit Application

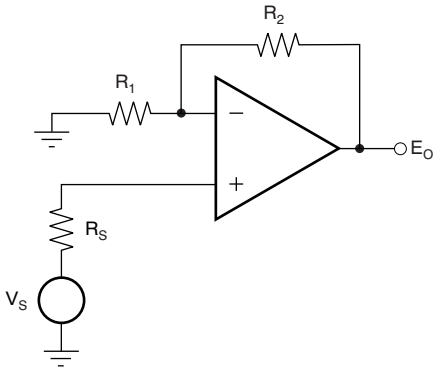
Figure 40 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

8.2 Typical Application

Noise in Noninverting Gain Configuration



Noise at the output:

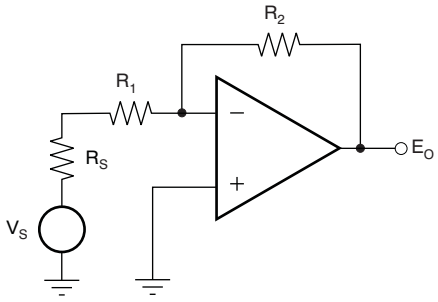
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

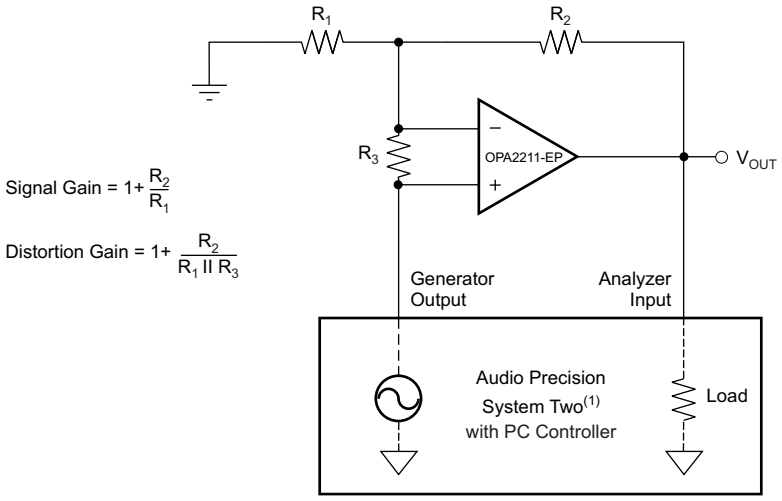
Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA211 series op amps at 1kHz, $e_n = 1.1nV/\sqrt{Hz}$ and $i_n = 1.7pA/\sqrt{Hz}$.

Figure 41. Noise Calculation in Gain Configurations



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω

(1) For measurement bandwidth, see Figure 43, Figure 44, and Figure 45.

Figure 42. Distortion Test Circuit

Typical Application (continued)

8.2.1 Design Requirements

The design requirements for Signal Gain = 11 are:

$$\text{Signal Gain} = 1 + \frac{R_2}{R_1}$$

where

- Supply voltage: 30 V (±15 V)
- R_1 = 100 Ω
- R_2 = 1 kΩ
- R_3 = 11 Ω (1)

8.2.2 Detailed Design Procedure

8.2.2.1 Total Harmonic Distortion Measurements

OPA2211-EP series operational amplifiers have excellent distortion characteristics. THD + Noise is below 0.0002% (G = +1, VOUT = 3VRMS) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600-Ω load. The distortion produced by OPA2211-EP series operational amplifiers is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in Figure 47 can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. Figure 47 shows a circuit that causes the operational amplifier distortion to be 101 times greater than that normally produced by the operational amplifier. The addition of R3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the operational amplifier are the same as with conventional feedback without R3. The value of R3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

8.2.3 Application Curves

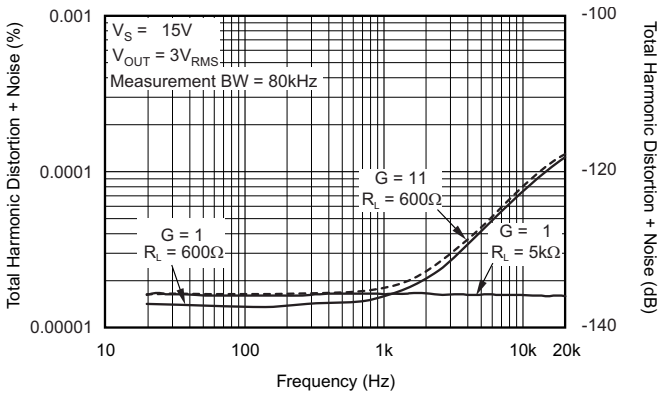


Figure 43. THD+N Ratio vs Frequency

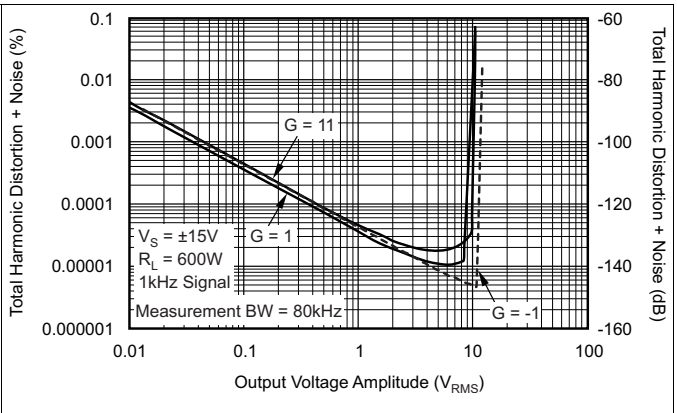


Figure 44. THD+N Ratio vs Output Voltage Amplitude

Typical Application (continued)

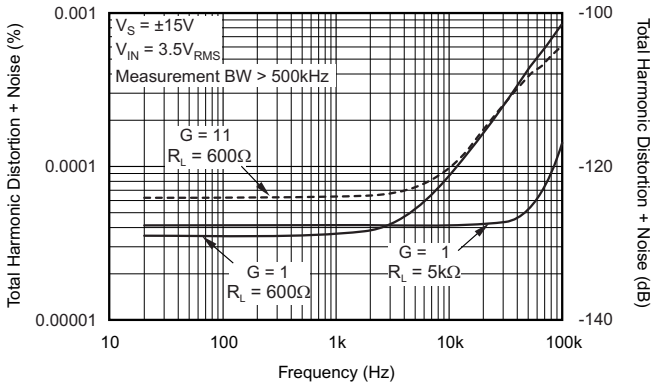


Figure 45. THD+N Ratio vs Frequency

9 Power Supply Recommendations

9.1 Operating Voltage

OPA2211-EP series operational amplifiers operate from ±2.25-V to ±18-V supplies while maintaining excellent performance. The OPA2211-EP series can operate with as little as +4.5 V between the supplies and with up to +36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA2211-EP series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25 V with the negative supply at –5 V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, T_A = –55°C to 125°C. Parameters that vary significantly with operating voltage or temperature are shown in *Typical Characteristics*.

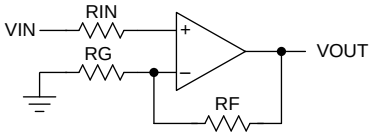
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 46, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example



(Schematic Representation)

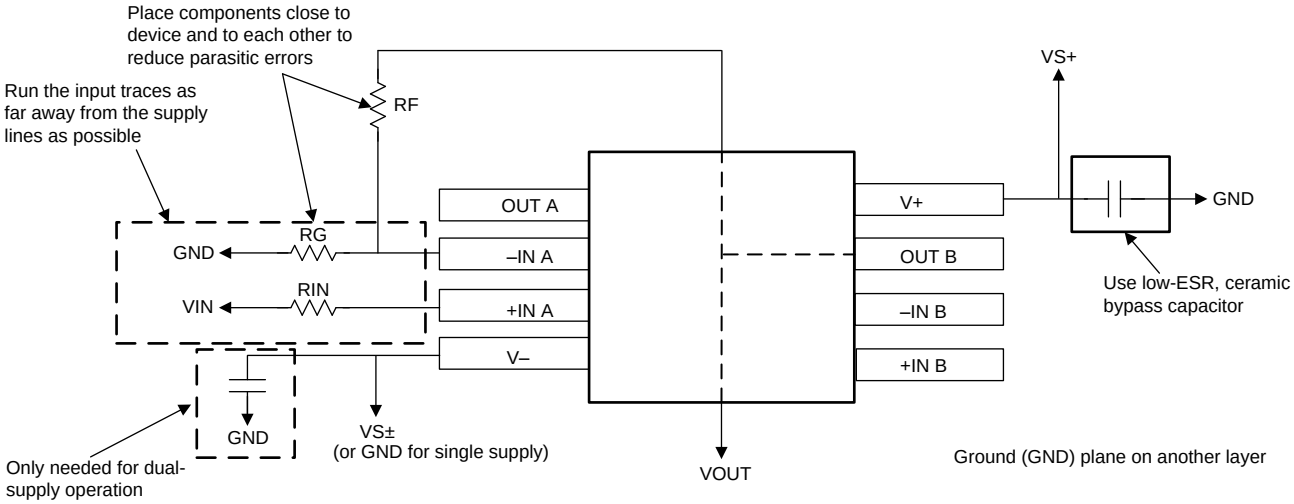


Figure 46. Operational Amplifier Board Layout for Noninverting Configuration

10.3 Thermal Considerations

The primary issue with all semiconductor devices is junction temperature (T_J). The most obvious consideration is assuring that T_J never exceeds the absolute maximum rating specified for the device. However, addressing device thermal dissipation has benefits beyond protecting the device from damage. Even modest increases in junction temperature can decrease operational amplifier performance, and temperature-related errors can accumulate. Understanding the power generated by the device within the specific application and assessing the thermal effects on the error tolerance lead to a better understanding of system performance and thermal dissipation needs.

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2211MDRGTEP	ACTIVE	SON	DRG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OCQM	Samples
V62/15606-01XE	ACTIVE	SON	DRG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OCQM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

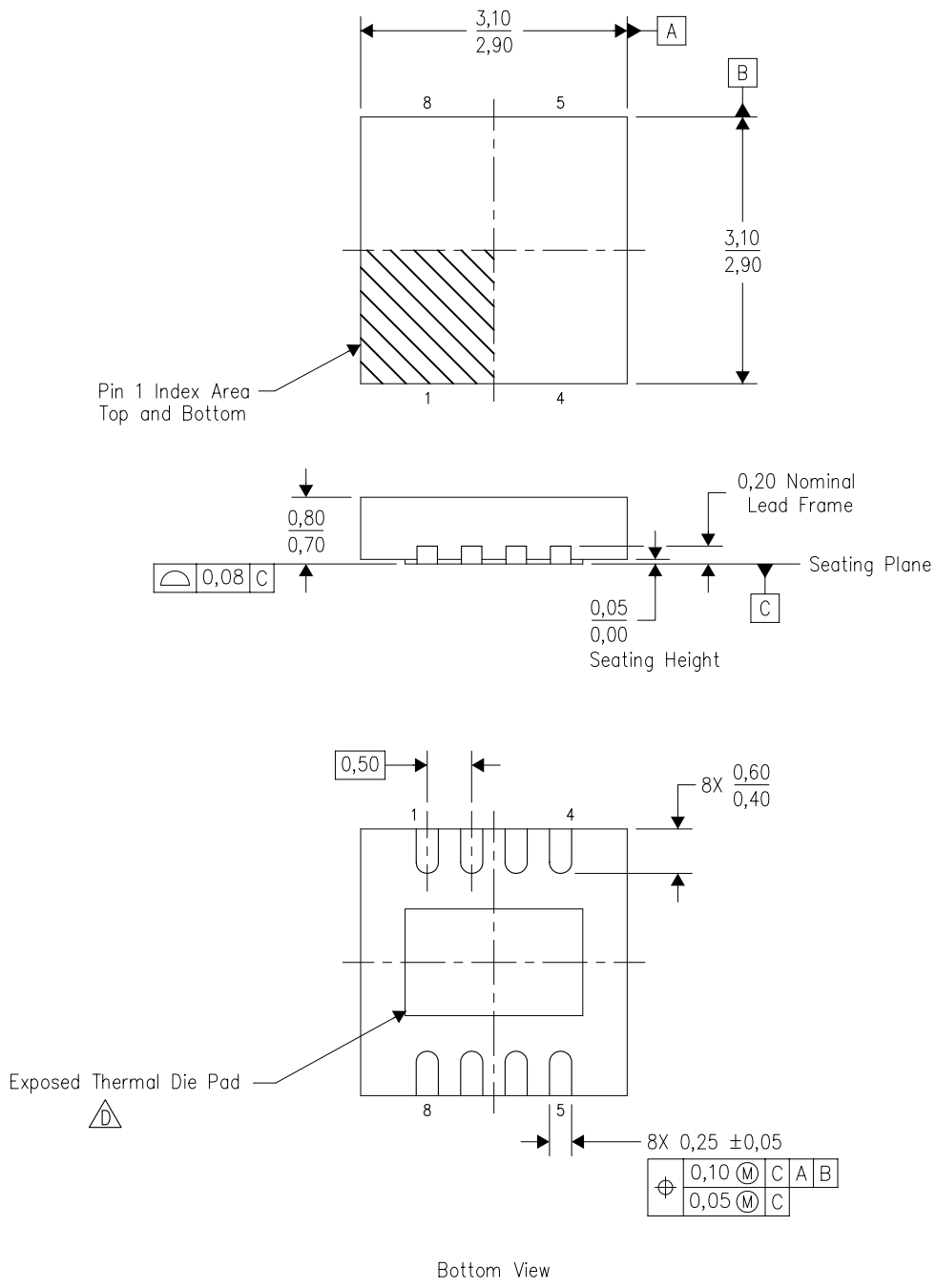
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



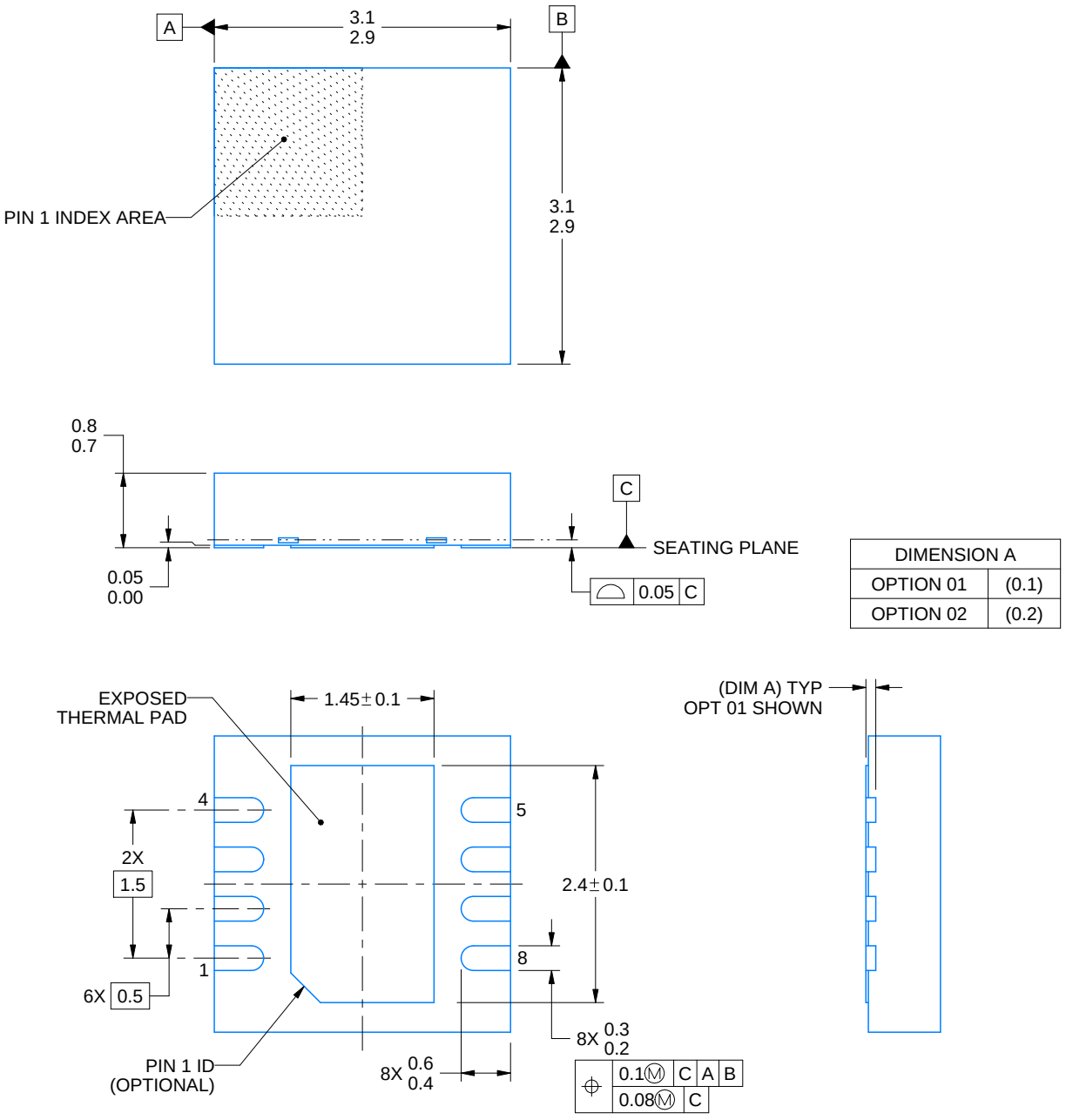
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

DRG0008B

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

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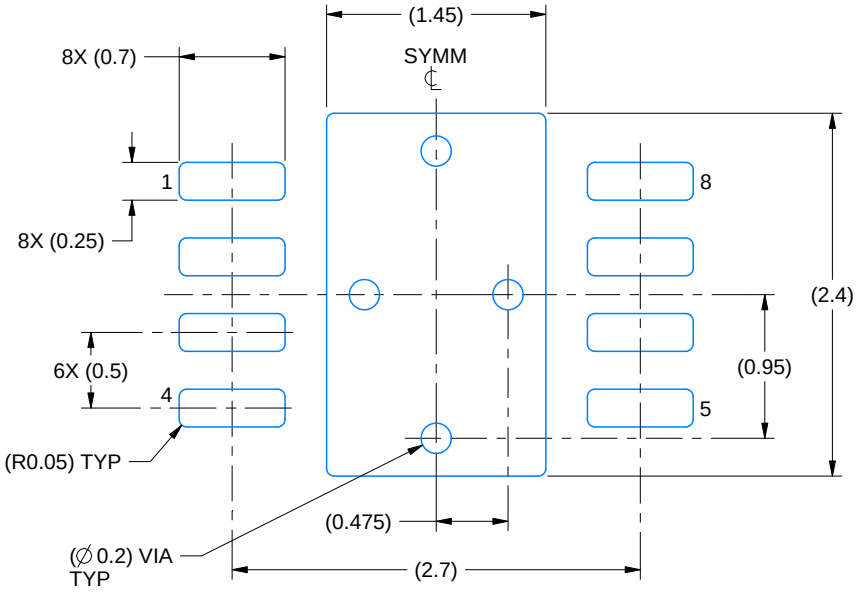
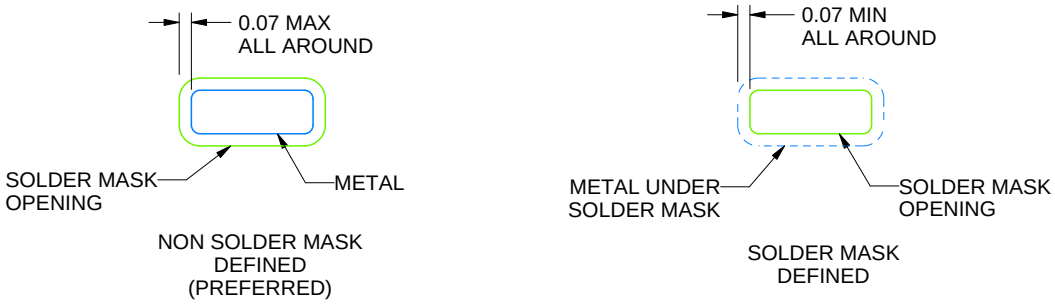
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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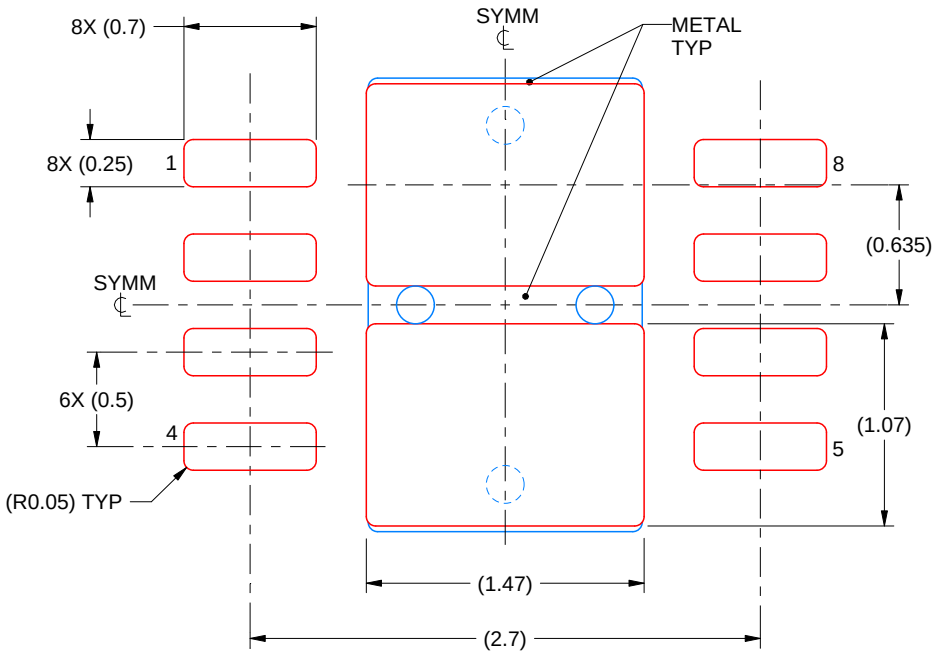
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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