SNx5ALS180 差分驱动器和接收器对

1 特性

- 符合或超出 TIA/EIA-422-B、TIA/EIA-485-A 的要求 [1] 和 ITU 建议 V.11
- 高速高级低功耗肖特基电路
- 专为串行和并行应用中的 25Mbaud 运行而设计
- 低器件间延迟：6ns（最大值）
- 低电源电流要求：30 mA（最大值）
- 具有双 V_{CC} 和双 GND 的独立驱动器和接收器 I/O 引脚
- 宽正负输入/输出总线电压范围
- 驱动器输出容量：±60mA
- 热关断保护
- 驱动器正负电流限制
- 接收器输入阻抗：12kΩ 最小值
- 接收器输入灵敏度：±200mV（最大值）
- 接收器输入迟滞：60 mV（典型值）
- 由一个 5V 单电源供电运行
- 无干扰上电和断电保护

2 说明

SN65ALS180 和 SN75ALS180 差分驱动器和接收器对是专为多点总线传输线路上的双向数据通信而设计的集成电路。这些器件专为平衡传输线路而设计，符合 TIA/EIA-422-B、TIA/EIA-485-A 和 ITU 建议 V.11。

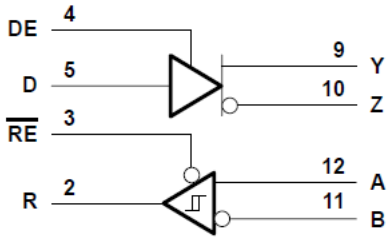
SN65ALS180 和 SN75ALS180 整合了一个三态差分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端连接到单独的终端以实现更大的灵活性，这些端口用于在禁用驱动器或 V_{CC} = 0 时为总线提供最小负载。

这些端口具有正负宽共模电压范围，使得该器件非常适用于合用线应用。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
SNx5ALS176	D (SOIC)	8.65mm x 3.91mm
	N (PDIP)	19.3mm x 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

[1] 这些器件符合或超出 TIA/EIA-485-A 的要求，但发生器争用测试（第 3.4.2 段）和发生器电流限制（第 3.4.3 段）除外。对于 SN75ALS180，所施加的测试电压范围为 –6V 至 8V；对于 SN65ALS180，所施加的测试电压范围为 –4V 至 8V。

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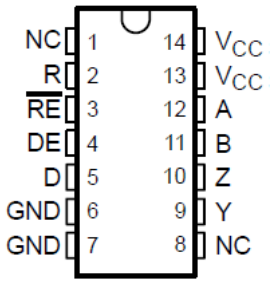
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (April 2003) to Revision H (January 2023)	Page
• 将文档更改为了最新 TI 格式	1
• Deleted the Package thermal impedance from the *Absolute Maximum Ratings*	4
• Added the *Thermal Information* table	4
• Changed the *Typical Characteristics* graphs	8

4 Pin Configuration and Functions



NC – No internal connection

图 4-1. SN65ALS180 D Package
SN75ALS180 D or N Package
(Top View)

表 4-1. Pin Functions

NO	Name	Type	Description
1	NC	-	No Internal connection
2	R	O	Receive data output
3	$\overline{RE}$	I	Receiver enable, active low
4	DE	I	Driver enable, active high
5	D	I	Driver data input
6, 7	GND	GND	Device ground
8	NC	-	No Internal connection
9	Y	O	Digital bus output, Y (Complementary to Z)
10	Z	O	Digital bus output, Z (Complementary to Y)
11	A	I	Bus input, A (complementary to B)
12	B	I	Bus input, B (complementary to A)
13, 14	V_{CC}	SUPPLY	4.75V to 5.25V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	-10	15	V
V_I	Enable input voltage		5.5	V
T_J	Operating virtual junction temperature		150	℃
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	℃
T_{stg}	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)				12	V
					–7	
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	μA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature	SN65ALS180	–40		85	°C
		SN75ALS180	0		70	

(1) Differential-input/output bus voltage is measured at the noninverting terminal, A/Y, with respect to the inverting terminal, B/Z.

5.3 Thermal Information

THERMAL METRIC(1)		N (PDIP)	D (SOIC) (SN65 Devices)	D (SOIC) (SN75 Devices)	UNIT
		14-Pins	14-Pins	14-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	93.2	83.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	40	47.5	39.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	49.4	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	11.2	7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	48.9	39.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See 图 6-1	1/2V_{OD1} or 2(3)			V
		R_L = 54 Ω	See 图 6-1	1.5	2.5	5	
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See 图 6-2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(4)	R_L = 54 Ω or 100 Ω	See 图 6-1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω	See 图 6-1			3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(4)	R_L = 54 Ω or 100 Ω	See 图 6-1			±0.2	V
I_O	Output current	Output disabled(6)	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	μA
I_{OS}	Short-circuit output current(5)	V_O = –6 V	SN75ALS180			–250	mA
		V_O = –4 V	SN65ALS180			–250	
		V_O = 0	All			–150	
		V_O = V_{CC}	All			250	
		V_O = 8 V	All			250	
I_{CC}	Supply current	No load	Driver outputs enabled, Receiver disabled		25	30	mA
			Outputs disabled		19	26	

(1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3	3	8	13	ns
	Pulse skew ($\|t_{d(ODH)} - t_{d(ODL)}\|$)	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		1	6	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3	3	8	13	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω	See 图 6-4			23	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω	See 图 6-5			19	24	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω	See 图 6-4			8	13	ns

5.5 Switching Characteristics - Driver (continued)

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
t_{PLZ}	Output disable time from low level	R_L = 110 Ω	See 图 6-5			8	13	ns

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.6 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, Vo_b
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t(R_L = 100 Ω)	V_t(R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|V_t\|\|$	$\|\|V_t\| - \|V_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

5.7 Electrical Characteristics - Receivers

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})					60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –400 μA,	See 图 6-6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA,	See 图 6-6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input = 0 V(3)	V_I = 12 V				1	mA
			V_I = –7 V				–0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	mA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					–100	mA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0		–15		–85	mA
I_{CC}	Supply current	No load	Receiver outputs enabled, Driver inputs disabled			19	30	mA
			Outputs disabled			19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.8 Switching Characteristics - Receivers

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,	9	14	19	ns
	Skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,		2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See 图 6-8		7	14	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See 图 6-8		7	14	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See 图 6-8		20	35	ns
t_{PLZ}	Output disable time from low level	C_L= 15 pF,	See 图 6-8		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.9 Typical Characteristics

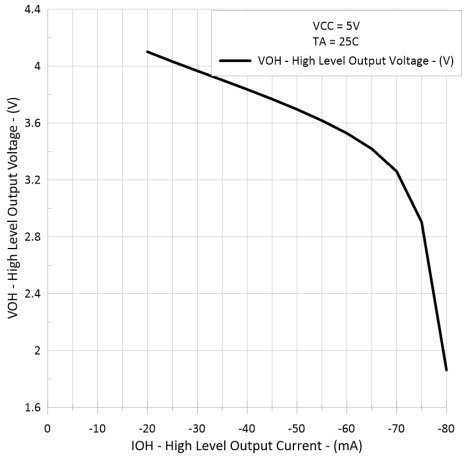


图 5-1. Drivers High-Level Output Voltage vs High-Level Output Voltage

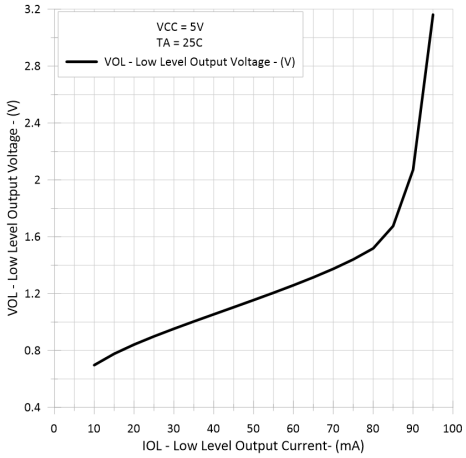


图 5-2. Drivers Low-Level Output Voltage vs Low-Level Output Current

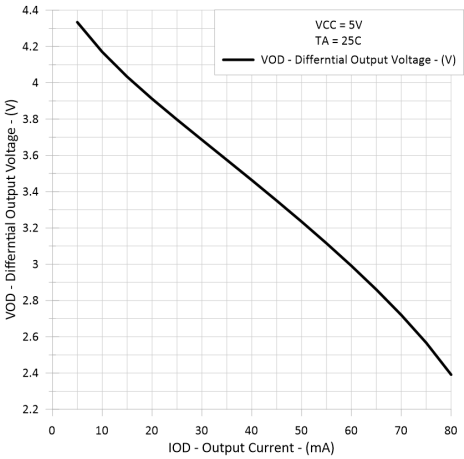


图 5-3. Drivers Differential Output Voltage vs Output Current

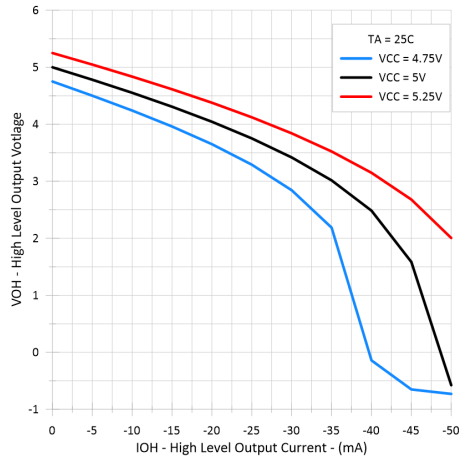


图 5-4. Receivers High-Level Output Voltage vs High-Level Output Current

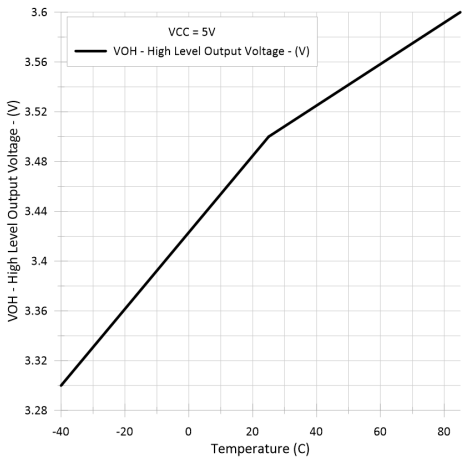


图 5-5. Receivers High-Level Output Voltage vs Free-Air Temperature

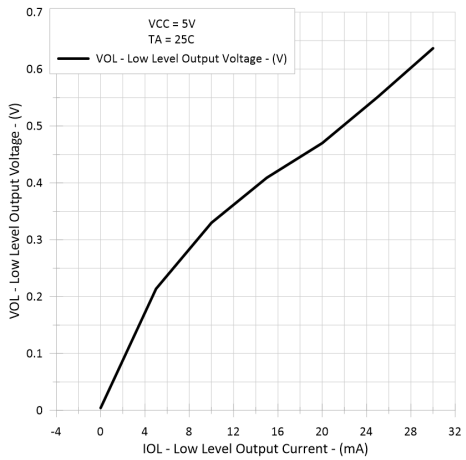


图 5-6. Receivers Low-Level Output Voltage vs Low-Level Output Current

5.9 Typical Characteristics (continued)

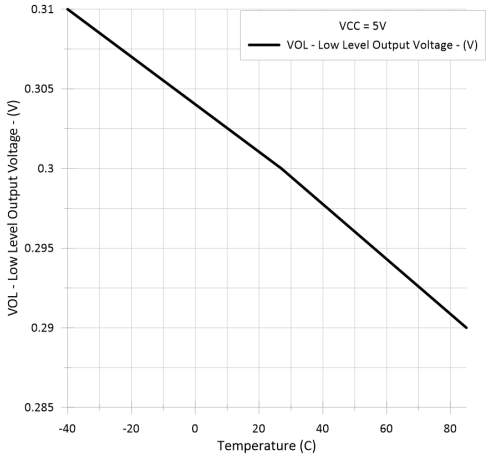


图 5-7. Receivers Low-Level Output Voltage vs Free-Air Temperature

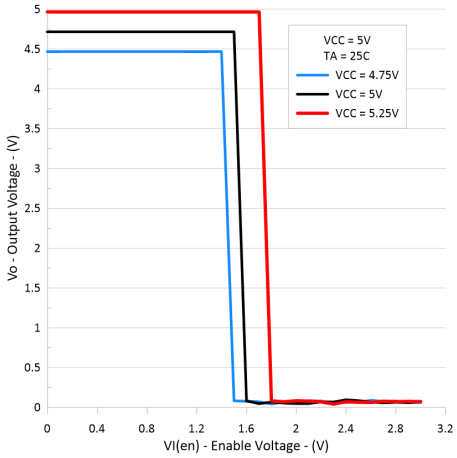


图 5-8. Receivers Output Voltage vs Enable Voltage

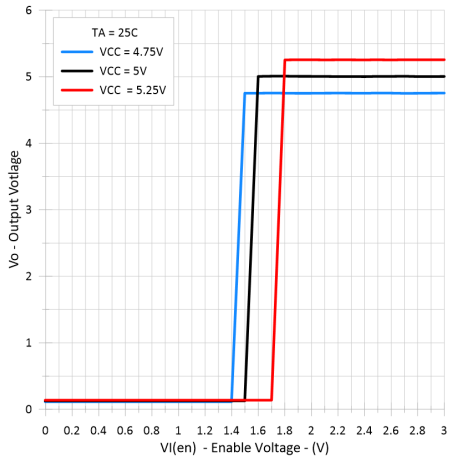


图 5-9. Receivers Output Voltage vs Enable Voltage

6 Parameter Measurement Information

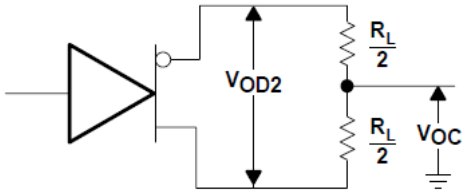


图 6-1. Driver V_{OD} and V_{OC}

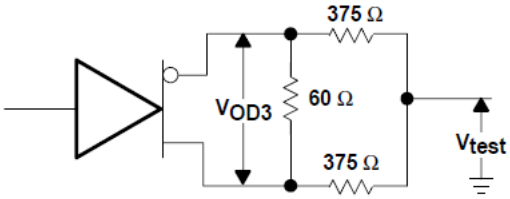
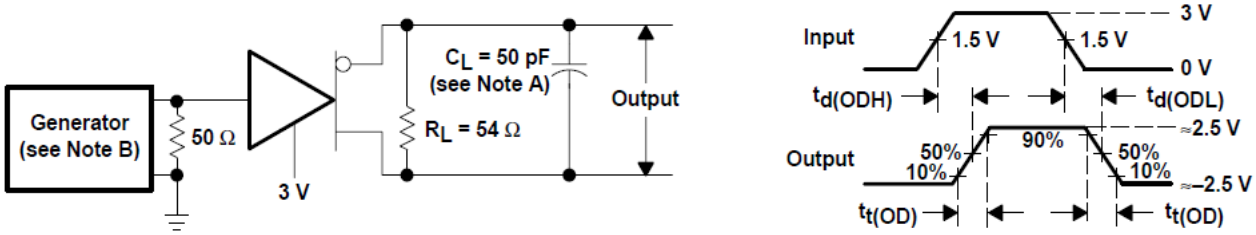


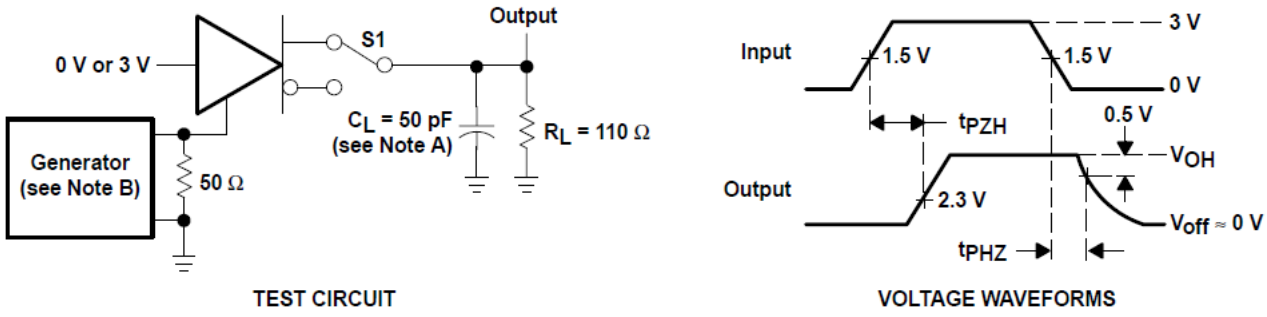
图 6-2. Driver V_{OD3}



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6ns, Z_O = 50 Ω.

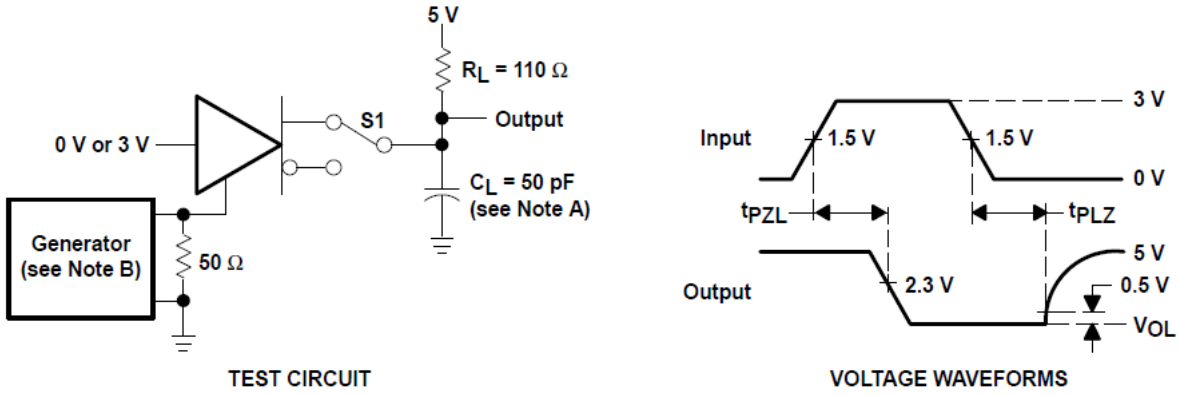
图 6-3. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6ns, Z_O = 50 Ω.

图 6-4. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6ns, Z_O = 50 Ω.

图 6-5. Driver Test Circuit and Voltage Waveforms

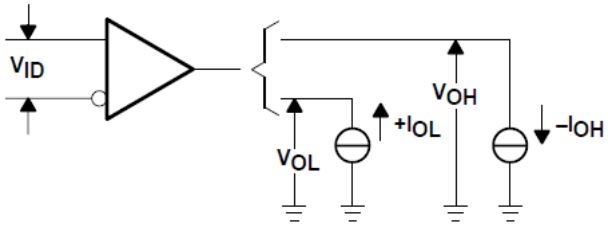
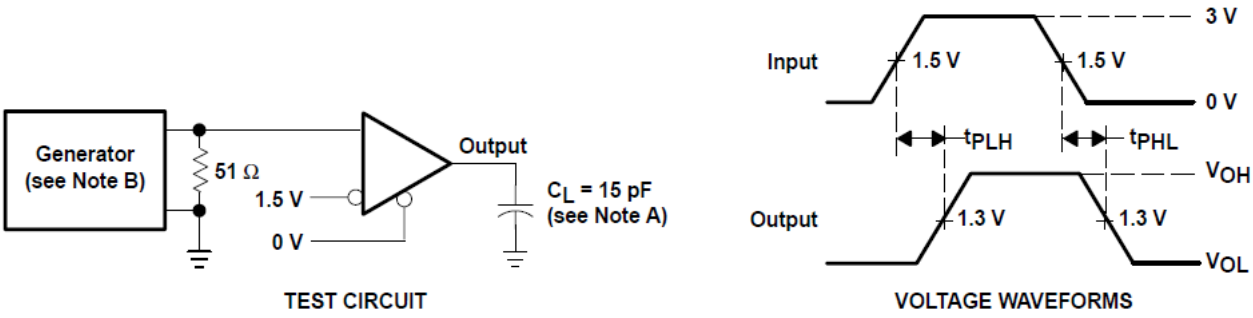


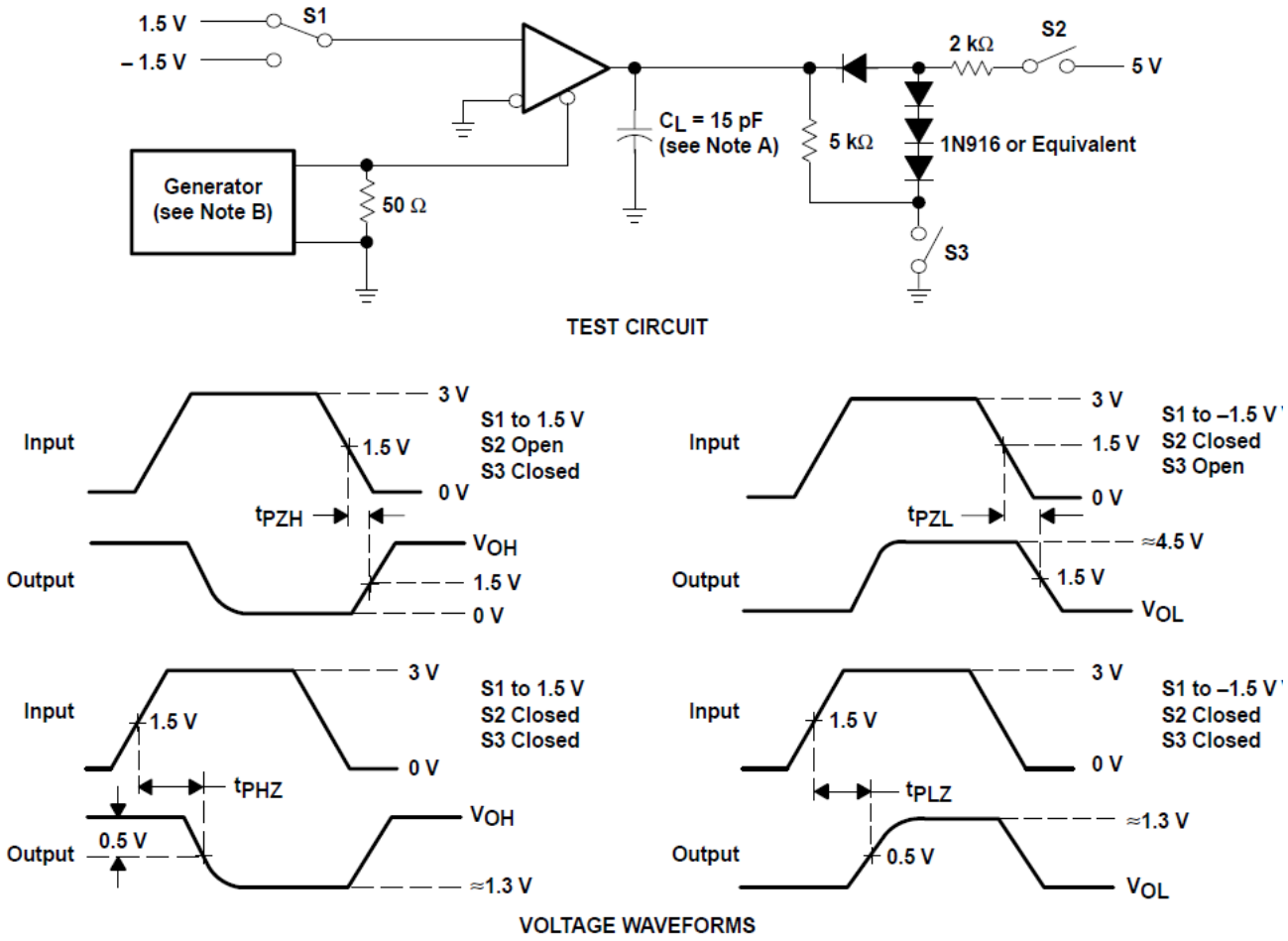
图 6-6. Receiver V_{OH} and V_{OL}



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6ns, Z_O = 50 Ω.

图 6-7. Receiver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6ns, Z_O = 50 Ω.

图 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

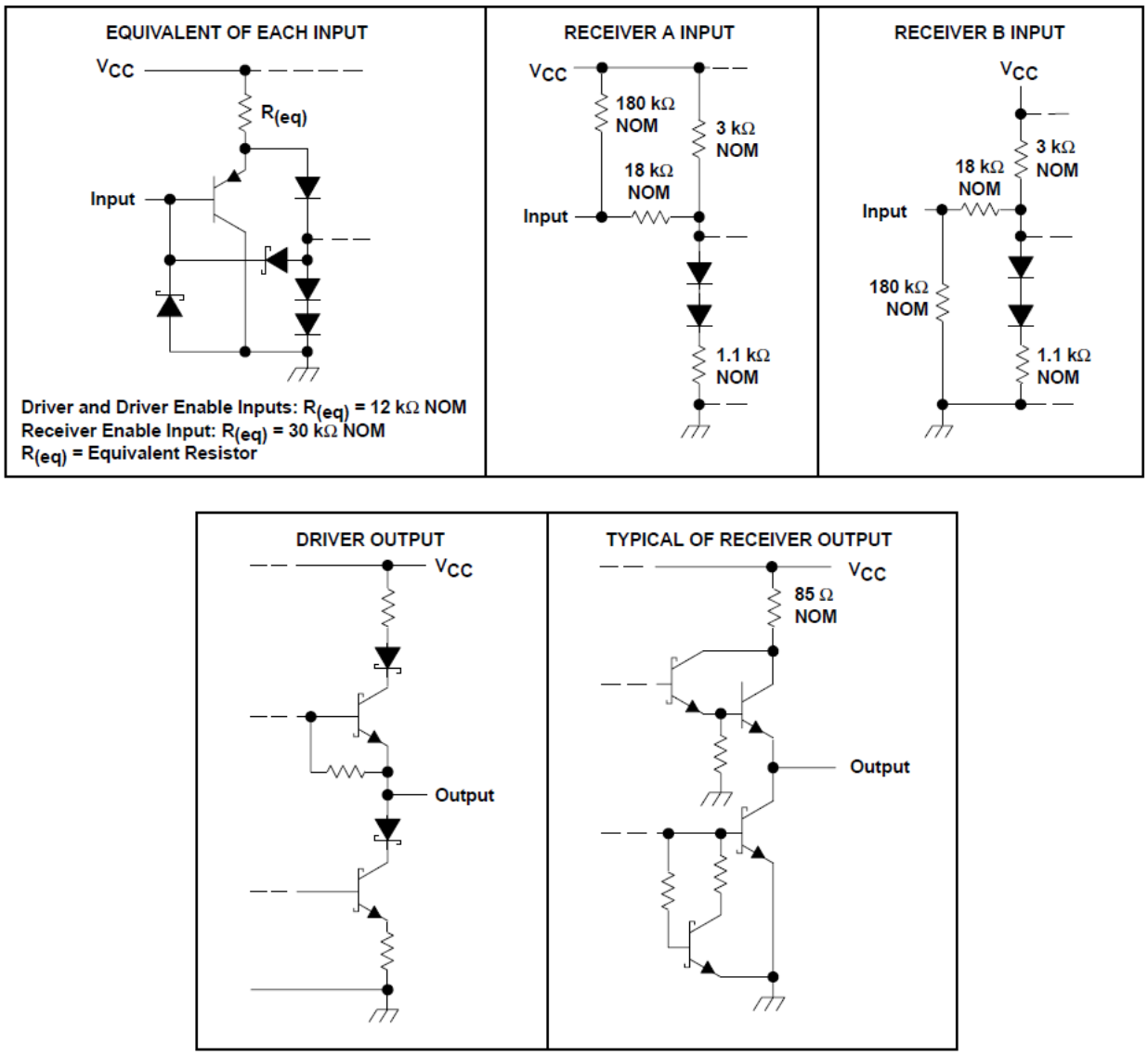


图 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

表 7-2. Receiver(1)

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

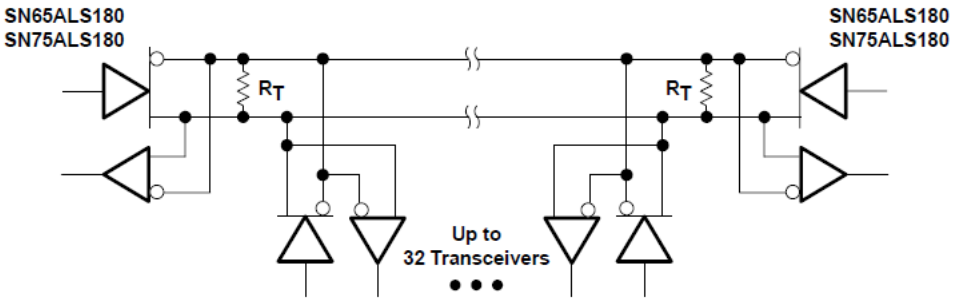
8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application



A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS180DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN65ALS180DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN75ALS180N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS180N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

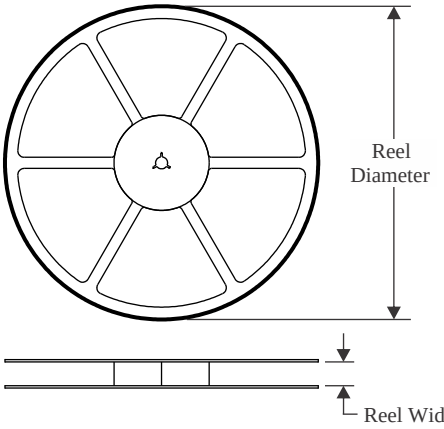
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

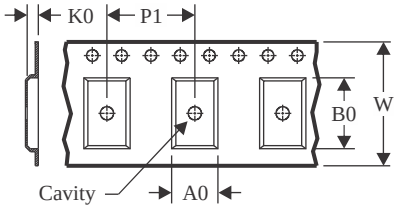
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

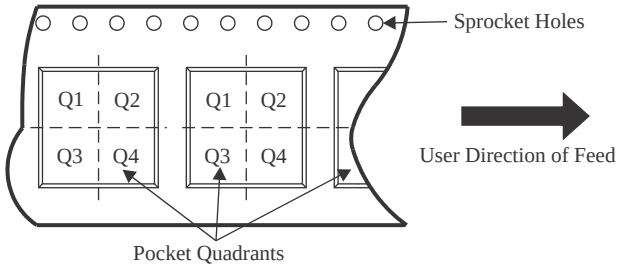


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

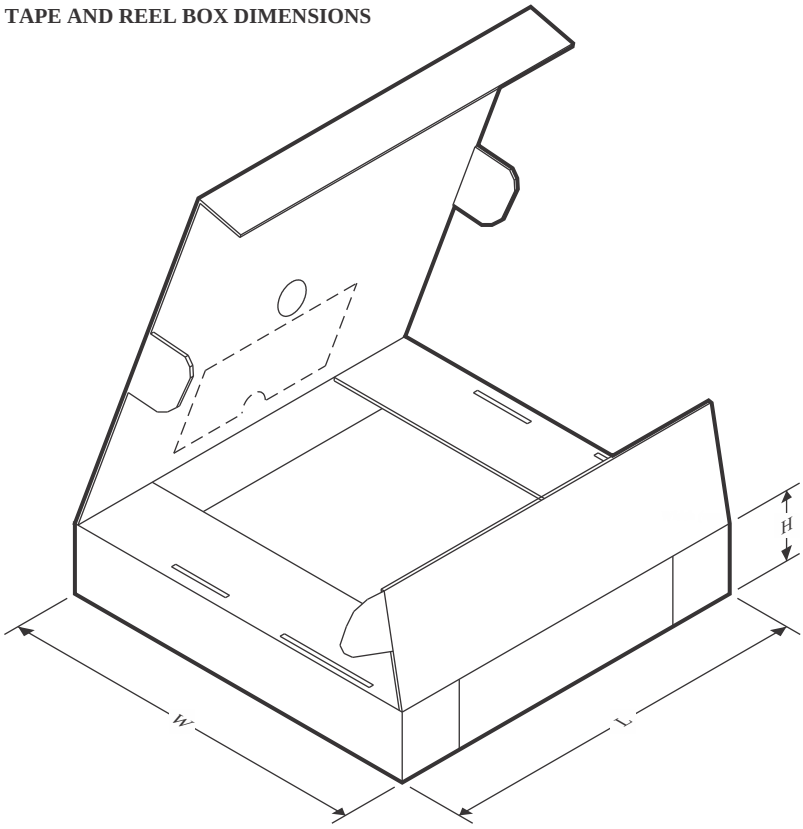
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65ALS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

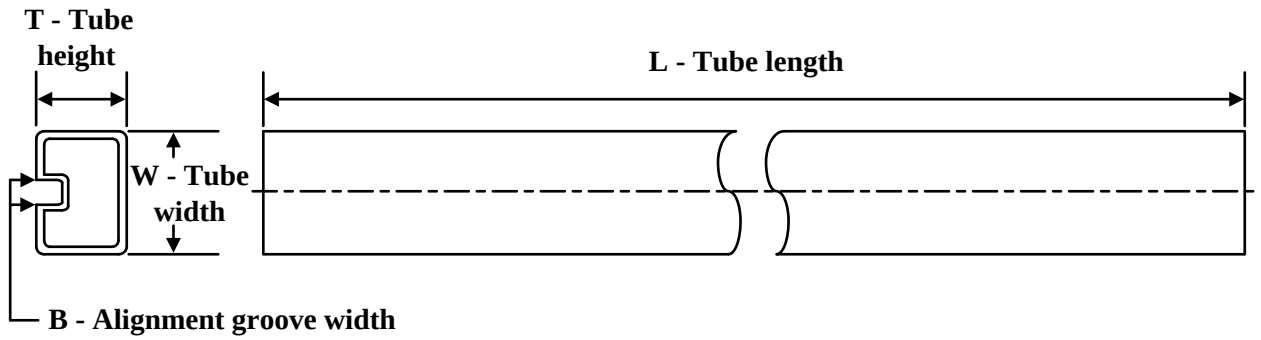
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS180DR	SOIC	D	14	2500	356.0	356.0	35.0
SN65ALS180DR	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



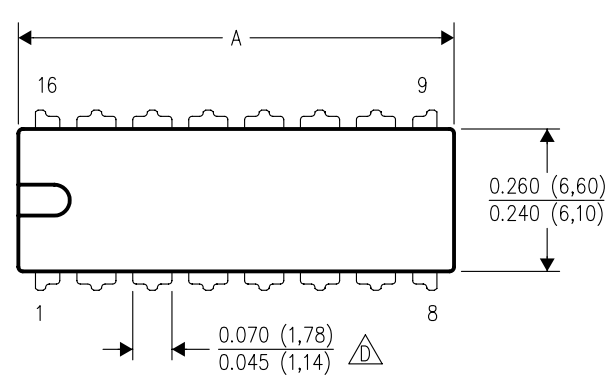
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS180N	N	PDIP	14	25	506	13.97	11230	4.32

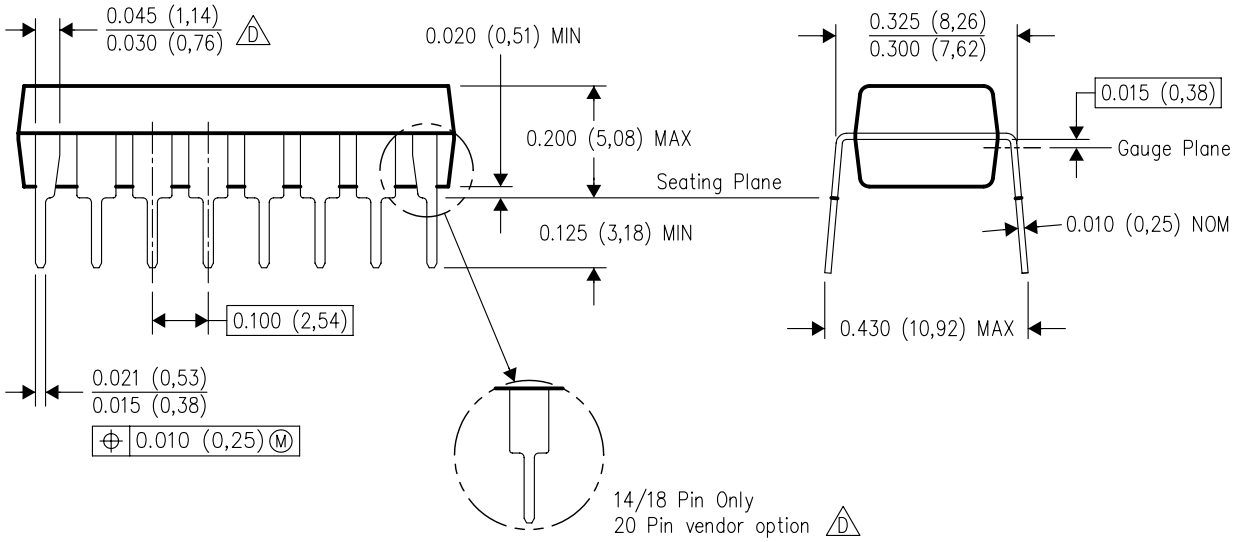
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



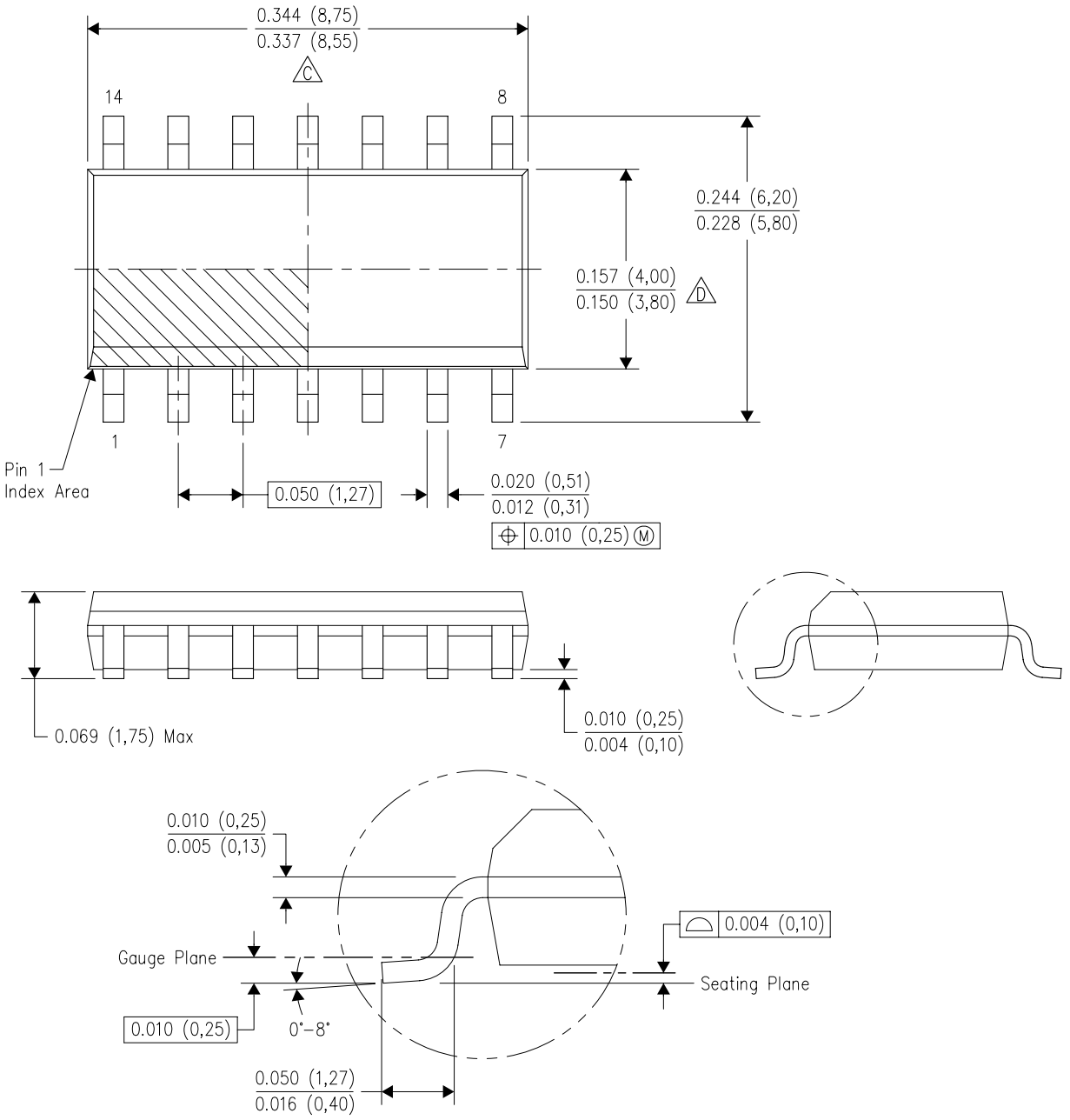
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

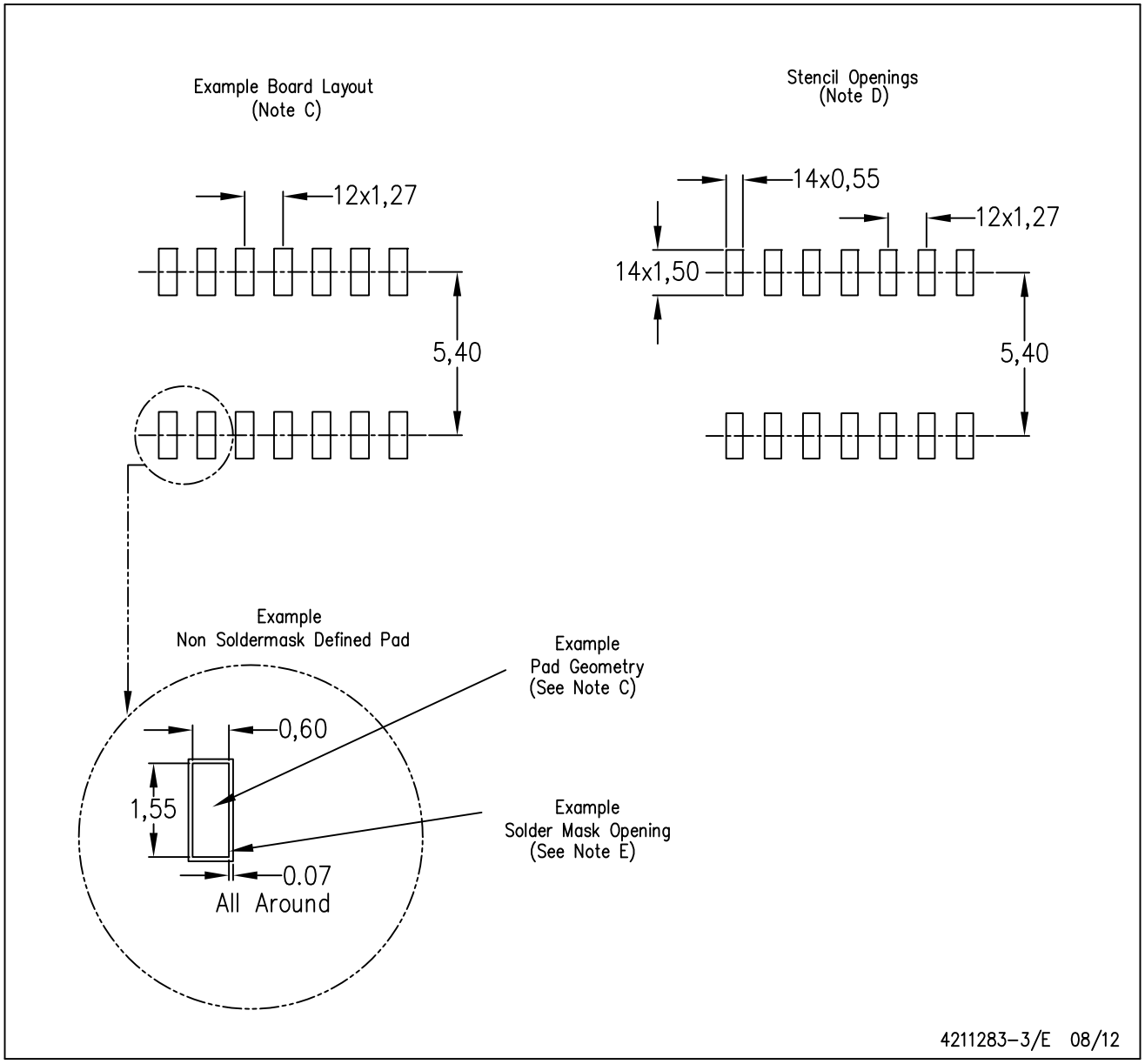
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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