SN65HVD82 稳健耐用型 RS-485 收发器

1 特性

- 总线 I/O 保护
  - ±16kV 人体模型 (HBM) 保护
  - ±12kV IEC 61000-4-2 接触放电
  - +4kV IEC61000-4-4 快速瞬态突发
- 工业温度范围：-40°C 至 85°C
- 用于噪声抑制的较大接收器滞后（典型值为 60mV）
- 低功耗
  - <1μA 待机电流
  - <1mA 静态电流
- 信号传输速率经优化高达 250kbps
- 借助 WEBENCH® 电源设计器，使用 SN65HVD82 创建定制设计方案

2 应用

- 电表
- 楼宇自动化
- 工业网络
- 安全电子器件

3 说明

该器件兼具驱动器和接收器功能，稳健耐用，可满足特定工业 应用中的严格要求。这些总线引脚可耐受 ESD 事件，并且具备符合人体模型、气隙放电和接触放电规范的高水平保护。

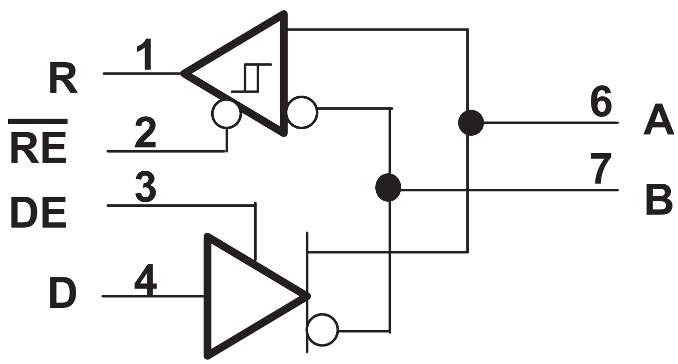
该器件将差分驱动器与差分接收器相结合，共同由单个 5V 电源供电。驱动器差分输出和接收器差分输入在内部连接，构成一个适用于半双工（两线制总线）通信的总线端口。该器件 具有 宽共模电压范围，因此适用于长线缆上的 多点 应用。该器件的额定温度范围介于 -40°C 和 85°C 之间。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN65HVD82	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

逻辑图（正逻辑）



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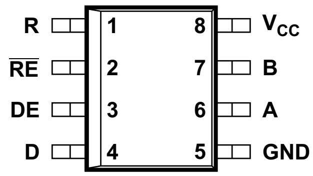
4 修订历史记录

Changes from Revision A (July 2015) to Revision B	Page
• 已将 WEBENCH 链接添加至数据表	1
• Changed pin 6 From: B To: A and pin 7 From: A To: B in Figure 19	15

Changes from Original (October 2012) to Revision A	Page
• 已添加 *引脚配置和功能部分，ESD 额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分*	1

5 Pin Configuration and Functions

D Package
16-Pin SOIC
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
	Voltage range at A or B Inputs	–18	18	V
	Input voltage range at any logic pin	–0.3	5.7	V
	Voltage input range, transient pulse, A and B, through 100Ω	–100	100	V
	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
	Continuous total power dissipation	See *Thermal Information*		
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	
		Machine model (MM), JEDEC Standard 22		±400	
		IEC 61000-4-2 ESD (Contact Discharge)	Bus terminals and GND	±12000	
		IEC 60749-26 ESD (Human Body Model)	Bus terminals and GND	±16000	
		IEC 61000-4-4 EMC (Fast Transient Burst Immunity)	Bus terminals and GND	±4000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)[1]	–7		12	V
V_{IH}	High-level input voltage (D, DE and $\overline{RE}$ inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (D, DE and $\overline{RE}$ inputs)	0		0.8	V
V_{ID}	Differential input voltage (A and B inputs)	–12		12	V
I_O	Output current, Driver	–60		60	mA
	Output current, Receiver	–8		8	mA
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
$1/t_{UI}$	Signaling rate			250	kbps
T_A	Operating free-air temperature (see *Application and Implementation* section for thermal information)	–40		85	°C
T_J	Junction Temperature	–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC[1]		SN65HVD82 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	See Figure 5, R_L = 60 Ω, 375 Ω on each output to –7 V to 12 V		1.5			V
		R_L = 54 Ω (RS-485)	See Figure 6	1.5	2		V
		R_L = 100 Ω (RS-422)		2	2.5		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF	See Figure 6	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors	See Figure 6	1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–0.2	0	0.2	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				850		mV
C_{OD}	Differential output capacitance				8		pF
V_{IT+}	Positive-going receiver differential input voltage threshold			See (1)	–70	-20	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			–200	–150	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – V_{IT-})			40	60		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = -8 mA		4	V_{CC}–0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2		2	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–10		10	µA
I_{OS}	Driver short-circuit output current	| I_{OS} | with V_A or V_B from –7 V to +12 V				150	mA
I_I	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V		75	125	µA
			V_I = –7 V	–100	–40		
I_{CC}	Supply current (quiescent)	Driver and Receiver enabled	DE = V_{CC}, RE=GND, No load			900	µA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, No load			650	
		Driver disabled, receiver enabled	DE = GND, RE = GND, No load			650	
		Driver and receiver disabled	DE = GND, D=GND, RE = V_{CC}, No load		0.4	2	
	Supply current (dynamic)	See *Typical Characteristics*					

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than V_{IT-}.

6.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 7		400	700	1200	ns
t_{PHL}, t_{PLH}	Driver propagation delay			90	700	1000	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} – t_{PLH}\|$				25	200	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 8 and Figure 9		50	500	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			500	1000	ns
		Receiver disabled			3	9	μs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, See Figure 10			18	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				85	195	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} – t_{PLH}\|$				1	15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				50	500	ns
$t_{PZL(1)}$, $t_{PZH(1)}$	Receiver enable time	Driver enabled, See Figure 11			20	130	ns
$t_{PZL(2)}$, $t_{PZH(2)}$		Driver disabled, See Figure 12			2	8	μs

6.7 Typical Characteristics

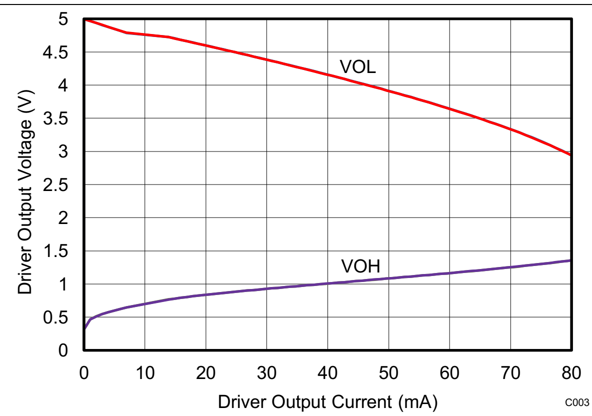


Figure 1. Driver Output Voltage vs Driver Output Current

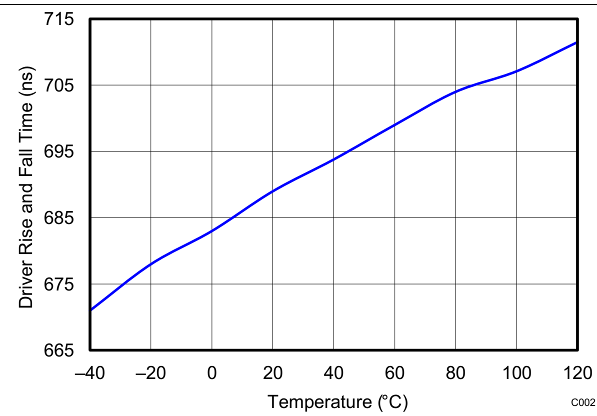


Figure 2. Driver Rise and Fall Time vs Temperature

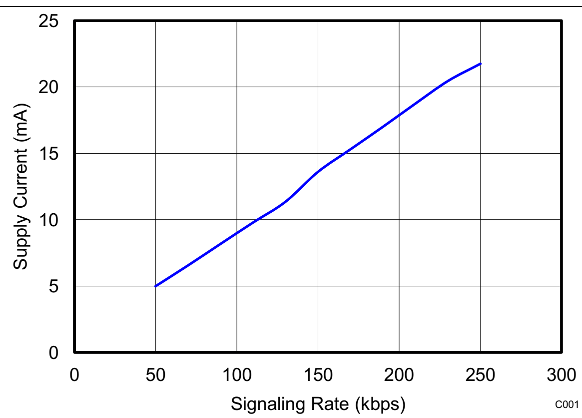


Figure 3. Supply Current vs Signaling Rate

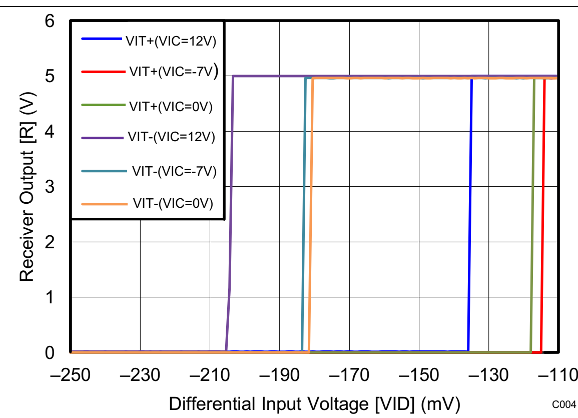


Figure 4. Receiver Output vs Differential Input Voltage

7 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

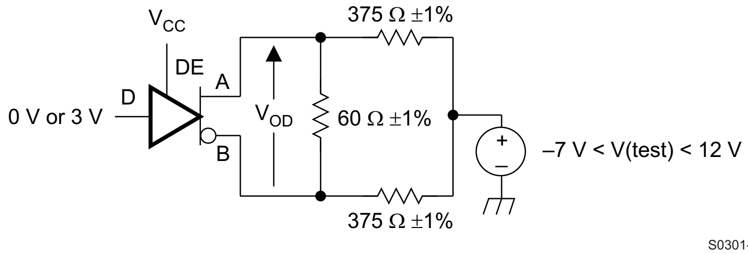


Figure 5. Measurement of Driver Differential Output Voltage With Common-Mode Load

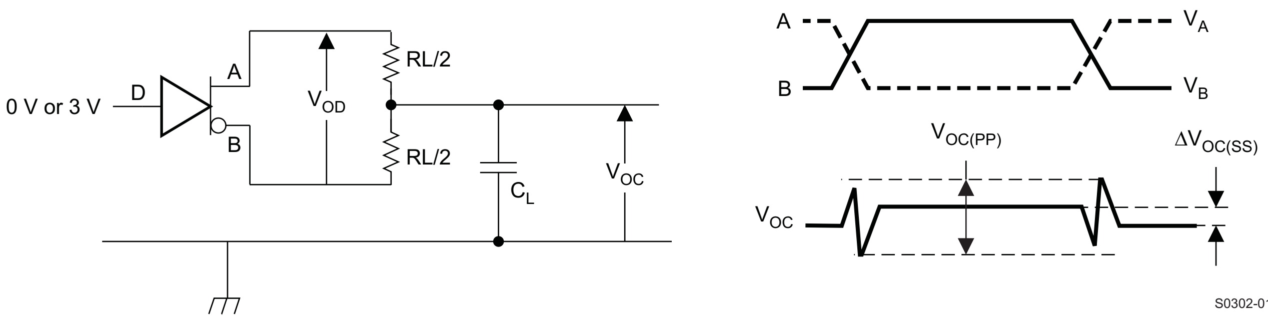


Figure 6. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

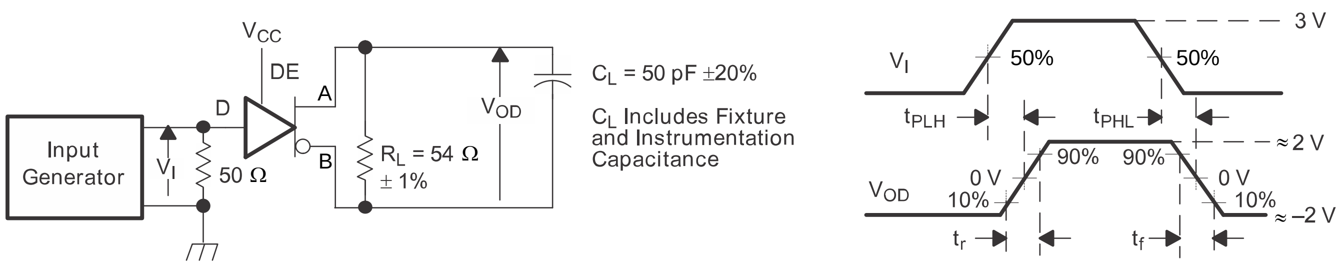
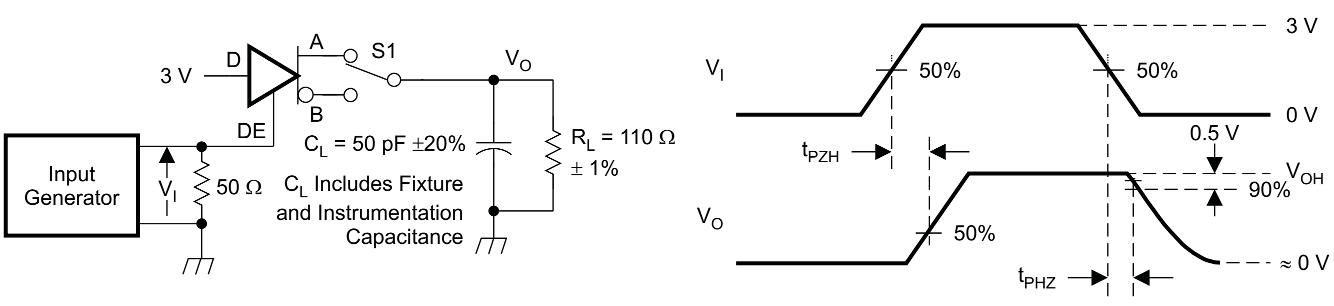


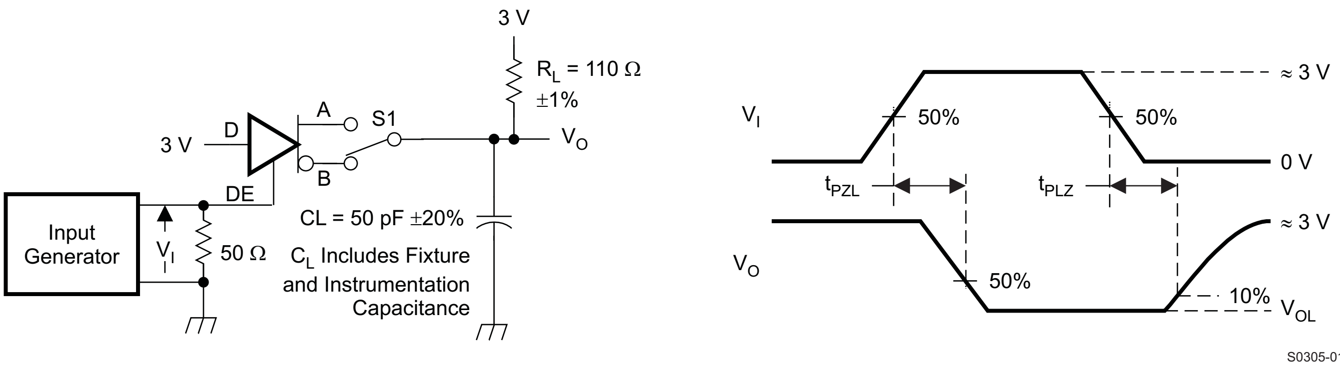
Figure 7. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3V to test non-inverting output, D at 0V to test inverting output.

Figure 8. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

Parameter Measurement Information (continued)



D at 0V to test non-inverting output, D at 3V to test inverting output.

Figure 9. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

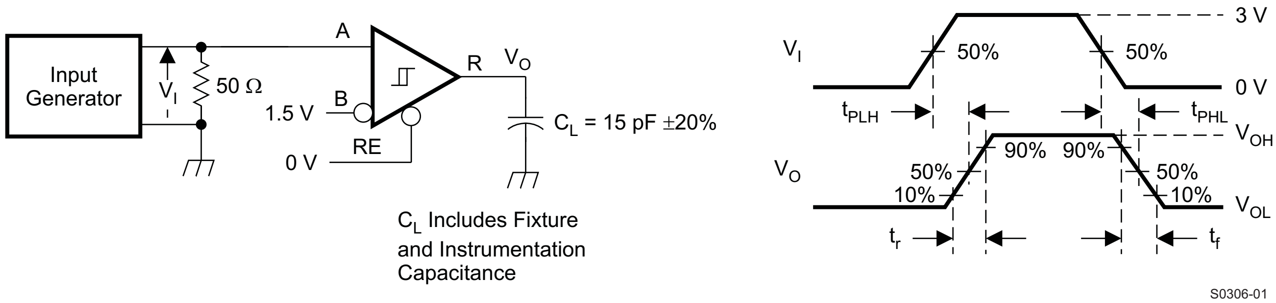


Figure 10. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

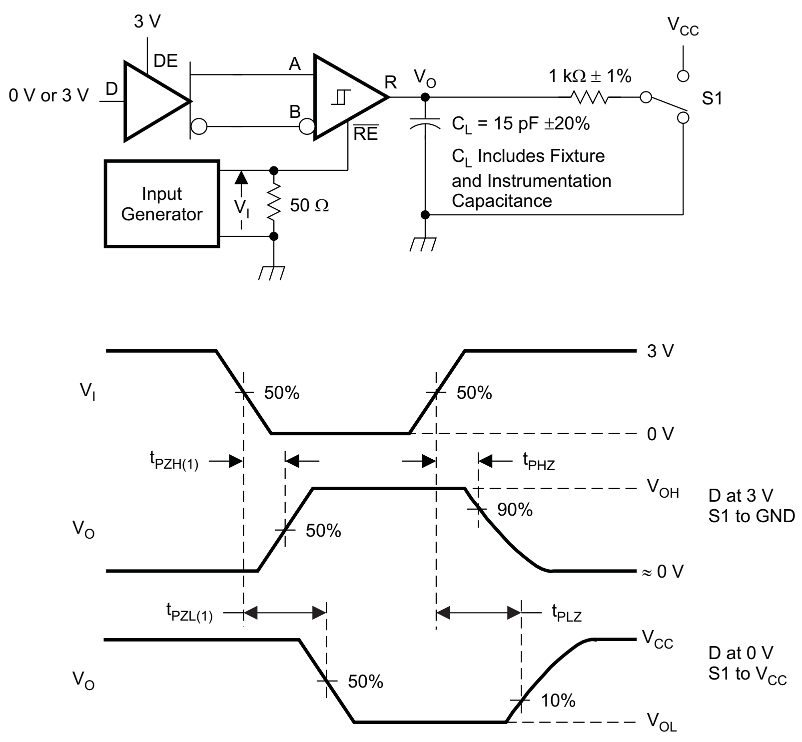


Figure 11. Measurement of Receiver Enable/Disable Times With Driver Enabled

Parameter Measurement Information (continued)

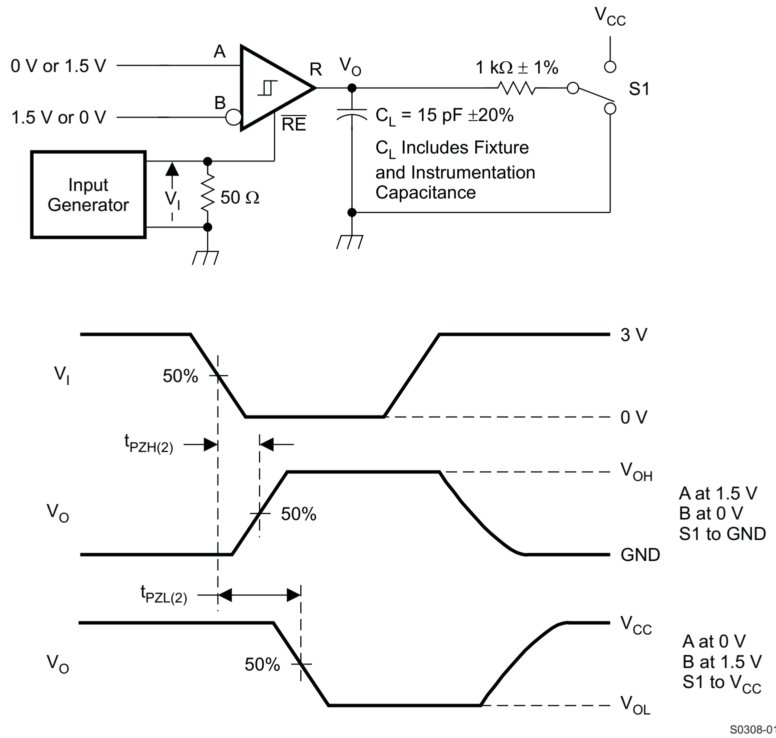


Figure 12. Measurement of Receiver Enable Times With Driver Disabled

8 Detailed Description

8.1 Overview

The SN65HVD82 device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 250 kbps over controlled-impedance transmission media (such as twisted-pair cabling). The device features a high level of internal transient protection, making it able to withstand up ESD strikes up to 12 kV (per IEC 61000-4-2) and EFT transients up to 4 kV (per IEC 61000-4-4) without incurring damage. Up to 256 units of SN65HVD82 may share a common RS-485 bus due to the device's low bus input currents. The device also features a low standby current consumption of 400 nA (typical).

8.2 Functional Block Diagram

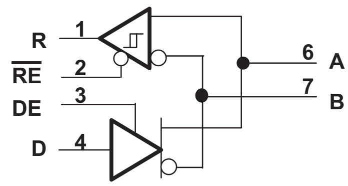


Figure 13. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Receiver Failsafe

The differential receiver is *failsafe* to invalid bus states caused by:

- open bus conditions such as a disconnected connector
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the "input indeterminate" range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when the V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. As seen in the Electrical Characteristics table, differential signals more negative than –200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

Signals which transition from positive to negative (or from negative to positive) will transition only once, ensuring no spurious bits.

8.3.2 Low-Power Standby Mode

When both the driver and receiver are disabled (DE transitions to a low state and RE transitions to a high state) the device enters standby mode. If the enable inputs are in this state for a brief time (e.g. less than 100 ns), the device does not enter standby mode. This prevents inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state a sufficient duration (e.g. for 300 ns or more), the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the steady-state supply current is typically less than 400 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

8.4 Device Functional Modes

Table 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A – V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

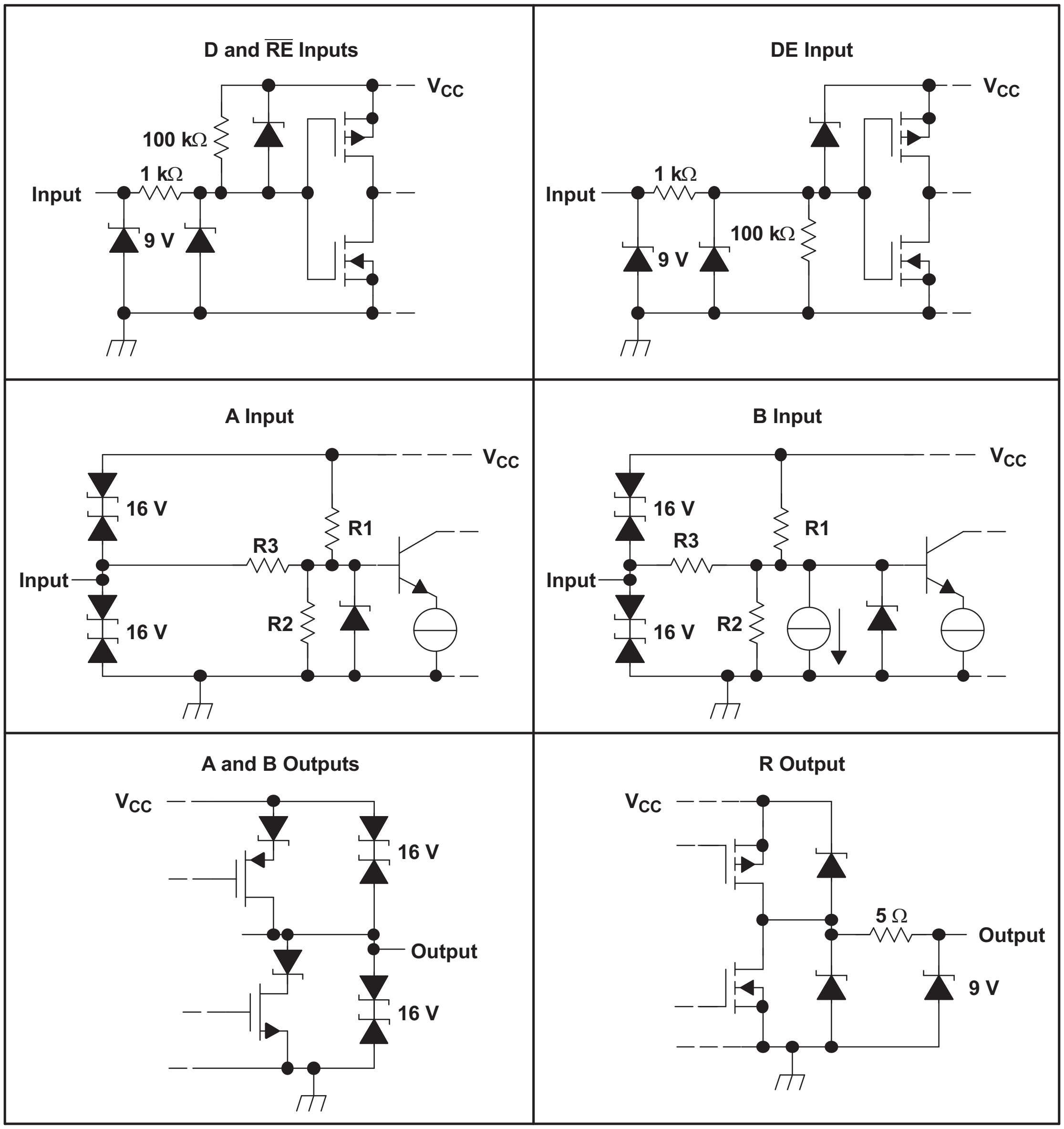


Figure 14. Equivalent Input and Output Schematic Diagrams

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Device Configuration

The SN65HVD82 is a half-duplex, 250-kbps, RS-485 transceiver operating from a single 5-V supply. The driver and receiver enable pins allow for the configuration of different operating modes.

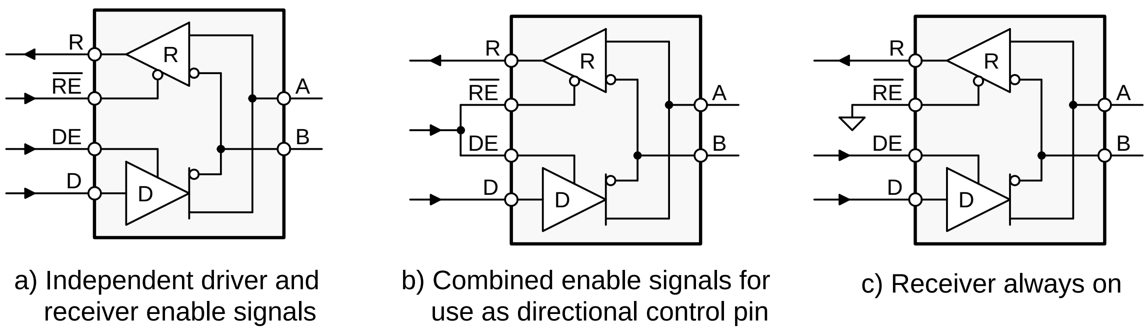


Figure 15. SN65HVD82 Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single, direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration a node not only receives the data from the bus, but also the data it sends and thus can verify that the correct data have been transmitted.

9.1.2 Bus – Design

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

Application Information (continued)

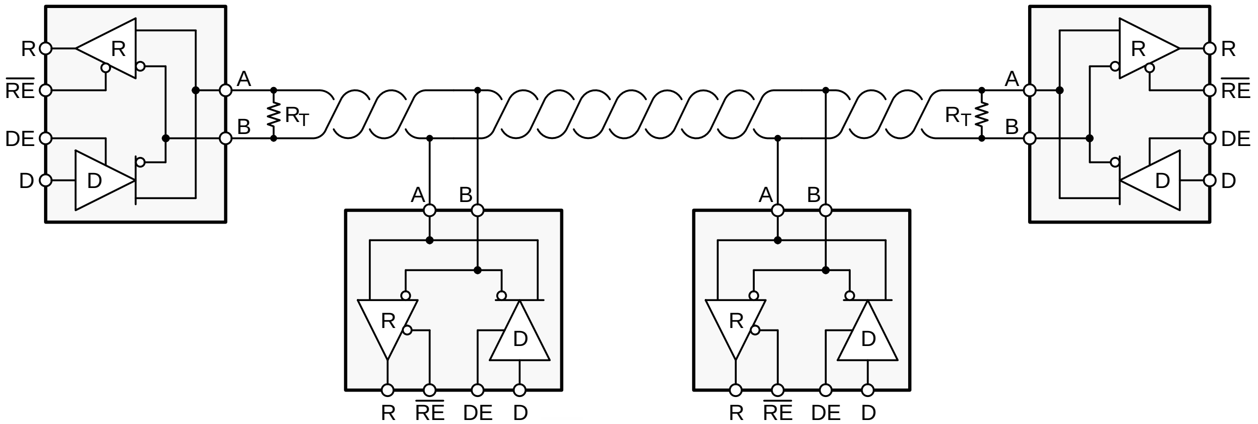


Figure 16. Typical RS-485 Network with SN65HVD82 Transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with Z_0 = 100 Ω, and proper RS-485 cable with Z_0 = 120 Ω.

Line measurements have shown that making R_T by up to 10% larger than Z_0 improves signal quality. Typical cable sizes are AWG 22 and AWG 24.

The theoretical maximum bus length is assumed with 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB.

The theoretical maximum number of bus nodes is determined by the ratio of the RS-485 specified maximum of 32 unit loads (UL) and the actual unit load of the applied transceiver. For example, the SN65HVD82 is a 1/8 UL transceiver. Dividing 32 UL by 1/8 UL yields 256 transceivers that can be connected to one bus.

9.1.3 Cable-Length Versus Data Rate

There is an inverse relationship between data rate and cable length. That is, the higher the data rate the shorter the cable and conversely the lower the data rate the longer the cable. While most RS-485 systems utilize data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 feet and above. This is possible by allowing for small signal jitter of up to 5 or 10%.

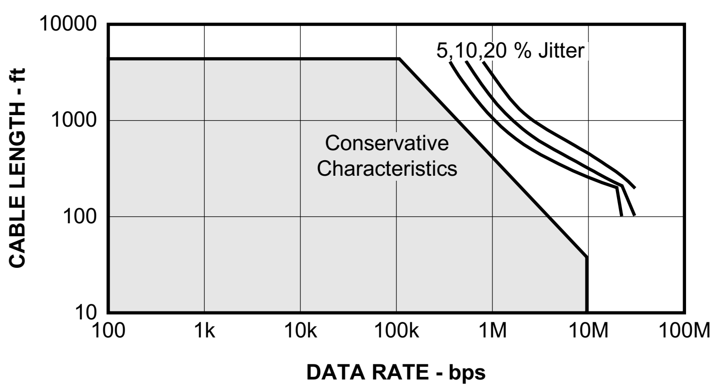


Figure 17. Cable Length vs Data Rate Characteristic

Application Information (continued)

9.1.4 Stub – Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for this is that a stub presents a non-terminated piece of bus line which can introduce reflections if too long. As a rule of thumb the electrical length or round-trip delay of a stub should be less than one tenth of the driver's rise time, thus leading to a maximum physical stub length of: $L_{Stub} \le 0.1 \times t_r \times v \times c$, with $\mathbf{t_r}$ as the driver's 10/90 rise time, **c** as the speed of light (3×10^8 m/s or 9.8×10^8 ft/s), and **v** as the signal velocity of the cable (v = 78%) or trace (v = 45%) as a factor of **c**.

Thus, for the SN65HVD82 with a minimum rise time of 400 ns the maximum *cable* stub length yields $L_{Stub} \le 0.1 \times 400 \times 10^{-9} \times 3\ 10^8 \times 0.78 = 9.4$ m or 30.6 ft.

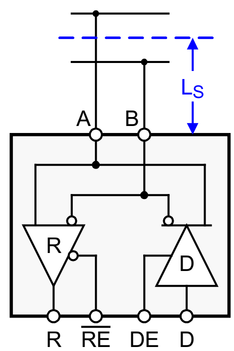


Figure 18. Stub Length

9.1.5 3-V to 5-V Interface

Interfacing the SN65HVD82 to a 3-V controller is easy. Because the 5-V logic inputs of the transceiver accept 3-V input signals they can be directly connected to the controller I/O. The 5-V receiver output, R, however must be level-shifted via a Schottky diode and a 10-kV resistor to connect to the controller input. When R is high, the diode is reverse biased and the controller supply potential lies at the controller input. When R is low, the diode is forward biased and conducts. In this case only the diode forward voltage of 0.2 V lies at the controller input.

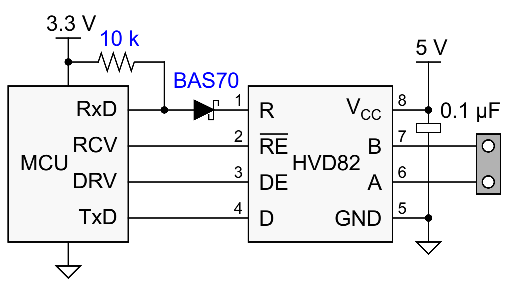


Figure 19. 3 V – 5 V Interface

9.1.6 Noise Immunity

The input sensitivity of a standard RS-485 transceiver is ±200 mV. When the differential input voltage, V_{ID}, is greater than +200 mV, the receiver output turns high, for $V_{ID} \le 200$ mV the receiver outputs low. Bus voltages in between these levels can cause the receiver output to go high, or low, or even toggle between logic states. Small bus voltages however occur every time during the bus access hand-off from one driver to the next as the low-impedance termination resistors reduce the bus voltage to zero. To prevent receiver output toggling during bus idling, and thus increasing noise immunity, external bias resistors must be applied to create a bus voltage that is greater than the input sensitivity plus any expected differential noise.

Application Information (continued)

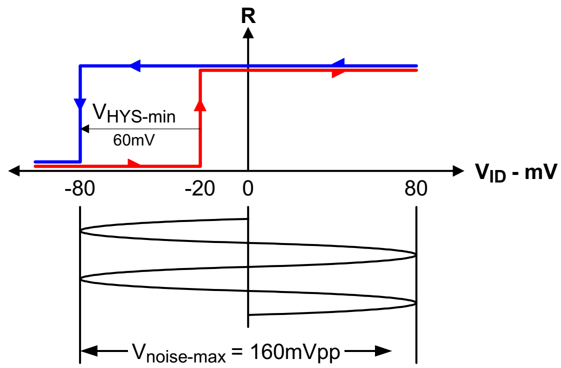


Figure 20. SN65HVD82 Noise Immunity

The SN65HVD82 transceiver circumvents idle-bus and differential noise issues by providing a positive input threshold of –20 mV and a typical hysteresis of 60 mV. In the case of an idle-bus condition therefore, a differential noise voltage of up to 160 mV_{PP} can be present without causing the receiver output to change states from high to low. This increased noise immunity eliminates the need for idle-bus failsafe bias resistors and allows for long haul data transmissions in noisy environment.

9.1.7 Transient Protection

The bus terminals of the SN65HVD82 transceiver family possess on-chip ESD protection against ±15 kV human body model (HBM) and ±12 kV IEC61000-4-2 contact discharge. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, CS, and 78% lower discharge resistance, RD of the IEC-model produce significantly higher discharge currents than the HBM-model.

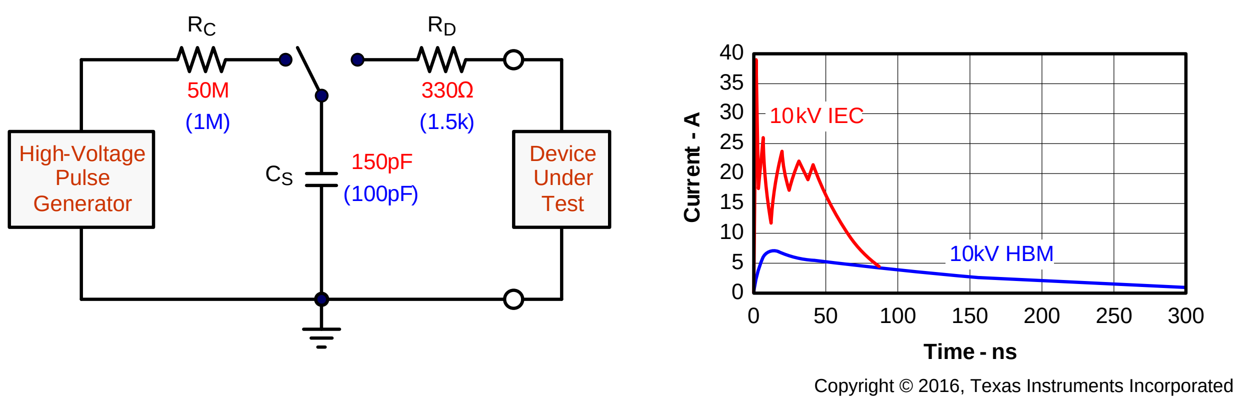


Figure 21. HBM and IEC-ESD Models and Currents in Comparison

EFTs are usually caused by relay contact bounce or the interruption of inductive loads, while surge transients often results from lightning strikes (direct strike or induced voltages and currents due to an indirect strike), or the switching of power systems including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Application Information (continued)

Figure 22 compares the pulse-power of the EFT and surge transients with the power caused by an IEC-ESD transient. As can be seen the tiny blue blip in the bottom left corner of the left diagram represents the power of a 10-kV ESD transient, which already dwarfs against the significantly higher EFT power spike and certainly against the 500-V surge transient. This type of transient power is well representative for factory environments in industrial and process automation. The right diagram compares the enormous power of a 6-kV surge transient, which more likely occurs in e-metering applications of power generating and power grid systems, with the aforementioned 500-V surge transient. *Note that the unit of the pulse-power changes from kW to MW, thus making the power of the 500-V surge transient almost dropping off the scale.*

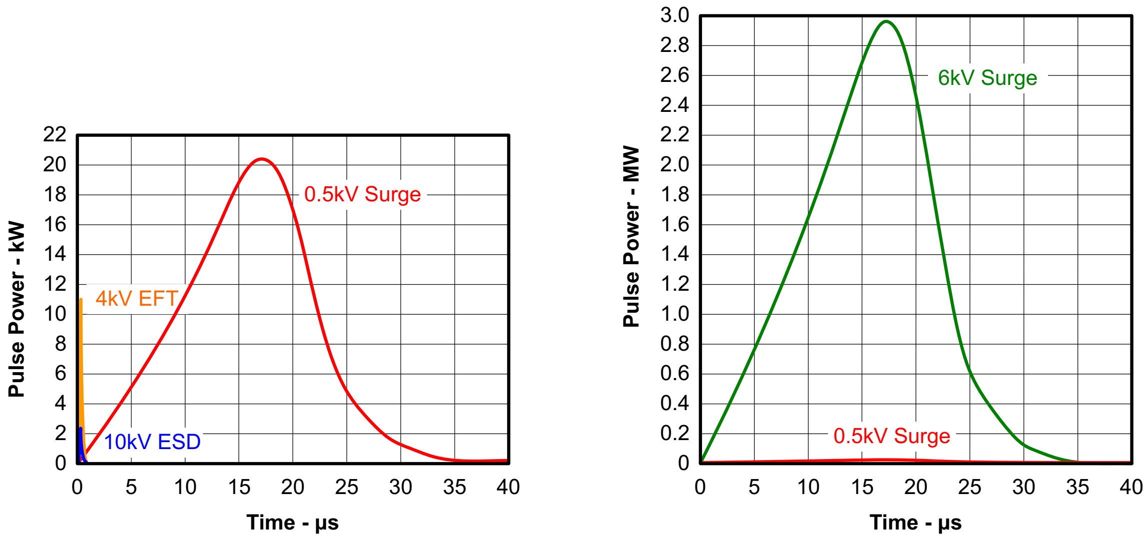


Figure 22. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, their long pulse duration and slowly decreasing pulse power signifies high energy content.

The electrical energy of a transient that is dumped onto the transceiver's internal protections cells is converted into thermal energy, or heat that literally fries the protection cells, thus destroying the transceiver. Figure 23 showcases the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

Application Information (continued)

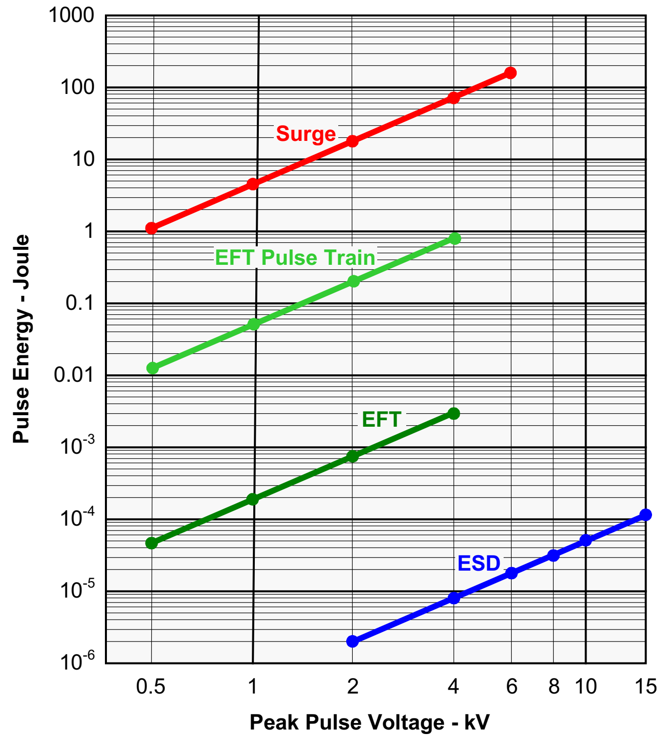


Figure 23. Comparison of Transient Energies

Figure 24 suggests two circuit designs providing protection against surge transients. Table 3 presents the associated bill of material.

Table 3. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3V, 250kbps RS-485 Transceiver	SN65HVD82D	TI
R1,R2	10Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1,TBU2	Bidirectional. 200mA Transient Blocking Unit	TBU-CA-065-200-WH	Bourns
MOV1,MOV2	200V, Metal-Oxide Varistor	MOV-10D201K	Bourns

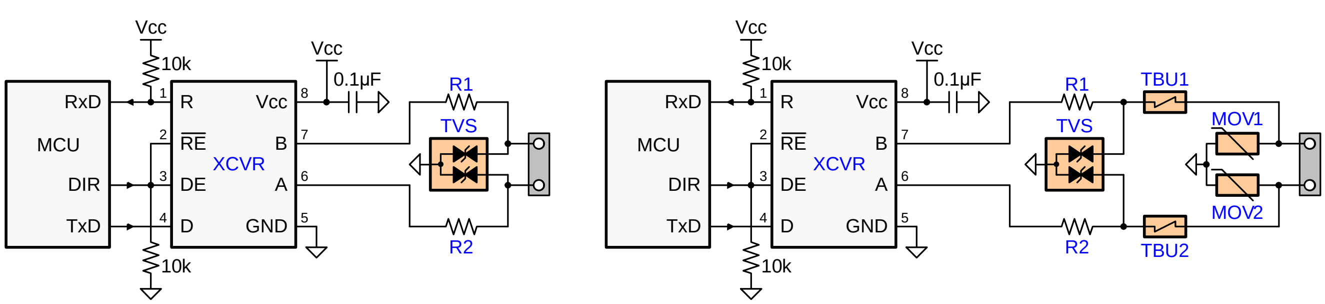


Figure 24. Transient Protection Against ESD, EFT, and Surge Transients

Both circuits are designed for 10-kV ESD and 4-kV EFT transient protection. The left however provides surge protection of ≥ 500-V transients only, while the right protection circuits can withstand 5-kV surge transients.

9.2 Typical Application

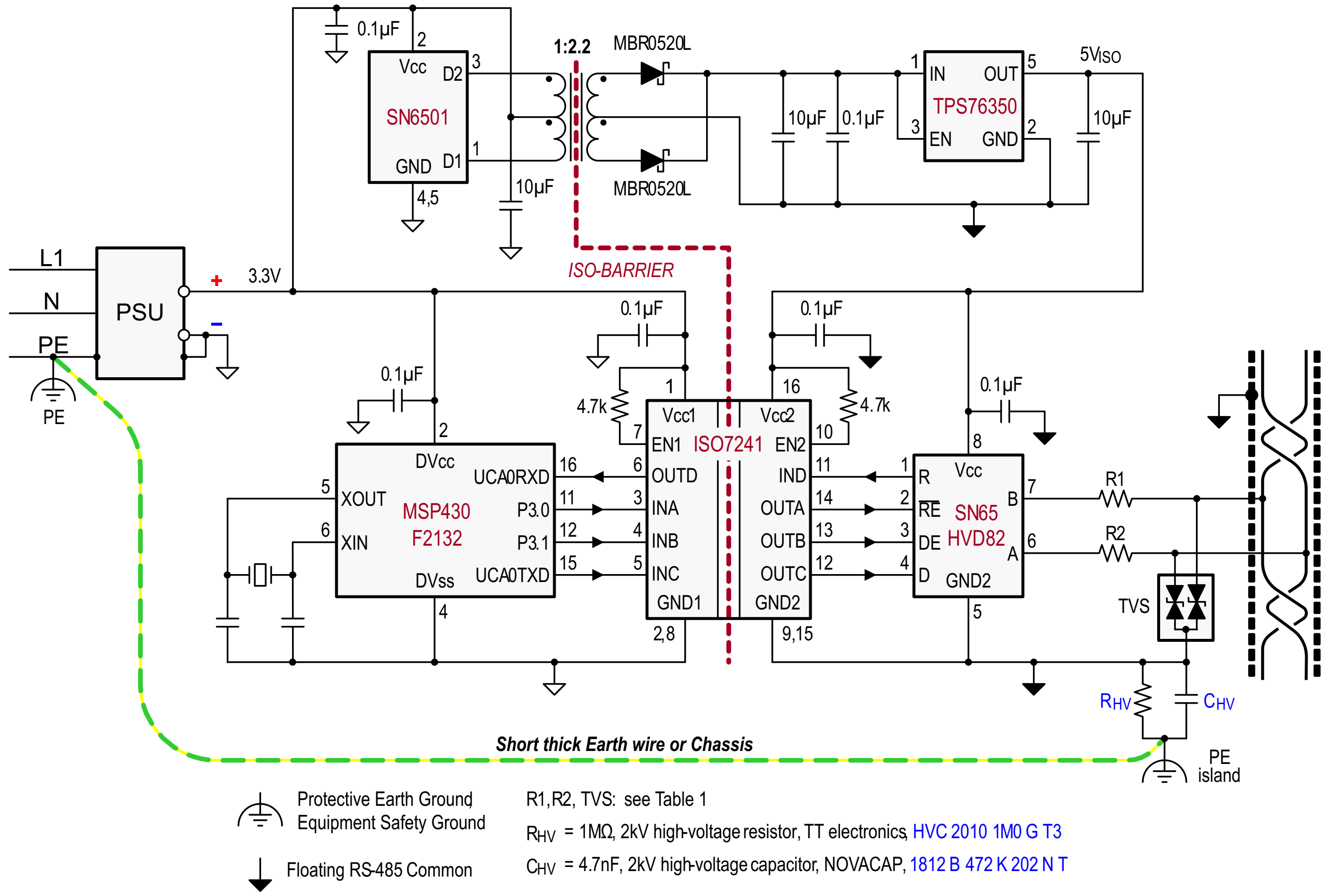


Figure 25. Isolated Bus Node With Transient Protection

9.2.1 Design Requirements

The following list outlines sample design requirements for the typical application example found in Figure 25

- RS-485-compliant bus interface (needs differential signal amplitude of at least 1.5 V under fully-loaded conditions – essentially, maximum number of nodes connected and with dual 120-Ω termination).
- Galvanic isolation of both signal and power supply lines.
- Able to withstand ESD transients up to 10 kV (per IEC 61000-4-2) and EFTs up to 4 kV (per IEC 61000-4-4).
- Full control of data flow on bus in order to prevent contention (for half-duplex communication).

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the SN65HVD82 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance

Typical Application (continued)

- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 25).

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TPS76350

Signal isolation utilizes the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7-kΩ resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 24 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if it is expected that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

9.2.3 Application Curve

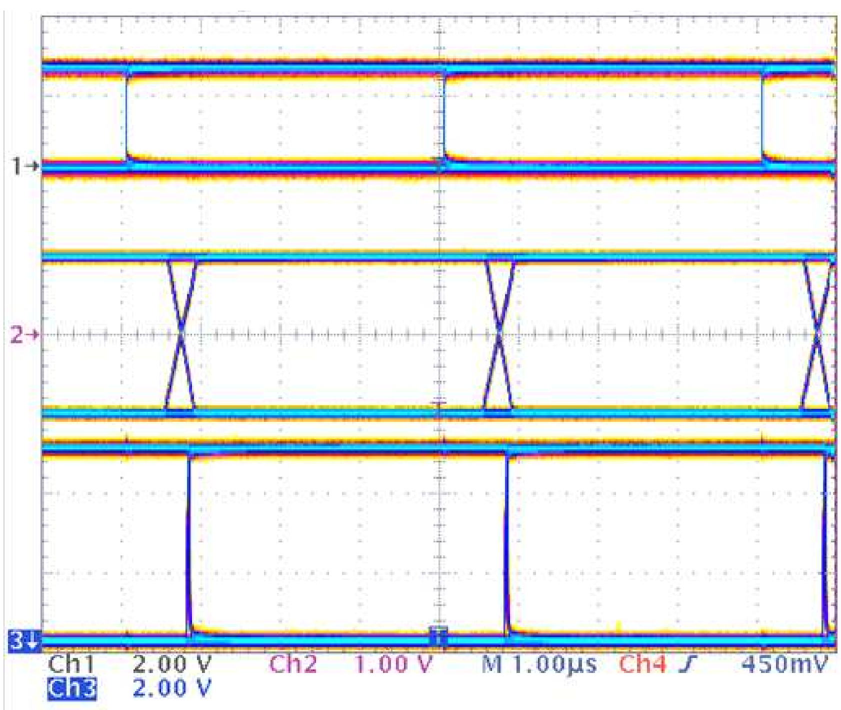


Figure 26. SN65GVD82 D Input (Top), Differential Output (Middle), and R Output (Bottom), 250 kbps Operation, PRBS Data Pattern

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

11.1.1 Design and Layout Considerations For Transient Protection

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the Vcc-pins of transceiver, UART, controller ICs on the board.
5. Use at least two vias for Vcc and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to some 200 mA.

11.2 Layout Example

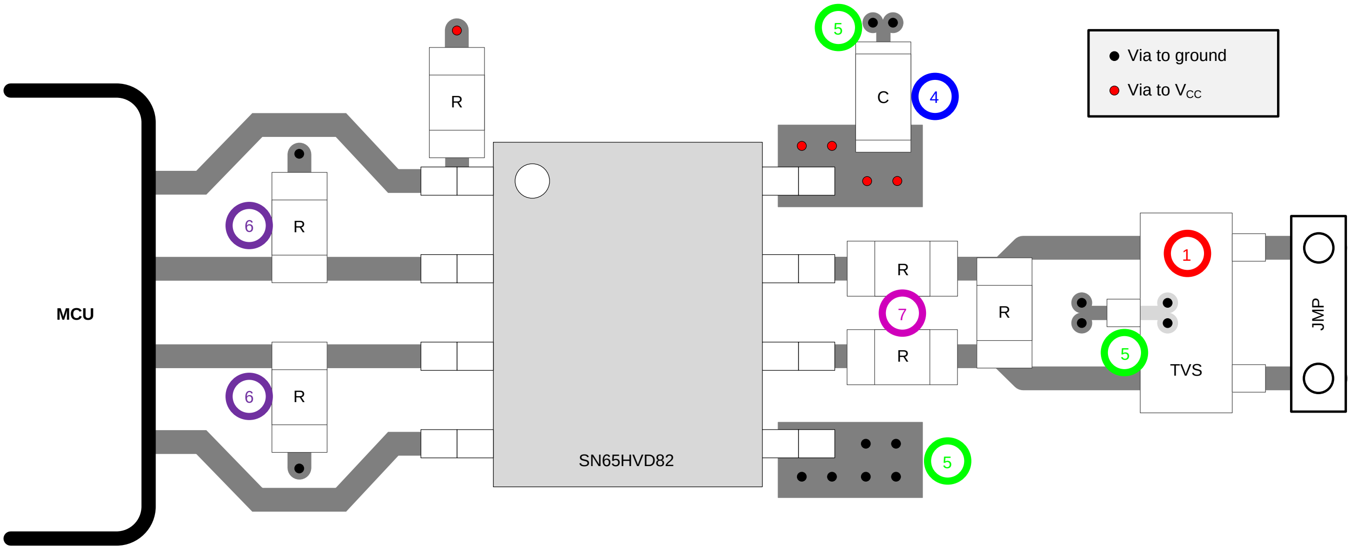


Figure 27. SN65HVD82 Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.1.2 使用 **WEBENCH®** 工具定制设计方案

单击此处，使用 SN65HVD82 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 在开始阶段键入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD82D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82	Samples
SN65HVD82DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD82	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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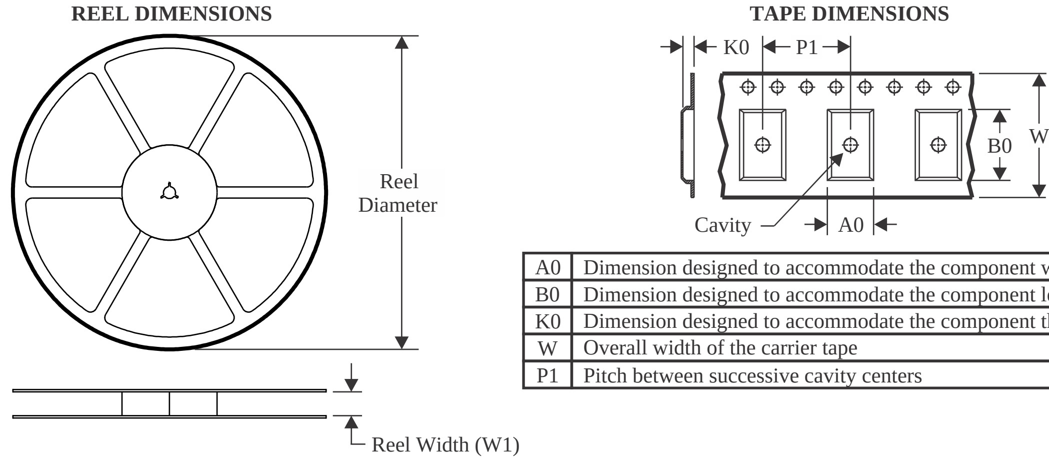
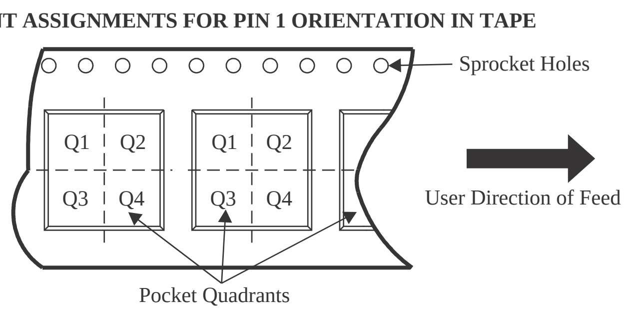
TAPE AND REEL INFORMATION



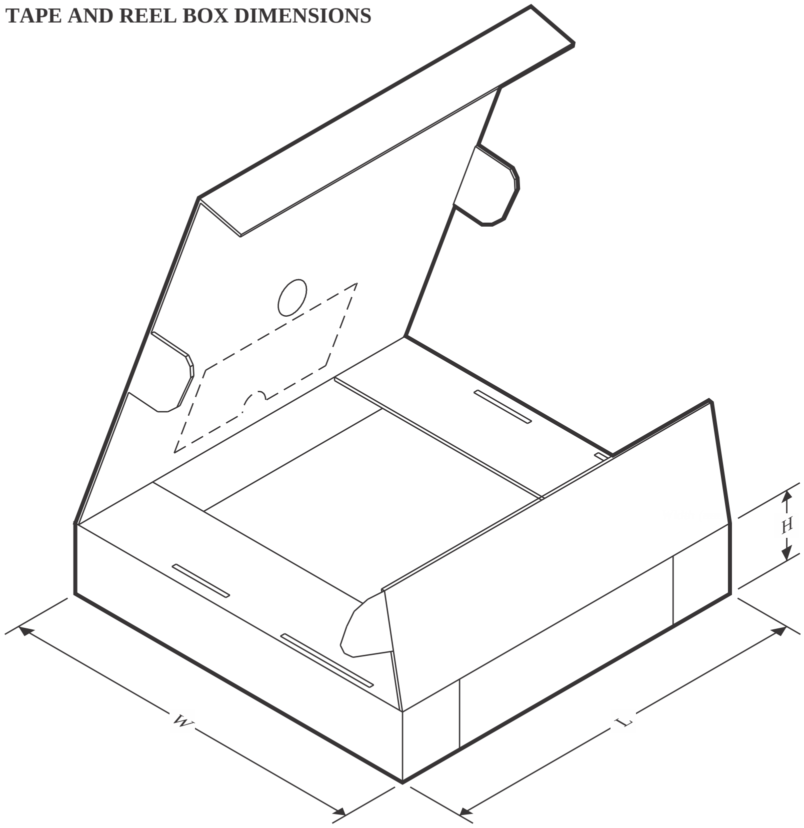
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD82DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

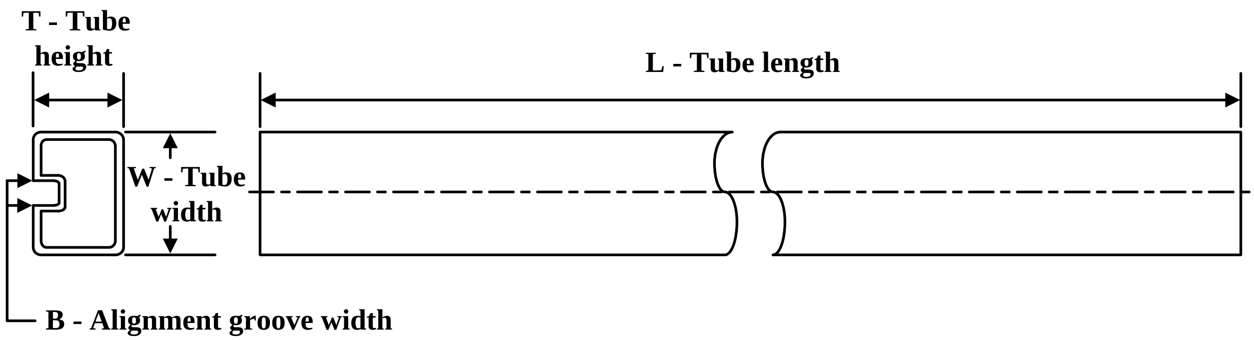
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

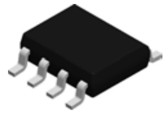
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD82DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD82D	D	SOIC	8	75	507	8	3940	4.32

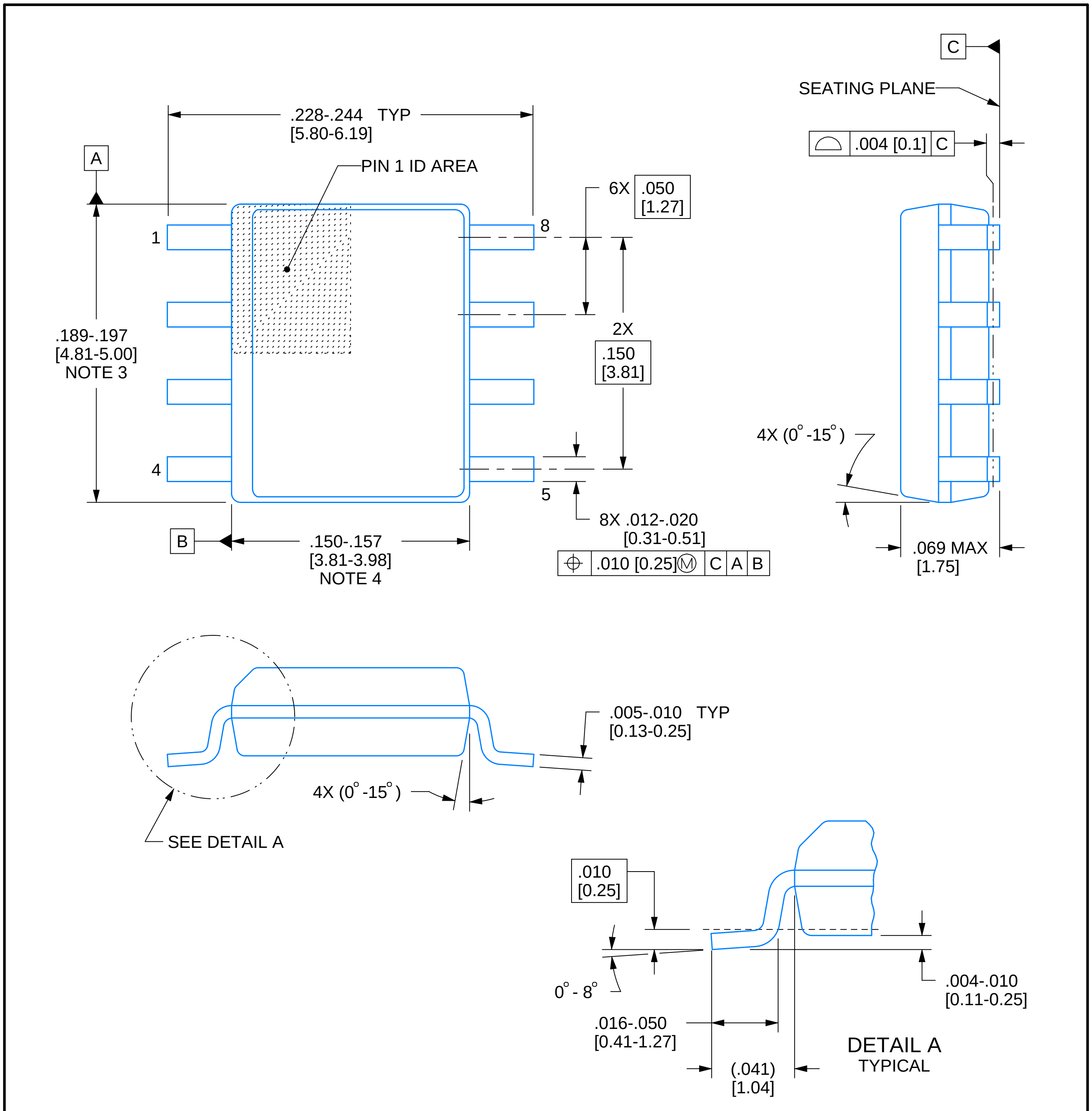


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

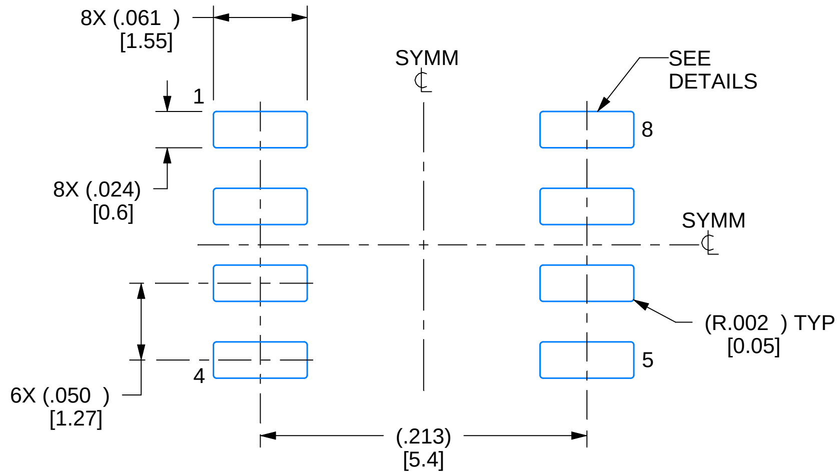
SMALL OUTLINE INTEGRATED CIRCUIT



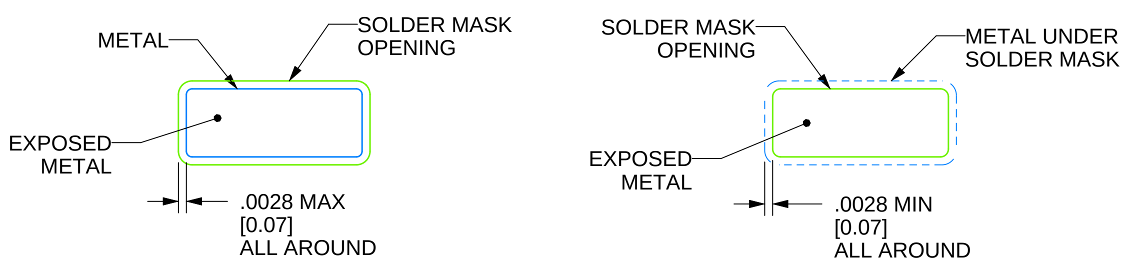
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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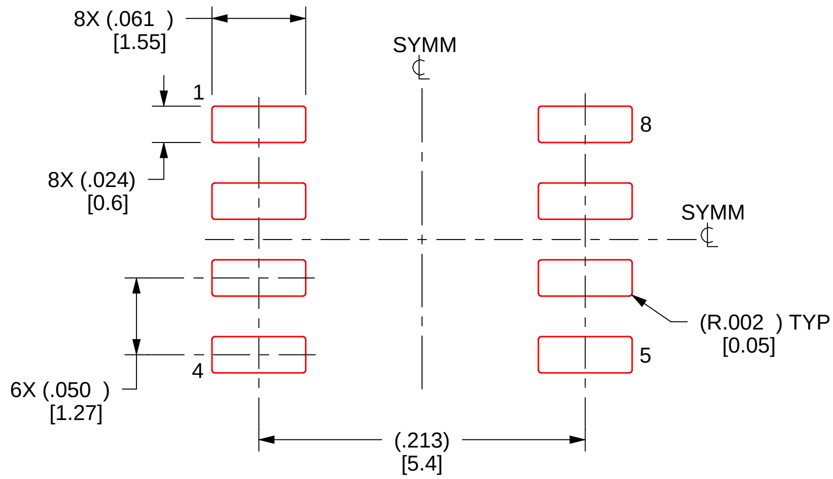
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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